EE142---Project_1

TRAFFIC LIGHT CONTROLLER

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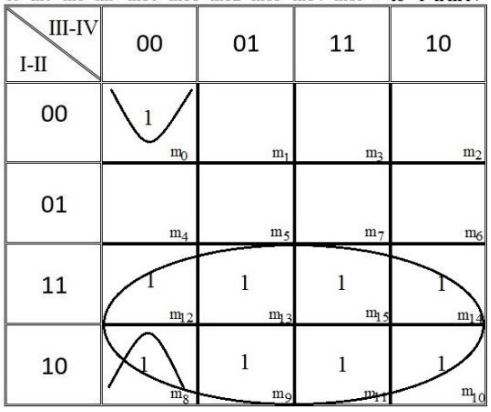
In this project, designing a traffic light controller for a crossroad is asked. In this kind of digital design problems, the design procedure should be followed.

1. ***Stating the problem:*** In this project, it is asked that to determine which traffic lights are red or which one is green. And it perceives whether there is a car in the road or not through the help of sensors then if there is a car, the green will be switched on. However, there are some conditions to be satisfied such as in the crossroad, only one traffic light will be switched green, and there is a priority so that if there are cars in both I and II, the traffic light at I should be green and so on.
2. ***Determining the number of available inputs and required outputs:*** In this project, there are four available inputs that perceive whether there is a car or not; if there is a car the input is 1 otherwise the input is 0. And there are also four required outputs that indicate whether the traffic light is green or red in each road.
3. ***Assigning labels to the variables:*** In the project, the first road is shown as I, the second road is shown as II, the third road is shown as III and the forth road is shown as IV. And the outputs are shown as following; Io, IIo, IIIo, IVo.
4. ***Developing the truth tables and Obtaining the simplified expression for each output:*** To determine the outputs' functions, firstly; the truth tables of the outputs should be drawn. The truth table of the outputs is shown on the right. Then, for each output, the Karnaugh map(K-map) of the output should be drawn.
   [*'→ inverter; (*+*)→Or; (*.*)→And; (*+*)'→Nor]
   a. *K-map of Io:* The K-map of Io is shown below.

Io=m0+m8+m9+m10+m11+m12+m13+m14+m15 => Io= I+II'III'IV'



Io=∑ (0,8,9,10,11,12,13,14,15)
Io=m_o+m_8+m_9+m_{10}+m_{11}+m_{12}+m_{13}+m_{14}+m_{15}
Io=I+II'.III'.IV' (the simplest expression)
Io=I+[(II+III)+IV]' (the least gate)

The Truth Table of The Functions

I	II	III	IV	Io	IIo	IIIo	IVo
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0

b. *K-map of IIo:* The K-map of IIo is shown below.

IIo=m4+m5+m6+m7 => IIo = I'II

I-II \ III-IV	00	01	11	10
00	m_0	m_1	m_3	m_2
01	1 m_4	1 m_5	1 m_7	1 m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

IIo=∑ (4,5,6,7)
IIo=m_4+m_5+m_6+m_7
IIo= I'.II (the simplest expression)
IIo=I'.II (the least gate)

c. *K-map of IIIo:* The K-map of IIIo is shown below.

IIIo=m3+m4 => IIIo = I'II'III

I-II \ III-IV	00	01	11	10
00	m_0	m_1	1 m_3	1 m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

IIIo=∑ (2,3)
IIIo=m_2+m_3
IIIo=I'.II'.III (the simplest expression)
IIIo=(I+II)'.III (the least gate)

d. *K-map of IVo:* The K-map of IVo is shown below.

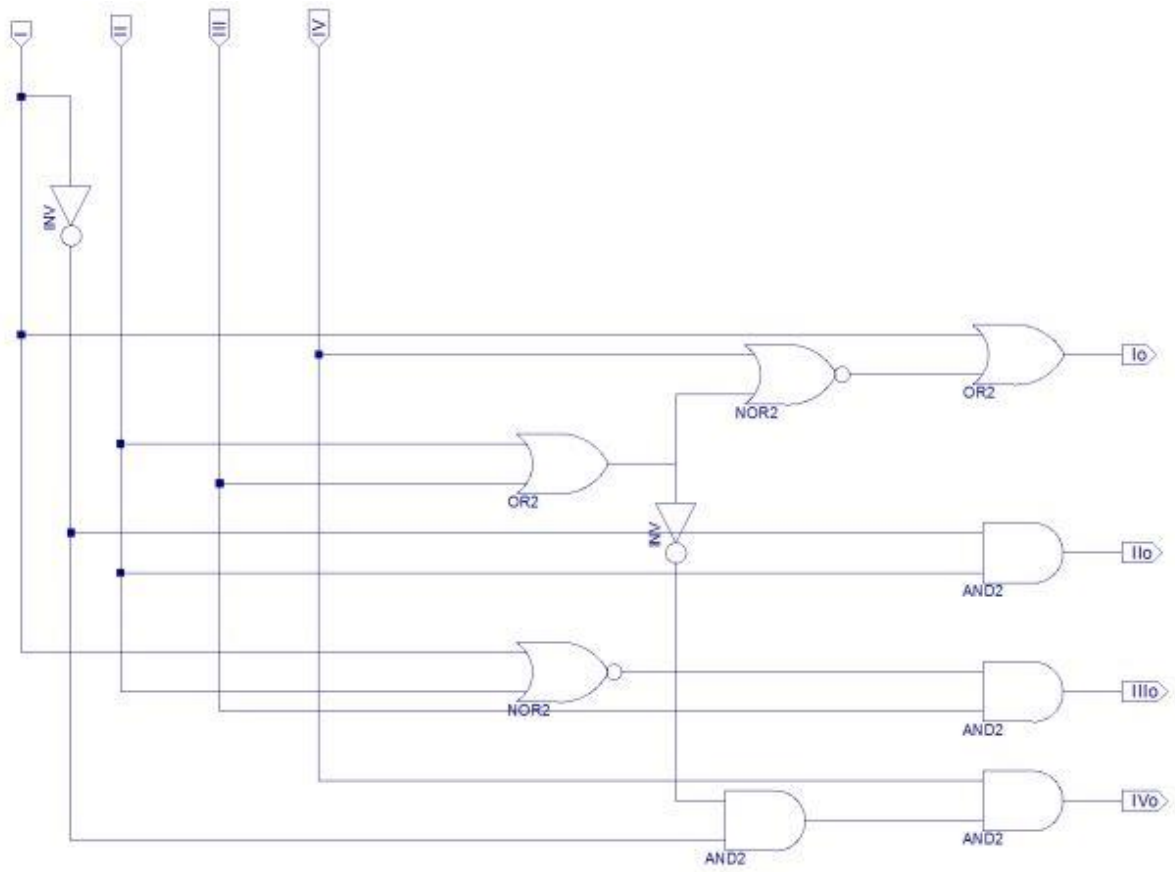
IVo = m1 => IVo = I'II'III'IV

I-II \ III-IV	00	01	11	10
00	m_0	1 m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

IVo=∑ (1)
IVo=m_1
IVo= I'.II'.III'.IV (the simplest expression)
IVo=I'.(II+III)'.IV (the least gate)

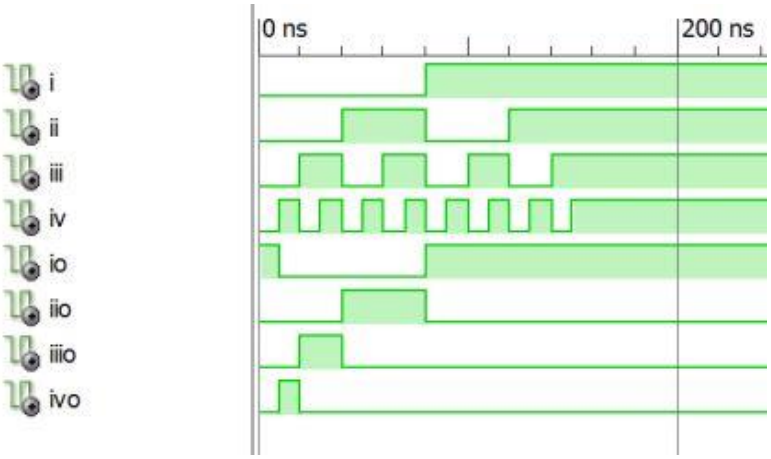
5. ***Drawing the logic circuit:*** In the project, Xilinx ISE Design Suite 14.7 is used to draw the circuit. And during the drawing, the least number of gates should be used due to effectiveness. The logic circuit of the project is below.

The Schematic of The Project



6. ***Implementing the logic circuit:*** To check the result whether it is true or false, the simulation of the logic circuit should be done via Xilinx.

The Simulation of The Project



Conclusion: Through the project, analyzing the problem according to the logical thinking, and binary algebra and converting the daily issues to the digital design system, and binary algebra and so on are expected to be learned.