EE464 2023 Spring

Hardware Project Simulation Report

Selin Ezgi Özcan, 2375475

Işık Emir Altunkol, 2442408

Özgür Gülsuna, 2307668

Mind the Cap

Electrical - Electronics Engineering
Middle East Technical University
Turkey

May 5, 2023

Contents

1 Introduction

This is the preliminary report for the hardware project of EE464 Static Power Conversion II course, prepared by the group Mind the Cap.

We have decided to implement a flyback converter topology to convert and input voltage range of 12-18V to 48V at 1A rated. In this report, the reader will find our decision process for topology selection, electrical and magnetic parameters selections, computer simulations both in ideal and nonideal cases, loss calculations and component selections for the product. A discussion of future work is provided at the end.

2 Topology

2.1 Topology Selection

We have decided to build a flyback converter. Basic topology of a flyback converter is given in Figure 1.

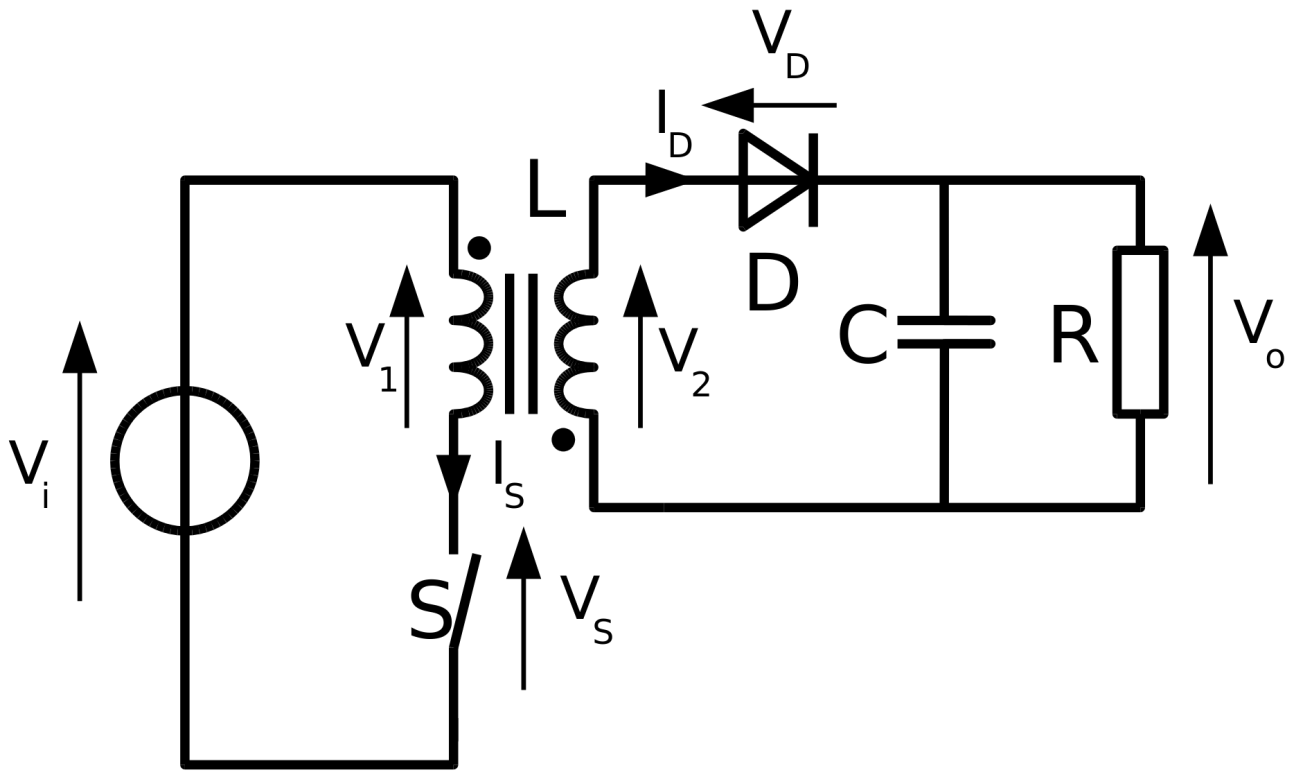

Figure 1: Flyback converter

Our alternative in choices were active clamp flyback converter and forward converter. The dominant advantages of active clamp topology are increased efficiency by applying ZVS and reduced switch voltage stress, which can also be achieved with snubbers in ordinary flyback converters. Although seemingly advantageous, we had to abandon the idea of active clamp flyback converter because all IC's we could find had startup voltages higher than the input voltage range of the project. This meant we had to use a digital controller, but it had to be quite precise to switch at the correct instant so that efficiency would be high and circuit would be linear. Our second alternative, forward converter, was disregarded because forward converter requires two inductors and two diodes. We preferred less components to deal with.

2.2 Parameter Selection

There are two main parameters in a flyback converter: the magnetizing inductance of the transformer and the turns ratio.

- DCM vs CCM selection:

  According to [7], peak MOSFET and diode currents are higher in DCM. Further, DCM losses are claimed to be higher than CCM losses. Combined with the fact that DCM means nonlinear operation, it may seem as if it is all negative. However, the same source provides the typical Bode plots of CCM and DCM, where we see that the control of DCM operation may be less tricky than CCM. Nonetheless, we selected an IC that can perform control. Thus, we chose CCM so that we could design our parameters in simpler linear relations.

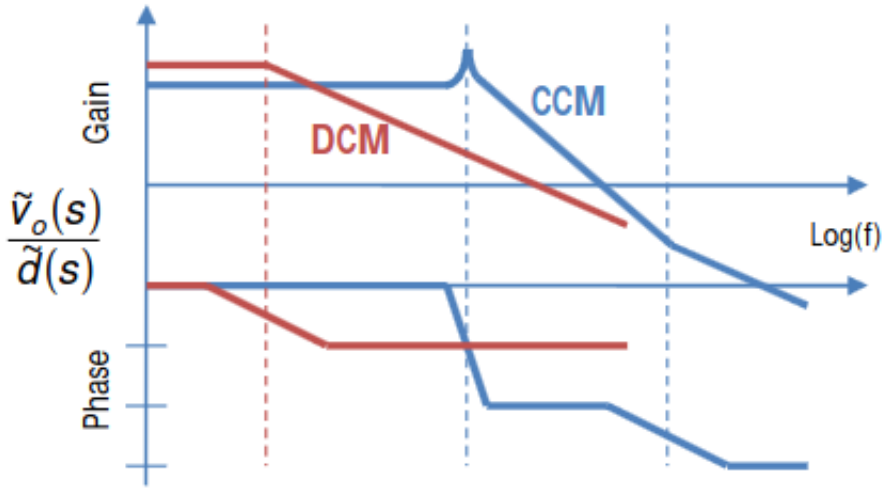

Figure 2: Bode plots in DCM and CCM

- Switch frequency f_s selection:

  We decided to operate at 200 KHz because it is possible by both by analog and digital controllers. All other selections were made upon this selection.

- Turns ratio $N = \frac{N_2}{N_1}$ selection:

  Input voltage ranges between 12V and 18V while output voltage must remain constant. In the ideal lossless case the voltage relation of a flyback converter is given as:

$$V_o = \frac{N_2}{N_1} \frac{D}{1 - D}$$

  Plot 3 shows the variation of maximum and minimum required duty cycle with respect to different $N = \frac{N_2}{N_1}$.

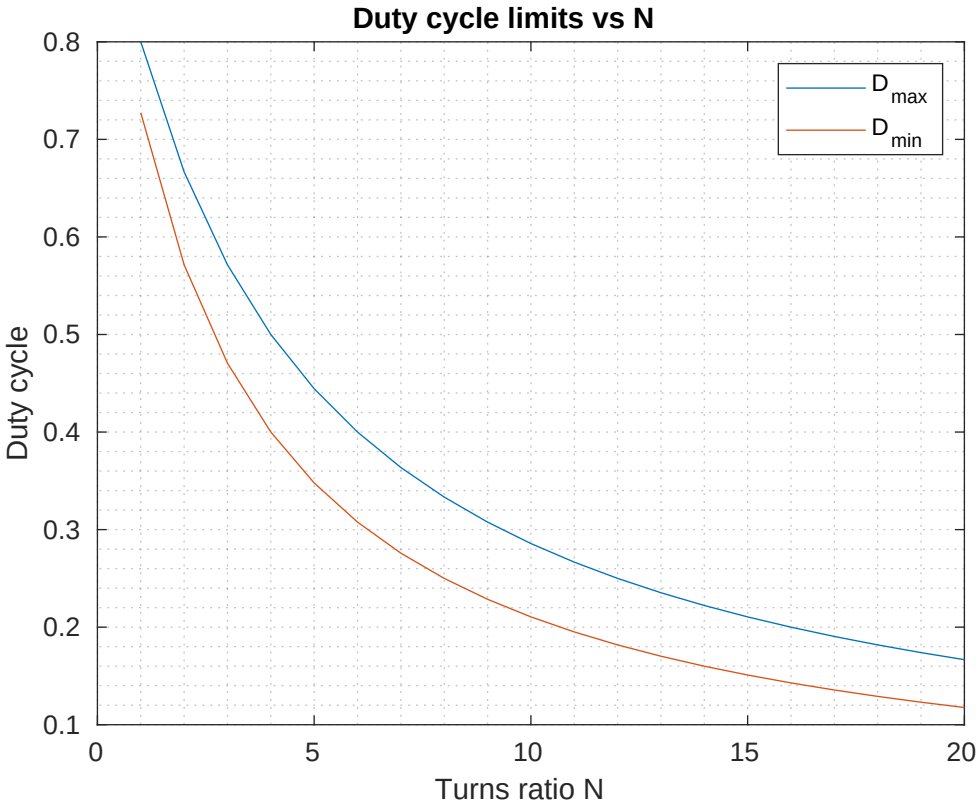

Figure 3: D vs N plot of Flyback converter

Using this plot, we decided on out duty cycle range. 0.4-0.5 is a good nominal operating interval because it allows us to compensate for unprecedented increase and decrease requirements. Therefore, we set the turns ratio as $N = 4$.

- Magnetizing inductance L_m selection:

  Next, we needed to determine the magnetizing inductance L_m. The key idea in choosing L_m is to both ensure CCM is possible and to use as much of the flux bearing capabilities of the core as possible. We decided 40% magnetizing current ripple is a reasonable value because it means we can continue to work in CCM even if load is much less than its rated value.

  Similarly to the previous part, we have used MATLAB to create the plot of required magnetizing inductance for each input current average case. Then we made sure that the inductance value satisfies the maximum 40% i_M ripple constraint in all cases. To do so, we have used the characteristic plots of the flyback converter to derive the following relationship:

$$I_{LM,avg} = \frac{I_{in,avg}}{D}$$

  Then, assuming a predicted and not so absurd 88% efficiency value, we determined the input current average for a number of input voltages. Finally, the given relation determines the L_m value with respect to any desired current ripple and input current:

$$L_m = \frac{V_{in}D}{f_{sLM}}$$

Figure 4 illustrates the relationship between the input voltage and the required L_m to ensure maximum 40% magnetizing current ripple.

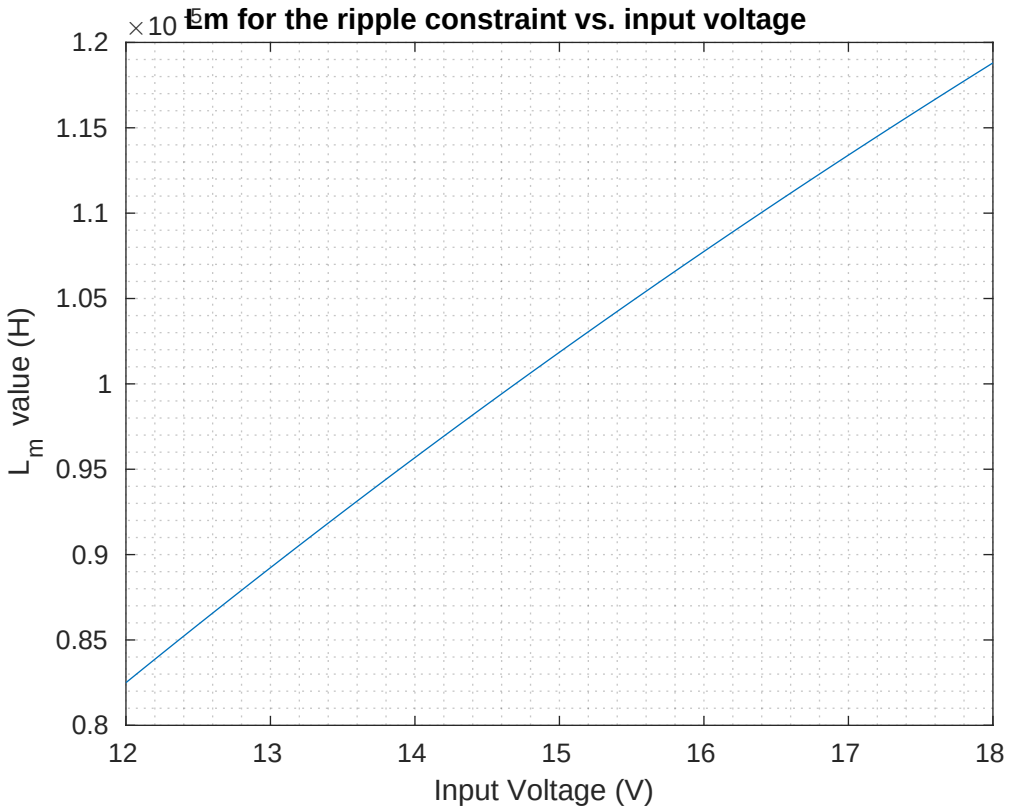

Figure 4: Required L_m at each input voltage

Referring to the Figure 4 we decided to set $L_m = 12\mu$H. Note that this value overestimates L_m than its ideal case.

Now we assure CCM operation and determine the output current limits for constant output voltage and varying input voltage. We continue with perfect efficiency in this calculation.

At the DCM and CCM boundary,

$$\Delta i_{LM} = 2i_{LMavg}$$
$$\frac{V_s D T_s}{L_m} = 2i_{LMavg} = \frac{2i_{in,avg}}{D}$$

Table 1: DCM boundary output average currents at maximum and minimum input voltage

Input Voltage (V)	**DCM Boundary Current (mA)**
12	156
18	225

Referrring to Table 4, we see that the least output current must be larger than 225 mA, which roughly corresponds to 25 % load. Even in this case, we continue to operate at CCM.

Table 2 is a table summarizing the electrical parameters of our flyback converter.

Table 2: Electrical Parameters of the Converter

Parameter	Value
DCM vs CCM	CCM
f_s	200 KHz
N	4
L_m	12μH

3 Magnetic Design

After finalizing L_m parameter, we then worked on magnetic design. A quick market research showed that many cores were not readily available on the market. Thus, we went on with a upcycled ferrite core. The reused ferrite core in hand is an E core made up of 3C94 material [1].

The concerns in magnetic design are whether or not the core gets saturated, if and how much air gap must be present and whether or not there is enough room to wind the wires around the legs of the core.

3.1 Core Design

Figure 5 is a photograph of our E core. All decisions are made for this core. There are two main parameters in core design; namely, air gap length and turn number.

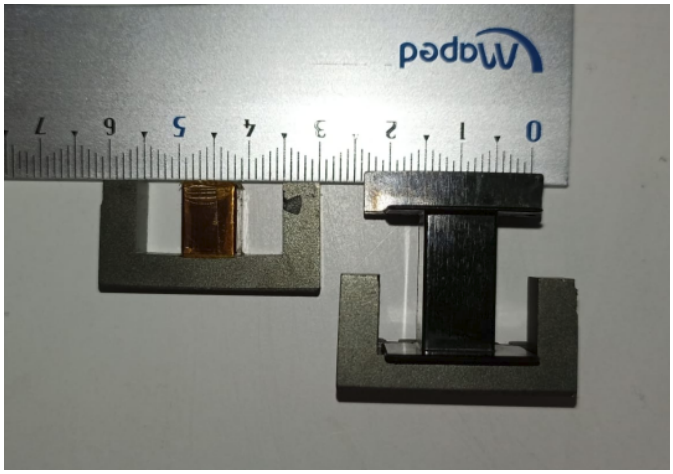

Figure 5: Our E core

Firstly, an air gap is necessary for flyback converters because flyback converter stores energy in the core during on time and releases the energy to the load during off time. Therefore, air gap is used to enhance the energy storing capability of the core.

- Gap length and primary side winding turn number:

  Up to this point, we only had the decision of $L_m = 12\mu$ H at hand and the inductance relation:

$$L = \frac{N_p^2}{R}$$

Reluctance is a function of air gap length so inductance is a function of both decision parameters. As an easy way of choosing both parameters at once, we decided to plot the variation of one parameter with respect to the other for the given inductance value. Since the permeability of air is much smaller than ferrite material, reluctance of the core with the gap almost equals the reluctance of the air gap. Therefore, we assumed core reluctance is zero without the air gap to have a sense of air gap and turn number. Figure 6 is the plot we obtained.

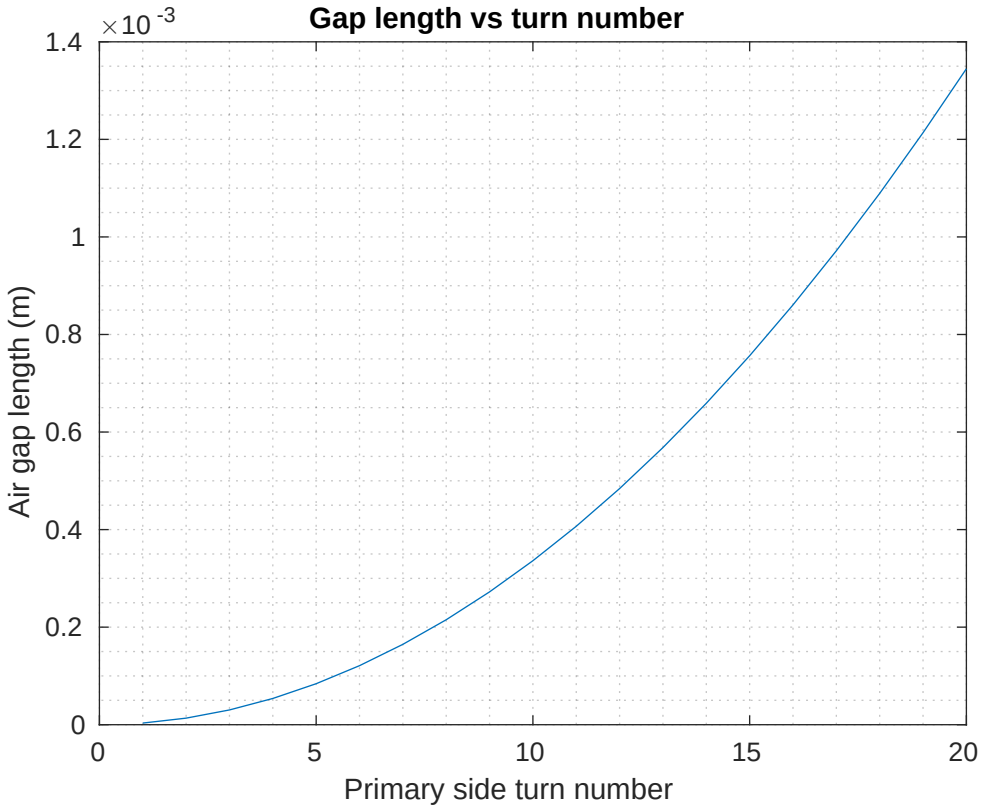

Figure 6: Air gap length and primary side turns for $L_m = 12\mu$H

After some iterations, we set primary side turn number to 9 so that air gap length is approximately 0.27mm. For reference, thickness of A4 paper is almost 0.1 mm. Note that almost 3 papers thick air gap verifies our approximation for the equivalent reluctance. Indeed, the reluctance of the air gap is 6750000 $\frac{Aturns}{Wb}$.

- Core magnetic flux density:

  One of the most important criteria in core design is ensuring the core stays linear, at least however much real life permits. To check this, maximum possible magnetizing current peak should not disrupt core linearity. In other words, such a flux should not lead to saturation.

  We have used the approximate reluctance value to sweep across primary peak currents to obtain the operating level flux densities.

$$I_{pri,peak} = I_{LMavg} + I_{LMavg}\frac{ripple\ ratio}{2}$$

The outer legs of the E core are slightly smaller in area than the middle leg. Therefore, magnetic flux densities are different at these two types of legs. We see both densities in figure 7.

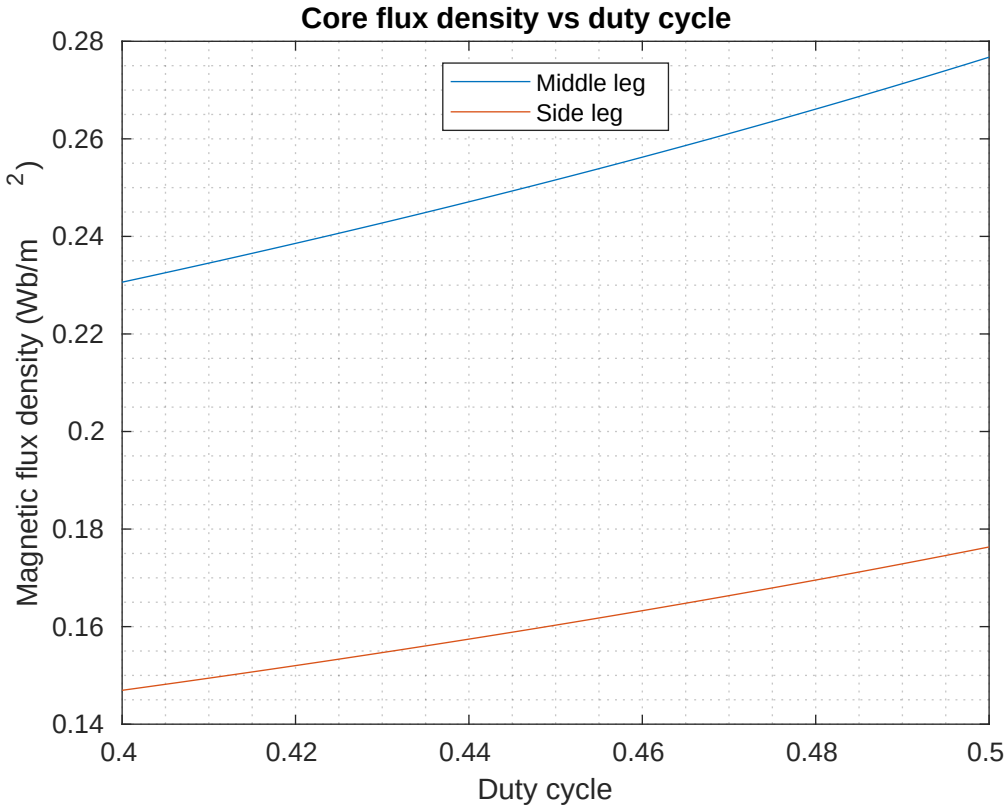

Figure 7: B field density vs duty cycle

The material saturates at around 300 mT [1] so we are within the limits and the converter remains linear.

Table 3: Core design parameters

Parameter	Value
Primary side turn number	9
Secondary side turn number	36
Air gap length	0.27mm
B field	140 mT - 280 mT

3.2 Winding Design

For the actual wires of the flyback transformer we considered two alternatives. The first analysis is done with standard single strand copper wires. First consideration on this is the skin depth since the switching

frequency is selected as 200 kHz and related AC losses are affected by skin depth a lot. For the selected F_{sw} the skin depth results in,

$$\delta = \sqrt{\frac{\rho}{\pi F_{sw} \mu_0}} = 1.4587 \cdot 10^{-4} m$$

Later, maximum allowable strand cross-section is yields,

$$\text{Strand Area} = \pi\delta^2 = 0.0668 mm^2$$

This is around 29 AWG. Current rating of this wire gauge is 0.182 amperes however we can define a risk factor to push the copper a little more to utilize the core more effectively. In another words, with a risk factor of 2 double the amount of current will pass through the wire.

The RMS of the input current is calculated as 4.55 amperes. Number of primary strands is, this RMS current divided into each strand. The result is we would need 33.3 parallel strands.

A side note on this is that the input current is highly discontinuous at the switching frequency. It does not have a ripple over a fixed current hence by the frequency decomposition, the component at the switching frequency is quite large.

For the secondary side, same analysis can be made. Again using the RMS value of the current over the transformer. This results in 7.33 parallel strands.
Primary wire count is number of parallel strands multiplied with the turn number,

$$\text{Primary Wire Area} = N_{pri} \cdot primary\_parallel = 1.9391 \cdot 10^{-5}$$

For the secondary

$$\text{Secondary Wire Area} = N_{pri} \cdot turns\_ratio \cdot secondary\_parallel = 1.7064 \cdot 10^{-5}$$

Numbers seem high however this consist of both parallel strands and the full wire length and it will be used to calculate the fill factor.

$$\text{Fill Factor} = \text{Total Wire Area/Total Window Area} = 31.87\%$$

Although the parallel wires are effectively acting as litz wires, a design with the actual litz wires are made, The design is given below and the total copper and fill factor are similar. This second design is expected to be better since the proximity and skin effect related losses will be less.

Turn Numbers	**Wire Diameter and # of Parallel**
9	0.9 mm × 2
36	0.9 mm × 1

Table 4: Transformer Winding Design with Litz Wire

The fill factor of the design with litz wire is calculated as 30%
This fill factors are both within the reasonable limits. The fill factors of 30 percent can be easily wound. The expected fill factor is actually will be smaller since the litz wire have around 1.28 packing factor which means that it has 0.22 percent empty spaces inside. On the hand created litz case, this is expected to be lower.

3.3 Losses

3.3.1 Copper Loss

For the copper loss we need to calculate the wire primary and secondary, total wire lengths.
The primary wire length calculated is 0.3341 meters. The secondary counterpart is 2.6964 meters.
The resistance is calculated as,

$$\text{R\_pri} = \frac{\rho l_{pri}}{A \cdot N_{parallel}} = 0.0056\Omega$$

$$\text{R\_sec} = \frac{\rho l_{sec}}{A \cdot N_{parallel}} = 0.0911\Omega$$

Power is then $P = i \cdot R^2$ with the RMS currents.
The total copper loss is, for primary 0.1586 W and for secondary 0.1916 W.
Total is calculated at the highest currents hence the performance will be better.

3.3.2 Core Loss

The core loss is calculated from the power loss density and the peak magnetic flux density curves at fixed frequency given by the manufacturer on the datasheet of the related core.
These are empirical values and the our selected data is from 200 kHz line.
The datapoints from the datasheet is digitized on matlab and a polynomial equation is fitted.
The magnetic flux density is different on the side legs of the E core than the center leg hence two volumes are calculated seperately.
The total loss is calculated from the ΔB but the data is for AC magnetic flux variation hence ΔB given is expected as the right approach for more accurate calculation. A safety factor of 2 is given for margins of errors. The total core loss for highest operation is found as 1.22 W.

4 Computer Simulations & Analysis

4.1 Ideal Simulations

After determining a value for L_m, ideal simulations are done in LTspice. Ideal Flyback converter circuit constructed for the simulation is given in Figure 8. The model includes an ideal diode, an almost ideal switch, an ideal transformer model with magnetizing inductance, and an output capacitance whose value is calculated to make output peak-to-peak voltage ripple equal to 2%. The components named with ”spice magic” are only included to increase simulation speed.

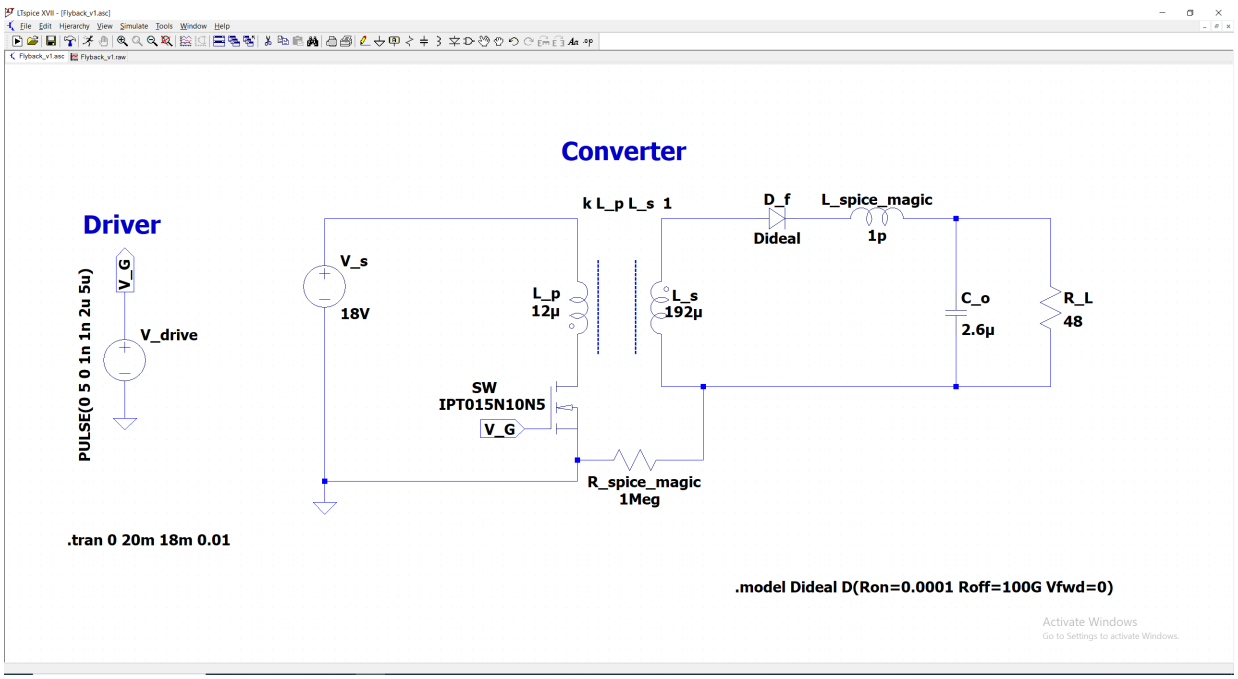

Figure 8: Simulated LTspice circuit schematic (ideal case)

The design choices were made so that the magnetizing current ripple is at least 40%. Primary and secondary current waveforms are given in Figures 9 and 10 for $12V$ and $18V$ input voltages, respectively. As one can see, we have desired current ripple which is consistent with our design.

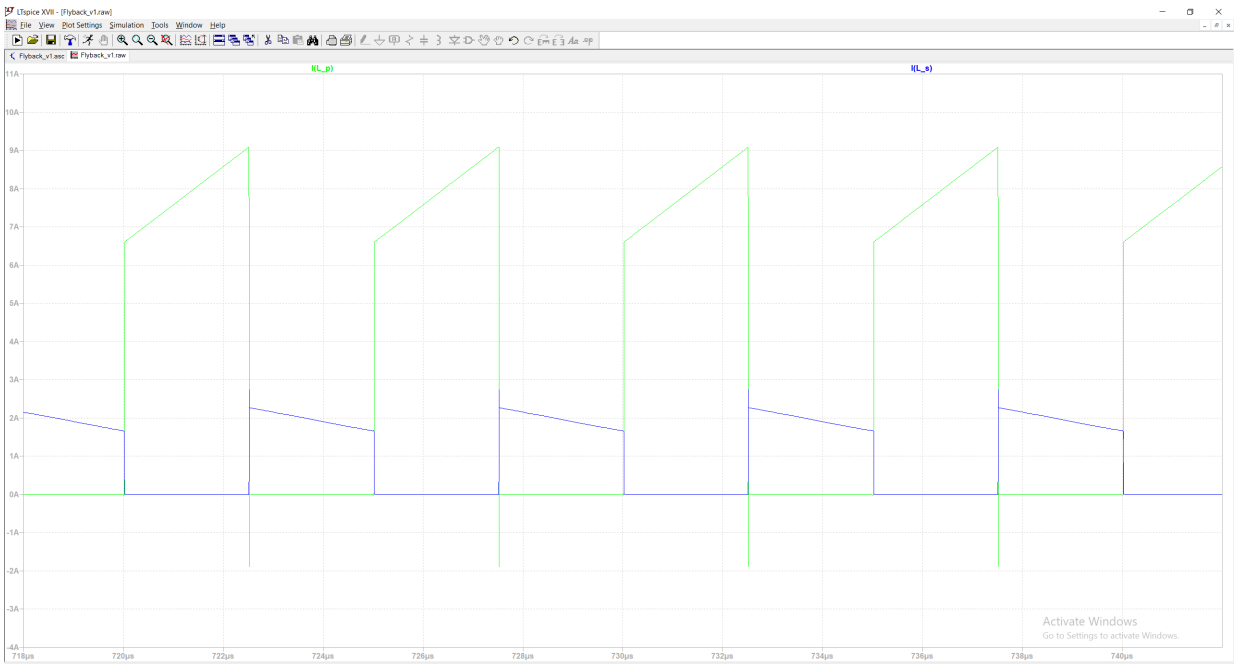

Figure 9: Primary and secondary current waveforms for 12V input voltage

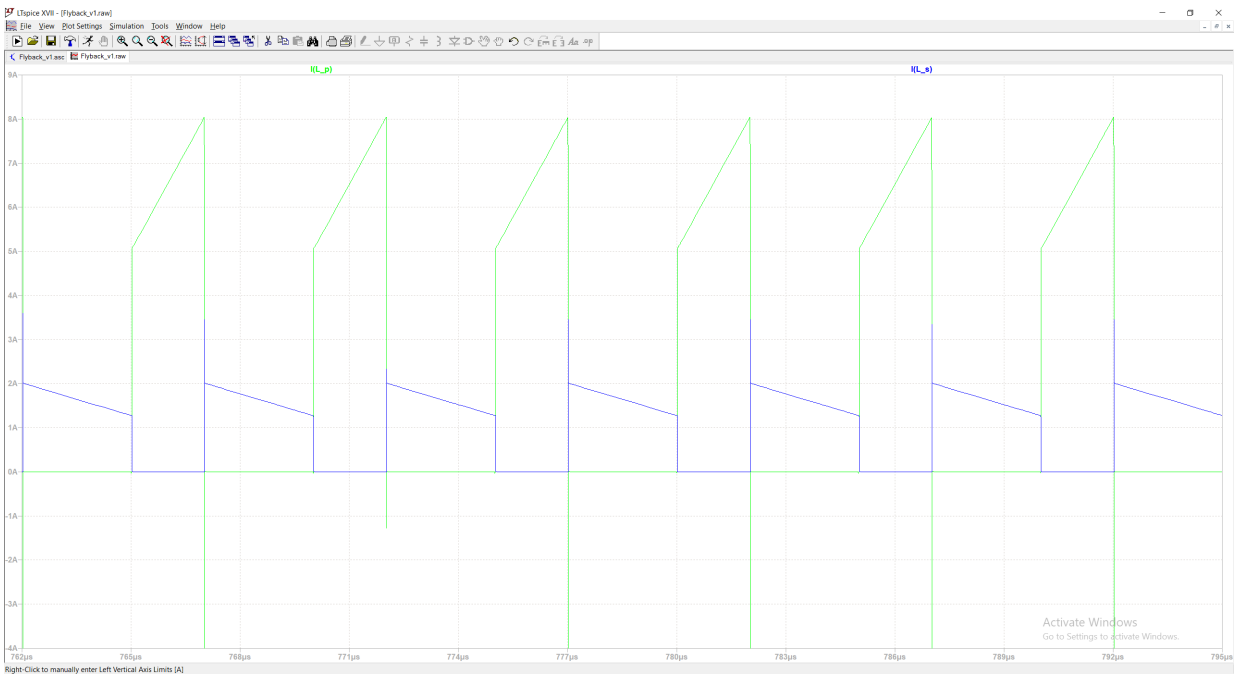

Figure 10: Primary and secondary current waveforms for 18V input voltage

We also observed the voltage stresses on the diode and on the switch in the simulation. The expected switch voltage during the off times are calculated as $V_{SW} = V_s + V_o \frac{N1}{N2} = 30V$, which is calculated for 18V input voltage (worst case). Also, the diode voltage is calculated as $V_D = V_s \frac{N2}{N1} + V_o = 120V$ during on times of the switch, again for the worst case. One can see from Figure 11 that the simulation result is consistent with the theoretical one.

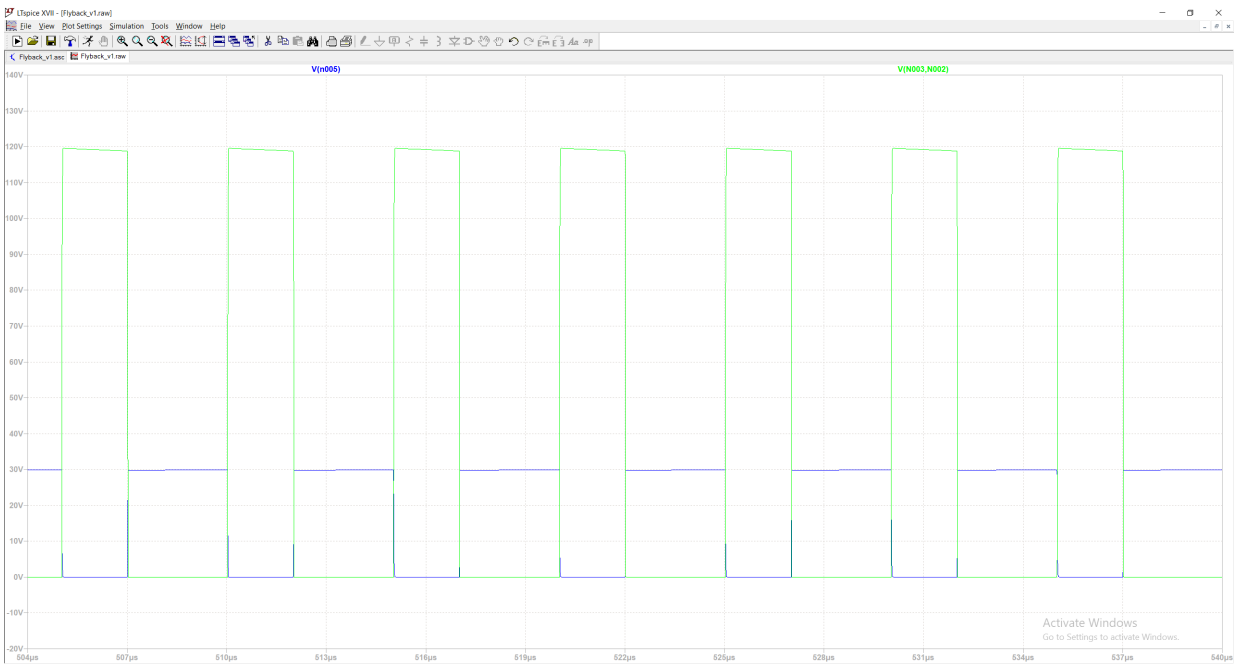

Figure 11: Diode and switch voltage stresses for 18V input voltage

Finally, the output voltage ripple can be calculated using the equation $\frac{\Delta V_o}{V_o} = \frac{D}{RCf_s} \approx 2\%$. One can see it

is consistent with Figure 12.

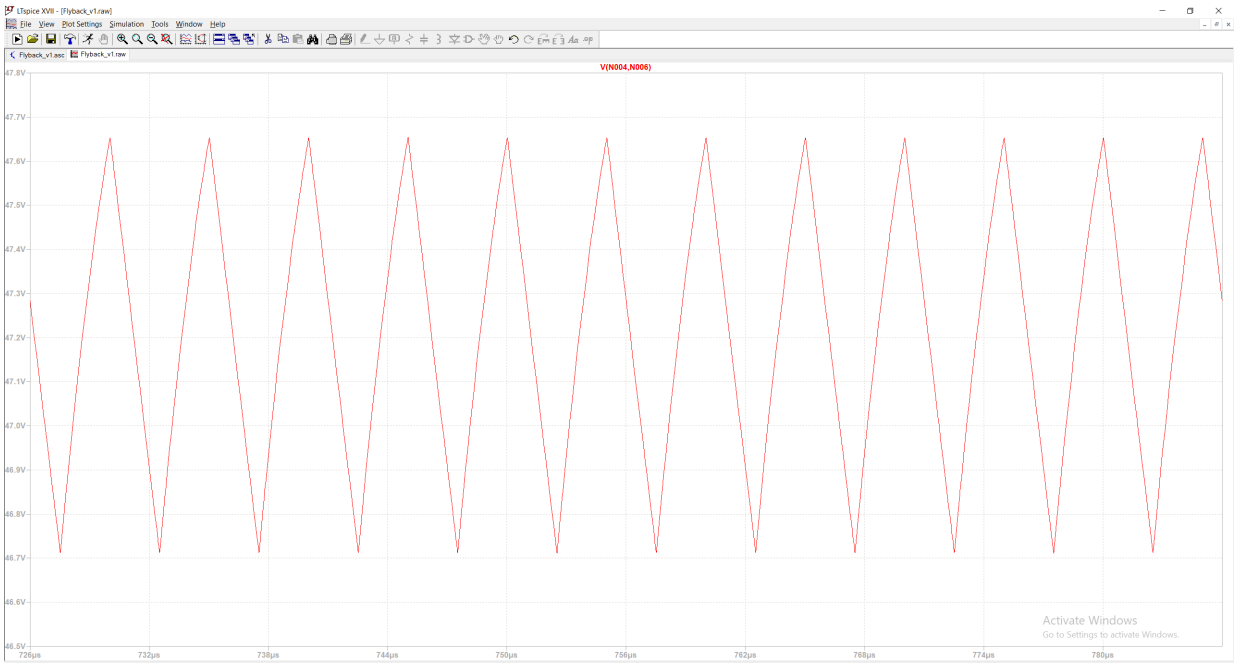

Figure 12: Output voltage waveform

4.2 Non-ideal Simulations

The parasitic effects, leakage inductances (which are calculated as 1% in the former sections), and non-ideal semiconductors are added to the ideal circuit. When we include the parasitic effects and simulate the circuit for 12V input voltage, the leakage inductance creates high voltage stress on the MOSFET during the transition to off-state. This will not blow up our MOSFET as the avalanche energy of the MOSFET is enough to absorb all the energy stored in the leakage inductance. However, since the voltage swing caused by the ringing will be too high, we either had to design a snubber or use a TVS (Transient Voltage Suppression) diode. We made simulations with a TVS diode with 30V rating, which is also included in the schematic. The non-ideal model of the circuit can be seen in Figure 13.

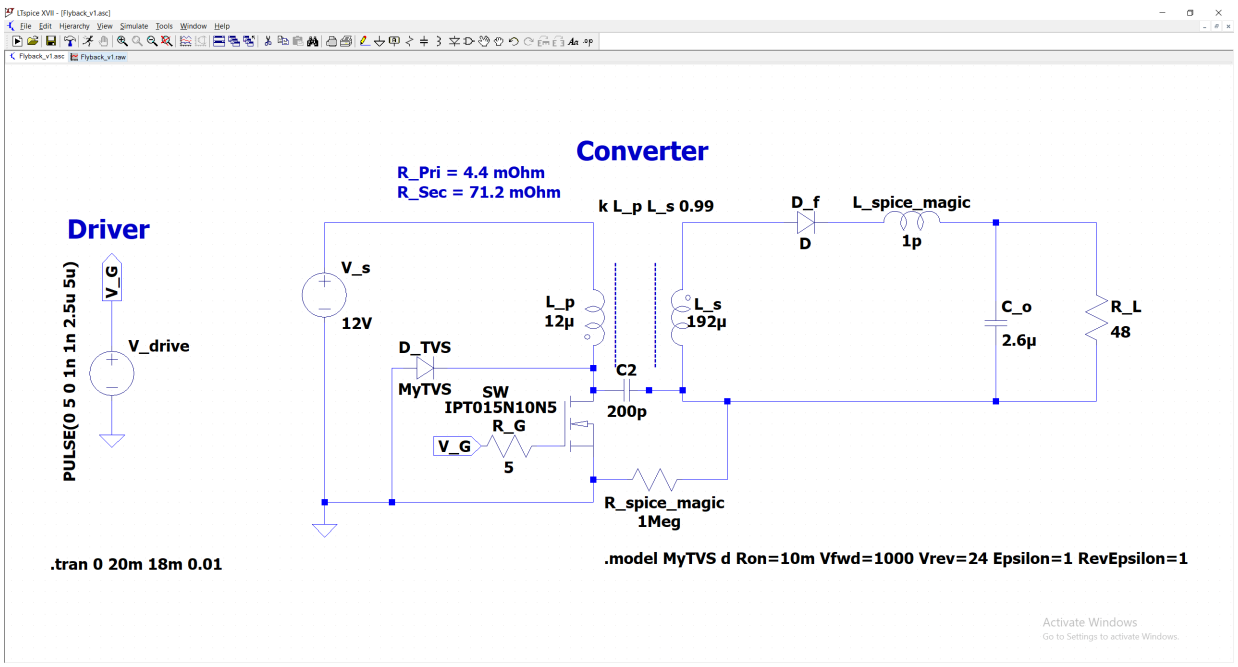

Figure 13: Simulated LTspice circuit schematic (non-ideal case)

Still, there will be some amount of ringing due to the unsuppressed energy. We will see its effect on the transients of the waveforms. The non-ideal simulation results for magnetizing current ripples are given in Figure **??**. The voltage stress on the switch is seen in Figure 15. Finally, the output voltage waveform is given in Figure 16. Note that with the duty for ideal case (which is 50% for 12V input) the output voltage is reduced to 40V. However, since the analog IC does close-loop control, it can increase the duty as much as it is required. Figure 16 shows the output voltage for 12V and 54% duty, also showing that our circuit is still stable at this operating point.

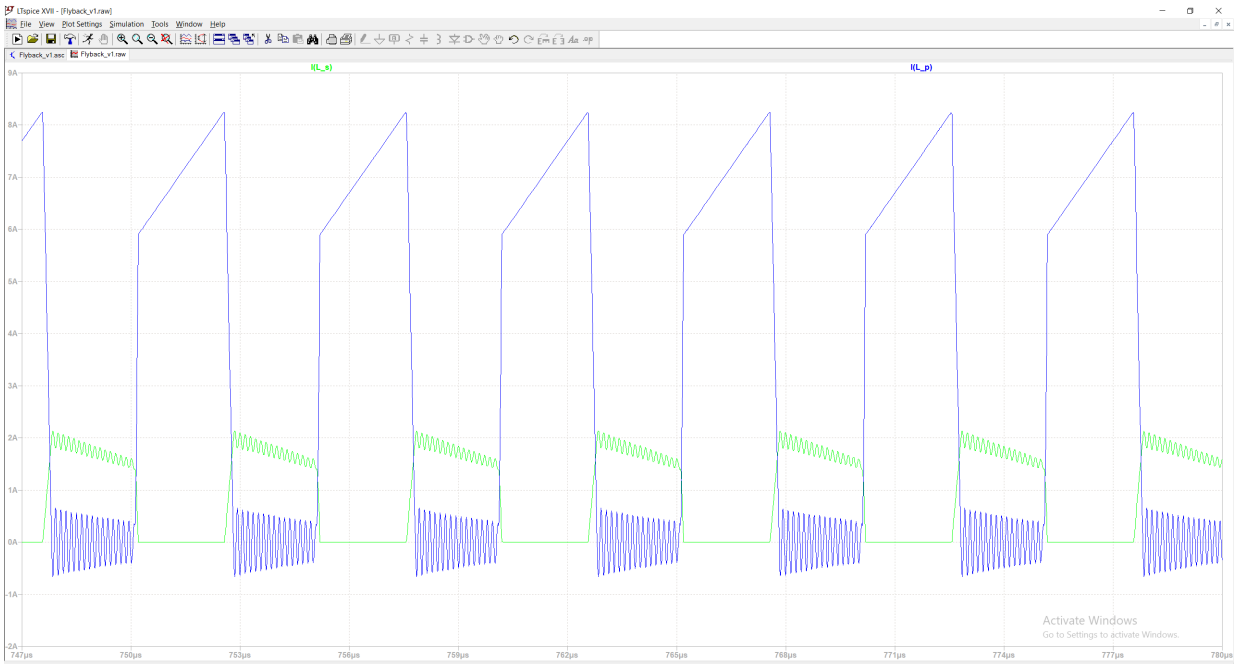

Figure 14: Primary and secondary current waveforms for 12V input voltage (non-ideal case)

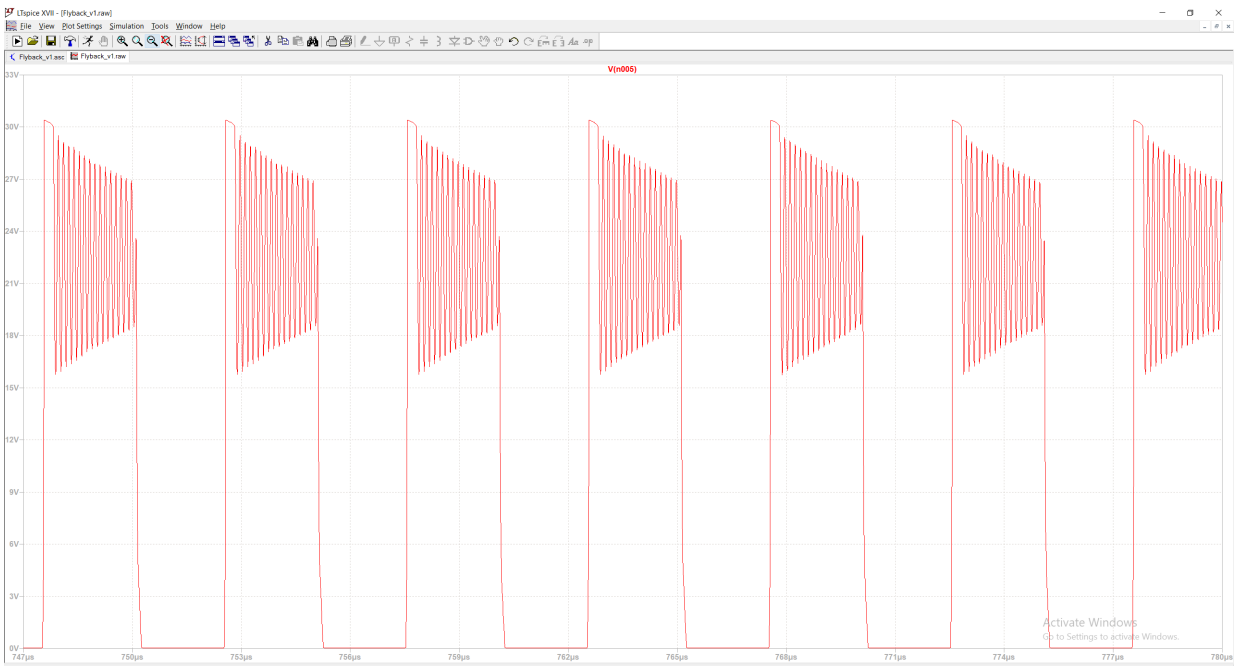

Figure 15: Switch voltage stress for 12V input voltage (non-ideal case)

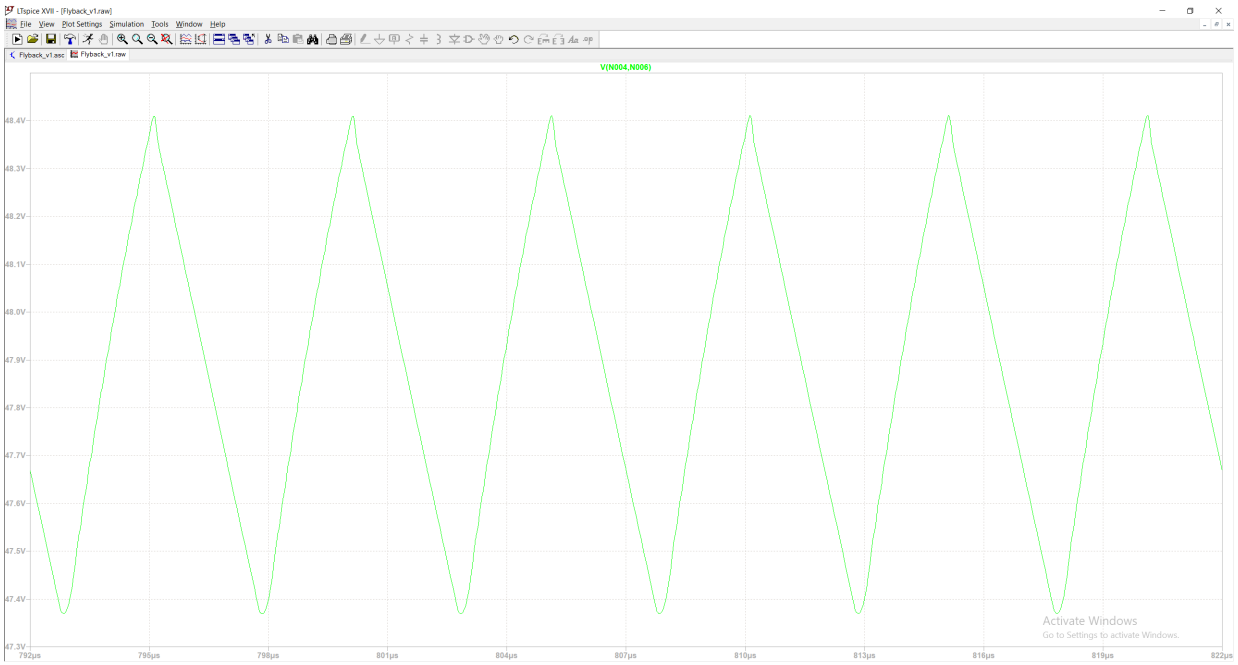

Figure 16: Output voltage ripple with 54% duty (non-ideal case)

5 Component Selection

Aside from the core, which was luckily found, there are 4 components to choose.

- IC: UC3843AN [2].

The criteria in choosing the PWM controller IC were that it is able to operate at out input voltage range so that no auxilliary windings are necessary and that it has no PWM limit.

UC3843AN satisfies both constraints. It operates at voltages higher than 8V and can provide 100% duty cycle. A separate feedback network can be built and connected to the IC for closed loop operation. Moreover, it can provide up to 1A gate current.

- MOSFET: CSD19534Q5A [3]

  The most important criteria in MOSFET selection are rated voltage and current as well as slew rate. CSD19534Q5A has 100V rating in addition to having 10A current rating. This MOS also benefits from low losses thanks to $12.6m\Omega$ on resistance.

- Diode: PDS3200-13 [4].

  The diode in the flyback converter suffers from high voltage stress because of secondary turn number being higher and the transformer polarity being reversed. In our simulations we saw the diode voltage climbed as much as 120V. Therefore we chose PDS3200-13, which has 200V, 3A rating as well as 780 mV forward voltage.

- Ceramic Capacitor: CL31B225KCHSNNE [5].

  The output capacitor is chosen as 2.2μF CL31B225KCHSNNE and two of these will be connected in parallel. The device itself is rated for 100V which is above 48V for safety reasons. Moreover, the datasheet provides ESR vs frequency rating for the device and at 200 KHz this capacitor have approximately $30m\Omega$ ESR. Two of them in parallel have even lower ESR.

- Core clamp: B66232A2010X000 [6]

  We have also selected a core clamp according to dimensions of our E core.

6 Discussions & Future Work

Magnetic design and the simulations for the specific requirements of the project is completed successfully. The next steps will be to wound the core with the determined parameter, and make the necessary measurements using LCR meter. We actually miscalculated L_m as $30\mu H$ at first and wound the primary winding according to that. We observed that we made consistent calculations with the measurement, which is seen in Figure 17. After we wound the core, we will finalize our design and draw our PCB to be produced.

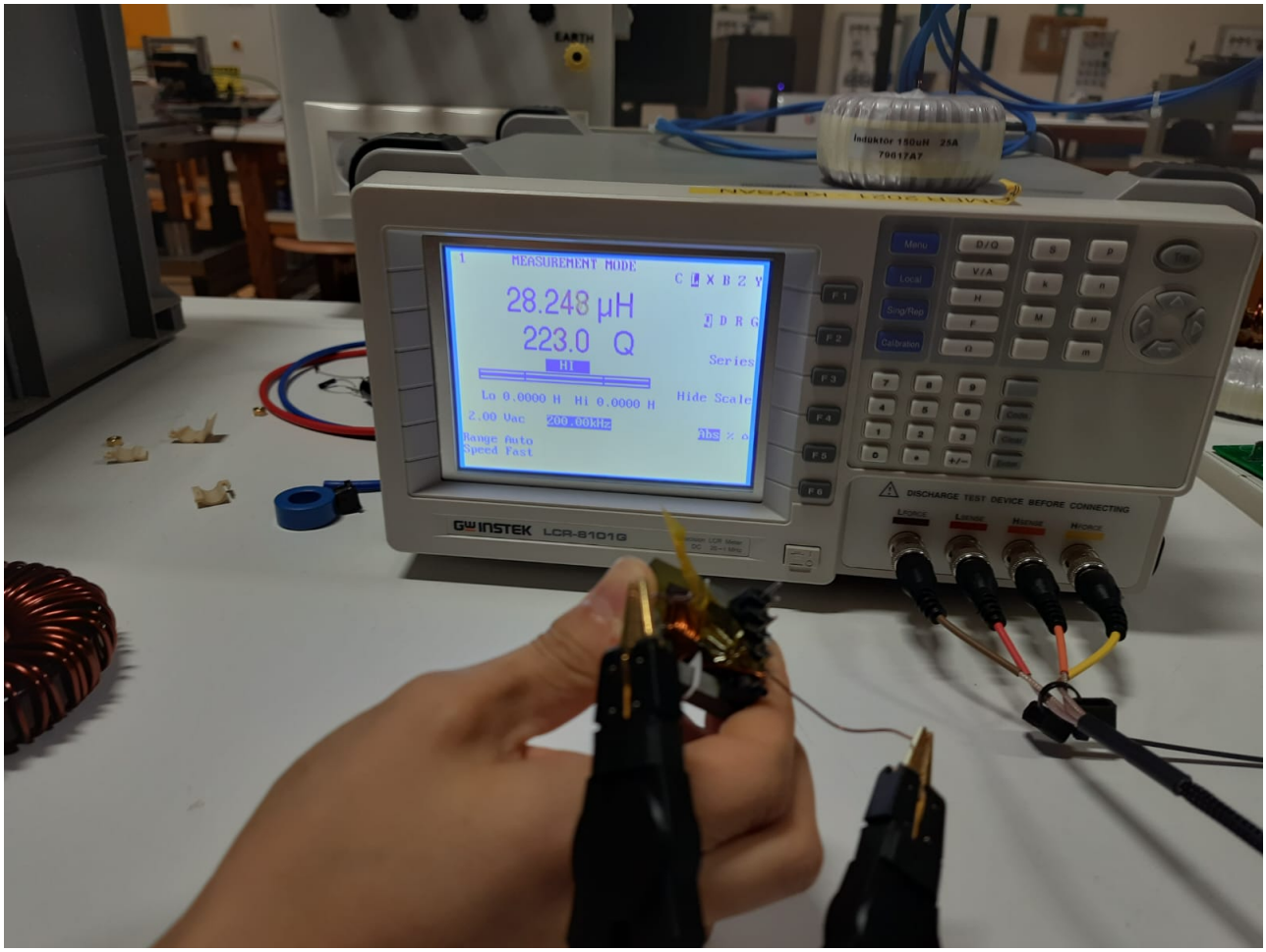

Figure 17: Proof-of-concept inductance measurement

7 References

[1] https://www.ferroxcube.com/upload/media/product/file/Pr_ds/E30_15_7.pdf

[2] https://ozdisan.com/entegre-devreler-ics/guc-entegreleri/dc-dc-voltaj-kontrolorleri/UC3843AN/732711

[3] https://ozdisan.com/Product/Detail/594986/CSD19534Q5A

[4] https://www.digikey.com/en/products/detail/diodes-incorporated/PDS3200-13/697102

[5] https://www.digikey.com/en/products/detail/samsung-electro-mechanics/CL31B225KCHSNNE/3888796

[6] https://www.digikey.com/en/products/detail/epcos-tdk-electronics/B66232A2010X000/3915550

[7] https://www.icbanq.com/icbank_data/online_seminar_image/Flyback_CCMVsDCM_Rev1p2.pdf