

EE464 2023 Spring

Hardware Project Final Report

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1 Introduction

This is the final report which is the complete design report for the hardware project of EE464 Static Power Conversion II course, prepared by the group Mind the Cap. The aim of this project is to implement a flyback converter topology to convert an input voltage range of 12-18V to 48V at 1A rated current (48W output). In this report, the reader will find our decision process for topology selection, electrical and magnetic parameter selections, controller design, computer simulations, loss calculations, component selections, and experiment results of the implemented converter. The report is concluded with the evaluation of the design process and the results.

2 Topology

2.1 Topology Selection

We have decided to build a flyback converter. Basic topology of a flyback converter is given in Figure 1.

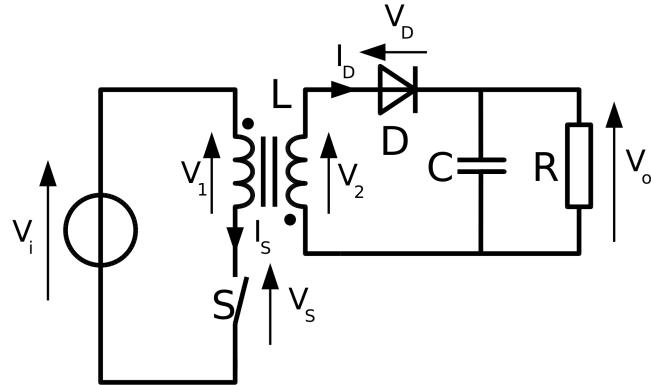


Figure 1: Flyback converter

Our alternative in choices were active clamp flyback converter and forward converter. The dominant advantages of active clamp topology are increased efficiency by applying ZVS and reduced switch voltage stress, which can also be achieved with snubbers in ordinary flyback converters. Although seemingly advantageous, we had to abandon the idea of active clamp flyback converter because all IC's we could find had startup voltages higher than the input voltage range of the project. This meant we had to use a digital controller, but it had to be quite precise to switch at the correct instant so that efficiency would be high and circuit would be linear. Our second alternative, forward converter, was disregarded because forward converter requires two inductors and two diodes. We preferred less components to deal with.

2.2 Parameter Selection

There are two main parameters in a flyback converter: the magnetizing inductance of the transformer and the turns ratio.

- DCM vs CCM selection:

According to [7], peak MOSFET and diode currents are higher in DCM. Further, DCM losses are claimed to be higher than CCM losses. Combined with the fact that DCM means nonlinear operation, it may seem as if it is all negative. However, the same source provides the typical Bode plots of CCM and DCM, where we see that the control of DCM operation may be less tricky than CCM. Nonetheless, we selected an IC that can perform control. Thus, we chose CCM so that we could design our parameters in simpler linear relations.

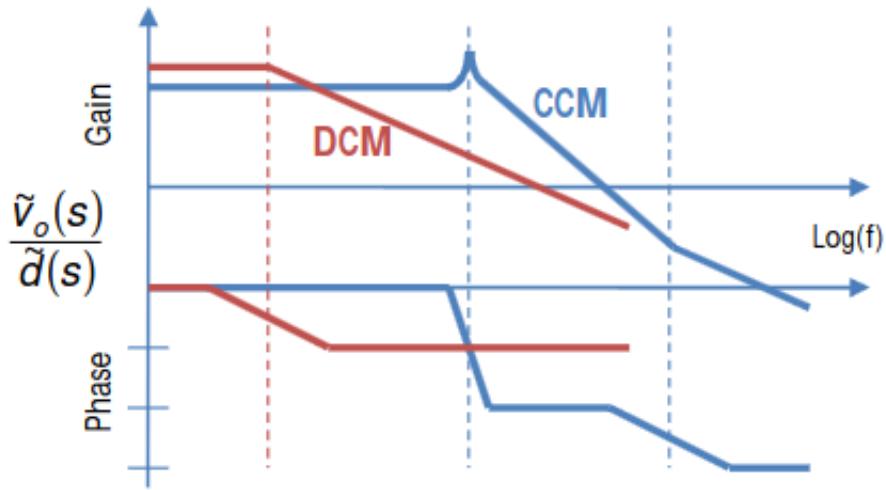


Figure 2: Bode plots in DCM and CCM

- Switch frequency f_s selection:

We decided to operate at 200 KHz because it is possible by both by analog and digital controllers. All other selections were made upon this selection.

- Turns ratio $N = \frac{N_2}{N_1}$ selection:

Input voltage ranges between 12V and 18V while output voltage must remain constant. In the ideal lossless case the voltage relation of a flyback converter is given as:

$$V_o = \frac{N_2}{N_1} \frac{D}{1 - D}$$

Plot 3 shows the variation of maximum and minimum required duty cycle with respect to different $N = \frac{N_2}{N_1}$.

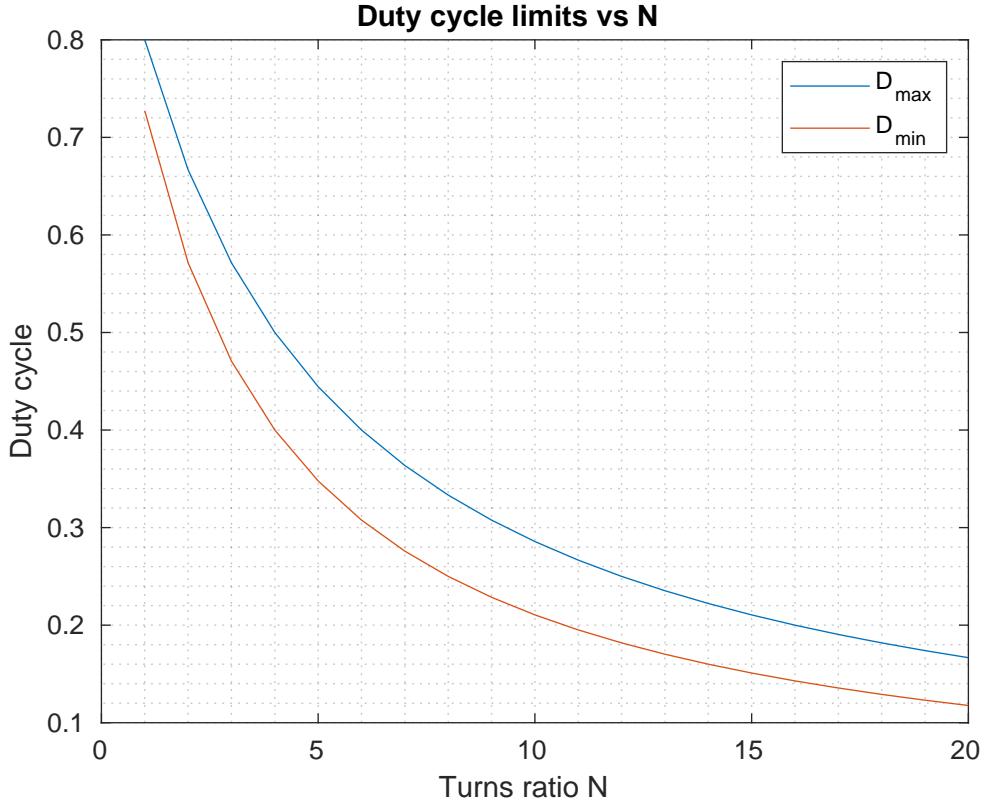


Figure 3: D vs N plot of Flyback converter

Using this plot, we decided on out duty cycle range. 0.4-0.5 is a good nominal operating interval because it allows us to compensate for unprecedented increase and decrease requirements. Therefore, we set the turns ratio as $N = 4$.

- Magnetizing inductance L_m selection:

Next, we needed to determine the magnetizing inductance L_m . The key idea in choosing L_m is to both ensure CCM is possible and to use as much of the flux bearing capabilities of the core as possible. We decided 40% magnetizing current ripple is a reasonable value because it means we can continue to work in CCM even if load is much less than its rated value.

Similarly to the previous part, we have used MATLAB to create the plot of required magnetizing inductance for each input current average case. Then we made sure that the inductance value satisfies the maximum 40% i_M ripple constraint in all cases. To do so, we have used the characteristic plots of the flyback converter to derive the following relationship:

$$I_{LM,avg} = \frac{I_{in,avg}}{D}$$

Then, assuming a predicted and not so absurd 88% efficiency value, we determined the input current average for a number of input voltages. Finally, the given relation determines the L_m value with respect to any desired current ripple and input current:

$$L_m = \frac{V_{in}D}{f_s \Delta I_{LM}}$$

Figure 4 illustrates the relationship between the input voltage and the required L_m to ensure maximum 40% magnetizing current ripple.

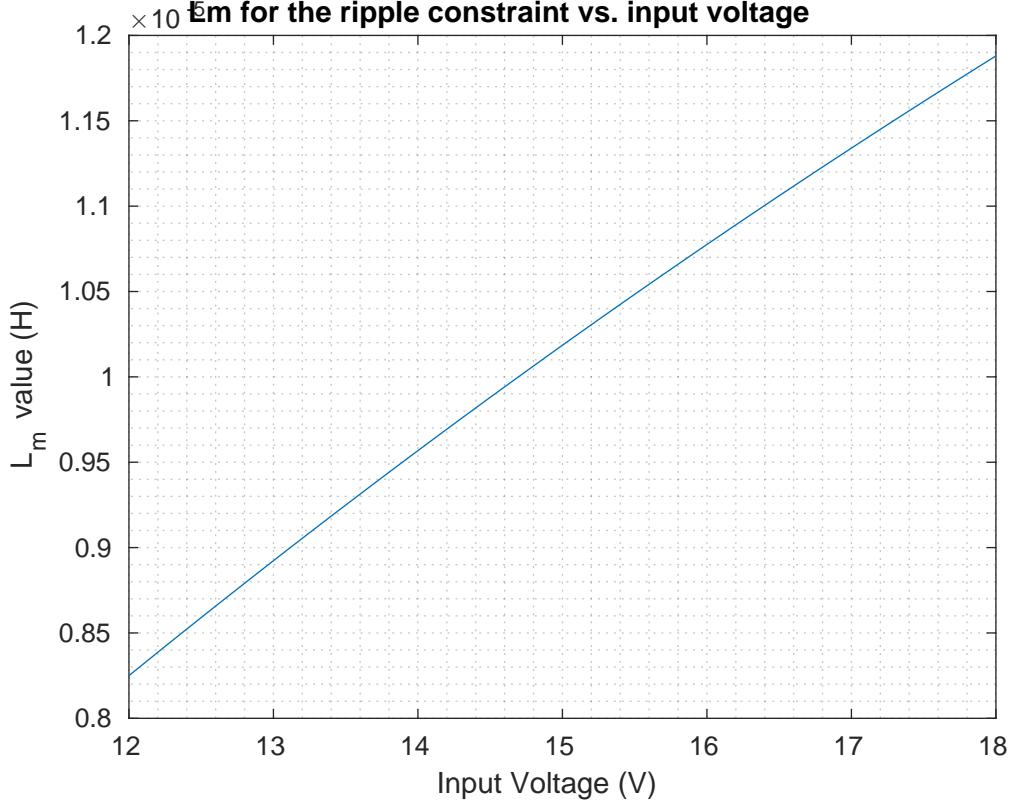


Figure 4: Required L_m at each input voltage

Referring to the Figure 4 we decided to set $L_m = 12\mu\text{H}$. Note that this value overestimates L_m than its ideal case.

Now we assure CCM operation and determine the output current limits for constant output voltage and varying input voltage. We continue with perfect efficiency in this calculation.

At the DCM and CCM boundary,

$$\Delta i_{LM} = 2i_{LMavg}$$

$$\frac{V_s DT_s}{L_m} = 2i_{LMavg} = \frac{2i_{in,avg}}{D}$$

Table 1: DCM boundary output average currents at maximum and minimum input voltage

Input Voltage (V)	DCM Boundary Current (mA)
12	156
18	225

Referrring to Table 5, we see that the least output current must be larger than 225 mA, which roughly corresponds to 25 % load. Even in this case, we continue to operate at CCM.

Table 2 is a table summarizing the electrical parameters of our flyback converter.

Table 2: Electrical Parameters of the Converter

Parameter	Value
DCM vs CCM	CCM
f_s	200 KHz
N	4
L_m	$12\mu\text{H}$

3 Magnetic Design

After finalizing L_m parameter, we then worked on magnetic design. A quick market research showed that many cores were not readily available on the market. Thus, we went on with a upcycled ferrite core. The reused ferrite core in hand is an E core made up of 3C94 material [1].

The concerns in magnetic design are whether or not the core gets saturated, if and how much air gap must be present and whether or not there is enough room to wind the wires around the legs of the core.

3.1 Core Design

Figure 5 is a photograph of our E core. All decisions are made for this core. There are two main parameters in core design; namely, air gap length and turn number.

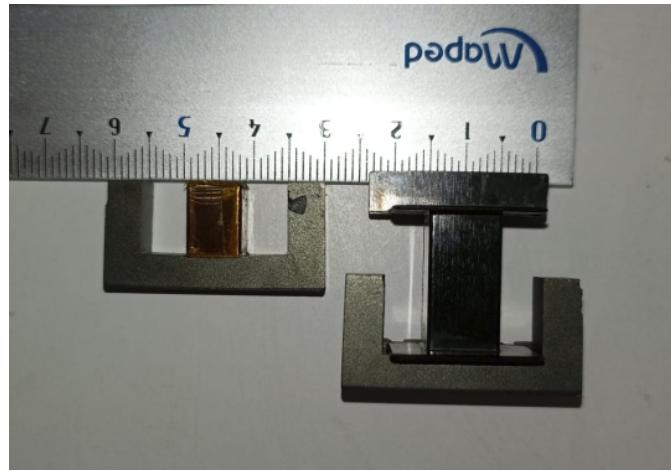


Figure 5: Our E core

Firstly, an air gap is necessary for flyback converters because flyback converter stores energy in the core during on time and releases the energy to the load during off time. Therefore, air gap is used to enhance the energy storing capability of the core.

- Gap length and primary side winding turn number:

Up to this point, we only had the decision of $L_m = 12\mu H$ at hand and the inductance relation:

$$L = \frac{N_p^2}{R}$$

Reluctance is a function of air gap length so inductance is a function of both decision parameters. As an easy way of choosing both parameters at once, we decided to plot the variation of one parameter with respect to the other for the given inductance value. Since the permeability of air is much smaller than ferrite material, reluctance of the core with the gap almost equals the reluctance of the air gap. Therefore, we assumed core reluctance is zero without the air gap to have a sense of air gap and turn number. Figure 6 is the plot we obtained.

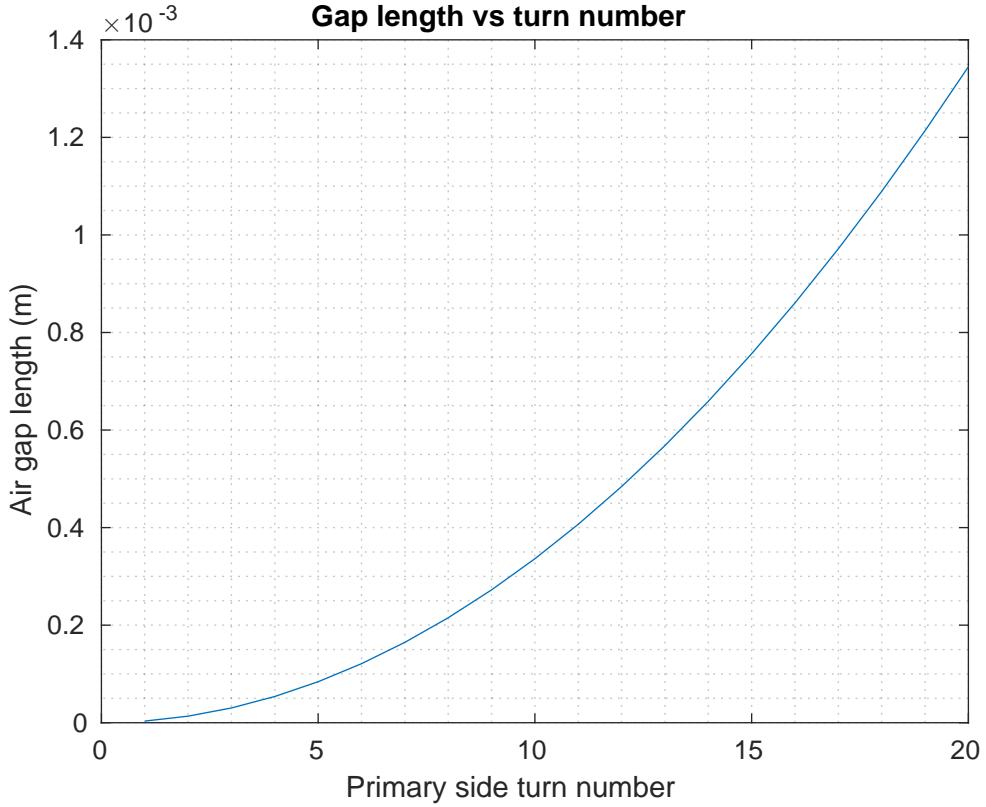


Figure 6: Air gap length and primary side turns for $L_m = 12\mu\text{H}$

After some iterations, we set primary side turn number to 9 so that air gap length is approximately 0.27mm. For reference, thickness of A4 paper is almost 0.1 mm. Note that almost 3 papers thick air gap verifies our approximation for the equivalent reluctance. Indeed, the reluctance of the air gap is $6750000 \frac{\text{Aturns}}{\text{Wb}}$.

- Core magnetic flux density:

One of the most important criteria in core design is ensuring the core stays linear, at least however much real life permits. To check this, maximum possible magnetizing current peak should not disrupt core linearity. In other words, such a flux should not lead to saturation.

We have used the approximate reluctance value to sweep across primary peak currents to obtain the operating level flux densities.

$$I_{pri,peak} = I_{LMavg} + I_{LMavg} \frac{\text{ripple ratio}}{2}$$

The outer legs of the E core are slightly smaller in area than the middle leg. Therefore, magnetic flux densities are different at these two types of legs. We see both densities in figure 7.

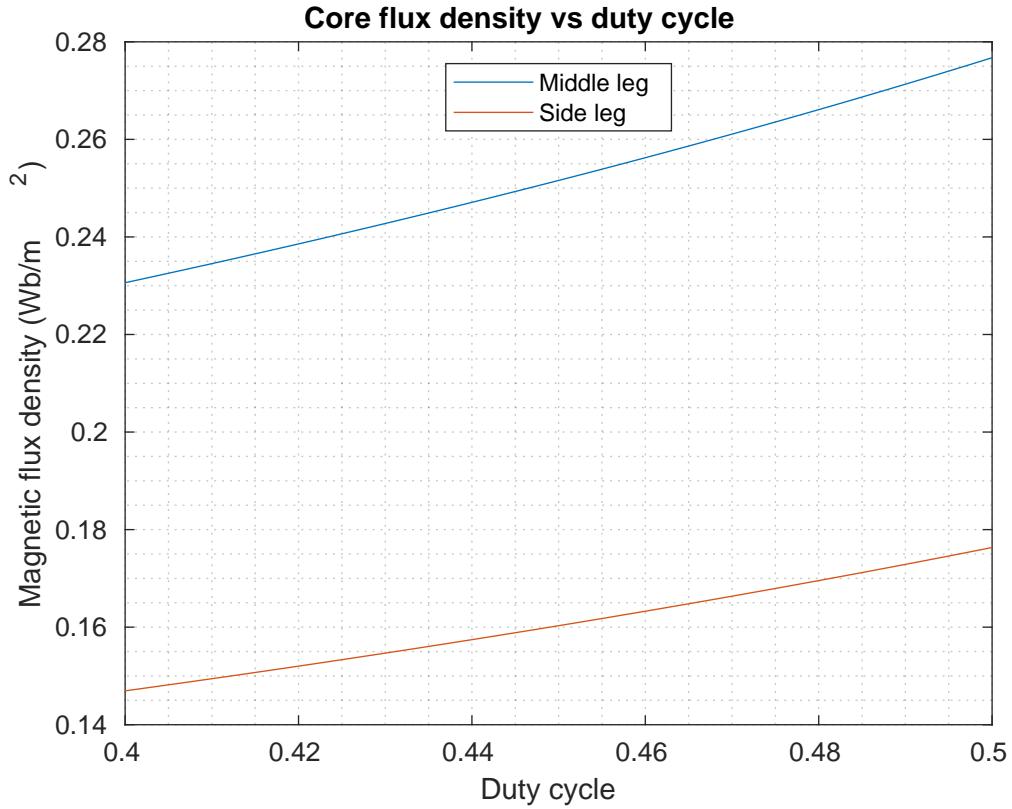


Figure 7: B field density vs duty cycle

The material saturates at around 300 mT [1] so we are within the limits and the converter remains linear.

Table 3: Core design parameters

Parameter	Value
Primary side turn number	9
Secondary side turn number	36
Air gap length	0.27mm
B field	140 mT - 280 mT

3.2 Winding Design

For the actual wires of the flyback transformer we considered two alternatives. The first analysis is done with standard single strand copper wires. First consideration on this is the skin depth since the switching frequency is selected as 200 kHz and related AC losses are affected by skin depth a lot. For the selected F_{sw} the skin depth results in,

$$\delta = \sqrt{\frac{\rho}{\pi F_{sw} \mu_0}} = 1.4587 \cdot 10^{-4} m$$

Later, maximum allowable strand cross-section is yields,

$$\text{Strand Area} = \pi \delta^2 = 0.0668 mm^2$$

3.2.1 Solid Copper Variant

This is around 29 AWG. Current rating of this wire gauge is 0.182 amperes however we can define a risk factor to push the copper a little more to utilize the core more effectively. In another words, with a risk factor of 2 double the amount of current will pass through the wire.

The RMS of the input current is calculated as 4.55 amperes. Number of primary strands is, this RMS current divided into each strand. The result is we would need 33.3 parallel strands.

A side note on this is that the input current is highly discontinuous at the switching frequency. It does not have a ripple over a fixed current hence by the frequency decomposition, the component at the switching frequency is quite large.

For the secondary side, same analysis can be made. Again using the RMS value of the current over the transformer. This results in 7.33 parallel strands.

Primary wire count is number of parallel strands multiplied with the turn number,

$$\text{Primary Wire Area} = N_{pri} \cdot \text{primary_parallel} = 1.9391 \cdot 10^{-5}$$

For the secondary

$$\text{Secondary Wire Area} = N_{pri} \cdot \text{turns_ratio} \cdot \text{secondary_parallel} = 1.7064 \cdot 10^{-5}$$

Numbers seem high however this consist of both parallel strands and the full wire length and it will be used to calculate the fill factor.

$$\text{Fill Factor} = \text{Total Wire Area} / \text{Total Window Area} = 31.87\%$$

3.2.2 Litz Variant

Although the parallel wires are effectively acting as litz wires, a design with the actual litz wires are made, The design is given below and the total copper and fill factor are similar. This second design is expected to be better since the proximity and skin effect related losses will be less.

Turn Numbers	Wire Diameter and # of Parallel
9	0.9 mm × 2
36	0.9 mm × 1

Table 4: Transformer Winding Design with Litz Wire

The fill factor of the design with litz wire is calculated as 30%

This fill factors are both within the reasonable limits. The fill factors of 30 percent can be easily wound. The expected fill factor is actually will be smaller since the litz wire have around 1.28 packing factor which means that it has 0.22 percent empty spaces inside. On the hand created litz case, this is expected to be lower.

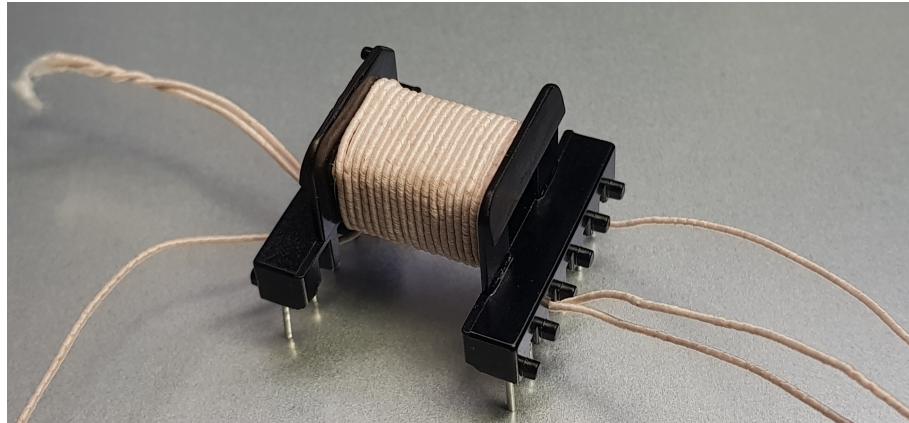


Figure 8: Photograph of the first version with Litz wire. (Fill factor 30%)

Later it is deduced that the core had plenty empty spaces inside. This space can be filled with copper to reduce the copper loss for the transformer, however the leakage inductance will get higher due to the windings move away from the center of the core. A new version for the litz is wound. This time the fill factor of the E cores with the litz cable is expected to be around 80% if wound tightly. The primary side wound with a cable that has double the previous wire diameter without paralleling and secondary side kept at the same cable dimensions with 2 parallels.

Turn Numbers	Wire Diameter and # of Parallel
9	1.8 mm × 1
36	0.9 mm × 2

Table 5: Transformer Winding Design with Litz Wire

The fill factor of the design with litz wire is calculated as 60%

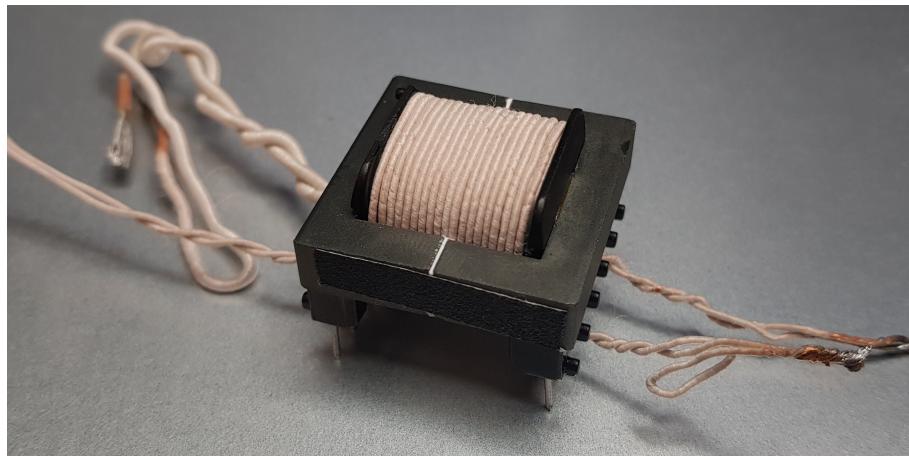


Figure 9: Photograph of the second version with Litz wire. (Fill factor 60%)

For the winding configuration, the layers are arranged such that first the half of the secondary is wound, then the primary is placed covered with the rest of the secondary. The sandwich pattern helps with reducing the leakage inductance.

3.2.3 Measurements of the Core

The core is then measured, $L_{pri} = 12.42\mu H$, $L_{sec} = 192.8\mu H$

A quick check for the turns ratio which should be 4,

$$\frac{N_{sec}}{N_{pri}} = \sqrt{\frac{192.8\mu H}{12.42\mu H}} = 3.94 \approx 4$$

For the leakage inductances measured from primary and secondary,
 $L_{leak,pri} = 0.32\mu H$, $L_{leak,sec} = 4.97\mu H$

Leakage inductance came out to be 2.5%.

3.3 Losses

3.3.1 Copper Loss

For the copper loss we need to calculate the wire primary and secondary, total wire lengths.

The primary wire length calculated is 0.3341 meters. The secondary counterpart is 2.6964 meters.
 The resistance is calculated as,

$$R_{pri} = \frac{\rho l_{pri}}{A \cdot N_{parallel}} = 0.0056\Omega$$

$$R_{sec} = \frac{\rho l_{sec}}{A \cdot N_{parallel}} = 0.0911\Omega$$

Power is then $P = i \cdot R^2$ with the RMS currents.

The total copper loss is, for primary 0.3242 W and for secondary 0.2083 W.

Total is calculated at the highest currents hence the performance will be better.

3.3.2 Core Loss

The core loss is calculated from the power loss density and the peak magnetic flux density curves at fixed frequency given by the manufacturer on the datasheet of the related core.

These are empirical values and the our selected data is from 200 kHz line.

The datapoints from the datasheet is digitized on matlab and a polynomial equation is fitted.

The magnetic flux density is different on the side legs of the E core than the center leg hence two volumes are calculated separately.

The total loss is calculated from the ΔB but the data is for AC magnetic flux variation hence ΔB given is expected as the right approach for more accurate calculation. A safety factor of 2 is given for margins of errors. The total core loss for highest operation is found as 1.22 W.

4 Controller Design

UC3843 allows for cascade peak current and voltage control. Both functionalities of the IC are used. The following circuit diagram 10 is taken from the datasheet of UC3843 [2] and demonstrates the recommended operation of the PWM controller.

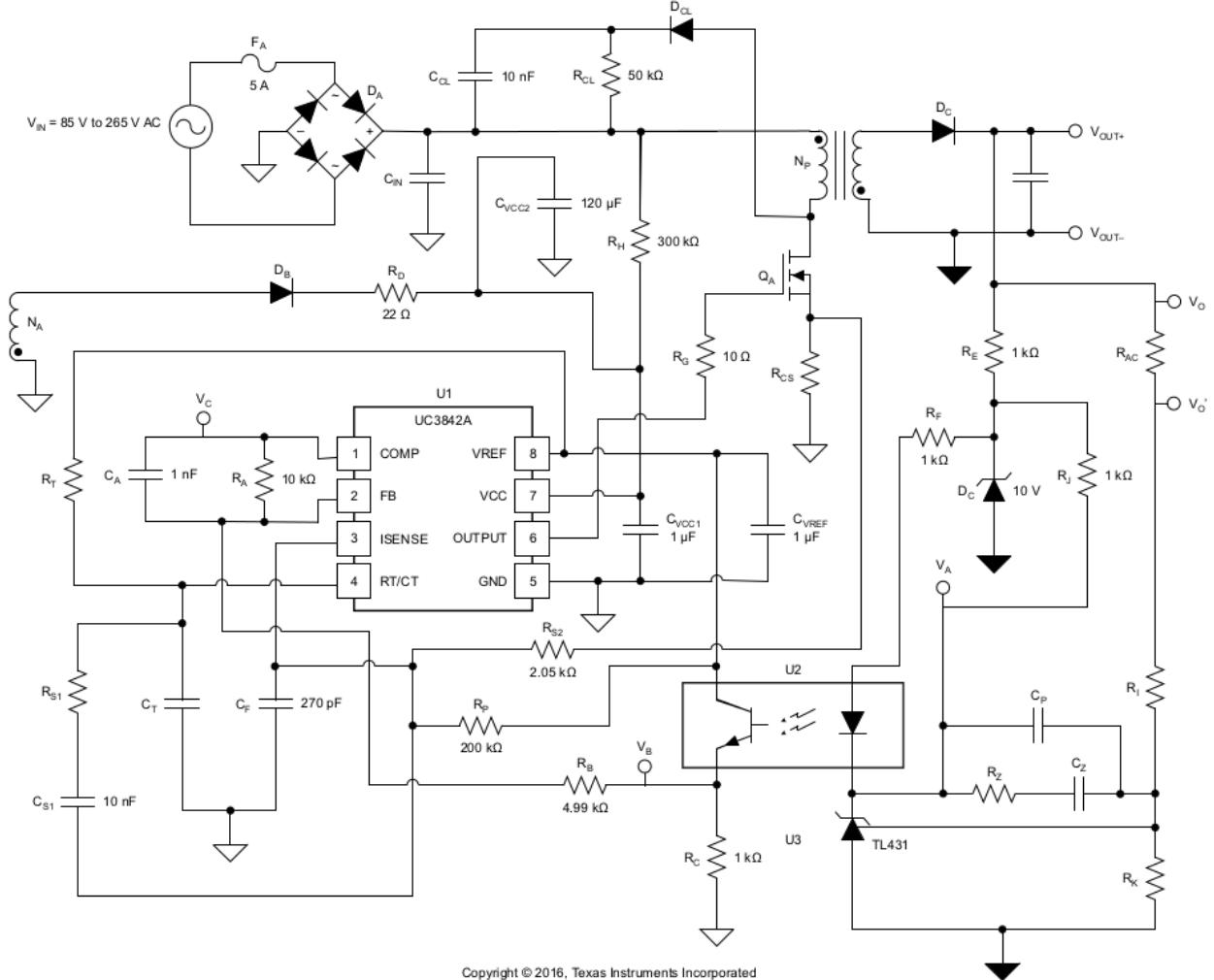


Figure 10: Circuit diagram demonstrating the recommended application of UC3843A [2]

We have implemented the recommended control circuit. Since our input is already DC we do not have the rectifier section as well as the auxiliary winding. In addition, we have decided to discard the pole placement capacitor C_P for the optocoupler network because we have achieved a satisfactory performance without its tuning. The circuit schematic with the values we have used for the components are given in Figure 11.

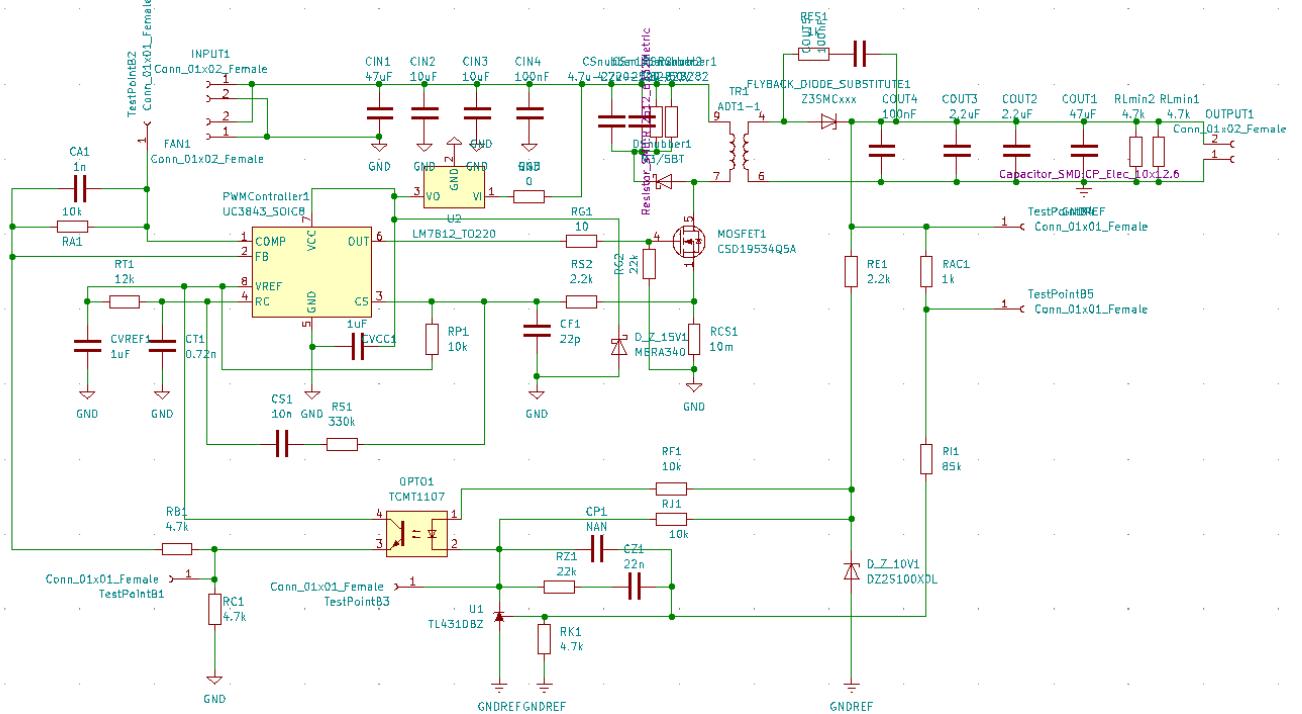


Figure 11: Circuit schematic with R and C values used in the circuit. Input and output capacitance may differ.

While components like R_z , C_z , R_A , C_A , R_B are tuned by trial and error, some components entailed detailed calculations. To begin with, R_K and R_L are selected to set 2.5V at TL431 reference when output is exactly 48V. Pull up resistor for the current sense leg R_P is set as $10.67\text{ k}\Omega$ to set the operating range of the current sense leg to in between 0.6 and 0.8V approximately with $10m\Omega$ current sense resistor. This value for the pull up resistor was determined by simulations. R_T and C_T are determined according to the formula $f_s = 1.72/(R_T C_T)$.

Component	Value (Ω for resistors, F for capacitors)
R_A, R_F, R_J, R_P	10k
R_B, R_C, R_K	4.7k
R_E, R_S	2.2k
R_{G2}, R_Z	22k
C_A	1n
C_F	220p
C_S	10n
C_T	0.72n
C_Z	22n
R_{AC}, R_{ES}	1k
R_{CS1}	10m
R_G	10
R_I	85k
R_S	330k
R_T	12k

Table 6: Values used in the control circuit

5 Computer Simulations & Analysis

5.1 Ideal Simulations

After determining a value for L_m , ideal simulations are done in LTspice. Ideal Flyback converter circuit constructed for the simulation is given in Figure 12. The model includes an ideal diode, an almost ideal switch, an ideal transformer model with magnetizing inductance, and an output capacitance whose value is calculated to make output peak-to-peak voltage ripple equal to 2%. The components named with "spice magic" are only included to increase simulation speed.

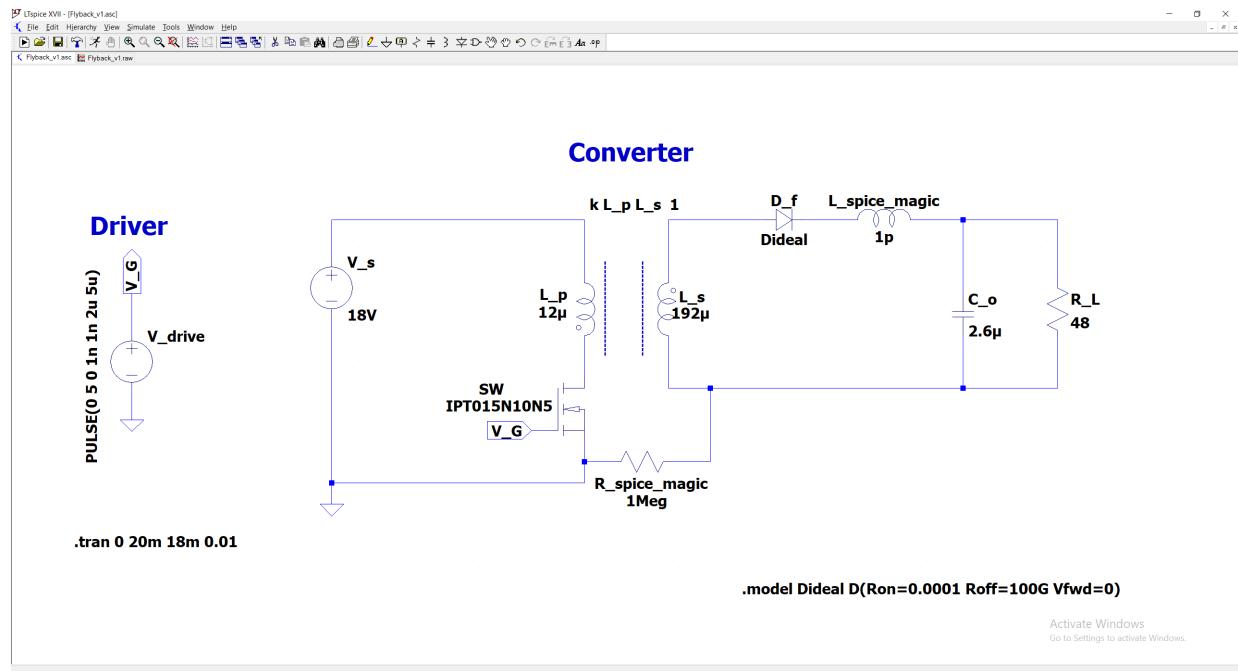


Figure 12: Simulated LTspice circuit schematic (ideal case)

The design choices were made so that the magnetizing current ripple is at least 40%. Primary and secondary current waveforms are given in Figures 13 and 14 for 12V and 18V input voltages, respectively. As one can see, we have desired current ripple which is consistent with our design.

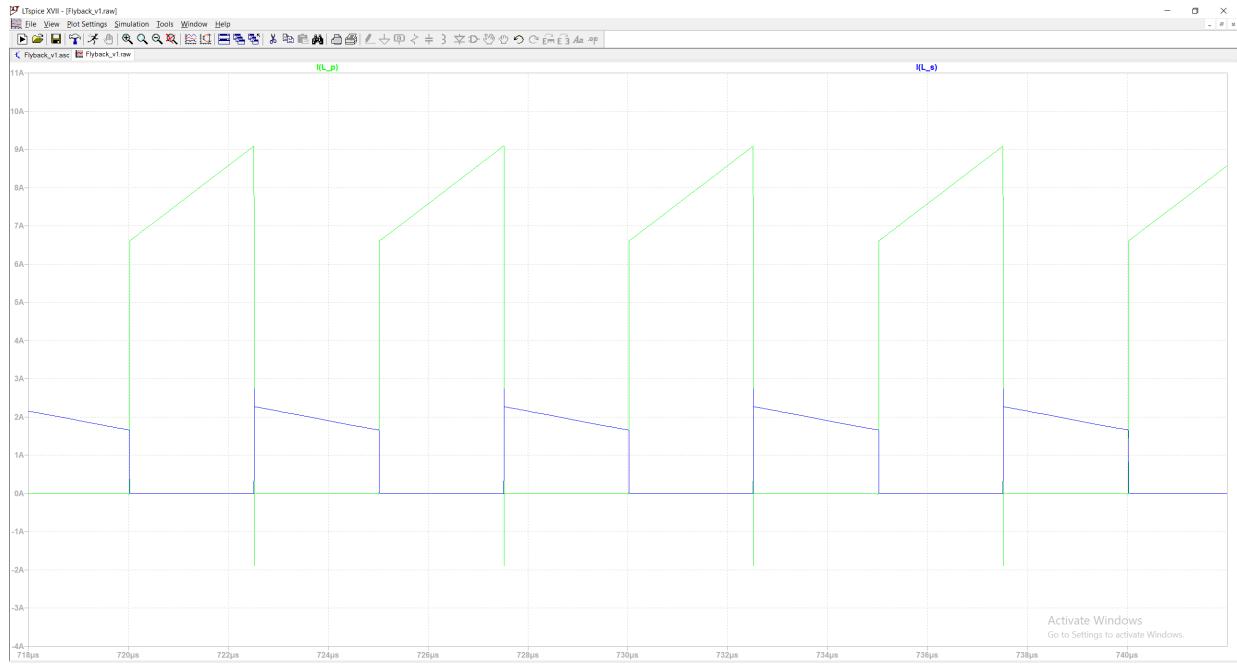


Figure 13: Primary and secondary current waveforms for 12V input voltage

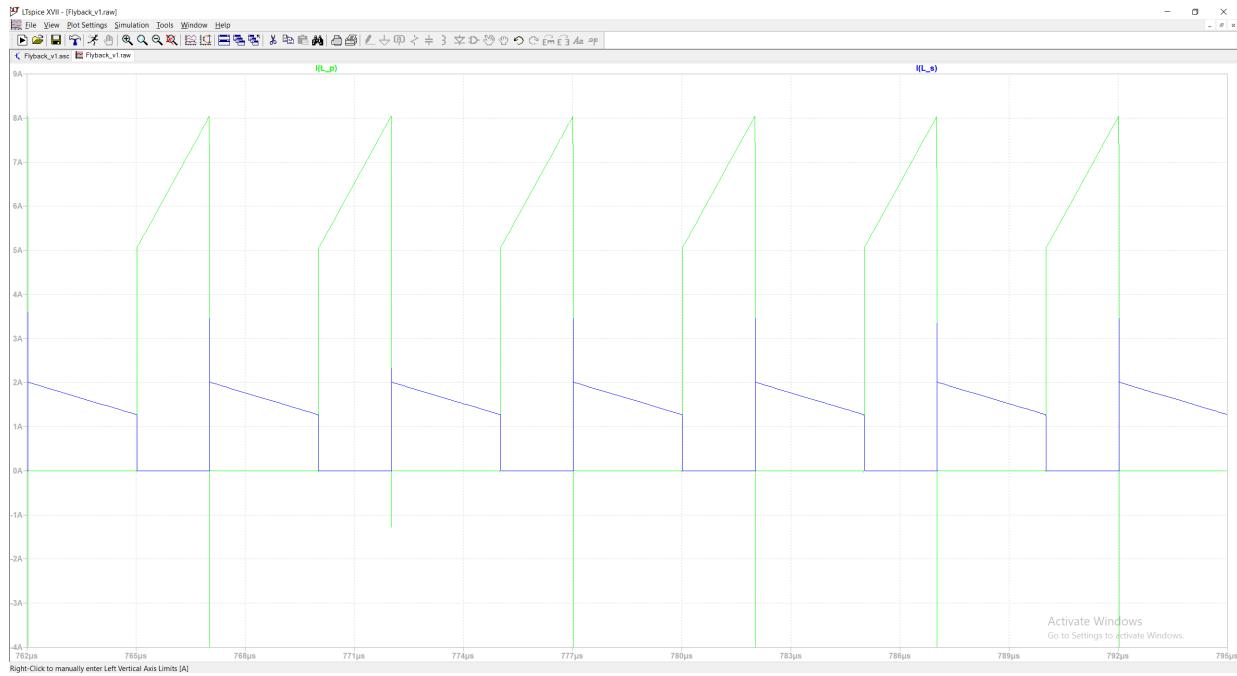


Figure 14: Primary and secondary current waveforms for 18V input voltage

We also observed the voltage stresses on the diode and on the switch in the simulation. The expected switch voltage during the off times are calculated as $V_{SW} = V_s + V_o \frac{N_1}{N_2} = 30V$, which is calculated for 18V input voltage (worst case). Also, the diode voltage is calculated as $V_D = V_s \frac{N_2}{N_1} + V_o = 120V$ during on times of the switch, again for the worst case. One can see from Figure 15 that the simulation result is consistent with the theoretical one.

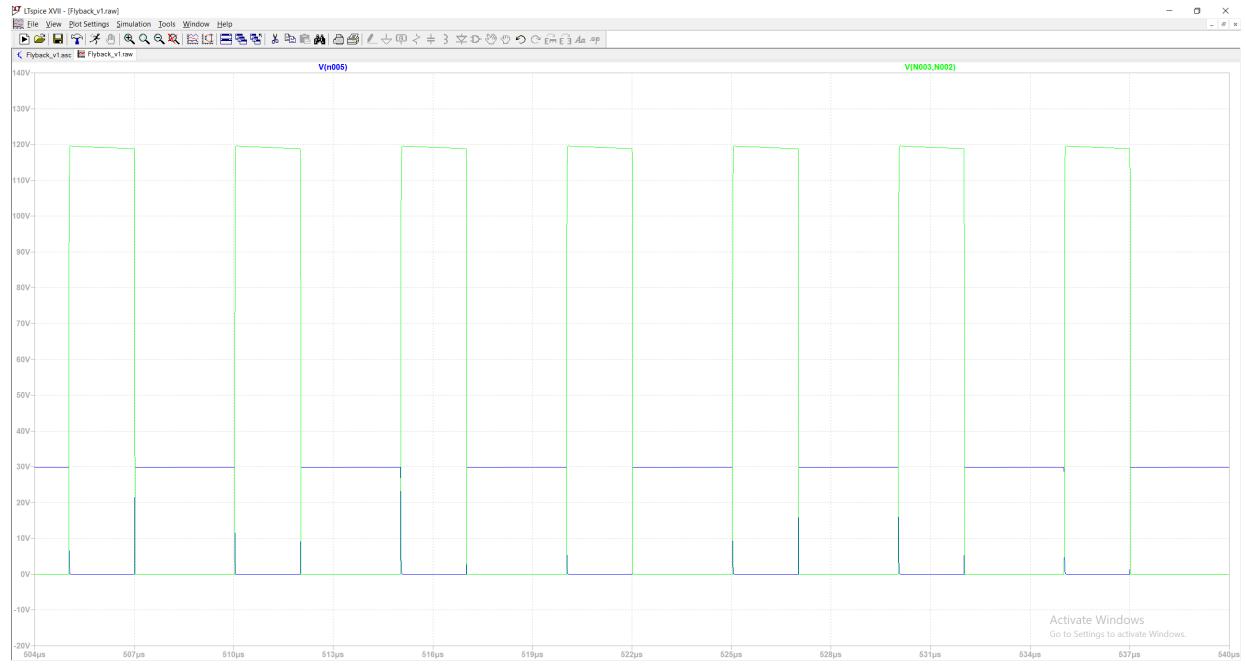


Figure 15: Diode and switch voltage stresses for 18V input voltage

Finally, the output voltage ripple can be calculated using the equation $\frac{\Delta V_o}{V_o} = \frac{D}{RCf_s} \approx 2\%$. One can see it is consistent with Figure 16.

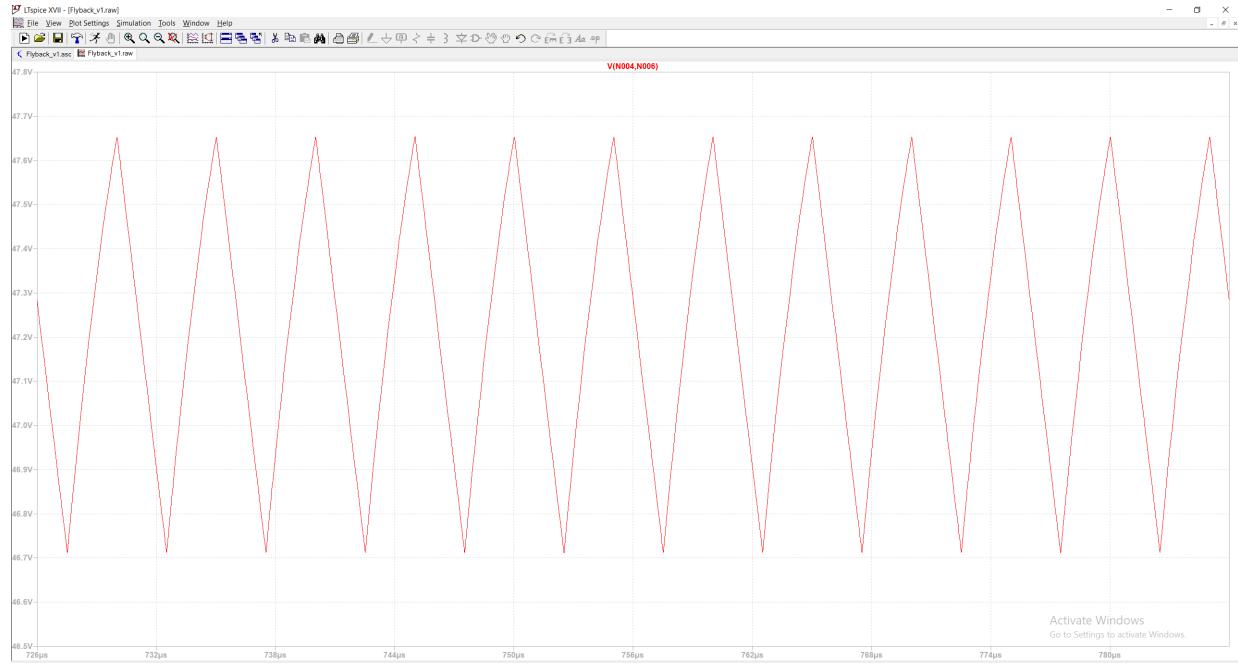


Figure 16: Output voltage waveform

5.2 Non-ideal Simulations & Snubber Design

The parasitic effects, primary leakage inductance (which is measured as 3%), and non-ideal semiconductors are added to the ideal circuit. When we include the parasitic effects and simulate the circuit for 12V

input voltage, the leakage inductance creates high voltage stress on the MOSFET during the transition to off-state. This will not blow up our MOSFET as the avalanche energy of the MOSFET is enough to absorb all the energy stored in the leakage inductance. However, since the voltage swing caused by the ringing will be too high, we either had to design a snubber or use a TVS (Transient Voltage Suppression) diode. We made simulations with a TVS diode with 30V rating, which is also included in the schematic. The non-ideal model of the circuit can be seen in Figure 17.

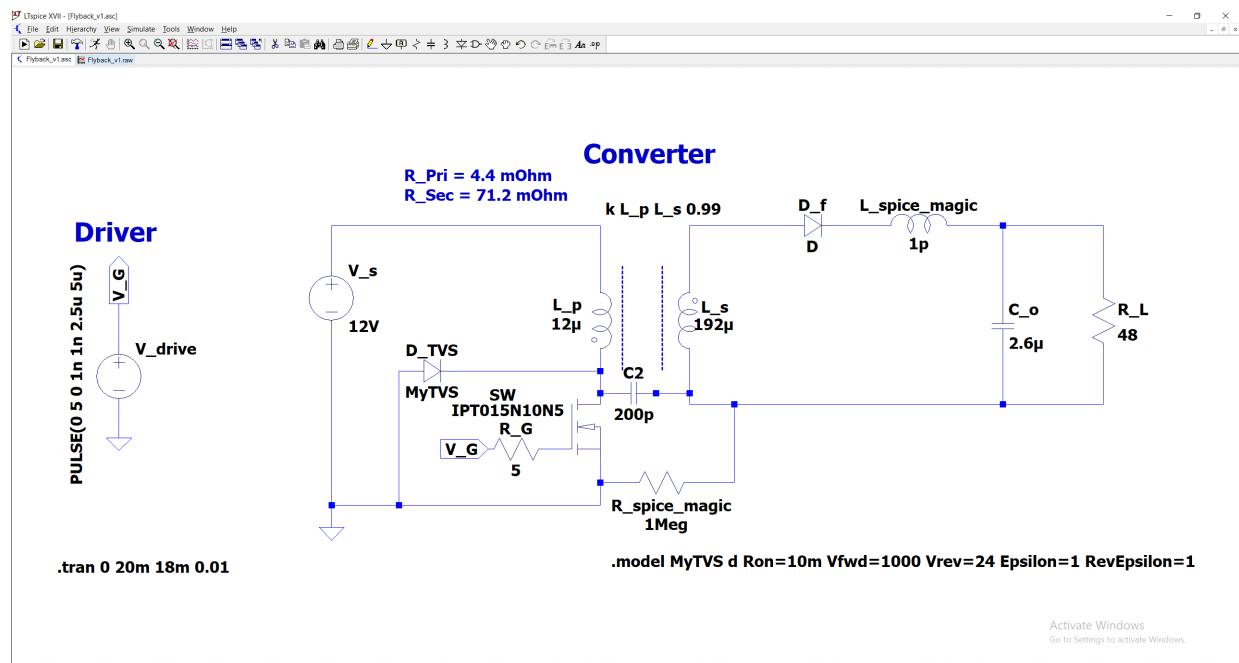


Figure 17: Simulated LTspice circuit schematic (non-ideal case)

Still, there will be some amount of ringing due to the unsuppressed energy. We will see its effect on the transients of the waveforms. The non-ideal simulation results for magnetizing current ripples are given in Figure 18. The voltage stress on the switch is seen in Figure 19. Finally, the output voltage waveform is given in Figure 20. Note that with the duty for ideal case (which is 50% for 12V input) the output voltage is reduced to 40V. However, since the analog IC does close-loop control, it can increase the duty as much as it is required. Figure 20 shows the output voltage for 12V and 54% duty, also showing that our circuit is still stable at this operating point.

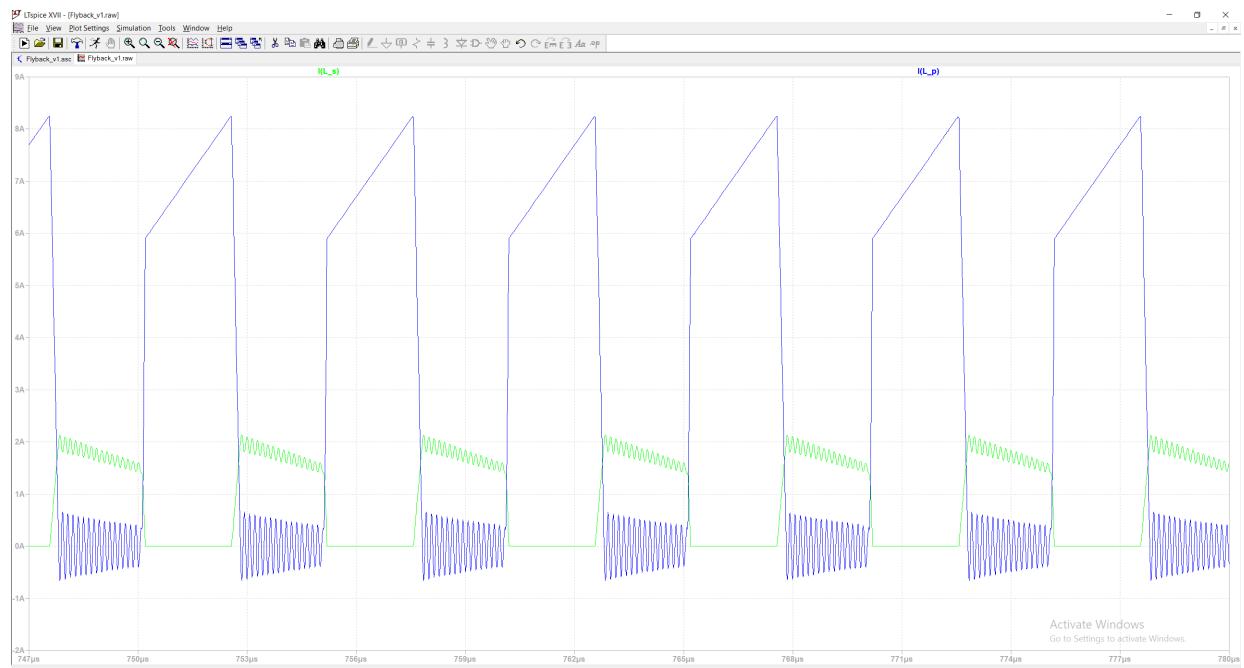


Figure 18: Primary and secondary current waveforms for 12V input voltage (non-ideal case)

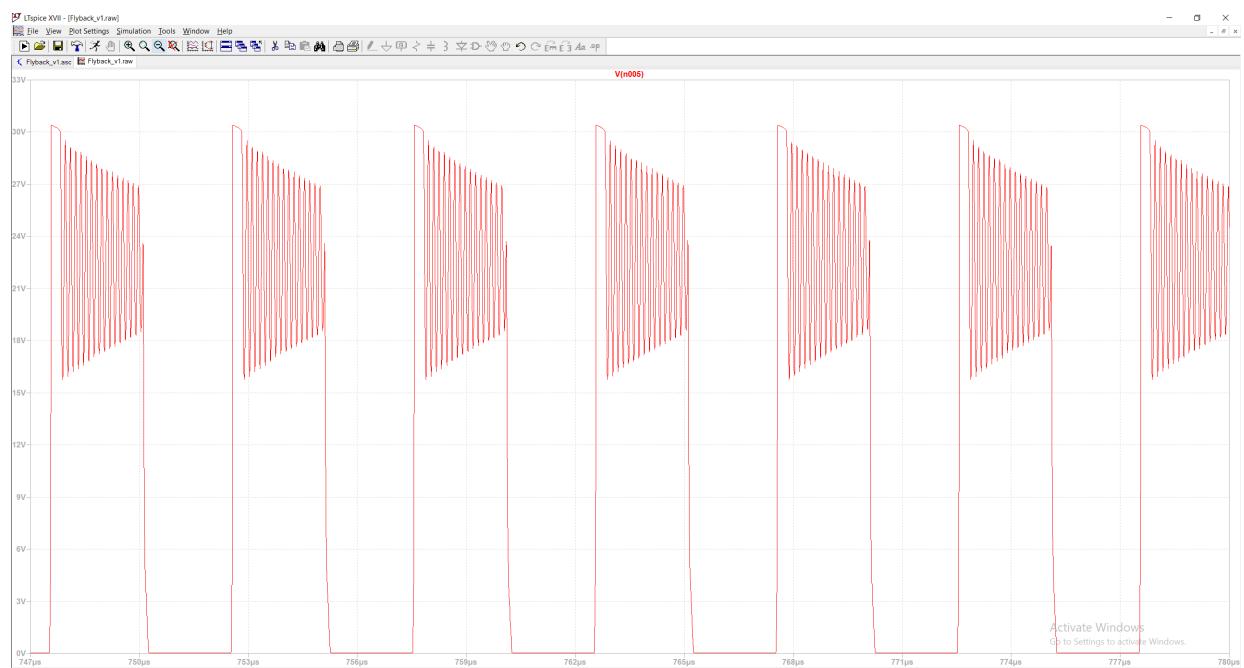


Figure 19: Switch voltage stress for 12V input voltage (non-ideal case)

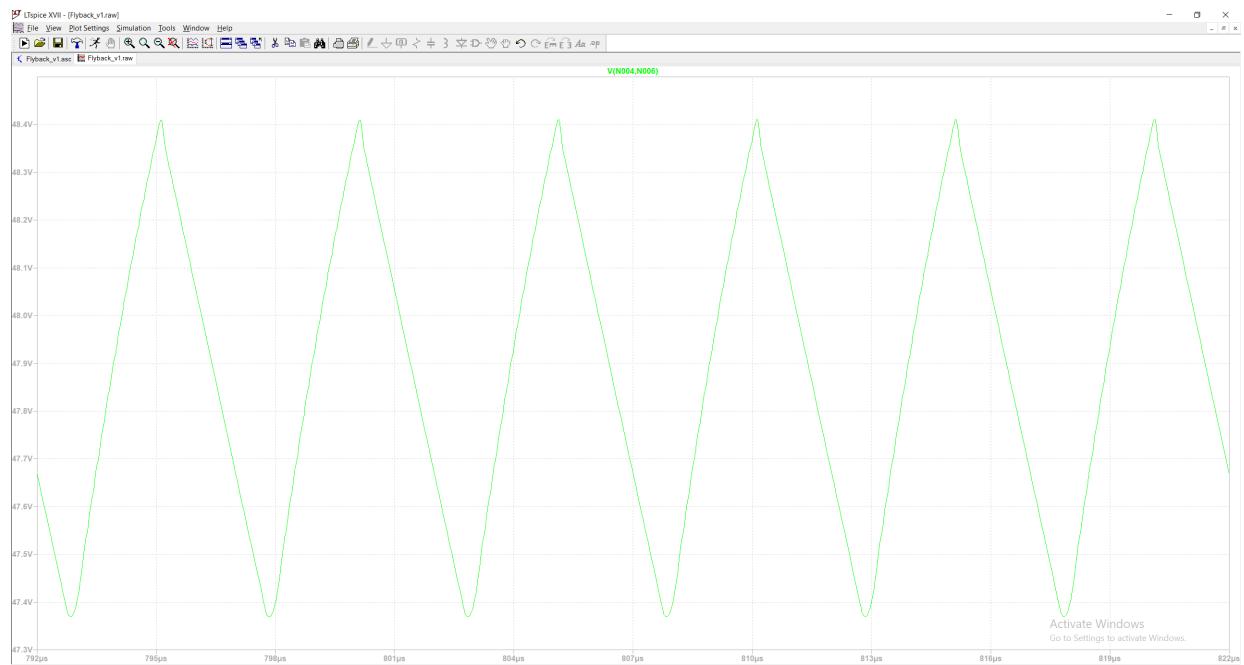


Figure 20: Output voltage ripple with 54% duty (non-ideal case)

However, we realized that this method is not sensible since the energy dissipated on the TVS is extremely high. Hence, we decided to use an RCD snubber. We made many simulations (with various snubber types) to decide on sensible snubber resistance and capacitance values for our case, which limits the ringing to an extent (smaller than 80V max) but also does not increase the losses drastically. The schematic for the final version of the snubber in the primary side is given in Figure 21. The ringing on the MOSFET voltage for these values are given in Figure 22.

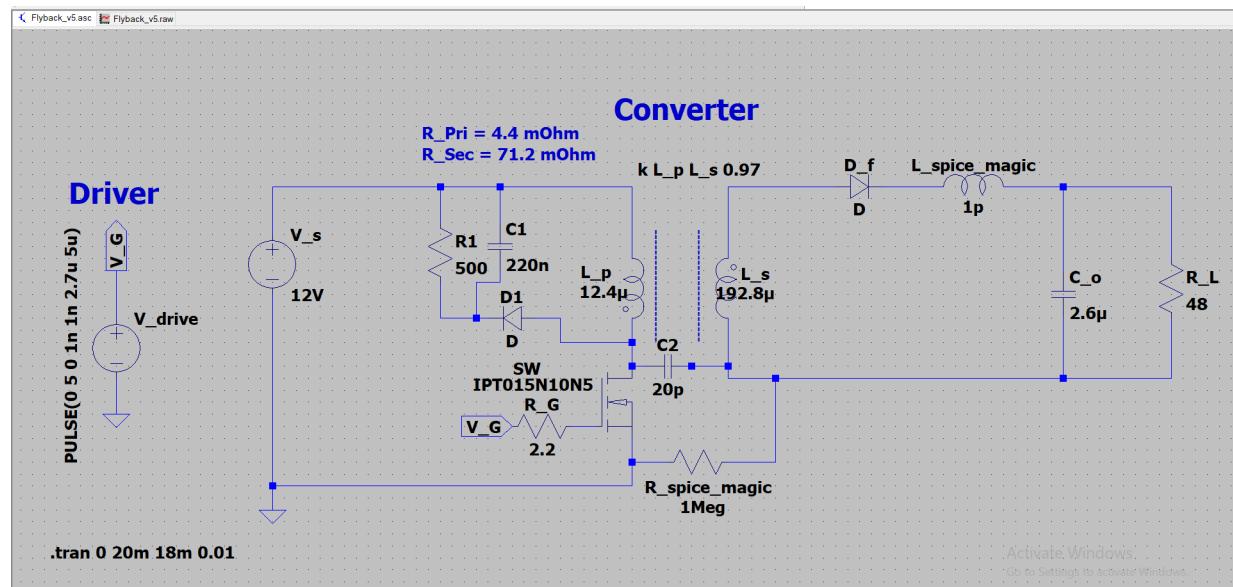


Figure 21: Snubber circuit simulation schematic for the primary side

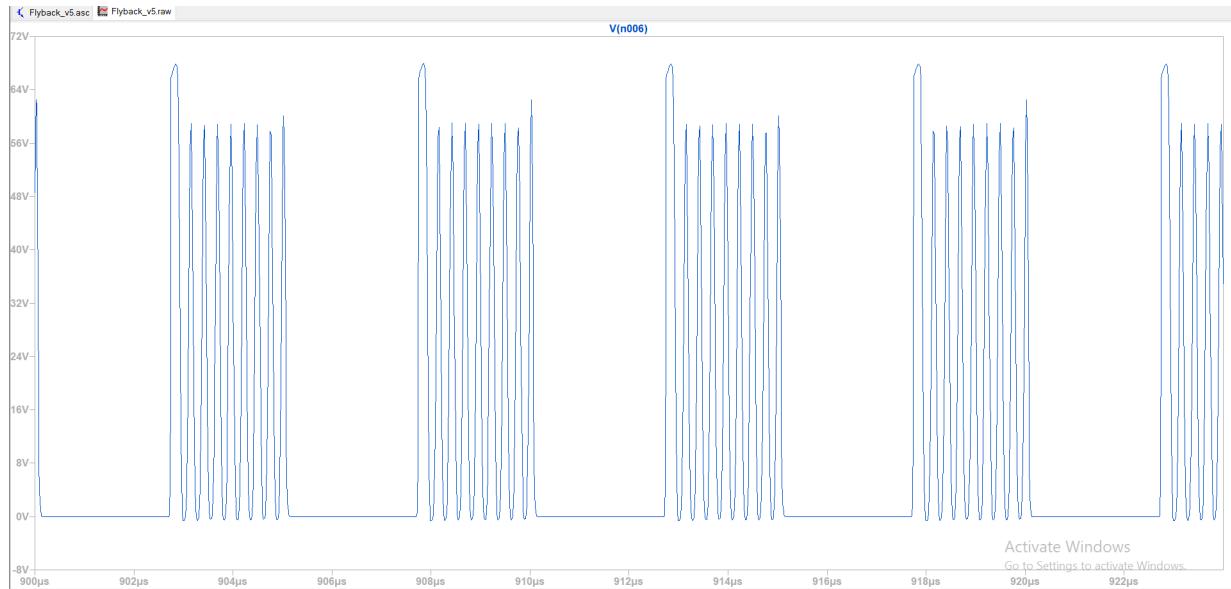


Figure 22: Ringing on the MOSFET with the RCD snubber (simulation results)

We can see that there is still a lot of ringing, but considering our MOSFETs voltage ratings (100V with high avalanche rating) this is not harmful. Furthermore, the Spice simulation somehow creates more ringing; possible parasitic or other effects damps the ringing very fast in the real case, as seen from the experiments we did. The reflection of this ringing voltage may create voltage stress on the secondary side diode. Hence, we also added an RC snubber in parallel to the secondary side diode.

The losses on the snubber in the simulation is 5.93W, which is significantly high. However, this is due to the energy stored in the leakage inductance before the turn-off moment of the switch, due to high primary side peak current. The stored energy in the leakage is equal to $\frac{1}{2}Li^2$ and if all of the energy in the leakage is spent on the snubber, the power dissipated is equal to $\frac{1}{2}Li^2f_s = 3.72W$ for 10A peak current (which is the chosen limit for our peak current mode controller, for the ideal case). Hence, we saw that a large loss in the snubber is expected for this flyback topology, for an application with high input side current. A two switch topology, a zero-current switching topology, or something else might have been more appropriate for this case in terms of losses. Furthermore, the switching frequency may be reduced to a much lower value to lower the snubber losses.

5.3 Controller Simulations

Controller simulations also take part in the LTSpice environment. The controller is the main part of the simulations, however exact spice model is unavailable, as a solution a counterpart model LT1243 is used which has the same working principle and parameters.

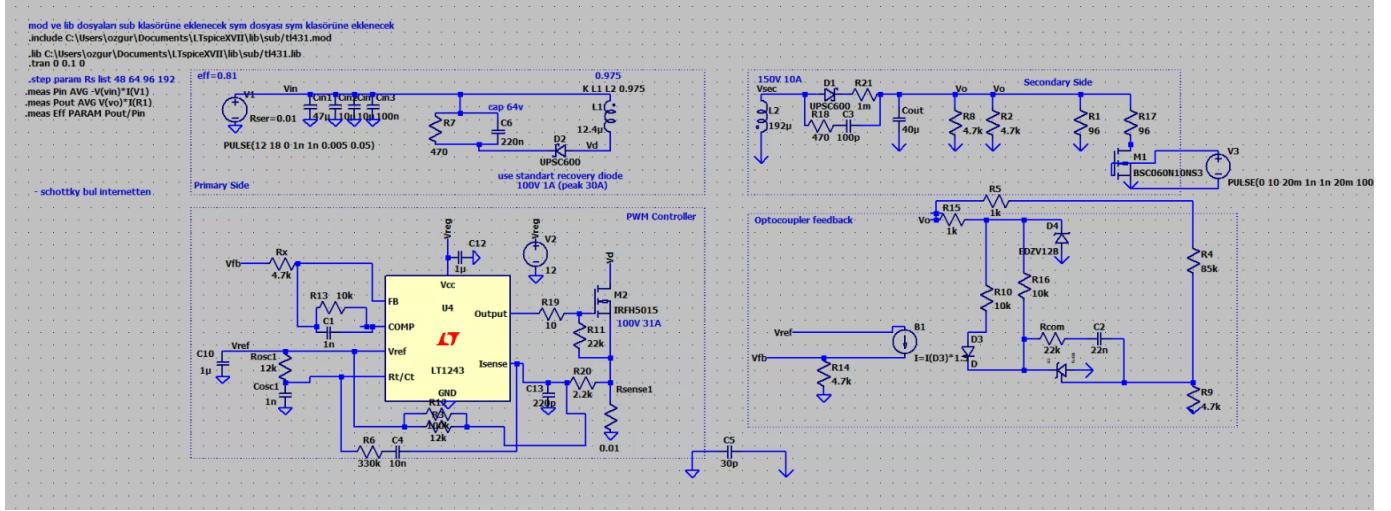


Figure 23: Controller integrated simulation in LTSpice.

Starting with the secondary side. The compensation circuitry is first designed allowing the output to set the desired voltage. Later in the transient case the output voltage is compensated with the R_{com} and C_2 . These values depend highly on the converters transfer function and operation range and are found via iterative testing.

The optocoupler is used in analog fashion, and proper biasing with R_{10} is required. The D_4 zener diode is used to set the high voltage to a constant 12V and the TL431 at the bottom changes with its feedback function to alter the voltage level at the cathode of the optocoupler diode.

The optocoupler is modelled with a behavioral current source with a gain factor similar to the one that is expected to be used. A generic optocoupler also works in this configuration but if not found this is a method to emulate the workings.

For the primary part this is where the active switching elements are used and controller takes place. The timer configuration for setting the switching frequency worked as expected with the formula mentioned before. Compensation part is continued for the primary side however a generic design is enough which is 10k for R_{13} and 1 nF for the C_1 . V_{cc} of the controller is regulated with a 12V voltage regulator that is LM78m12 and it is capable of supplying the controller and mosfet even for high frequencies such as 200 kHz.

Due to the high input currents, the shunt resistor is selected as 10 millionohms and expected to dissipate around 1W of power when RMS current is about 7.5 Amperes with peaks up to 12 Amperes. For higher resistance values for the shunt resistor, the power loss increases. The controllers peak current limit is however set to 1 volts meaning that the shunt resistor with 10 millionohms is uneffective for this configuration with resulting in a sensed voltage of 0.12 volts at peak current. The solution is biasing the current reading pin of the controller. A resistor that is connected between the reference voltage pin and the current sense pin effectively rises the sense value with that a current limit can be set. A quick note on that, the current sense filters resistor and the biasing resistor that mentioned just previously is used together to set the biasing hence the current limit can be set.

The filter on the current sense is important in order for the controller since high frequency noises can

introduce extra turn off signals for the mosfet hence the switching frequency might be altered. The used filter is not a harsh one but softer filters introduce aforementioned unexpected outcomes hence the filter is important at the current sense.

After the values for the components are set, the transformer is changed to the non-ideal case and the results stayed as expected. Then the transient tests are done in simulation environment with varying input voltage and changing the load. A single time sequence with varying input voltage and changing output load is shown below.

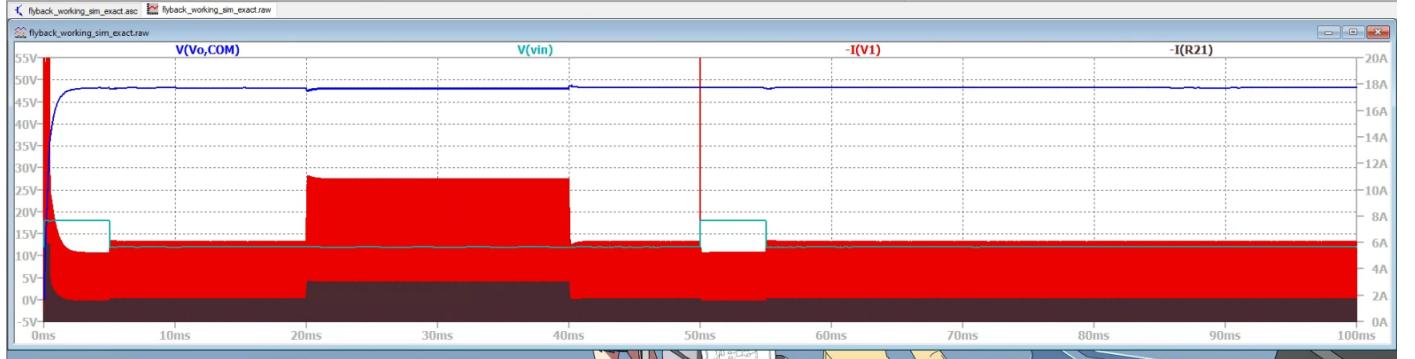


Figure 24: Transient simulation capturing all the necessary aspects.

6 Component Selection

Aside from the core, which was luckily found, there are 4 components to choose.

- IC: UC3843AN [2].

The criteria in choosing the PWM controller IC were that it is able to operate at out input voltage range so that no auxilliary windings are necessary and that it has no PWM limit.

UC3843AN satisfies both constraints. It operates at voltages higher than 8V and can provide 100% duty cycle. A separate feedback network can be built and connected to the IC for closed loop operation. Moreover, it can provide up to 1A gate current.

- MOSFET: CSD19534Q5A [3]

The most important criteria in MOSFET selection are rated voltage and current as well as slew rate. CSD19534Q5A has 100V rating in addition to having 10A current rating. This MOS also benefits from low losses thanks to $12.6\text{m}\Omega$ on resistance.

- Diode: PDS3200-13 [4].

The diode in the flyback converter suffers from high voltage stress because of secondary turn number being higher and the transformer polarity being reversed. In our simulations we saw the diode voltage climbed as much as 120V. Therefore we chose PDS3200-13, which has 200V, 3A rating as well as 780 mV forward voltage.

- Ceramic Capacitor: CL31B225KCHSNNE [5].

The output capacitor is chosen as $2.2\mu F$ CL31B225KCHSNNE and two of these will be connected in parallel. The device itself is rated for 100V which is above 48V for safety reasons. Moreover, the datasheet provides ESR vs frequency rating for the device and at 200 KHz this capacitor have approximately $30m\Omega$ ESR. Two of them in parallel have even lower ESR.

- Core clamp: B66232A2010X000 [6]

We have also selected a core clamp according to dimensions of our E core.

Even though the output capacitor is calculated using the continuous conduction mode assumption and found that $2.6\mu F$ is enough to reduce the steady state output voltage ripple, there are more considerations. Input and output capacitors are chosen carefully by inspecting relevant application notes such as [8]. Aluminum electrolytic and aluminum polymer capacitors are used as bulk capacitors both at the input and output sides. These have high capacitance values, decreasing the high current demand from the input supplies during transients, and increasing the output voltage control performance. Multiple ceramic capacitors with different capacitances are used in both sides to mitigate the effects of high ripple currents caused by the high frequency switching with their low ESR (Equivalent Series Resistance) and frequency responses. Capacitor voltage ratings for input and output sides are chosen as 50V and 100V, respectively, to have a safety margin. SMD capacitors are used to preserve compactness and rigidness. Also, ripple current ratings and losses were of consideration while choosing capacitors to input and output sides.

7 PCB Design, Mechanical Design, and Thermal Considerations

We decided to realize our circuit on a PCB (Printed Circuit Board). PCB has several advantages such as allowing a more compact and reliable design with better thermal management and enhanced electrical design options. When designing a PCB for an isolated flyback converter with a switching frequency of 200kHz, there are several important things to consider. Some of them can be summarized as follows:

- Current loops with high ripple should be kept as small as possible to reduce EMI and noise which may affect the controller performance or induce unwanted voltage stresses. (Also, the direction and position of these loops should be carefully considered.)
- All the paths (especially the high current carrying paths) should have a low impedance return path to the ground.
- The input and output side voltages should be carefully separated to ensure galvanic isolation.
- Gate loop of the switch should be as small as possible to protect the switch.
- Feedback signals should be protected from noise.
- Ground loops should be avoided.
- Enough clearance should be given to avoid voltage sparks around high voltage nodes.
- Thermal interface for lossy elements should be carefully considered.
- Test points should be added to ease the prototyping and testing process.

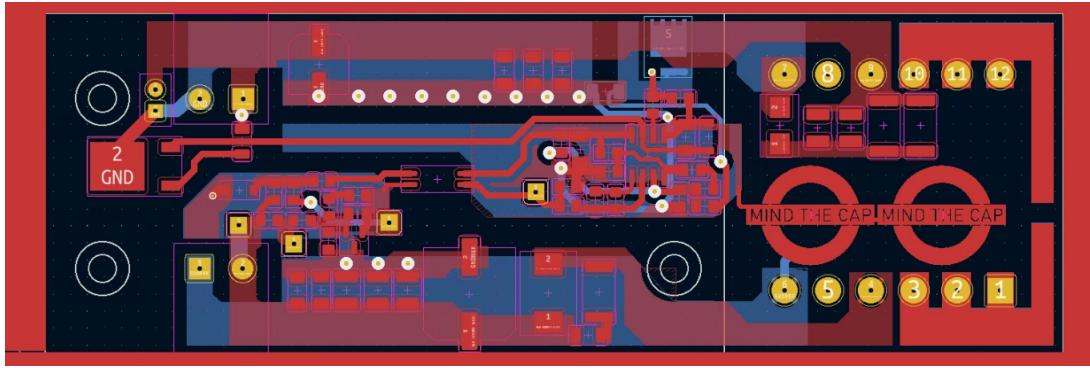


Figure 25: Printed Circuit Board design with logo as the stitching capacitor.

Besides all these requirements, we wanted our converter to be small-sized and aesthetic. Also, we wanted to ease the production with adjusting proper spacing and positioning of the components and copper tracks. We designed our PCB by considering all of these requirements using KiCAD environment.

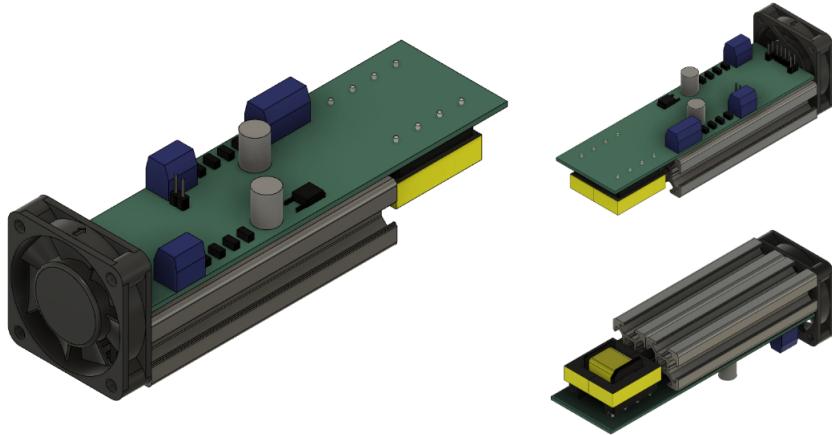


Figure 26: Initial thoughts on the mechanical and thermal aspects of the design.

An aluminum profile is used as a solid mechanical frame upon which the PCB will be constructed. This profile is also used as an heatsink to cool down the MOSFET in the circuit. Appropriate connectors are found for input and output connections. A place and a connector for a cooling fan is also placed for optional use. Finally, a plexiglass case is designed and produced for the converter. The photograph of the produced converter is given in Figure 28. Size of the converter with the case is 50mm x 50mm x 140mm.

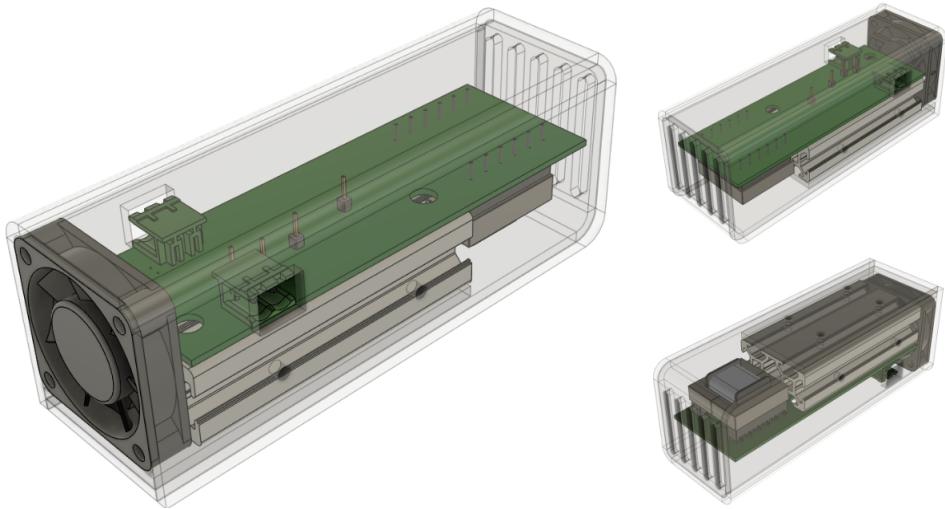


Figure 27: Final 3D design and the acryllic case.

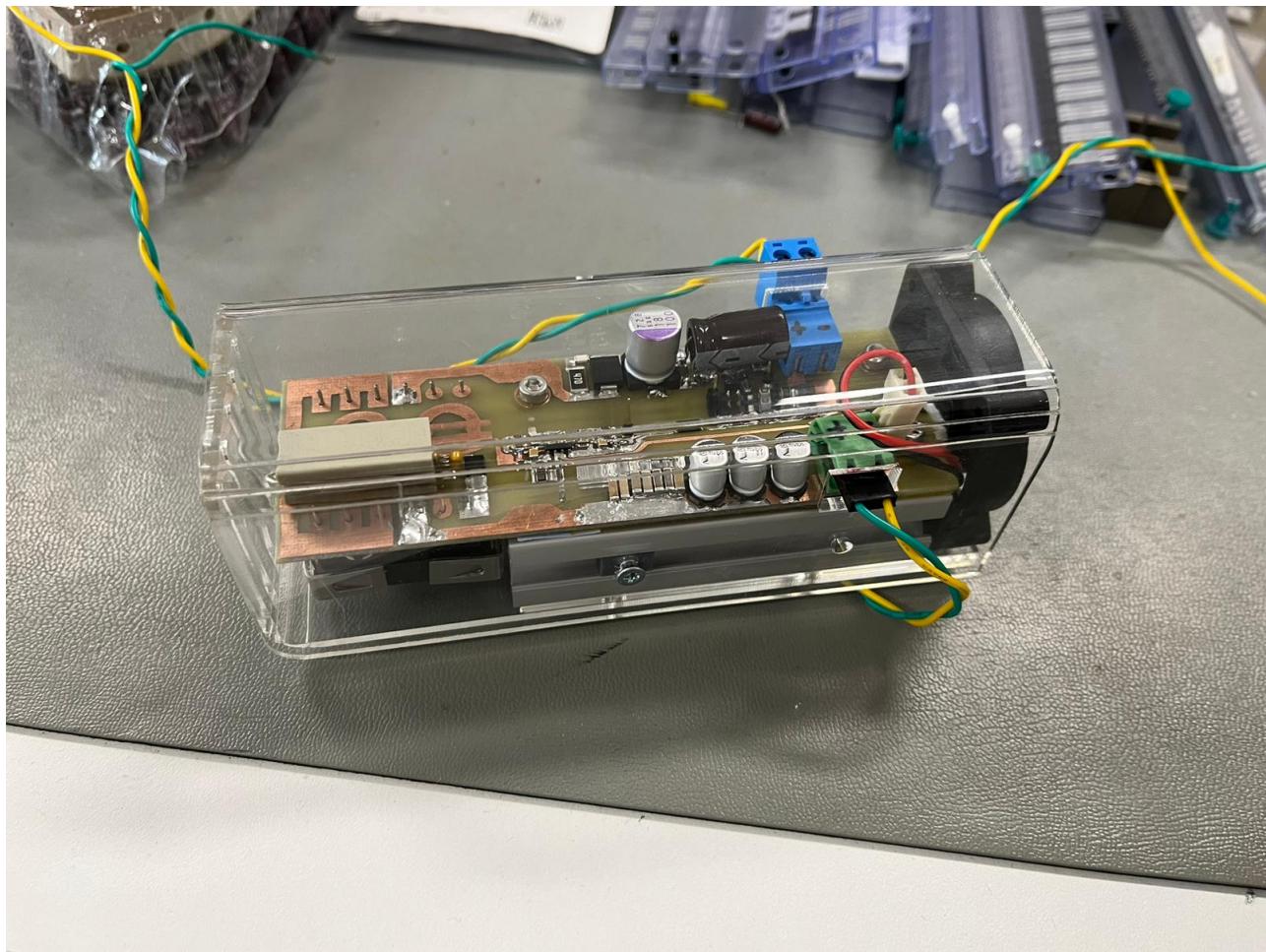


Figure 28: The 48V-48W flyback converter designed and produced by Mind the Cap

8 Experiments and Performance

Here we present the experimental data obtained during development and final demo.

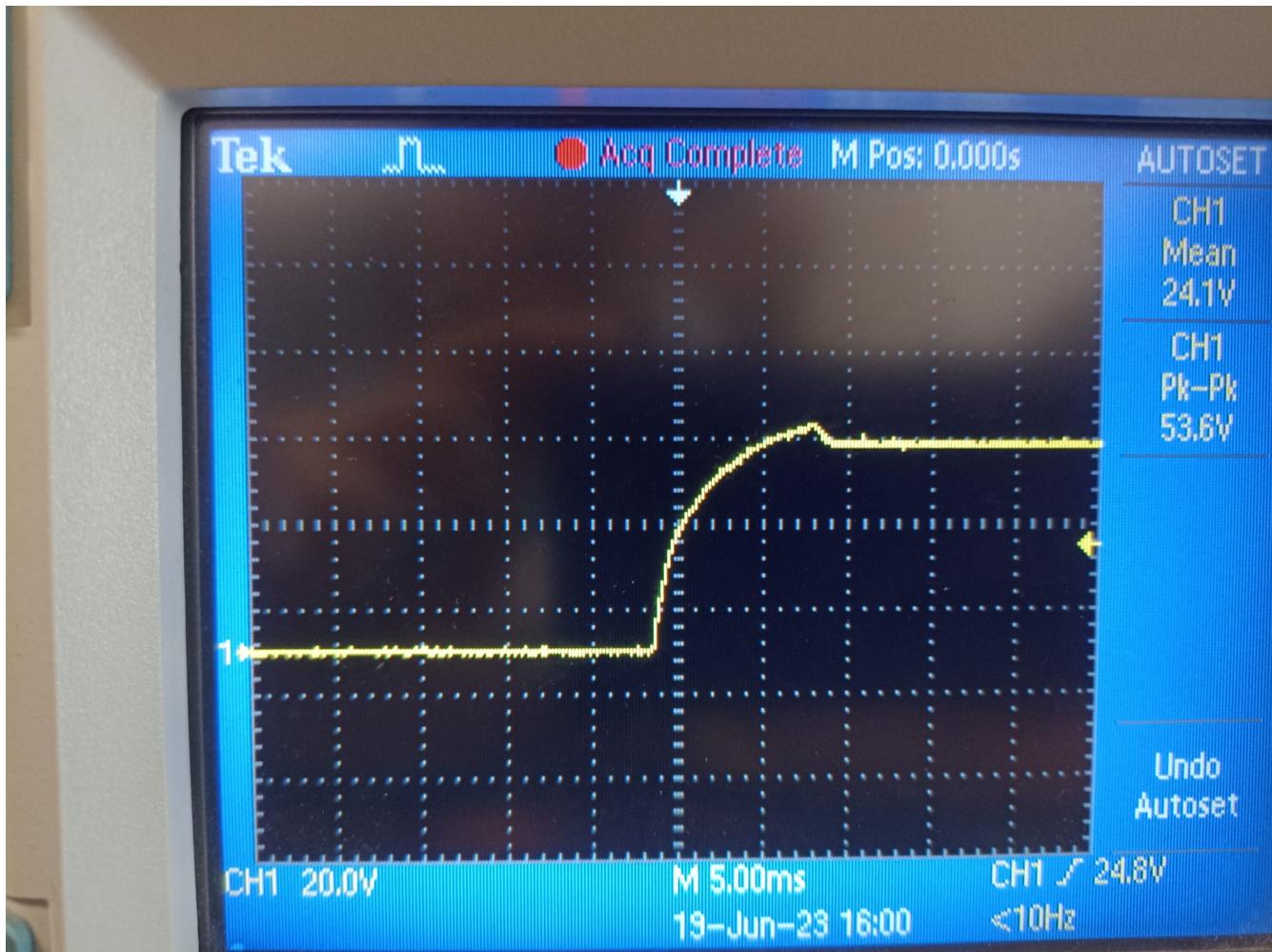


Figure 29: Step response to input voltage at half load

Figure 29 is the step response of the system to input voltage at half rated load. An overshoot is observed, which is likely caused by the lack of pole placement capacitor in the optocoupler network that adjusts the phase margin. The overshoot is about 5.6V corresponding to 11% of the steady state voltage. This ratio indicates that the phase margin is less than 45° under second order assumption. The figure also shows that the settling time is around 10ms.

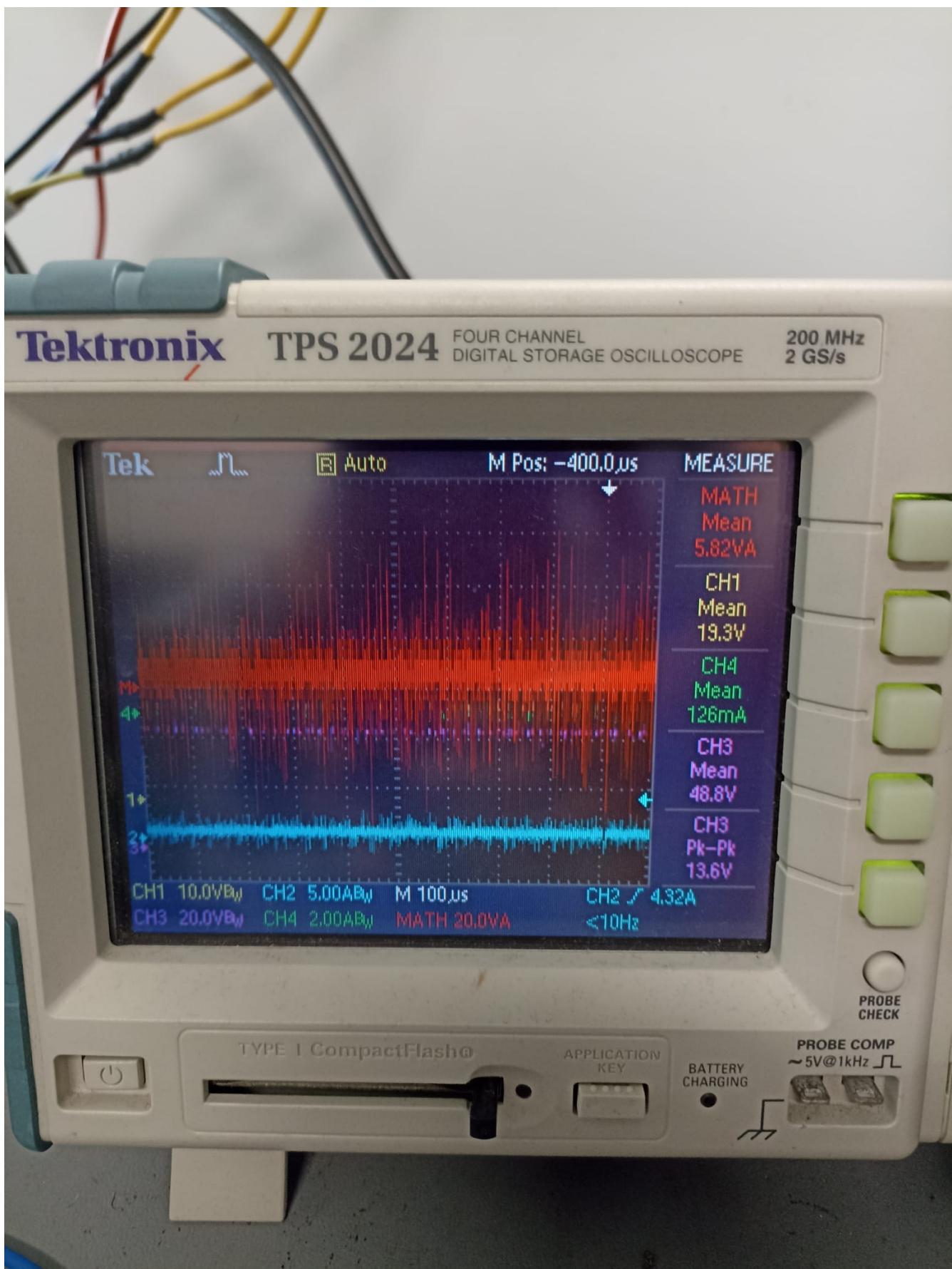


Figure 30: Measurements at 18V input and 10% load

In Figure 30 we see the measurements at 10% load. At this stage, output was 48.488V.

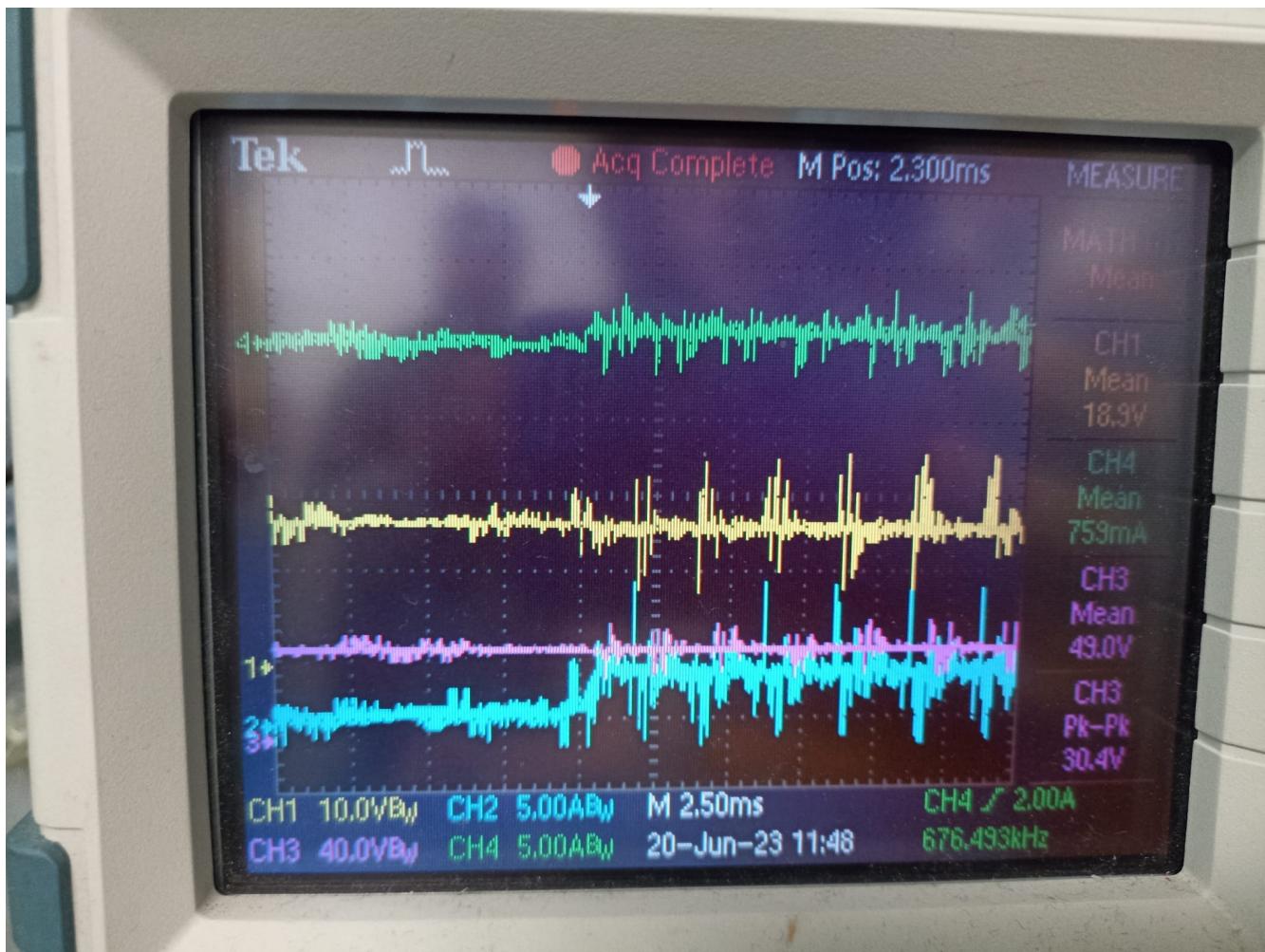


Figure 31: Measurements during load change to full load at 18V input

In Figure 31 we see the measurements during change to full load at 18V input.

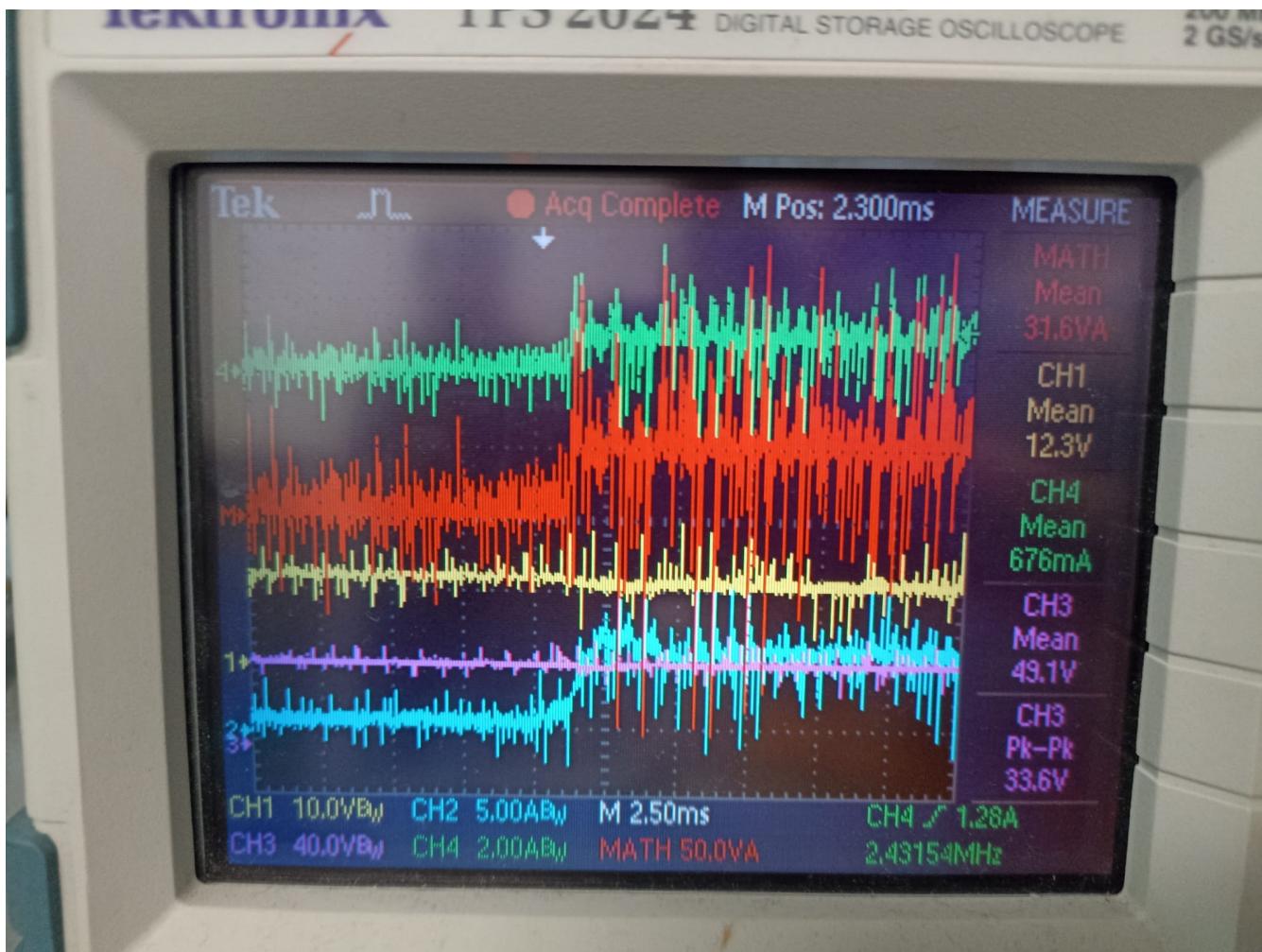


Figure 32: Response to load change to full load at 12V input

Figure 32 is the response to load change at 12V.

The efficiency is calculated at full load for 12V and 18V as 69% and 74%, respectively. Overall, except for the low efficiency (which is discussed to be expected for this flyback topology with this switching frequency and input-output voltage ranges) the control and regulation performance of the converter is satisfactory.

9 Discussions & Conclusions

In this report, the design process of a 48V-48W flyback converter is discussed extensively. It is observed that the control performance is robust during transients such as sudden load changes, and output voltage is consistently 48V, with a ripple less than 2%. Snubber circuits are necessary for both primary and secondary sides to protect switching elements during turn-off moments of the switch, due to leakage inductance. However, the losses in the snubber circuit reduced the efficiency significantly. Hence, from an efficiency standpoint, it is observed that another topology such as two switch flyback would be more appropriate since it reduces the effects of the switching off the leakage inductance current and reduces the voltage stresses on the elements. Note that if one uses a lower switching frequency such as 50kHz, the snubber losses will be reduced as well as other losses in the circuit, increasing the efficiency. In

conclusion, flyback converter topology is still a simple and convinient topology with its simple control and low component count, making it a viable solution for isolated DC-DC converter applications.

10 References

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