PK35 Design Rule

Rev.2.0

PHENITEC SEMICONDUCTOR Corp.

Contents

1. Layer Information

1.1 Layer Definitions

Gds No.	Layer Name	Description	Design Grid
20	DNW	Deep N-well area	0.005um
3	NWELL	N-well area	0.005um
4	PWELL	P-well data for CD patterns (circuit pattern is generated from NWELL)	0.005um
1	AA	Active area separated from Field area	0.005um
48	PVT	5V P-ch Standard-Vt channel implant area	0.005um
47	PLVT	5V P-ch Low-Vt channel implant area	0.005um
84	PLLVT	5V P-ch Very Low-Vt channel implant area	0.005um
49	NVT	5V N-ch Standard-Vt channel implant area	0.005um
50	NLVT	5V N-ch Low-Vt channel implant area	0.005um
51	NDVT	5V N-ch Depletion-Vt channel implant area	0.005um
19	RH	High-Resistor area on CRP	0.005um
65	RM	Medium-Resistor area on CRP	0.005um
66	RL	Low-Resistor area on CRP	0.005um
17	CRP	Poly-Si Resistor and bottom plate of PIP	0.005um
7	POLY	Gate, interconnect polycide and upper plate of PIP	0.005um
6	NCH	N+S/D and LDD implant area	0.005um
5	PCH	P-ch data for CD patterns (circuit pattern is generated from NCH and NOIMP)	0.005um
71	ESD	5V ESD implant area	0.005um
18	NOIMP	Resistor and Fuse area	0.005um
8	CONT	Contact	0.005um
9	1METAL	1st Metal	0.005um
10	1VIA	Via hole between 1st and 2nd metal	0.005um
11	2METAL	2nd Metal	0.005um
12	2VIA	Via hole between 2nd and 3rd metal	0.005um
13	3METAL	3rd Metal	0.005um
16	PAD	Pad open	0.005um
46	FUSE	Poly Fuse opening area	0.005um
69	PI	Polyimide opening area	0.005um
83	NWL_CD	NWELL data for CD patterns (not to be PWELL)	0.005um
86	NCH_CD	NCH data for CD patterns (not to be PCH)	0.005um
40	WAKU	Chip outline	5.000um
57	NODRC	DRC exception area	0.005um
58	SRING	Seal_ring identification for Extraction	0.005um
73	ZD	Diode identification for Extraction	0.005um
74	ZB	Bipolar transistor identification for Extraction	0.005um
75	ZR	Resistor identification for Extraction	0.005um
76	ZC	Capacitor identification for Extraction	0.005um
87	ZRMET1	1METAL Resistor identification for Extraction	0.005um
88	ZRMET2	2METAL Resistor identification for Extraction	0.005um
89	ZRMET3	3METAL Resistor identification for Extraction	0.005um
90	ZPSUB2	PSUB separation area identification for Extraction	0.005um
41	TEXT	TEXT	
77	TXTPO	Poly text for Extraction	
78	TXT1M	1Metal text for Extraction	
79	TXT2M	2Metal text for Extraction	
80	TXT3M	3Metal text for Extraction	

1.1 Layer Definitions ~ continued ~

Gds No.	Layer Name	Description	Design Grid
23	GO	5V area definition	0.005um
24	NL3(*1)	3.3V N-ch Vth, Pocket and LDD implant area (circuit pattern is generated from NCH and GO)	0.005um
25	NL5(*1)	5V N-ch LDD implant area (circuit pattern is generated from NCH and GO)	0.005um
26	PL3(*1)	3.3V P-ch Pocket implant area (circuit pattern is generated from NWELL, NCH, NOIMP and GO)	0.005um
37	RECOGR	3.3V Resistor identification for Extraction	0.005um
30	Boundary	Cell outline	
28	TEXT	TEXT (in 3.3V sample cell)	
41	MTEXT1_10	1Metal text for Extraction (in 3.3V sample cell)	
42	MTEXT2_10	2Metal text for Extraction (in 3.3V sample cell)	
43	MTEXT3_10	3Metal text for Extraction (in 3.3V sample cell)	

(*1) GDS data for circuit pattern is generated by Calibre calculation file.

1.2 Mask Specifications

No.	Process Layer Name	Mask Layer Name	C/D	Drawing Gds No.	Mask Calculation		Memo
					Gds No.	Layer Name	
1	DNW	B2	C	20	20	DNW	Deep_Nwell area
2	NWELL	W2	C	3	3	NWELL	Nwell area
3	PWELL	W1	D	–	3	NWELL	reverse of Nwell area
4	AA	L1	D	1	1	AA	Active area
5	PVT	T1	C	48	48	PVT	5V Pch Standard Vth Imp. area
6	PLVT	T2	C	47	47	PLVT	5V Pch Low Vth Imp. area
7	PLLVT	T3	C	84	84	PLLVT	5V Pch Very Low Vth Imp. area
8	NVT	T5	C	49	49	NVT	5V Nch Standard Vth Imp. area
9	NLVT	T7	C	50	50	NLVT	5V Nch Low Vth Imp. area
10	NDVT	T8	C	51	51	NDVT	5V Nch Depletion Vth Imp. area
11	MRPA	P4	D	19	19	RH	High Resistance Definition area
12	MRPB	P5	D	65	19+65	RH+RM	Medium Resistance Definition area
13	LRPA	P7	D	66	19+65+66	RH+RM+RL	Low Resistance Definition area
14	CRP	P8	D	17	17	CRP	Poly_Si Resistor & bottom plate of PIP
15	POLY	P1	D	7	7	POLY	Gate Poly & upper plate of PIP
16	NCH	S2	C	6	6	NCH	N+Source/Drain/Tap & PiP bottom plate & N+ Contact Plug area
17	ESD	S4	C	71	71	ESD	5V ESD Imp. area
18	PCH	S1	D	–	6+18(*1)	NCH+NOIMP	P+Source/Drain/Tap & P+ Contact Plug area
19	CONT	C1	C	8	8	CONT	Contact
20	1METAL	A1	D	9	9	1METAL	Metal1 interconnect
21	1VIA	C2	C	10	10	1VIA	Vias between metal1 and metal2
22	2METAL	A2	D	11	11	2METAL	Metal2 interconnect
23	2VIA	C3	C	12	12	2VIA	Vias between metal2 and metal3
24	3METAL	A3	D	13	13	3METAL	Metal3 interconnect
25	PAD	O1	C	16	16	PAD	Passivation opening area
26	FUSE	O3	C	46	46	FUSE	Poly Fuse opening area
27	PI	O4	C	69	69	PI	PIX opening area (PAD,FUSE)
28	GO	G1	D	23	23	GO	5V area definition
29	NL3	S6	C	24	6 not 23	NCH not GO	3.3V N-ch Vth, Pocket & LDD Imp. area
30	NL5	S3	C	25	6 and 23	NCH and GO	5V N-ch LDD Imp. area
31	PL3	S5	C	26	3 not {(6+18) not 23}	NWELL not {(NCH+NOIMP) not GO}	3.3V P-ch Pocket Imp. area
(*1)	NOIMP	–	–	18	–	–	Resistor and Fuse area

1.3 Process Mask table

No.	Process step	Process Layer	Layer Name	comment
1	AA Mask	AA	AA	Active area
2	DNW Mask	DNW	DNW	Deep_Nwell area
3	NWELL Mask	NWELL	NWELL	Nwell area
4	PVT3 Mask	PL3	NWELL not {(NCH+NOIMP) not GO}	3.3V Pch Vth Imp. area
5	PVT Mask	PVT	PVT	5V Pch Standard Vth Imp. area
6	PLVT Mask	PLVT	PLVT	5V Pch Low Vth Imp. area
7	PLLVT Mask	PLLVT	PLLVT	5V Pch Very Low Vth Imp. area
8	PWELL Mask	PWELL	NWELL	reverse of Nwell area
9	NVT3 Mask	NL3	NCH not GO	3.3V Nch Vth Imp. area
10	NVT Mask	NVT	NVT	5V Nch Standard Vth Imp. area
11	NLVT Mask	NLVT	NLVT	5V Nch Low Vth Imp. area
12	NDVT Mask	NDVT	NDVT	5V Nch Depletion Vth Imp. area
13	GOX Mask	GO	GO	3.3V Nch/Pch Vth Imp. & Ox Etch area
14	MRPA Mask	MRPA	RH	High Resistance Definition area
15	MRPB Mask	MRPB	RH+RM	Medium Resistance Definition area
16	LRPA Mask	LRPA	RH+RM+RL	Low Resistance Definition area
17	CRP Mask	CRP	CRP	Poly_Si Resistor & bottom plate of PIP
18	Poly Mask	POLY	POLY	Gate Poly & upper plate of PIP
19	NLD3 Mask	NL3	NCH not GO	3.3V Nch Pocket & LDD Imp. area
20	NLD5 Mask	NL5	NCH and GO	5V Nch LDD Imp. area
21	PLD3 Mask	PL3	NWELL not {(NCH+NOIMP) not GO}	3.3V Pch Pocket Imp. area
22	PLD Mask	PCH	NCH+NOIMP	Pch LDD Imp. area
23	NCH Mask	NCH	NCH	N+Source/Drain/Tap & PiP bottom plate
24	ESD(NSD2) Mask	ESD	ESD	5V ESD Imp. area
25	PCH Mask	PCH	NCH+NOIMP	P+Source/Drain/Tap area
26	CONT Mask	CONT	CONT	Contact
27	N Plug Mask	NCH	NCH	N+ Contact Plug area
28	P Plug Mask	PCH	NCH+NOIMP	P+ Contact Plug area
29	1METAL Mask	1METAL	1METAL	Metal1 interconnect
30	1VIA Mask	1VIA	1VIA	Vias between metal1 and metal2
31	2METAL Mask	2METAL	2METAL	Metal2 interconnect
32	2VIA Mask	2VIA	2VIA	Vias between metal2 and metal3
33	3METAL Mask	3METAL	3METAL	Metal3 interconnect
34	FUSE Mask	FUSE	FUSE	Poly Fuse opening area
35	PAD Mask	PAD	PAD	Passivation opening area
36	PI Mask	PI	PI	PIX opening area (PAD,FUSE)

1.4 Device Description

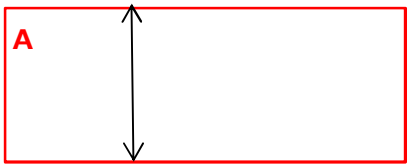
Device Names	Description
MPM	5V Pch Medium Vt MOS Transistor（N+Polycide gate）
MPL	5V Pch Low Vt MOS Transistor（N+Polycide gate）
MPL2	5V Pch Very Low Vt MOS Transistor（N+Polycide gate）
MPN	5V Pch Native Vt MOS Transistor（N+Polycide gate）
MPMI	5V Isolated Type Pch Medium Vt MOS Transistor（N+Polycide gate）
MPLI	5V Isolated Type Pch Low Vt MOS Transistor（N+Polycide gate）
MPL2I	5V Isolated Type Pch Very Low Vt MOS Transistor（N+Polycide gate）
MPNI	5V Isolated Type Pch Native Vt MOS Transistor（N+Polycide gate）
MNM	5V Nch Medium Vt MOS Transistor（N+Polycide gate）
MNH	5V Nch High Vt MOS Transistor（N+Polycide gate）
MNL	5V Nch Low Vt MOS Transistor（N+Polycide gate）
MND	5V Nch Depletion Vt MOS Transistor（N+Polycide gate）
MNN	5V Nch Native Vt MOS Transistor（N+Polycide gate）
MNE_LC	5V Nch ESD Protection MOS Transistor（N+Polycide gate）(8 finger)
MNE_PC	5V Nch ESD Protection MOS Transistor（N+Polycide gate）(10 finger)
MNMI	5V Isolated Type Nch Medium Vt MOS Transistor（N+Polycide gate）
MNHI	5V Isolated Type Nch High Vt MOS Transistor（N+Polycide gate）
MNLI	5V Isolated Type Nch Low Vt MOS Transistor（N+Polycide gate）
MNDI	5V Isolated Type Nch Depletion Vt MOS Transistor（N+Polycide gate）
MNNI	5V Isolated Type Nch Native Vt MOS Transistor（N+Polycide gate）
MNEI_LC	5V Isolated Type Nch ESD Protection MOS Transistor（N+Polycide gate）(8 finger)
MNEI_PC	5V Isolated Type Nch ESD Protection MOS Transistor（N+Polycide gate）(10 finger)
RPL	Low Resistance Poly-Si Resistor (95ohm/s)
RPM	Medium Resistance Poly-Si Resistor (330ohm/s)
RPH	High Resistance Poly-Si Resistor (5Kohm/s)
RPH2	High Resistance Poly-Si Resistor (8Kohm/s)
RNW	Nwell Diffusion Resistor
RN	N+ Diffusion Resistor
RP	P+ Diffusion Resistor
CPIP	PIP Capacitor
CND	Nch Depletion Vt MOS Capacitor（N+Polycide gate）
CNDI	Isolated Type Nch Depletion Vt MOS Capacitor（N+Polycide gate）
CPL2	Pch Very Low Vt MOS Capacitor（N+Polycide gate）
CPL2I	Isolated Type Pch Very Low Vt MOS Capacitor（N+Polycide gate）
PNP	Vertical PNP (P+/NWELL/Psub)
PNP2	Vertical PNP (P+/NWELL+DNW/Psub)
NPN	Vertical NPN (N+/PWELL/DNW)
RFS	Poly-Si Laser Trimming Fuse
DP	P+/Nwell Diode
DP2	P+/Nwell in Niso Diode
DN	N+/Pwell Diode
DN2	N+/Pwell in Niso Diode
P	3.3V Pch MOS Transistor（N+Polycide gate）
N	3.3V Nch MOS Transistor（N+Polycide gate）

1.5 Device to Layer Mapping Matrix

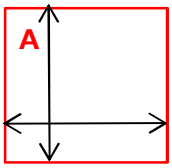
Device \ Layer		DNW	NWELL	AA	PLVT	PVT	PLLVT	NVT	NLVT	NDVT	RH	RM	RL	NOIMP	CRP	POLY	NCH	ESD	CONT	1METAL	FUSE	PI	ZD *ID layer	ZB *ID layer	ZR *ID layer	ZC *ID layer	GO
MOS-Transistor	5V MPM(Pch Medium)		O	O		O										O	O		O	O							O
	5V MPL(Pch Low)		O	O	O											O	O		O	O							O
	5V MPL2(Pch very Low)		O	O			O									O	O		O	O							O
	5V MPN(Pch Native)		O	O												O	O		O	O							O
	5V MPMI(Pch Medium Iso)	O	O	O		O										O	O		O	O							O
	5V MPLI(Pch Low Iso)	O	O	O	O											O	O		O	O							O
	5V MPL2I(Pch very Low Iso)	O	O	O			O									O	O		O	O							O
	5V MPNI(Pch Native Iso)	O	O	O												O	O		O	O							O
	5V MNM(Nch Medium)			O				O								O	O		O	O							O
	5V MNH(Nch High)			O	O											O	O		O	O							O
	5V MNL(Nch Low)			O		O			O							O	O		O	O							O
	5V MND(Nch Depletion)			O						O										O							O
	5V MNN(Nch Native)			O												O	O		O	O							O
	5V MNE_LC/MNE_PC(Nch Esd protection)			O	O	O										O	O	O	O	O							O
	5V MNMI(Nch Medium Iso)	O	O	O				O								O	O		O	O							O
	5V MNHI(Nch High Iso)	O	O	O	O	O										O	O		O	O							O
	5V MNLI(Nch Low Iso)	O	O	O					O							O	O		O	O							O
	5V MNDI(Nch Depletion Iso)	O	O	O						O										O							O
	5V MNNI(Nch Native Iso)	O	O	O												O	O		O	O							O
	5V MNEI_LC/MNEI_PC(Nch Esd protection Iso)	O	O	O	O	O										O	O	O	O	O							O
	3.3V P (Pch)		O	O												O	O		O	O							
	3.3V N (Nch)			O												O	O		O	O							
Resistor	RPL(Low sheet Poly Resistor)												O	O	O										O		
	RPM(Medium sheet Poly Resistor)											O		O	O										O		
	RPH(High sheet Poly Resistor[5kΩ/sl])										O			O	O										O		
	RPH2(High sheet Poly Resistor[8kΩ/sl])										O			O	O										O		
	RNW(Nwell Diff. Resistor)		O	O													O		O	O					O		O
	RN(N+ Diff. Resistor)			O													O		O	O					O		O
	RP(P+ Diff. Resistor)		O	O															O	O					O		O
Capacitor	CPIP(PIP Capacitor)														O	O	O		O	O					O	O	O
	CNDI(Nch Depletion Capacitor)			O						O						O	O		O	O					O	O	O
	CNDI2(Iso Nch Depletion Capacitor)	O	O	O						O						O	O		O	O					O	O	O
	CPL2(Pch Very Low Capacitor)		O	O			O									O	O		O	O							O
	CPL2I(Iso Pch Very Low Capacitor)	O	O	O			O									O	O		O	O							O
BJT	PNP(Vertical PNP (P+/NWELL/Psub))		O	O													O	O	O	O				O			O
	PNP2(Vertical PNP (P+/NWELL+DNW/Psub))	O	O	O													O	O	O	O				O			O
	NPN(Vertical NPN (N+/PWELL/DNW))	O	O	O													O		O	O				O			O
Fuse	RFS(Fuse)															O			O	O	O	O			O		
Diode	DP(P+/Nwell Diode)		O	O													O	O	O	O			O				O
	DP2(P+/Nwell in Niso Diode)	O	O	O													O	O	O	O			O				O
	DN(N+/Pwell Diode)			O													O	O	O	O			O				O
	DN2(N+/Pwell in Niso Diode)	O	O	O													O	O	O	O			O				O

1.6 Definition of the Layout Geometry

A width



A size



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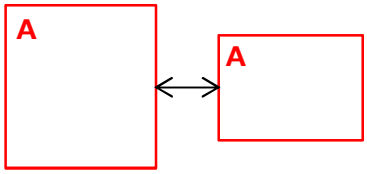
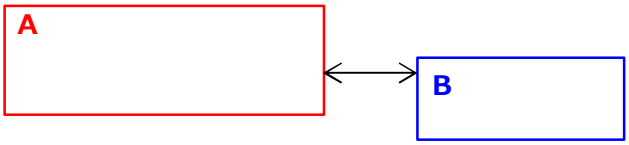
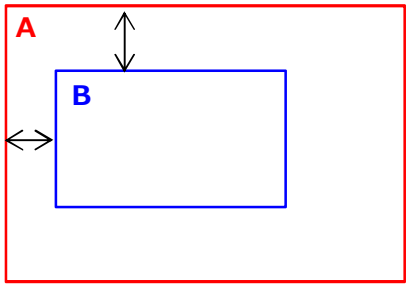


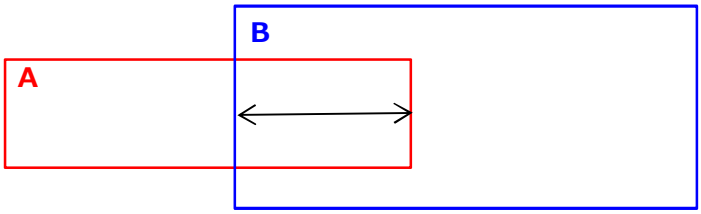
A spacing to B



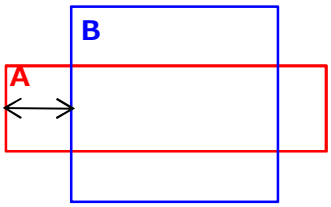
A enclosure of B
（かぶり幅）



A overlap of B
（重なり幅）



A extension beyond B
（突き出し量）

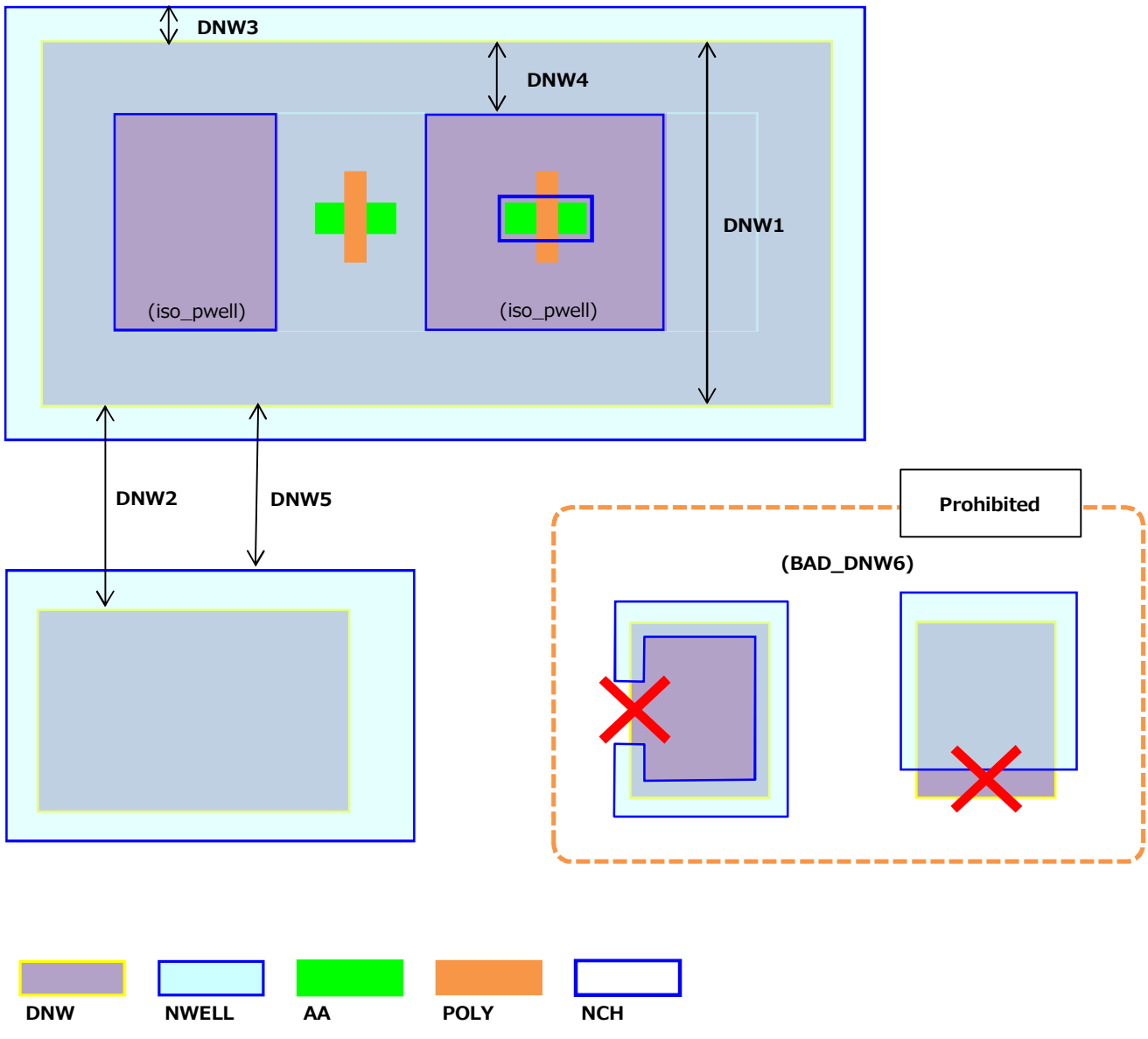


2. Layer Rules

2.1 DNW

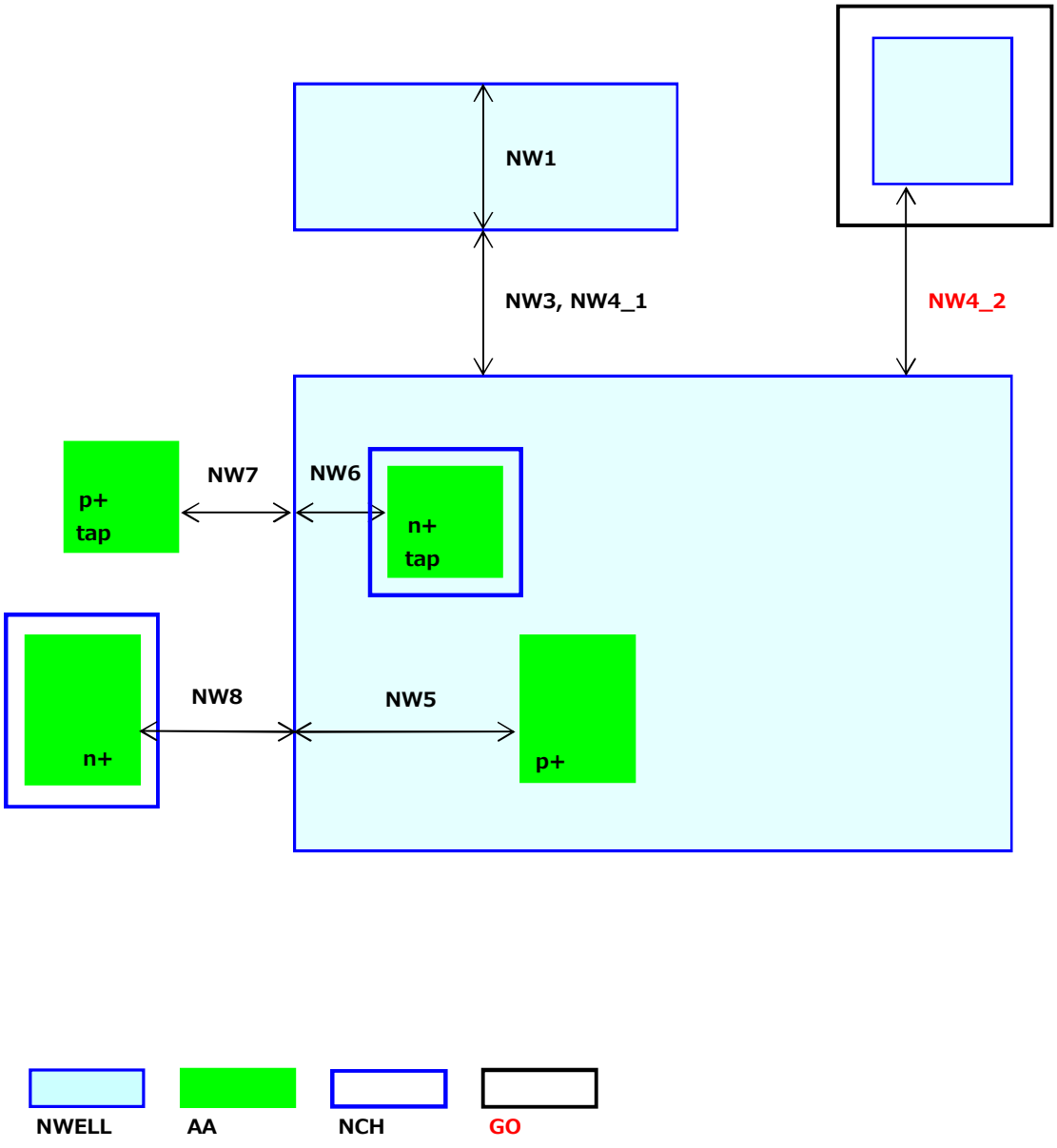
Rule No.	Description	class	Layout Rule (um)
DNW1	DNW width	min	5.00
DNW2	DNW spacing	min	5.00
DNW3	NWELL extension beyond DNW	min	1.50
DNW4	NWELL overlap to DNW	min	1.50
DNW5	DNW spacing to NWELL	min	3.50
BAD_DNW6	DNW_edge must be covered by NWELL		

* DNW potential must be kept higher than inner Pwell.



2.2 NWELL

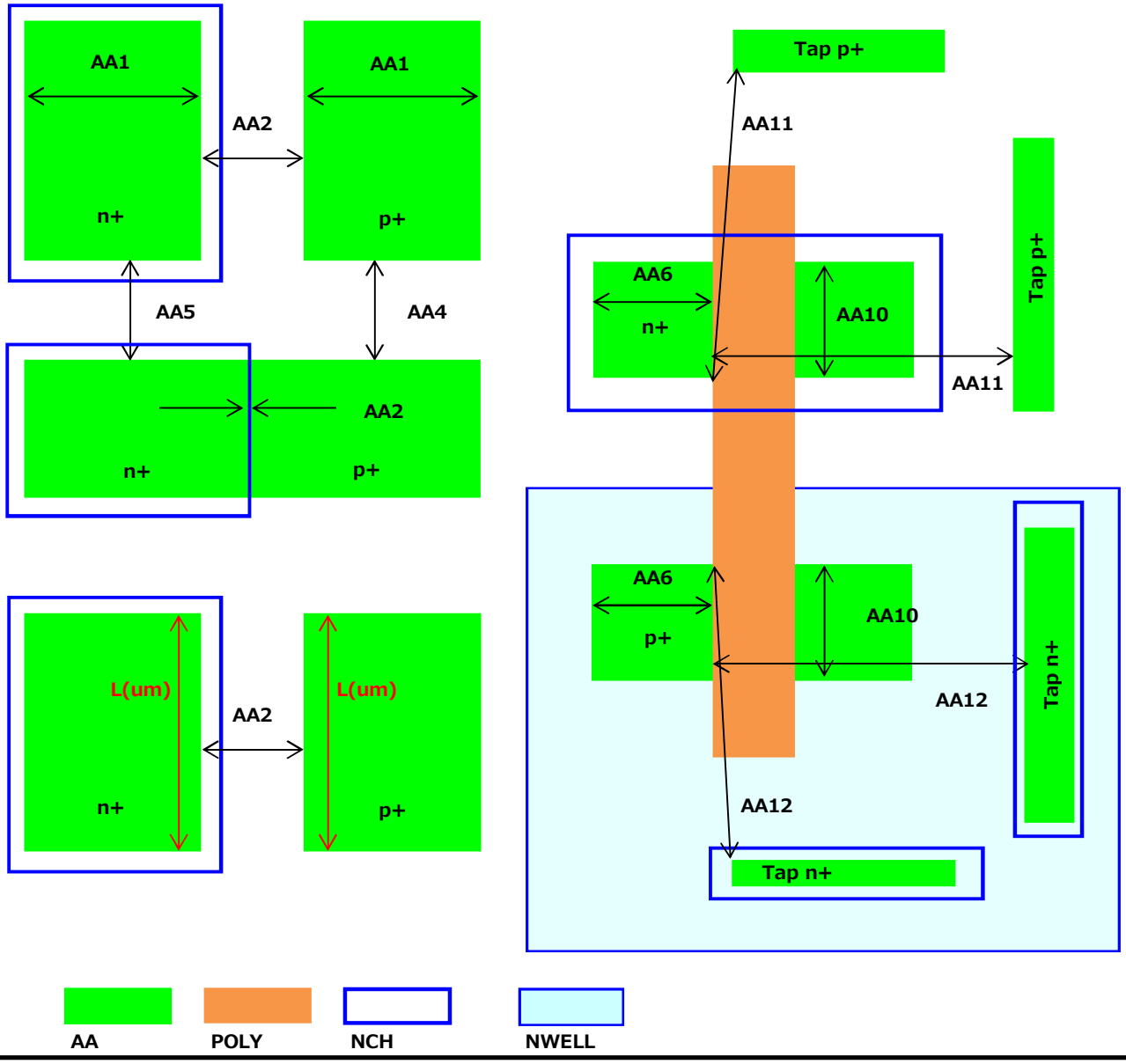
Rule No.	Description	class	Layout Rule (um)
NW1	NWELL width	min	1.20
NW3	NWELL spacing(same node)	min	1.20
NW4_1	NWELL spacing(different node)	min	5.00
NW4_2	@ NWELL(3.3V) spacing to NWELL(5V)	min	7.00
NW5	NWELL enclosure of AA(p+)	min	1.00
NW6	NWELL enclosure of AA(n+tap)	min	0.45
NW7	NWELL spacing to AA(p+tap)	min	0.45
NW8	NWELL spacing to AA(n+)	min	1.00



2.3 AA

Rule No.	Description		class	Layout Rule (um) 5V	3.3V
AA1	AA(p+,n+) width		min	0.45	
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69	0.55
AA2_2		same node @ L≧7.0um	min	0.50 or butting	0.55
AA2_3		same node @ L<7.0um			0.45
AA4	AA(p+) spacing		min	0.60	0.55
AA5	AA(n+) spacing		min	0.60	0.55
AA6	AA extension beyond gate		min	0.65	0.63
AA10_1	AA width in gate @ AA(N+)		min	0.70	0.50
AA10_2	@ AA(P+)				0.60
AA11	The distance from NMOS gate to the nearest Tap AA(p+)		max	30	
AA12	The distance from PMOS gate to the nearest Tap AA(n+)		max	100	

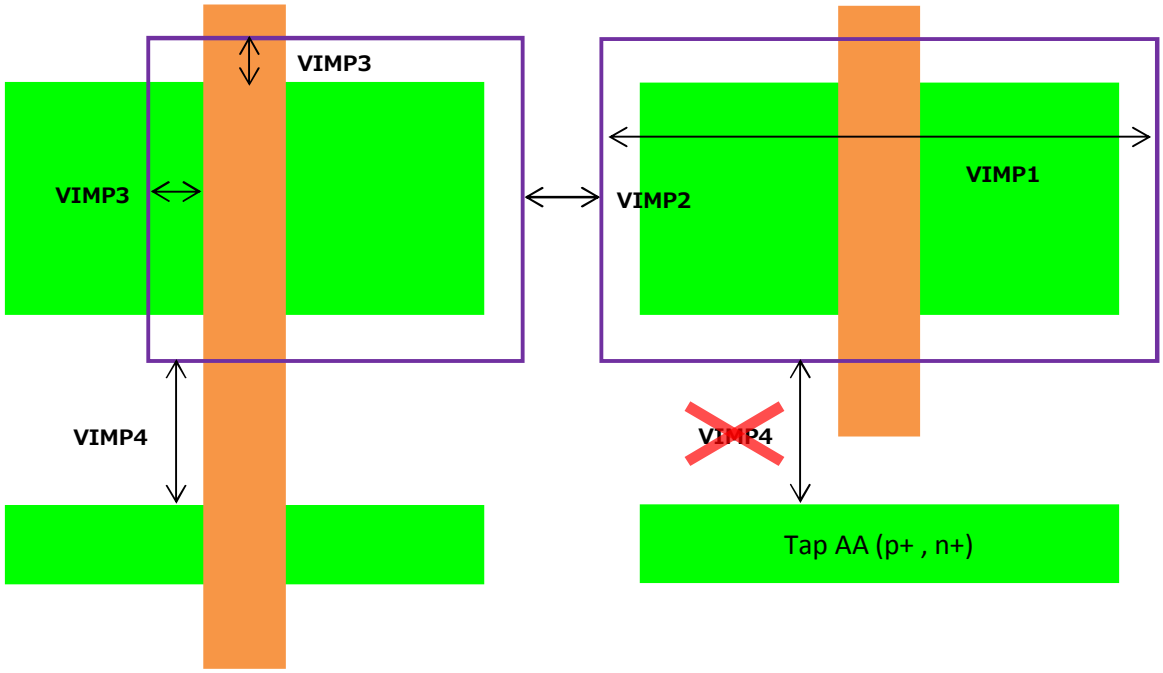
*Definition of gate is (POLY and AA).



2.4 VIMP (PLVT,PVT,PLLVT,NVT,NLVT,NDVT)

Rule No.	Description	class	Layout Rule (um)
VIMP1	VIMP width	min	0.80
VIMP2	same VIMP spacing	min	0.80
VIMP3	VIMP enclosure of gate (POLY and AA)	min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)	min	0.30

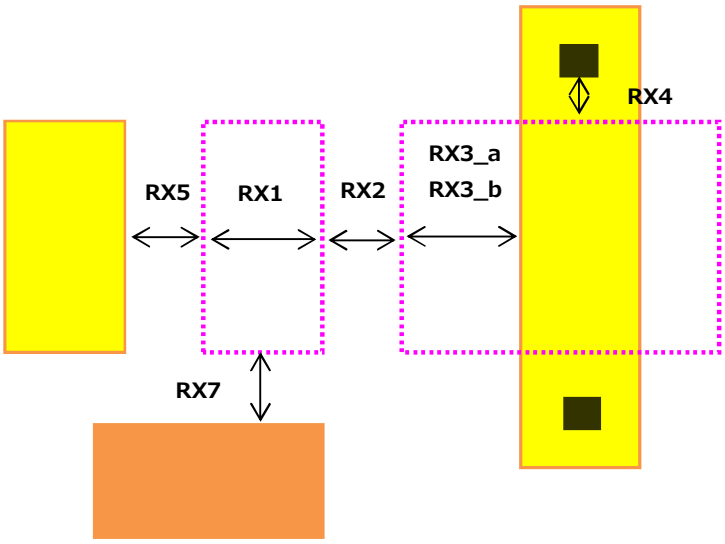
*PLVT, PVT, PLLVT, NVT, NLVT, NDVT are showed as representative VIMP

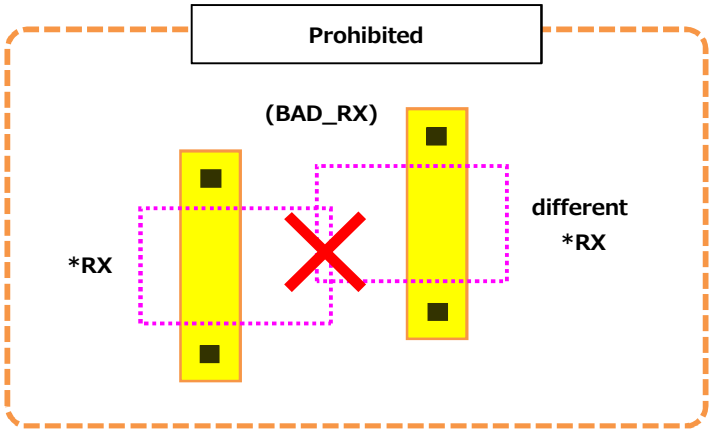


2.5 RX (RH,RM,RL)

Rule No.	Description	class	Layout Rule (um)
RX1	RX width	min	0.80
RX2	same RX spacing	min	0.80
RX3_a	RL extension beyond CRP for RPL	min	4.00
RX3_b	RM, RH extension beyond CRP for RPM,RPH	min	8.00
RX4	RX spacing to CONT for RPL,RPM,RPH	fix	0.56
RX5	RX spacing to CRP for RPL,RPM,RPH,PiP	min	3.50
RX7	RX spacing to POLY	min	3.50
BAD_RX	Overlap of different RXs is prohibited.		

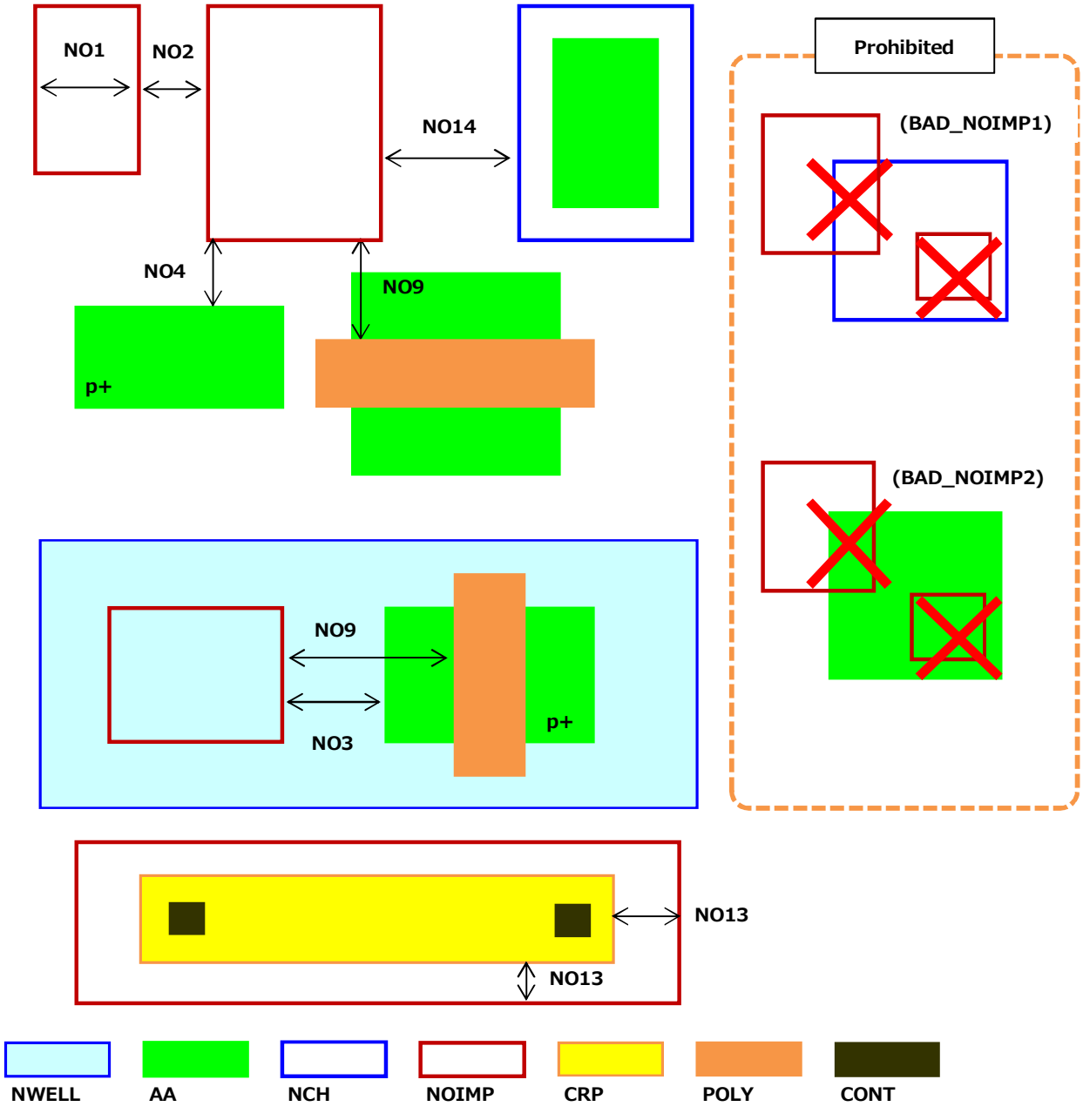
*RH, RM, RL are showed as representative RX (except for Rule.RX3)





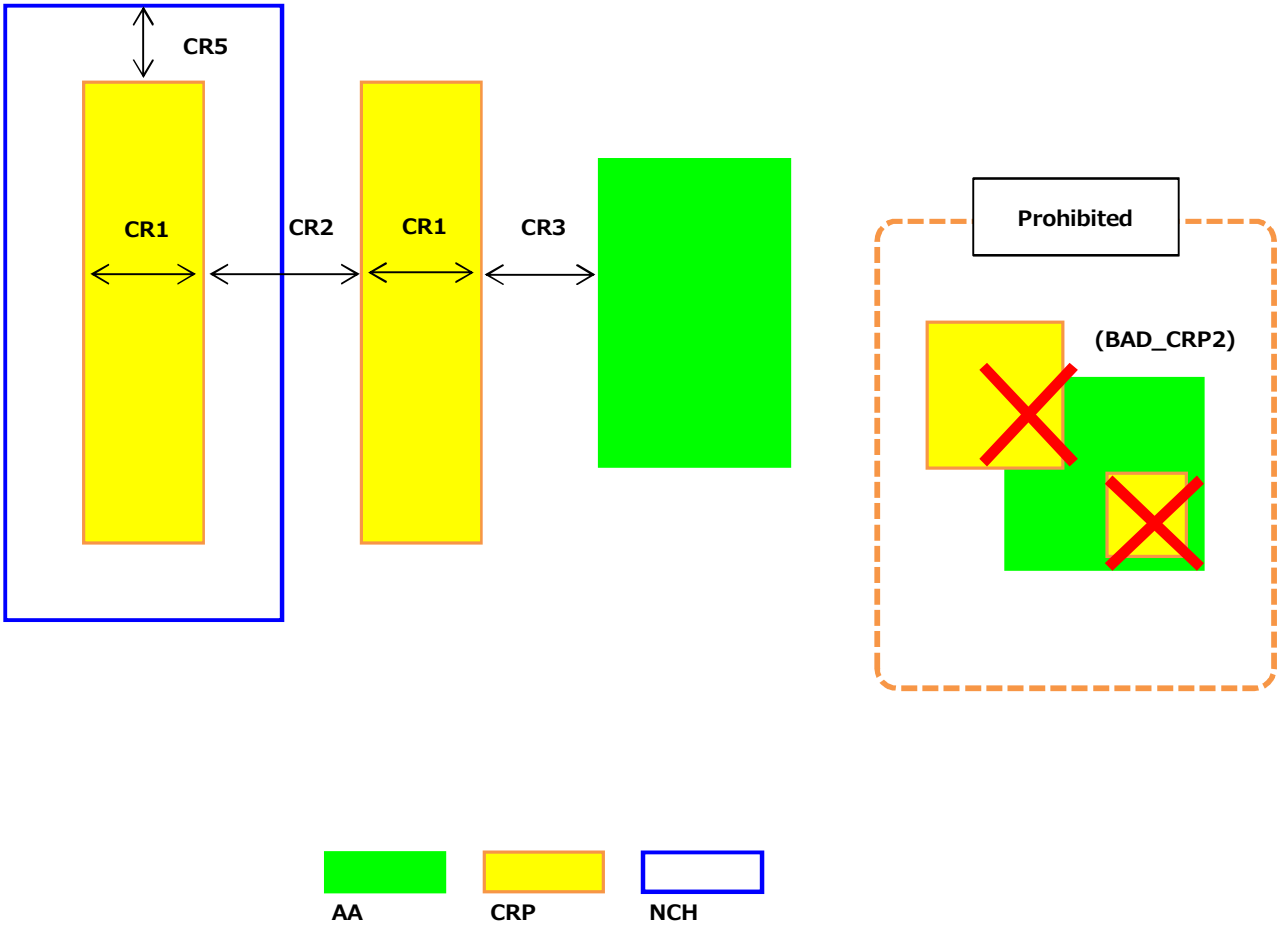
2.6 NOIMP

Rule No.	Description	class	Layout Rule (um)
NO1	NOIMP width	min	0.80
NO2	NOIMP spacing	min	0.80
NO3	NOIMP spacing to AA(p+) in NWELL	min	0.27
NO4	NOIMP spacing to AA(p+tap) in PWELL	min	0.13
NO9	NOIMP spacing to gate_POLY	min	0.86
NO13	NOIMP enclosure of CRP for RPL,RPM,RPH	min	0.48
NO14	NOIMP spacing to NCH	min	0.76 or butting
BAD_NOIMP1	NOIMP overlap NCH is prohibited		
BAD_NOIMP2	NOIMP overlap AA is prohibited		



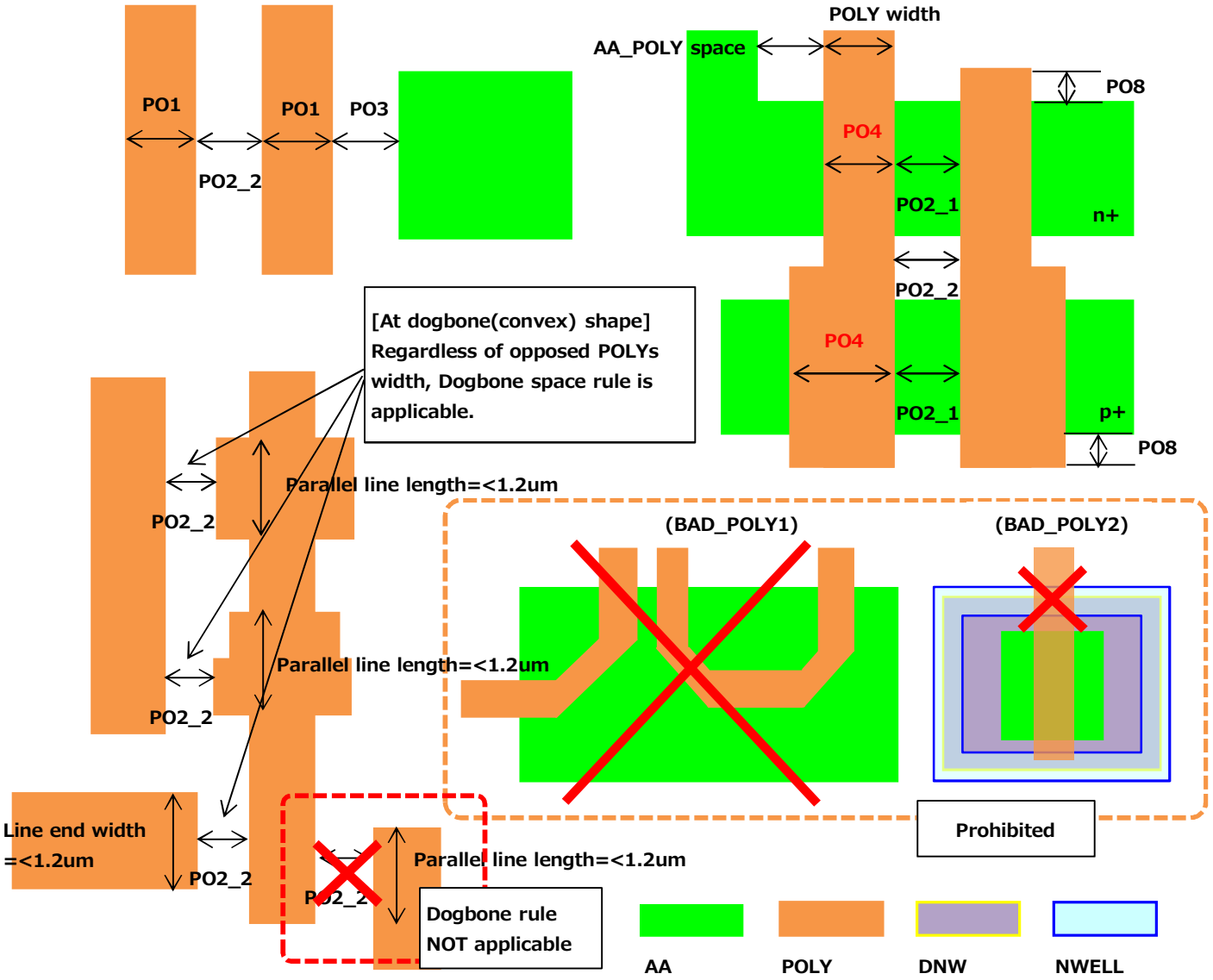
2.7 CRP

Rule No.	Description	class	Layout Rule (um)
CR1	CRP width	min	0.86
CR2	CRP spacing	min	0.62
CR3	CRP spacing to AA	min	0.23
CR5	NCH enclosure of CRP (only for CPIP)	min	0.48
BAD_CRP2	CRP overlap AA is prohibited		



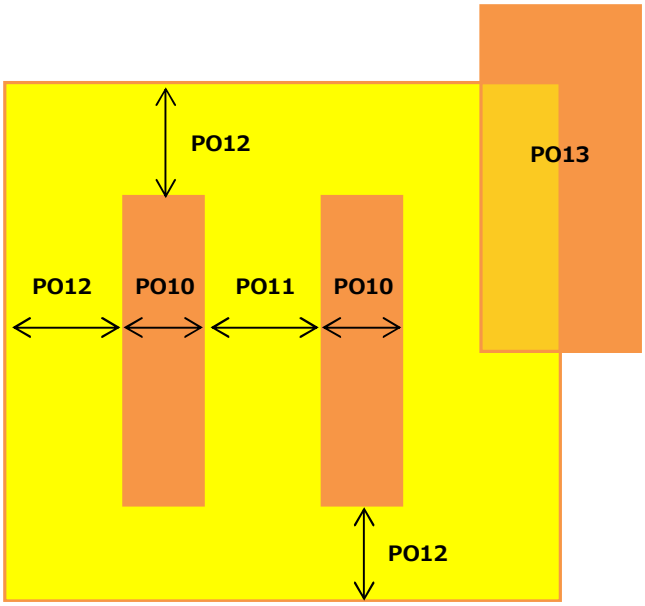
2.8 POLY (for polycide gate and interconnect polycide)

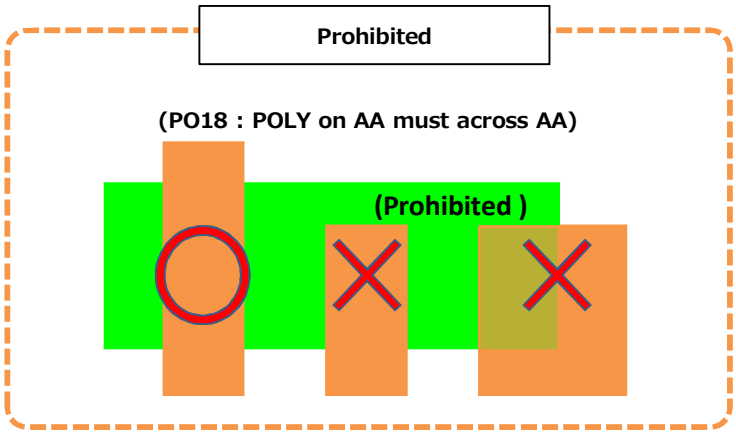
Rule No.	Description		class	Layout Rule (um)
PO1	POLY width on Field		min	0.37
PO2_1	POLY spacing (on AA)	@ either/both POLY width=<1.2um	min	0.39
		@ either/both POLY width>1.2um	min	0.49
PO2_2	POLY spacing (on Field)	@ both POLY width<0.5um	min	0.35
		@ 0.5um=<either/both POLY width=<1.2um	min	0.37
		@ either/both POLY width>1.2um	min	0.47
	@ dogbone space(Parallel line length or opposite line end width=<1.2um)		min	0.35
*) When a length of dogbone convex part is below 1.2um, the dogbone rule is applied without depending on opposing POLY width.				
PO3	POLY spacing to AA		min	0.10
PO4	POLY width on AA		min	0.39
PO8_1	POLY extension beyond AA	@ POLY width<0.5, AA-POLY space<0.44	min	0.76
PO8_2		@ POLY width<0.5, 0.44≦AA-POLY space	min	0.40
PO8_3		@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
BAD_POLY1	POLY bending is prohibited			
BAD_POLY2	POLY across NWELL of Isolated_Type_Nch_Transistor is prohibited			



2.8 POLY (for upper plate of capacitors and MOS capacitors)

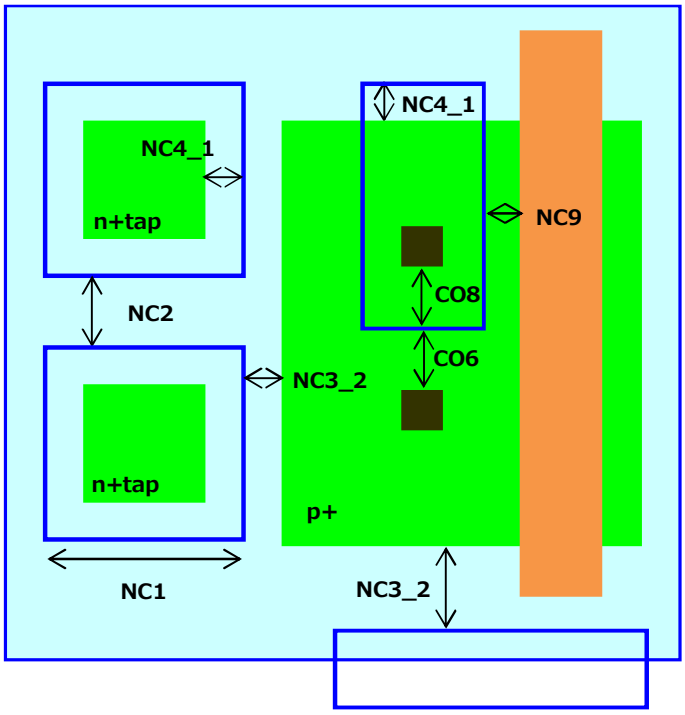
Rule No.	Description	class	Layout Rule (um)
PO10	POLY width (on CRP)	min	0.59
PO11	POLY spacing (on CRP)	min	0.52
PO12	CRP enclosure of POLY	min	0.60
PO13	POLY_edge must not cross CRP_edge		
PO18	POLY on AA must across AA		

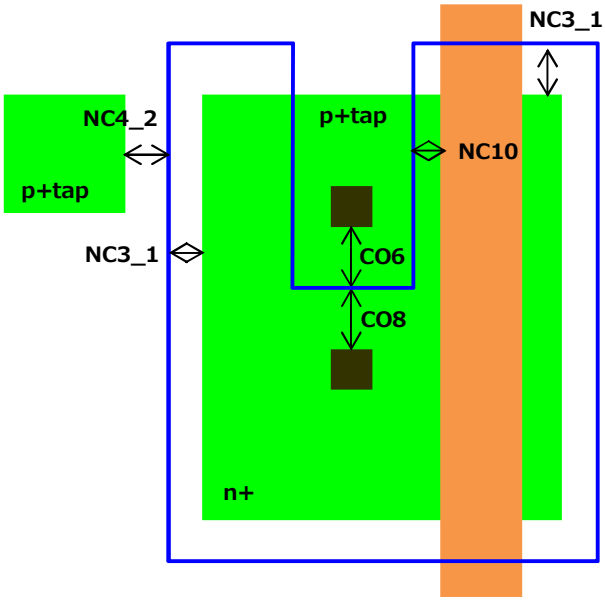


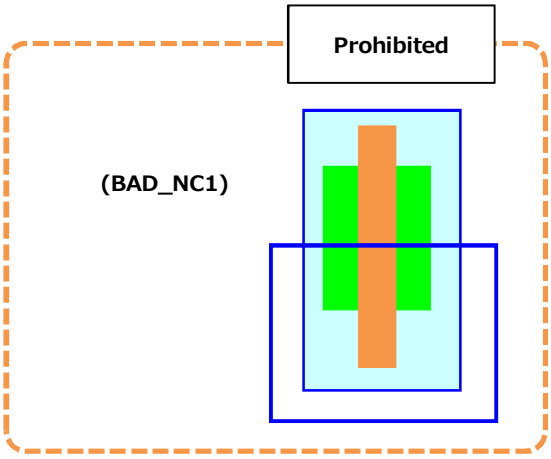


2.9 NCH

Rule No.	Description	class	Layout Rule (um)
NC1	NCH width	min	0.76
NC2	NCH spacing	min	0.76
NC3_1	NCH extension beyond AA(n+) in pwell	min	0.30
NC3_2	NCH spacing to AA(p+) in NWELL	min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL	min	0.15
NC4_2	NCH spacing to AA(p+tap) in pwell	min	0.15
NC9	NCH spacing to gate_POLY in AA	min	0.85
NC10	NCH extension beyond gate_POLY in AA	min	0.85
BAD_NC1	NCH crossing gate_POLY in AA is prohibited		

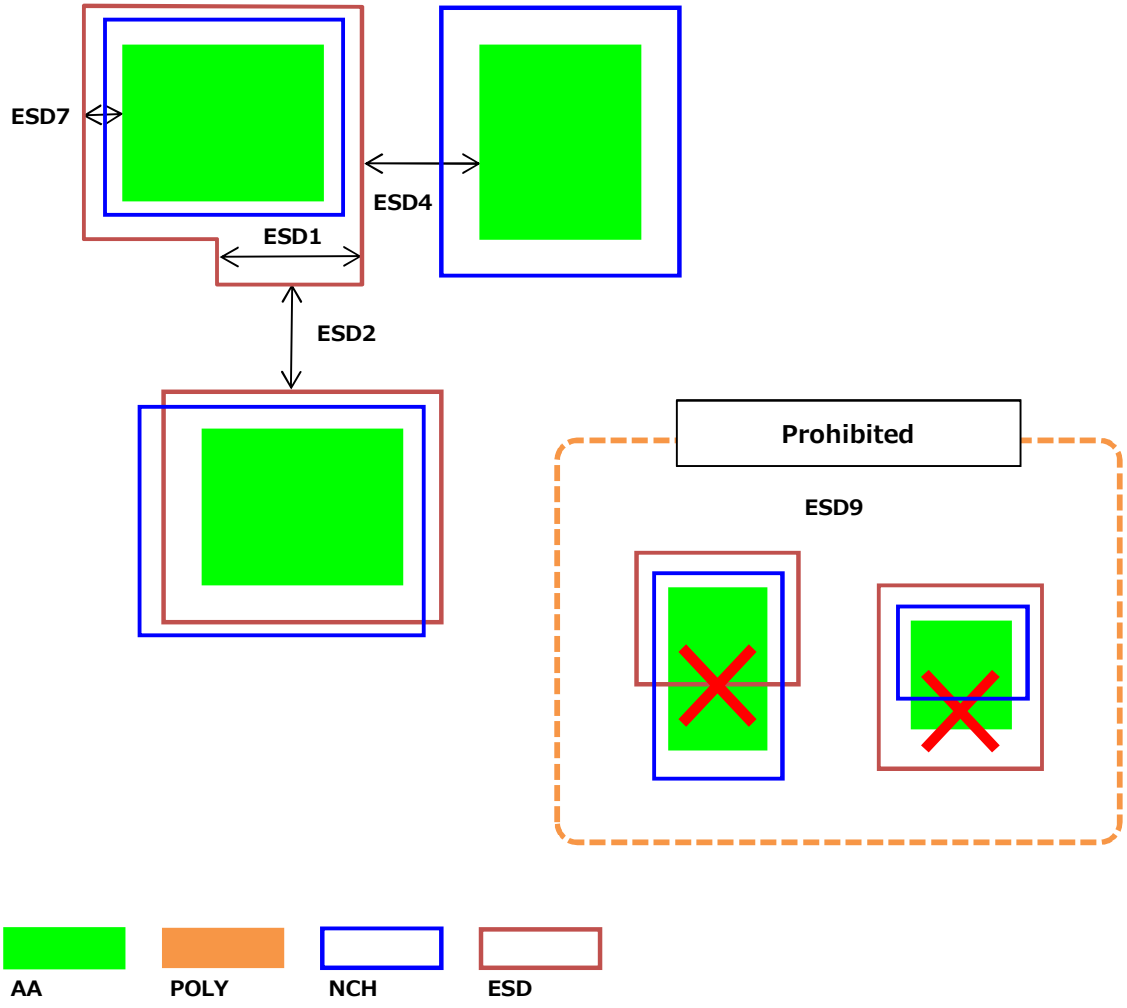






2.10 ESD

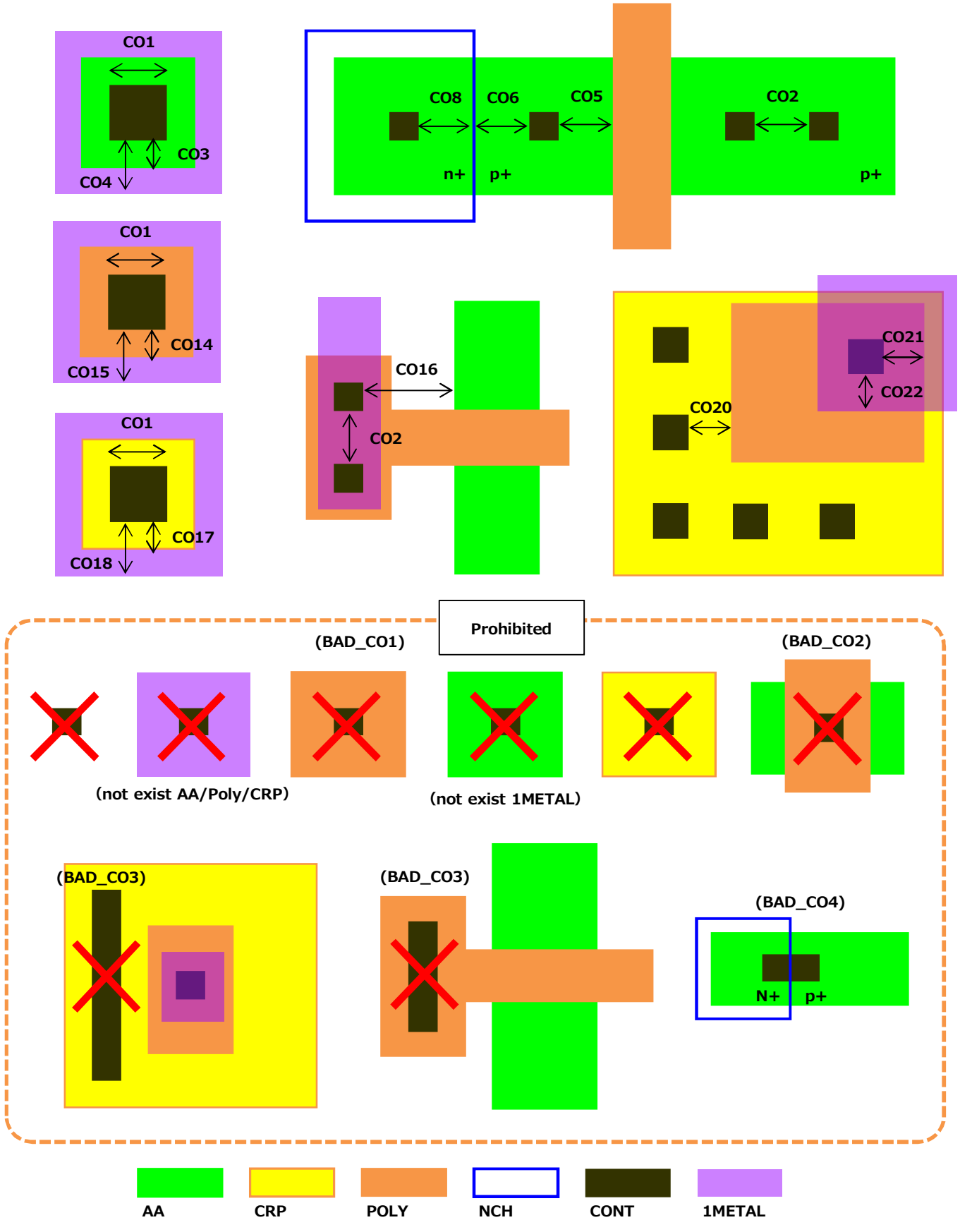
Rule No.	Description	class	Layout Rule (um)
ESD1	ESD width	min	0.80
ESD2	ESD spacing	min	0.80
ESD4	ESD spacing to AA	min	0.30
ESD7	ESD enclosure of AA	min	0.30
ESD9	AA on ESD must be enclosed by NCH and ESD		



2.11 CONT

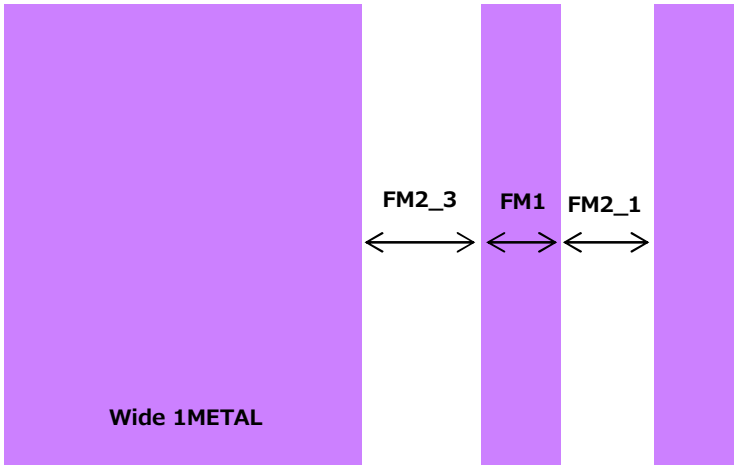
Rule No.	Description		class	Layout Rule (um)
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
For contact to AA [CONT_aa]				
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO4_1	1METAL enclosure of CONT	CONT size=0.40x0.40	min	0.13
CO4_2		CONT size=0.40xL (rectangle)	min	0.38
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO6_1	CONT spacing to NCH for butting diffusion	CONT size=0.40x0.40	min	0.36
CO6_2		CONT size=0.40xL (rectangle)	min	0.51
CO8_1	NCH enclosure of CONT for butting diffusion	CONT size=0.40x0.40	min	0.36
CO8_2		CONT size=0.40xL (rectangle)	min	0.51
For contact to POLY [CONT_poly]				
CO14	POLY enclosure of CONT		min	0.20
CO15	1METAL enclosure of CONT		min	0.13
CO16	CONT spacing to AA		min	0.29
For contact to CRP [CONT_crp]				
CO17	CRP enclosure of CONT		min	0.45
CO18	1METAL enclosure of CONT		min	0.25
CO20	CONT spacing to POLY (on CRP)		min	0.47
For contact to POLY(upper plate of capacitor) [CONT_up]				
CO21	POLY enclosure of CONT (on upper plate)		min	0.47
CO22	1METAL enclosure of CONT (on upper plate)		min	0.25
BAD_CO1	CONT must be sandwiched between AA/POLY/CRP and 1METAL.			
BAD_CO2	(gate) POLY CONT on AA is prohibited			
BAD_CO3	LONG CONT on POLY or CRP is prohibited			
BAD_CO4	butting contact is prohibited			

2.11 CONT ~ continued ~



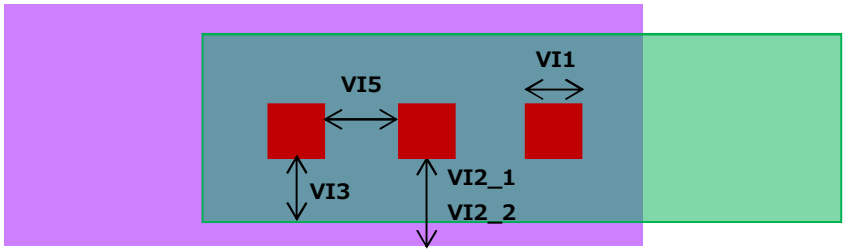
2.12 1METAL

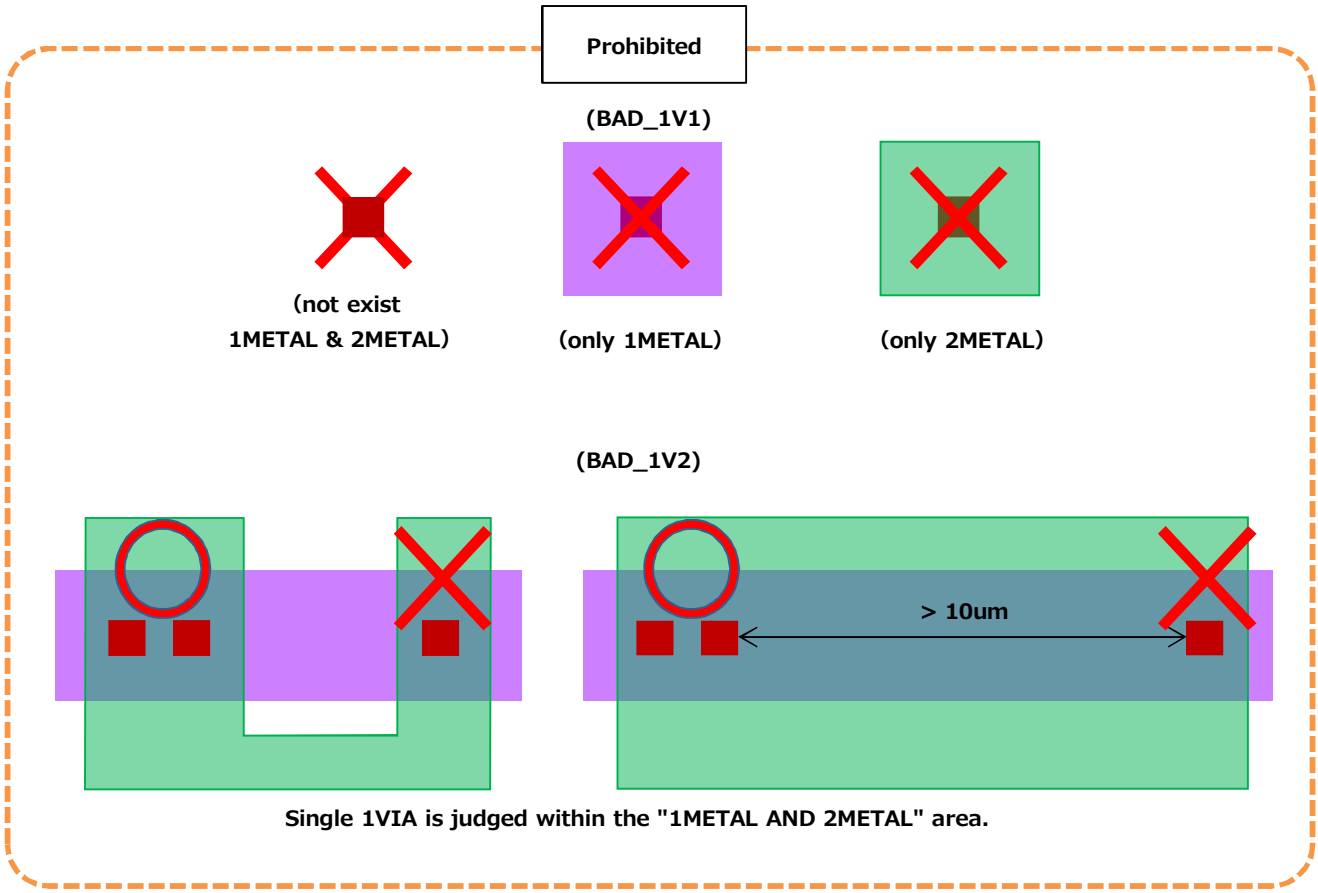
Rule No.	Description	class	Layout Rule (um)
FM1	1METAL width	min	0.40
FM2_1	1METAL spacing	min	0.40
FM2_3	1METAL spacing to wide_1METAL either/both 1METAL width>5um	min	0.50
Metal Slit Rule: referred to 2.18 Metal Slit Rule			
A wide 1METAL definition is reffered to 2.17 Wide Metal Definition			



2.13 1VIA

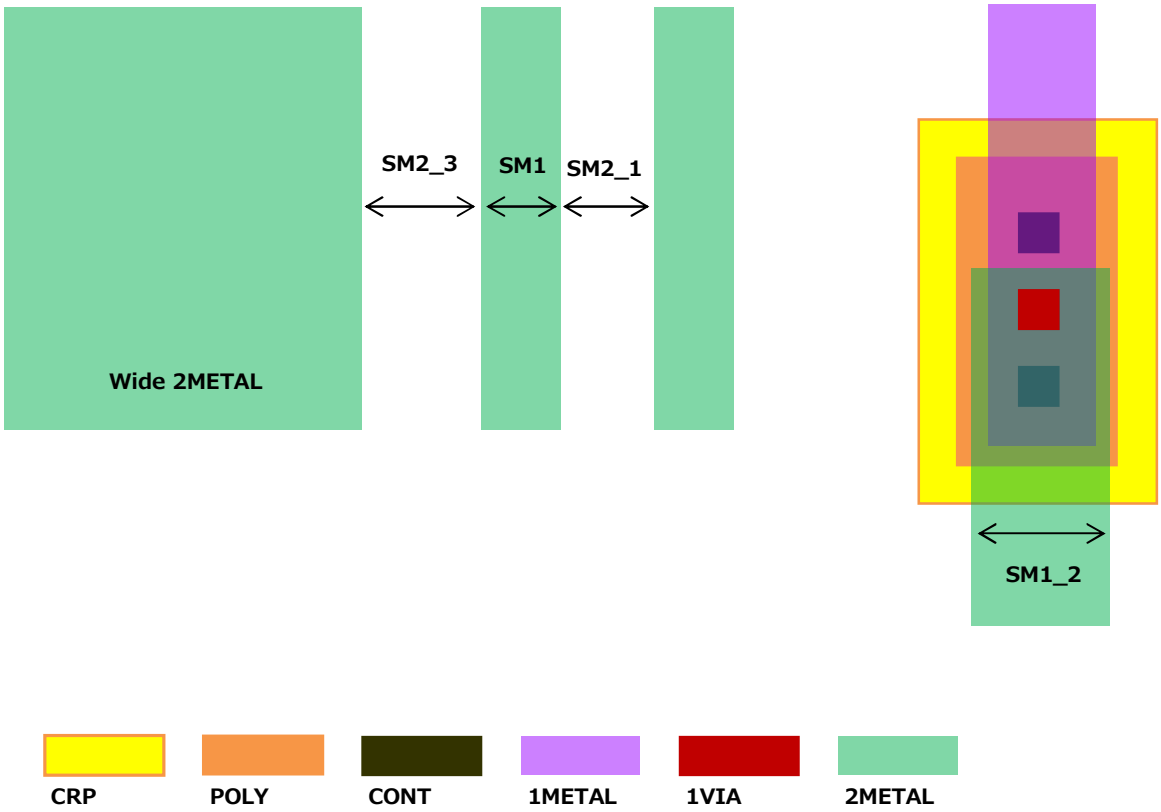
Rule No.	Description		class	Layout Rule (um)
VI1	1VIA size		fix	0.46x0.46
VI2_1	1METAL enclosure of 1VIA		min	0.20
VI2_2		on Wide 1METAL>5um	min	0.20
		on Wide 1METAL>10um	min	0.22
VI3	2METAL enclosure of 1VIA		min	0.15
VI5	1VIA spacing		min	0.45
VI6	1VIA density in chip area (refer to 2.23 chip area)		max	10%
BAD_1V1	1VIA must be sandwiched between 1METAL and 2METAL.			
BAD_1V2	Single 1VIA is prohibited. (1VIA spacing to the nearest 1VIA must be within 10 um)			
A wide 1METAL definition is reffered to 2.17 Wide Metal Definition				





2.14 2METAL

Rule No.	Description	class	Layout Rule (um)
SM1_1	2METAL width	min	0.50
SM1_2	on CPIP area (*)	min	0.65
SM2_1	2METAL spacing	min	0.45
SM2_3	2METAL spacing to wide_2METAL either/both 2METAL width>5um	min	0.55
Metal Slit Rule: referred to 2.18 Metal Slit Rule			
A wide 2METAL definition is reffered to 2.17 Wide Metal Definition			



SM1_2 Rule supplementation

The target range of SM 1_2 is obtained by the following (1) to (4).

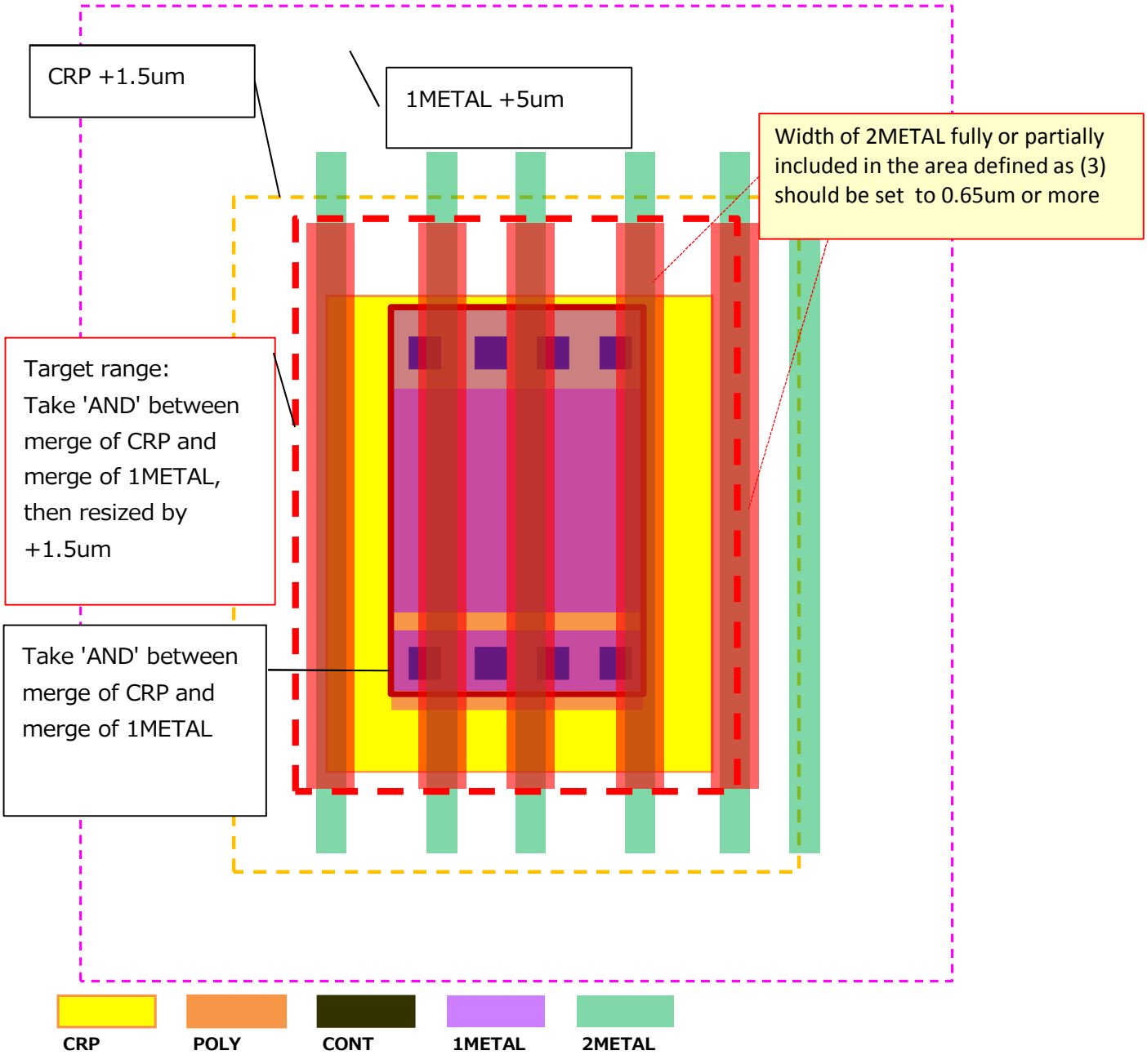
※On CPIP area

(1) Resize CRP by + 1.5μm and merge adjacent CRP into single one.
Then, resize by -1.5μm.

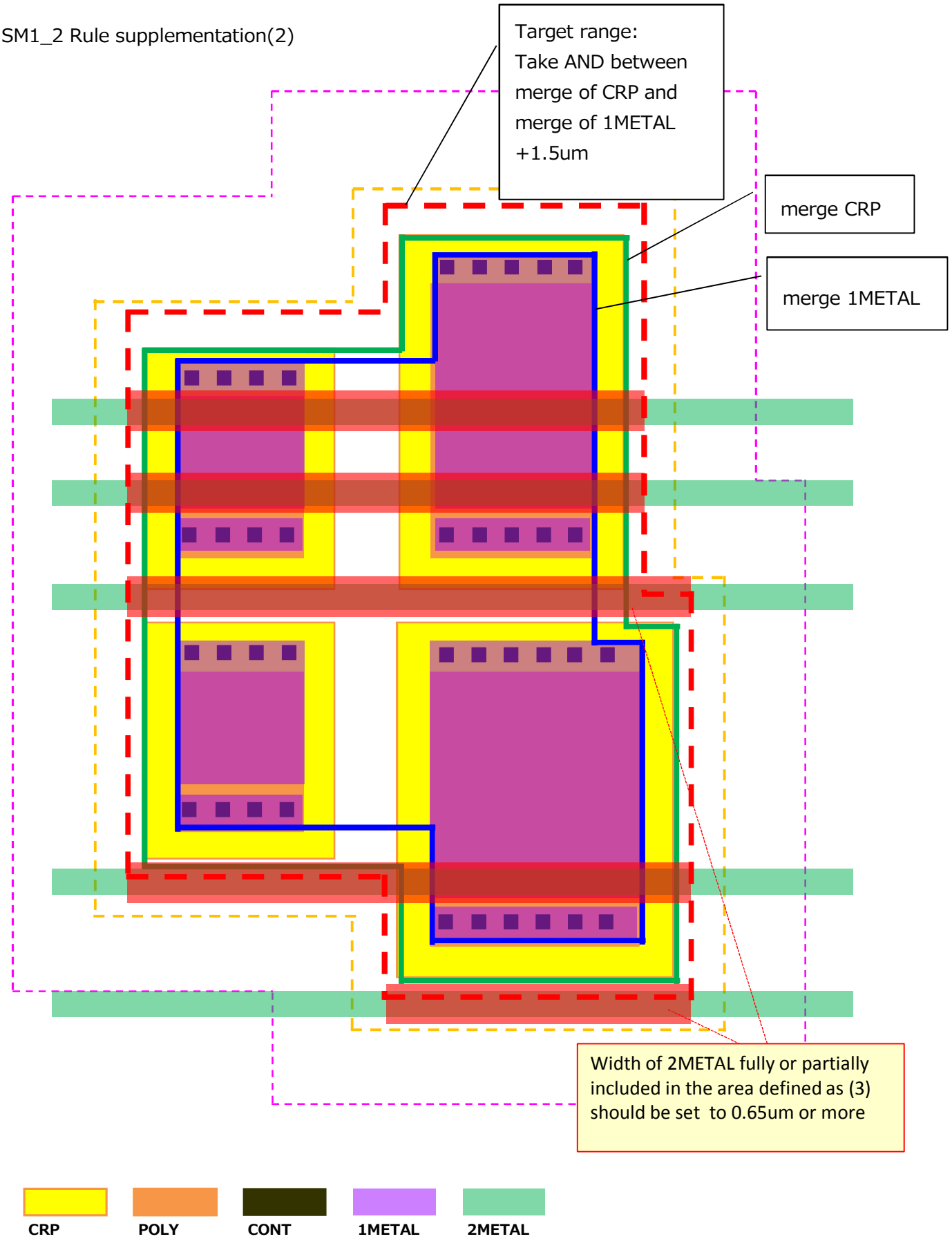
(2) Resize 1METAL on CRP by + 5.0μm and merge adjacent
1METAL into single one. Then, resize by -5.0 um.

(3) Take 'AND' between (1)CRP and (2)1METAL, then make 'AND' resized by +1.5um.

(4) Width of 2METAL fully or partially included on the area defined as (3) should be set to 0.65μm or more.

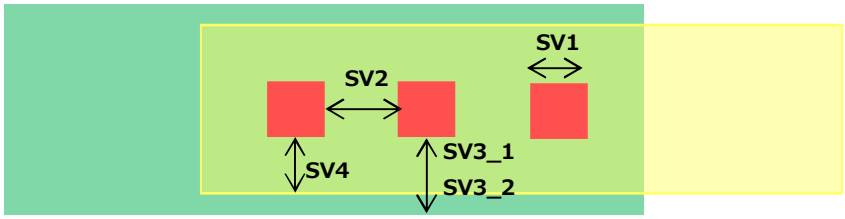


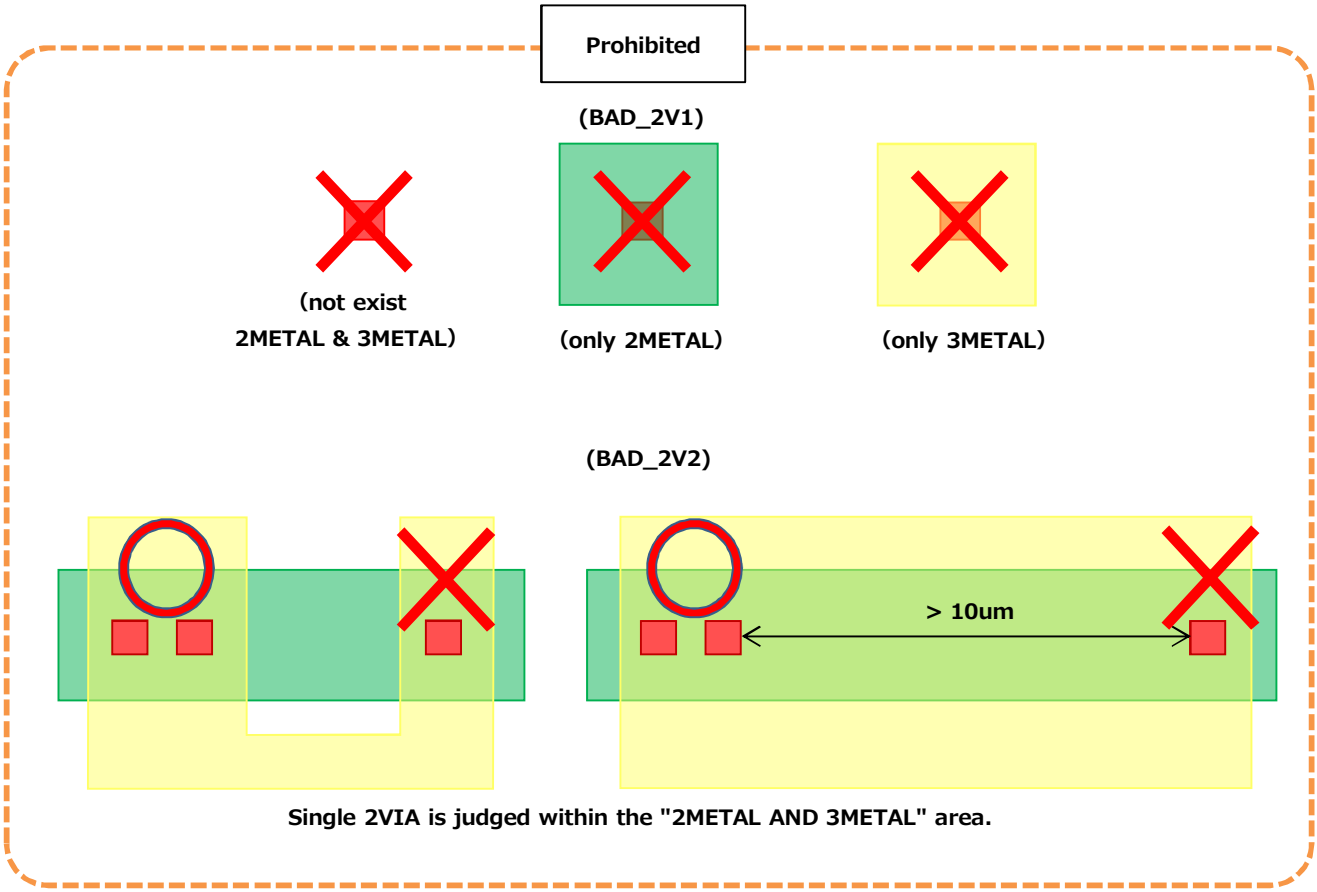
SM1_2 Rule supplementation(2)



2.15 2VIA

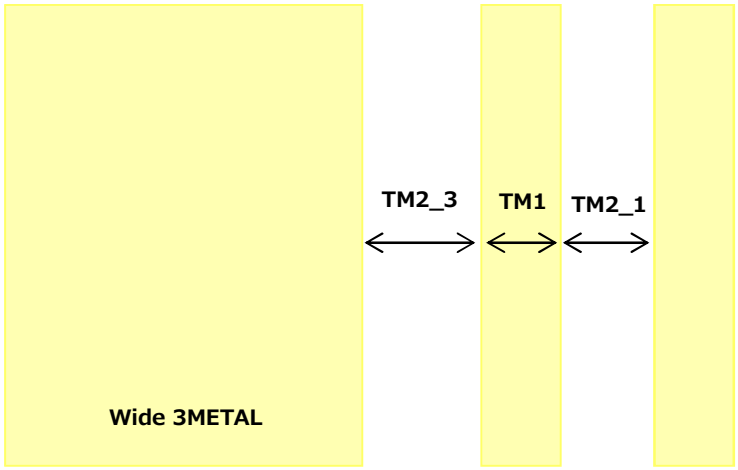
Rule No.	Description		class	Layout Rule (um)
SV1	2VIA size		fix	0.50x0.50
SV2	2VIA spacing		min	0.50
SV3_1	2METAL enclosure of 2VIA		min	0.20
SV3_2		on Wide 2METAL>5um	min	0.20
		on Wide 2METAL>10um	min	0.42
SV4	3METAL enclosure of 2VIA		min	0.16
SV5	2VIA density in chip area (refer to 2.23 chip area)		max	10%
BAD_2V1	2VIA must be sandwiched between 2METAL and 3METAL.			
BAD_2V2	Single 2VIA is prohibited. (2VIA spacing to the nearest 2VIA must be within 10 um)			
A wide 2METAL definition is reffered to 2.17 Wide Metal Definition				

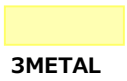




2.16 3METAL

Rule No.	Description	class	Layout Rule (um)
TM1	3METAL width	min	0.65
TM2_1	3METAL spacing	min	0.55
TM2_3	3METAL spacing to wide_3METAL either/both 10um<3METAL width	min	1.00
A wide 3METAL definition is reffered to 2.17 Wide Metal Definition			



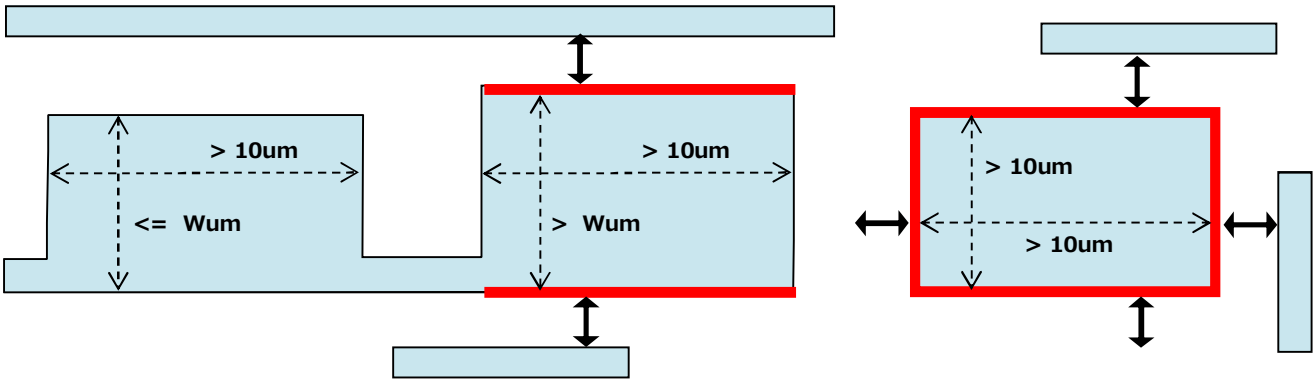


2.17 Wide Metal definition

Definition of wide metal in FM2_3, VI2_2, SM2_3, SV3_2, TM2_3.
W is 5μm and 10μm for 1METAL and 2METAL, 10μm for 3METAL.

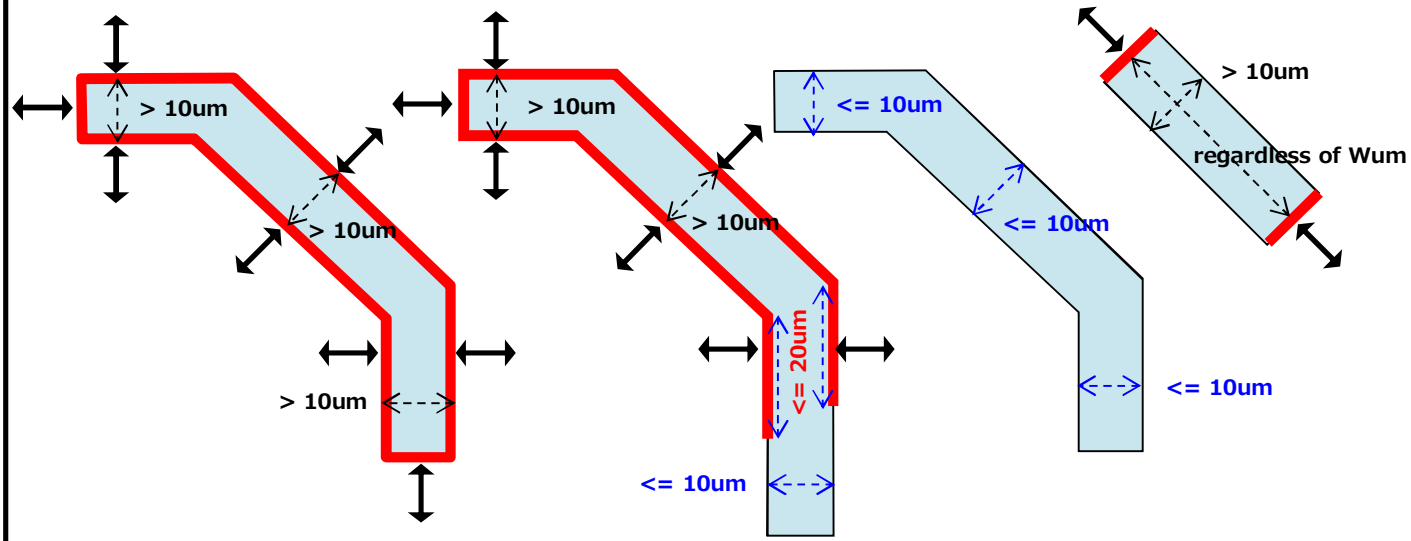
Metal lager than 10μm x Wμm is a wide metal. For the side where the distance between the opposing sides in the same metal is larger than Wμm (Please refer to the bold line in the figure below), wide metal space will be applied.

Arrow part is subject to DRC



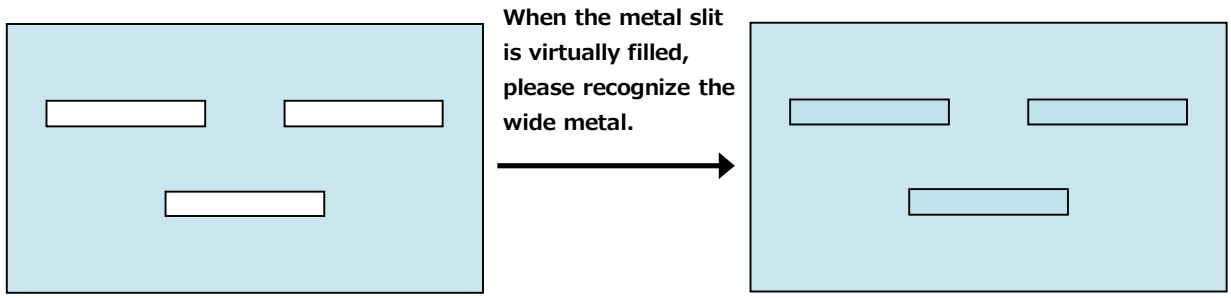
【Metal routing containing oblique line】

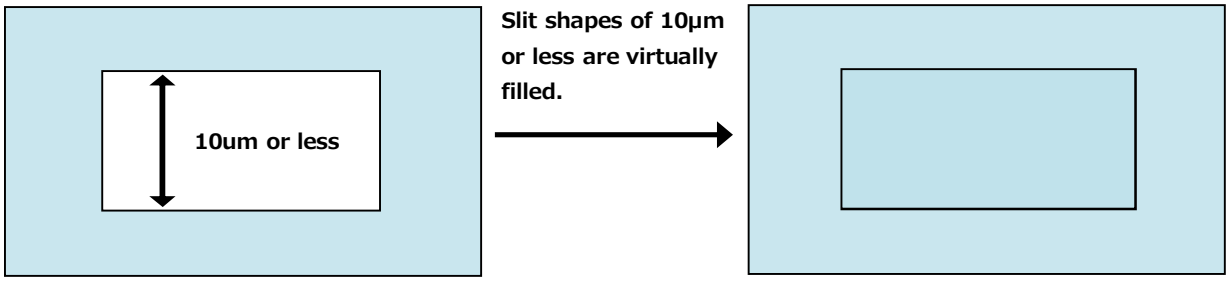
For the Metal routing containing *oblique line of larger than 10μm*,
wide metal space is applied to the oblique line and the line within 20um from the oblique line.
Only if *all metal line of less than 10μm including oblique line*, wide metal spaces will *NOT be applied.*
According to above constraint, oblique line is not recommended.

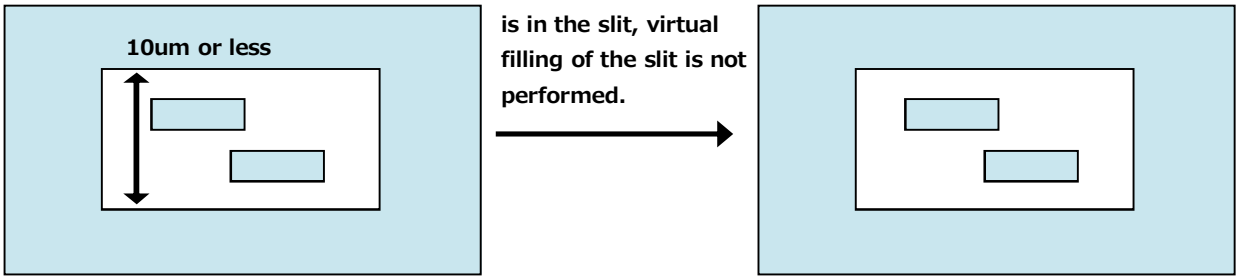


2.17 Wide Metal definition ~continued~

Caution 2.
Recognize the wide metal in a state where the shape similar to the metal slit and the metal slit of 10μm width or less is virtually filled.



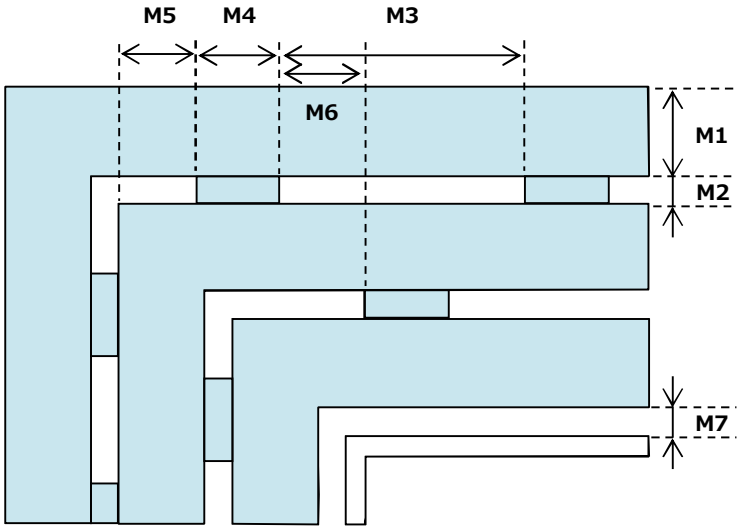


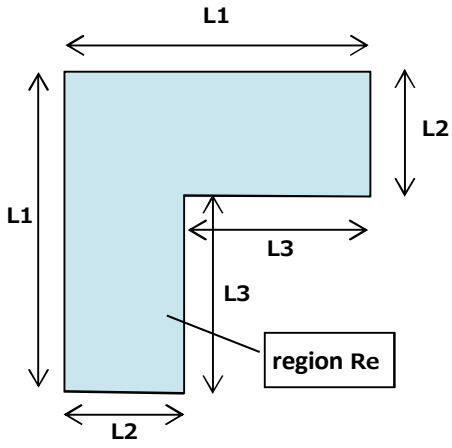


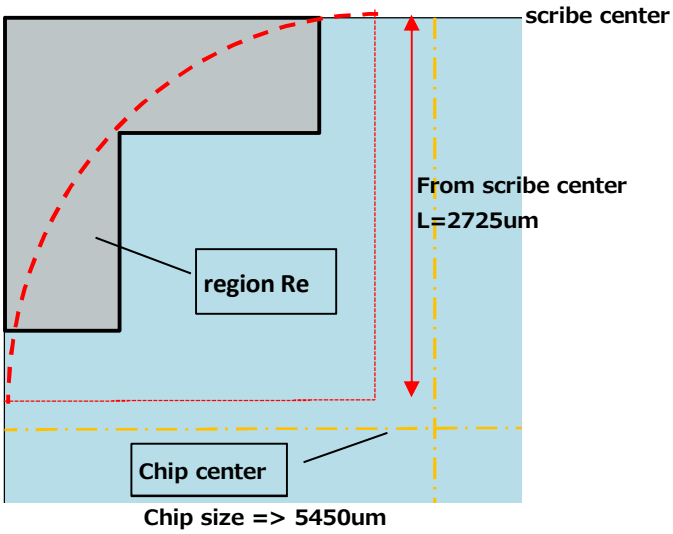
2.18 Metal Slit Rule

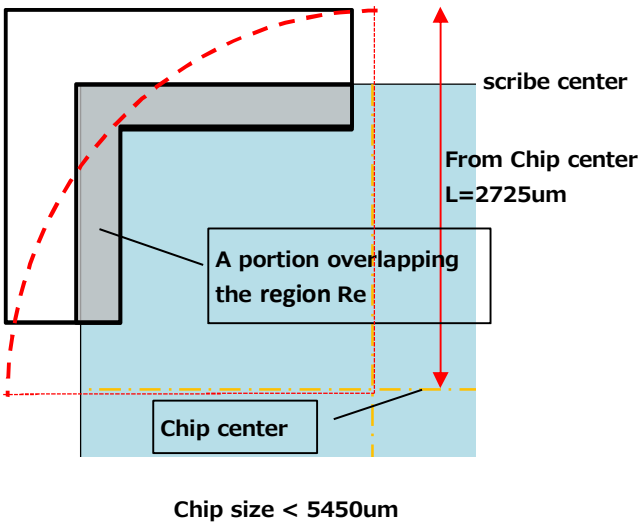
Rule No.	Description		class	Layout Rule (um)
When you use a Metal interconnect width which is wider than following L1~L3, please put slits in that Metal interconnect.				
L1	Apply the Metal Slit rule within the region Re in the figure below.		min	2220.00
L2			min	800.00
L3			min	1420.00
M1	Metal width		max	25.00
M2	Slits width		min	3.00
M3	Slits length		min	50.00
			max	200.00
M5		Metal interconnect is bent	min	50.00
M4	Slits space	on the same line	max	25.00
M6		on the different line	min	12.50
M7	space a METAL with slit to adjacent METAL		min	3.00

Appendix A : Metal Slit Rule

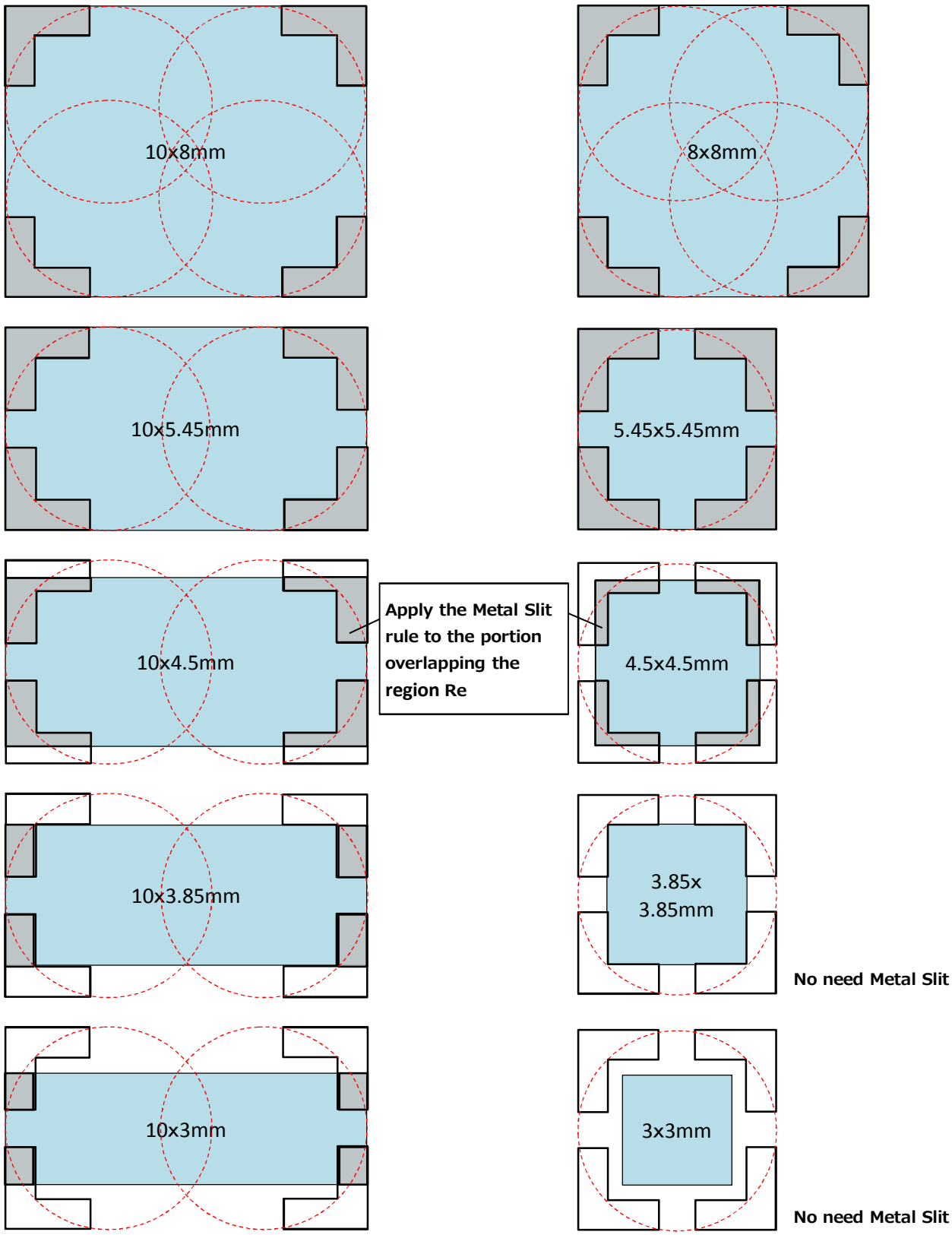








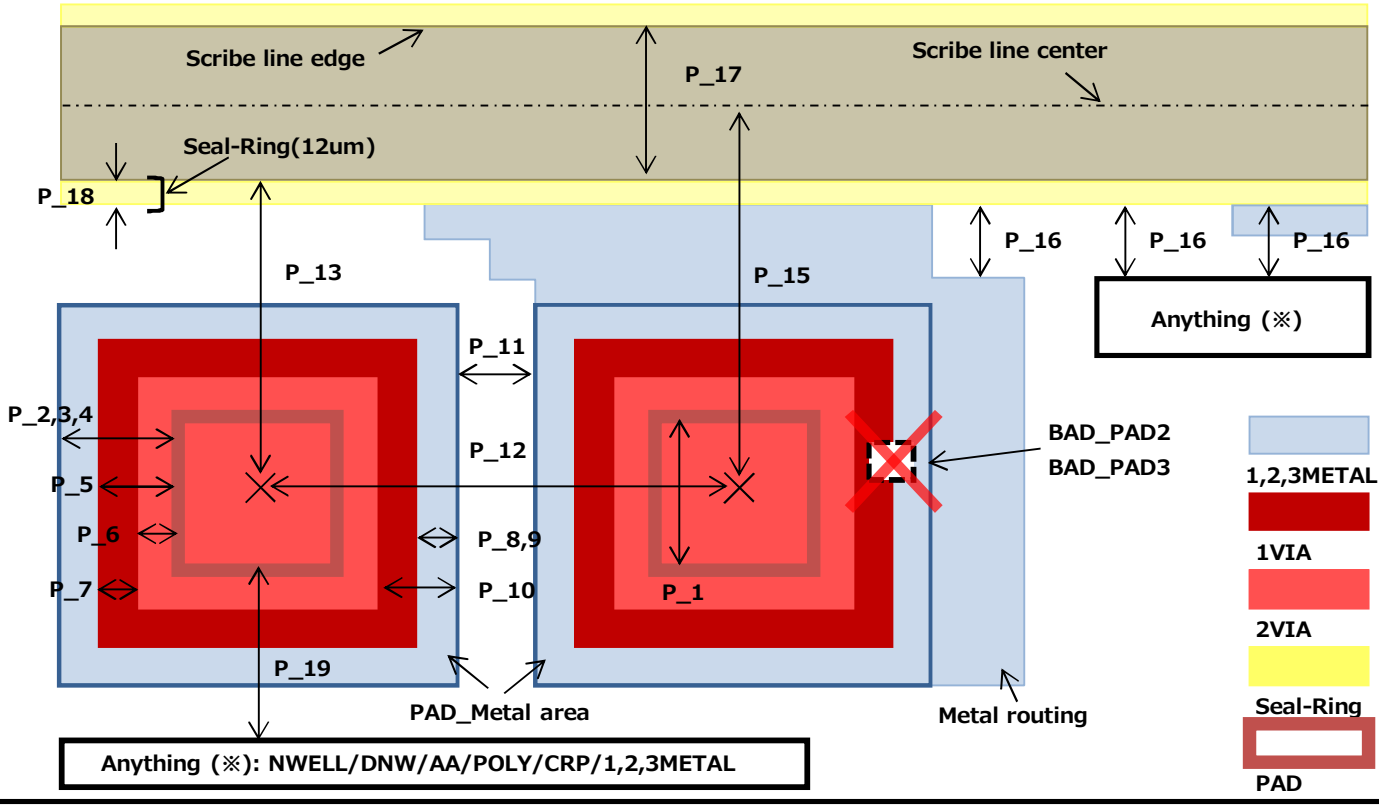
2.18 Metal Slit Rule ~ continued ~



2.19 PAD

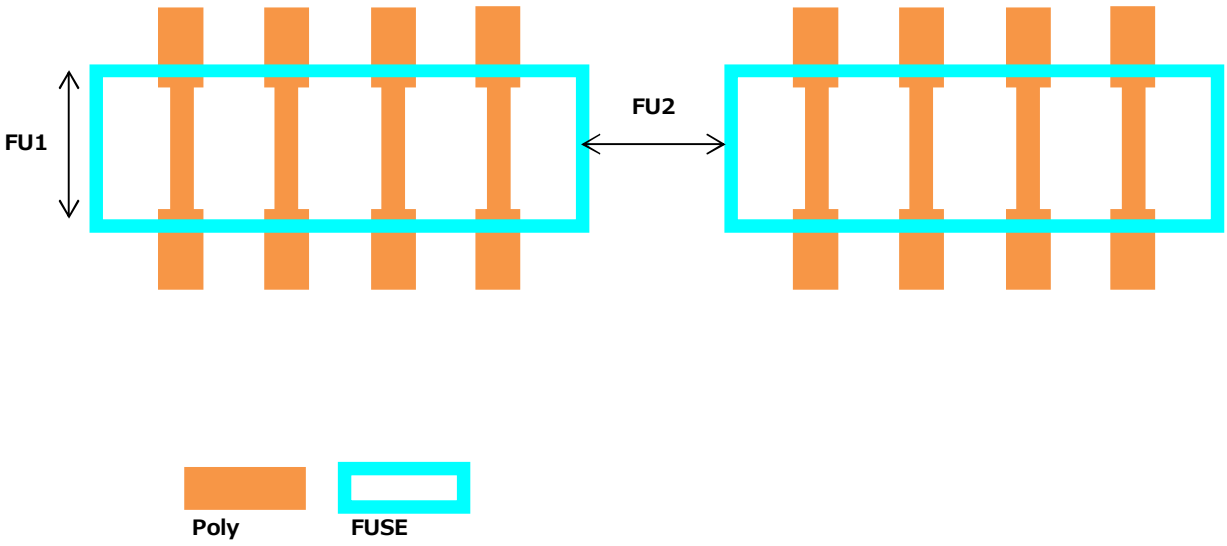
***After confirm the assembly or manufacturer's request, please decide the numerical value.**

Rule No.	Description	class	Layout Rule (um)	
P_1	PAD opening size	min	56.00	*
P_2	1METAL enclosure of PAD	min	4.50	
P_3	2METAL enclosure of PAD	min	4.50	
P_4	3METAL enclosure of PAD	min	5.00	
P_5	1VIA enclosure of PAD	min	3.50	
P_6	2VIA enclosure of PAD	min	1.50	
P_7	1VIA enclosure of 2VIA	min	2.00	
P_8	1METAL enclosure of 1VIA	min	1.00	
P_9	2METAL enclosure of 1VIA	min	1.00	
P_10	3METAL enclosure of 2VIA	min	3.50	
P_11	Pad metal spacing	min	4.00	
P_12	PAD pitch	min	70.00	*
P_13	PAD_center spacing to scribe_line_edge	min	65.00	*
P_15	PAD_center spacing to scribe center	max	200.00	*
P_16	Seal-Ring edge spacing to Anything(※)	min	20.00	*
P_17	Scribe line width	min	60.00	*
P_18	Seal-Ring width *refer to 2.22(Seal-Ring structure)	fix	12.00	
P_19	PAD spacing to Anything(※)	min	14.00	*
P_20	PAD density in chip area (refer to 2.23 chip area)	max	30%	
BAD_PAD1	1Metal/2Metal/3Metal must exists under PAD			
BAD_PAD2	No plural data of 1METAL,2METAL,3METAL,1VIA,2VIA,PAD must exist in the PAD_Metal area except for Metal routing.			
BAD_PAD3	No data of AA,POLY,CRP,CONT must exist in the PAD_Metal area except for Metal routing.			



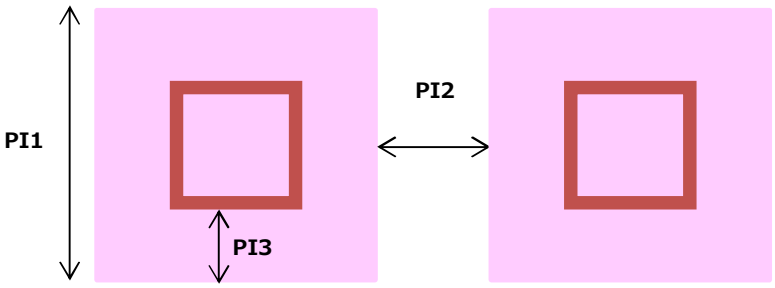
2.20 FUSE

Rule No.	Description	class	Layout Rule (um)
FU1	FUSE width	min	8.00
FU2	FUSE spacing	min	8.00



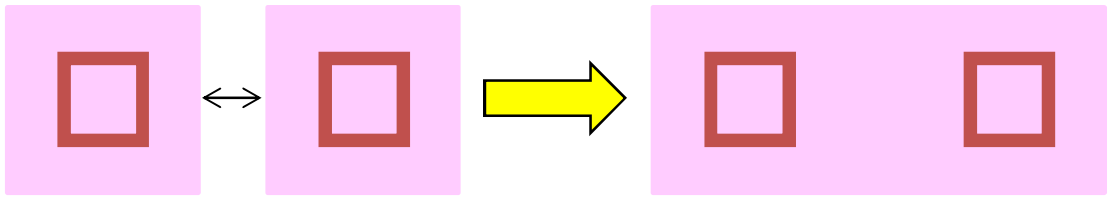
2.21 PI

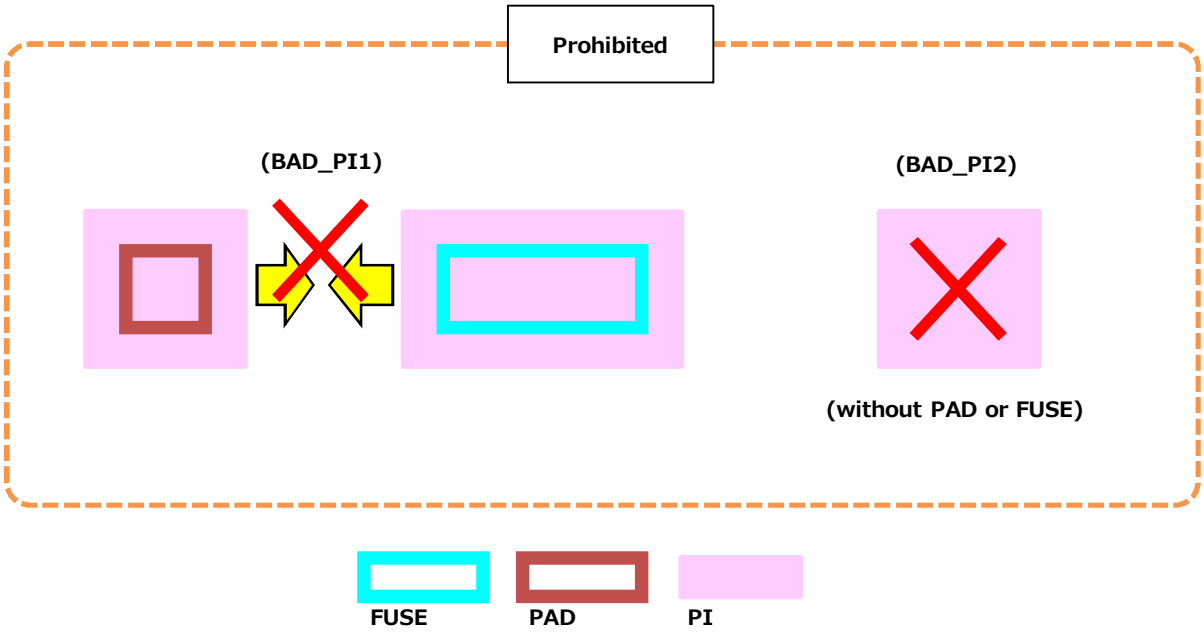
Rule No.	Description	class	Layout Rule (um)
PI1	PI width	min	8.00
PI2	PI spacing	min	20.00 or Merge
PI3	PI enclosure of PAD (except merged area)	fix	10.00
BAD_PI1	Merge between PI(Pad) and PI(Fuse) is prohibited		
BAD_PI2	PI without Pad or Fuse is prohibit		



PI2 < 20um(less than 20um)

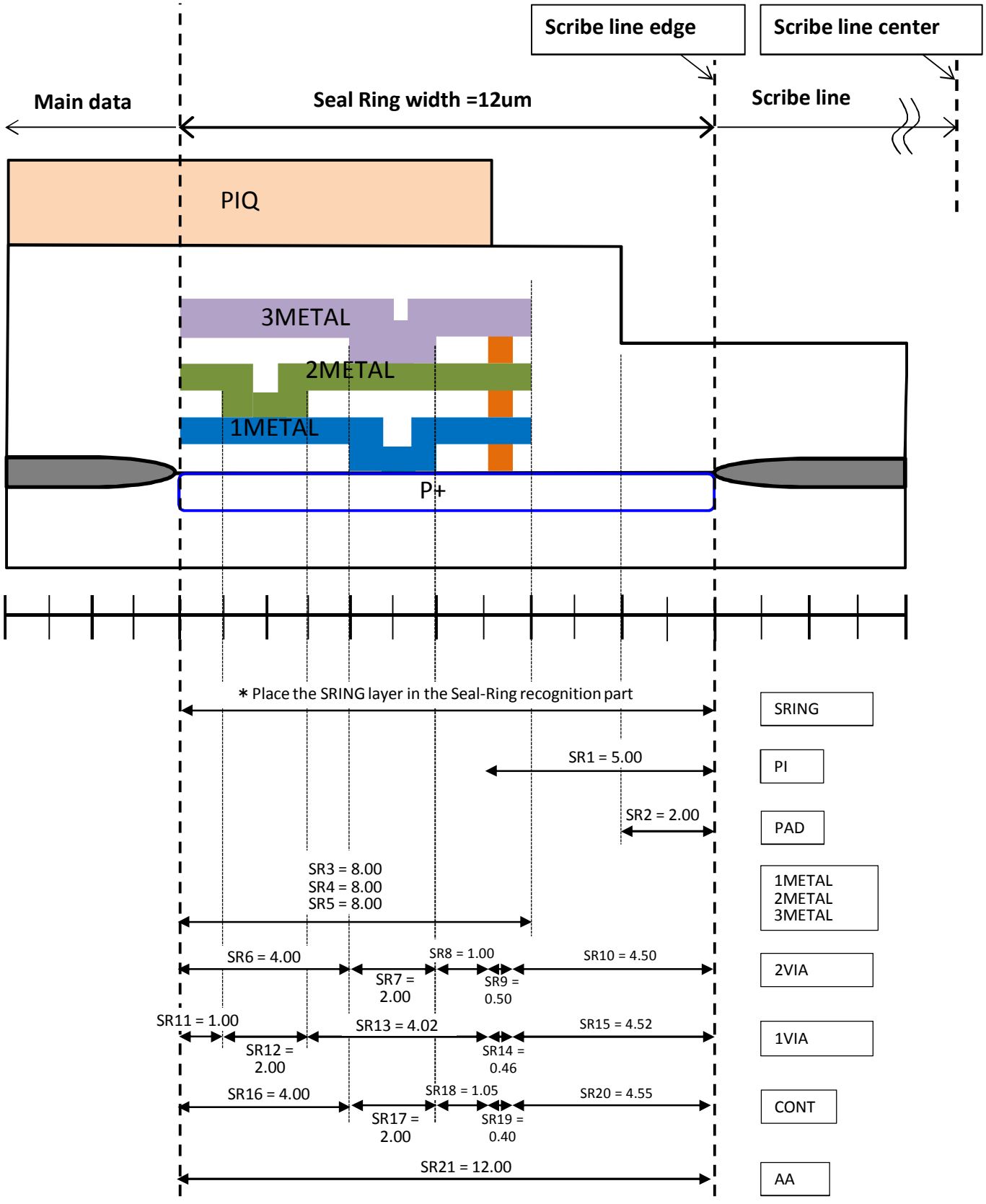
must merge PIs if PI2 < 20um





2.22 Seal-Ring Structure

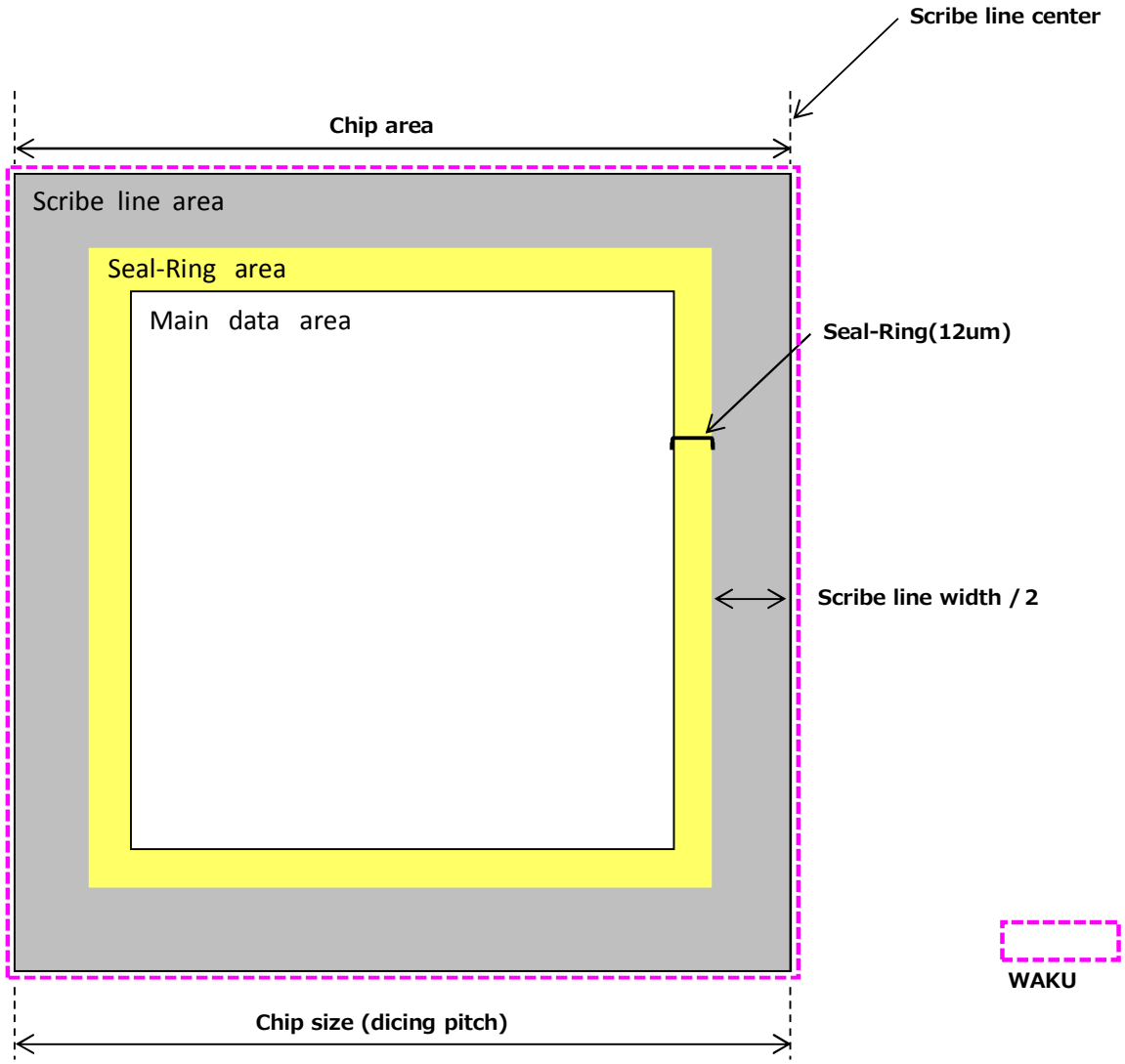
＊Seal-Ring should be hand-drawn.(Seal-Ring is not supported by T-Cell.)



2.23 Chip area

1. Customer's data area should be coincident with chip size including scribe line area.

2. Customer must not place any data in the scribe line area.



＊Place the WAKU layer in the Chip area recognition part (Flush with the outer edge of the Scribe line center) .

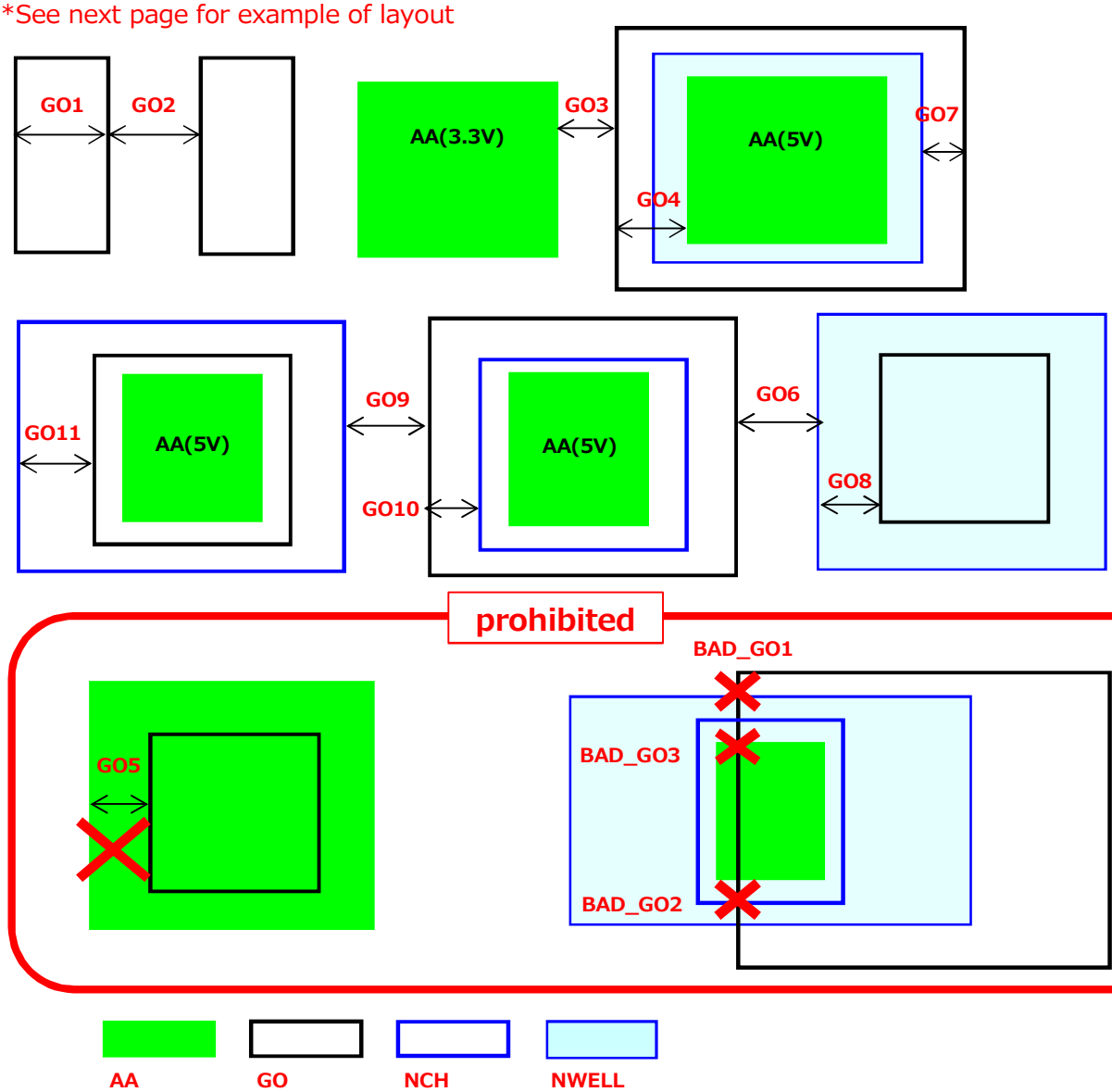
Chip size (dicing pitch)
=Main data size (um) + Seal-Ring width(12um)*2 + Scribe line width (um)

2.24 GO

For 3.3V or 3.3V/5V mixed, GO must cover specified area.

Rule No.	Description	class	Layout Rule (um)
GO1	GO width	min	1.30
GO2	GO space	min	1.30
GO3	GO spacing to AA(3.3V)	min	0.60
GO4	GO enclosure of AA(5V)	min	0.60
GO5	AA(5V) must be enclosed by GO (AA enclosure of GO is prohibited.)		
GO6	GO spacing to NWELL	min	0.00
GO7	GO enclosure of NWELL	min	0.00
GO8	NWELL enclosure of GO	min	0.00
GO9	GO spacing to NCH	min	0.00
GO10	GO enclosure of NCH	min	0.00
GO11	NCH enclosure of GO	min	0.80
BAD_GO1	NWELL edge crossing GO edge is prohibited.		
BAD_GO2	NCH edge crossing GO edge is prohibited.		
BAD_GO3	AA edge crossing GO edge is prohibited.		

*See next page for example of layout

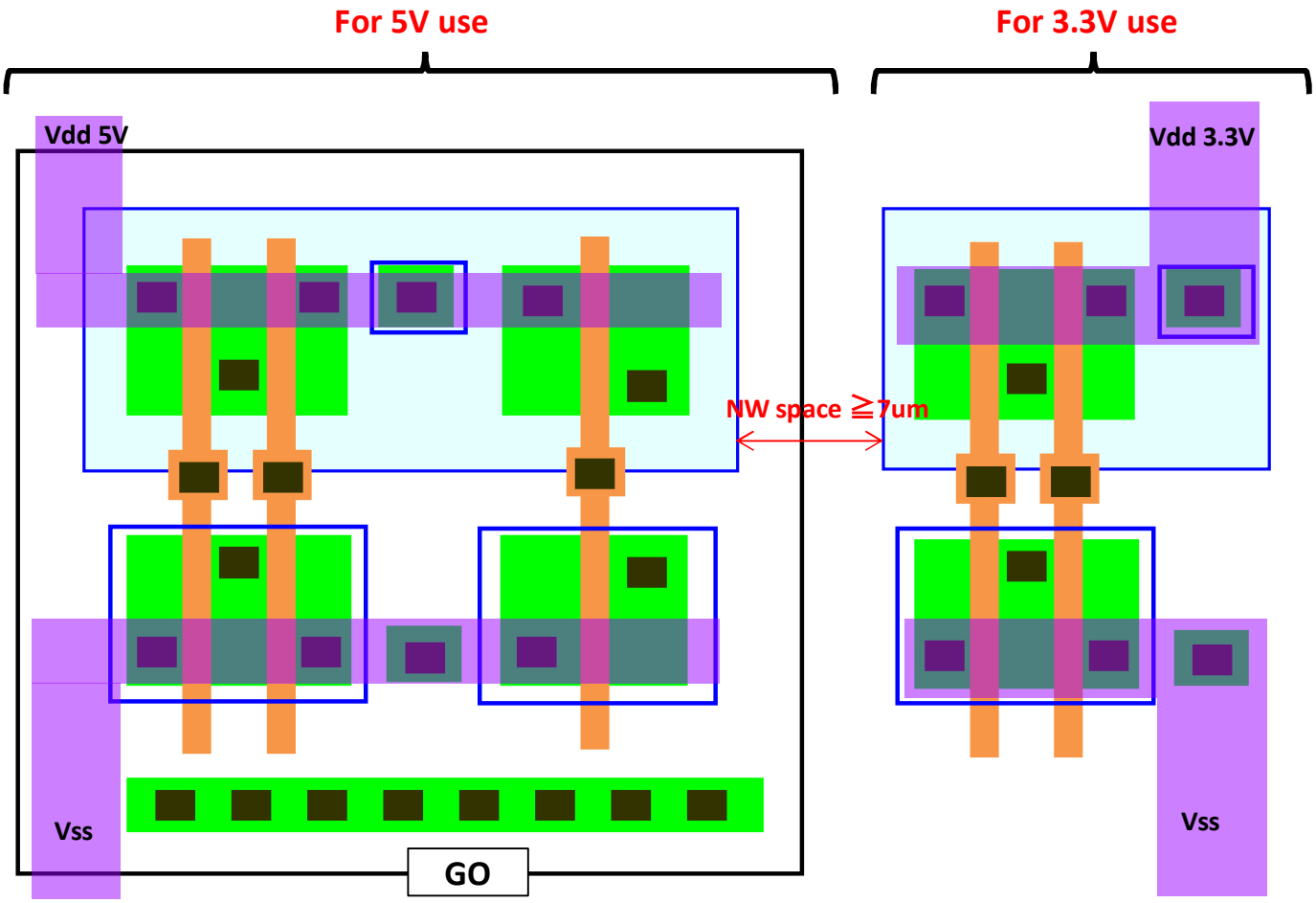


2.24 GO ~continued~

GO example of layout

・It is recommended GO encloses whole 5V area or cell.

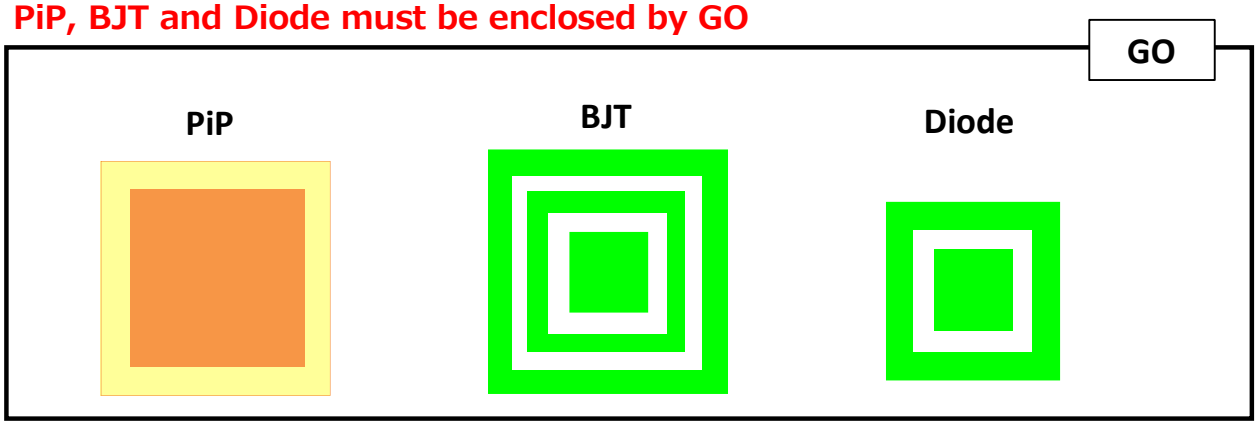
・In case 5V area is close to 3.3V area, each NWELL spacing must be more than 7.0um.



・Even though GO is the layer for processing dual gate oxide and it may be placed enclosing 5V gate and related AA without AA resistor or Tap, it is strongly ***recommended GO encloses whole 5V parts(except metal interconnect) for design flexibility.***

Notice !

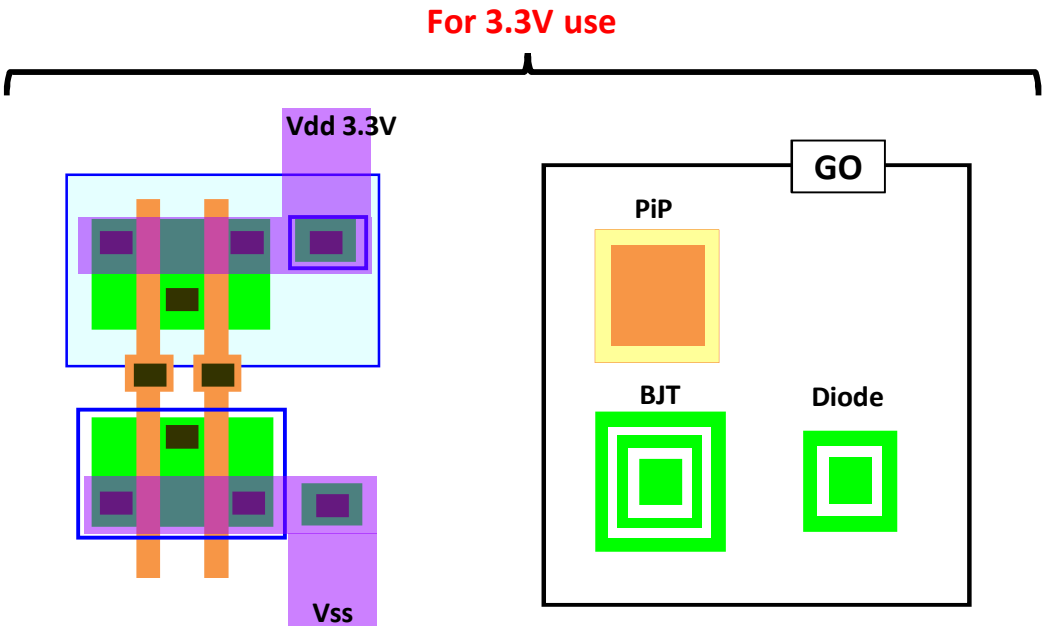
PiP, BJT and Diode must be enclosed by GO



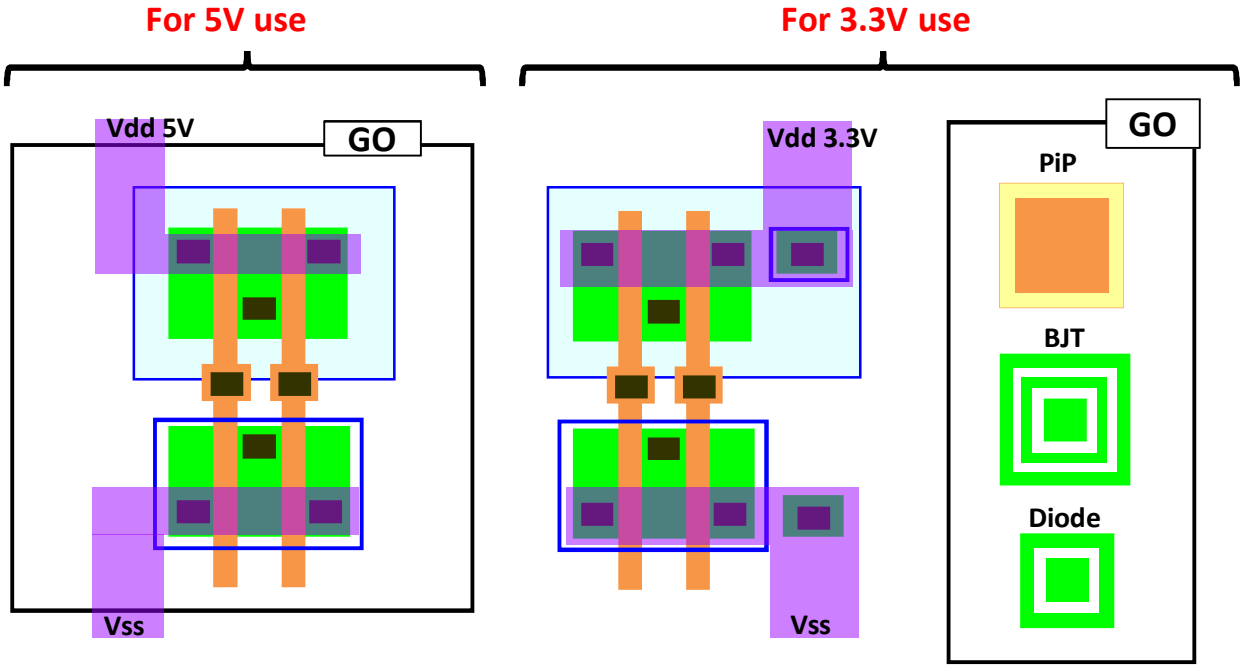
2.24 GO ~continued(2)~

For 3.3V or 3.3V/5V mixed, GO must cover specified area.

1. For 3.3V design, GO must cover PiP, BJT and Diode area.



2. For 3.3V/5V mixed design, GO must cover 5V area and PiP, BJT, Diode area.

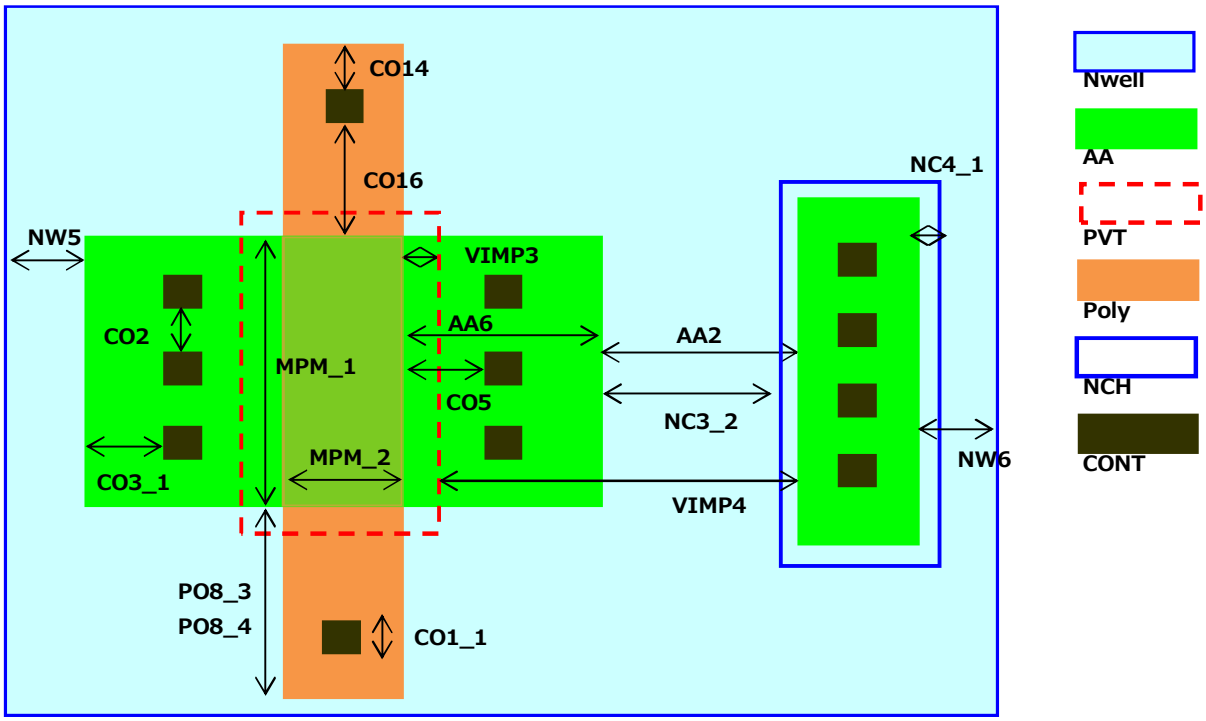


3. For 5V design, GO is not necessary.

3. Device Rules

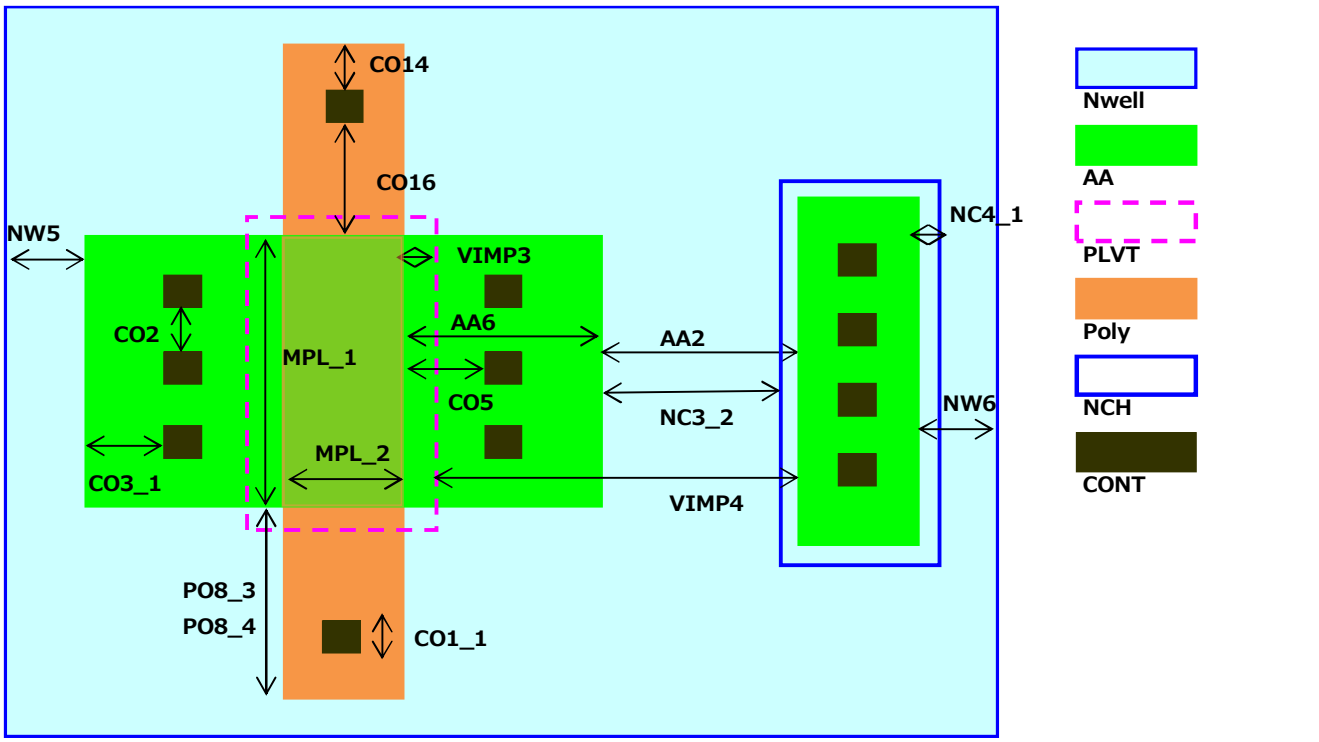
3.1 MPM ・・・ Pch Medium Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MPM_1a	Transistor Width		min	3.30
MPM_1b			max	100.00
MPM_2a	Transistor Length		min	0.70
MPM_2b			max	100.00
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



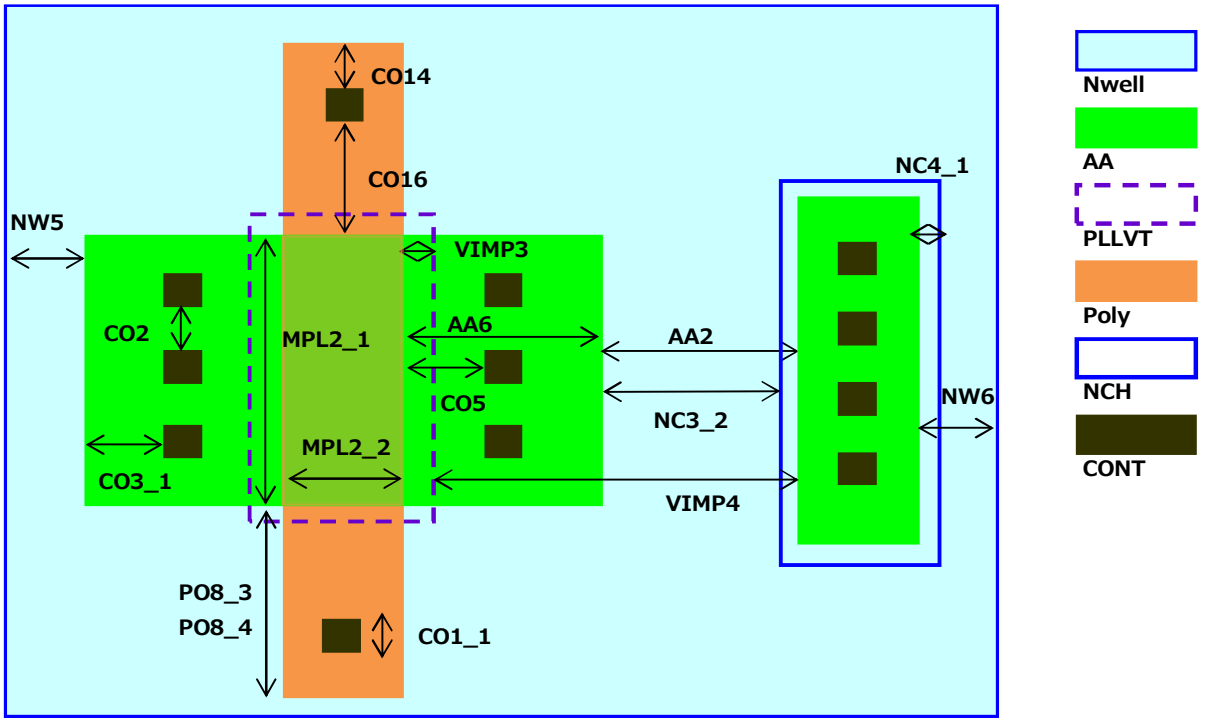
3.2 MPL ・・・ Pch Low Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MPL_1a	Transistor Width		min	3.30
MPL_1b			max	100.00
MPL_2a	Transistor Length		min	0.80
MPL_2b			max	100.00
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



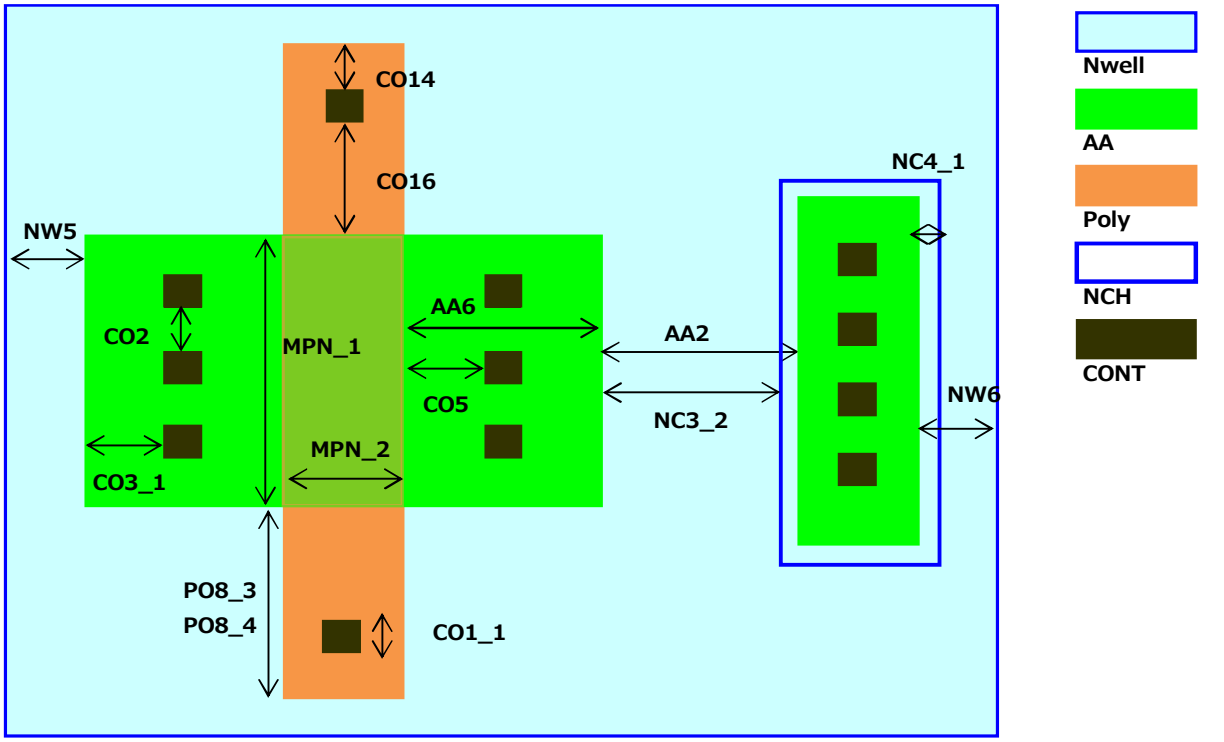
3.3 MPL2 ・・・ Pch Very Low Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MPL2_1a	Transistor Width		min	3.30
MPL2_1b			max	100.00
MPL2_2a	Transistor Length		min	1.00
MPL2_2b			max	100.00
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



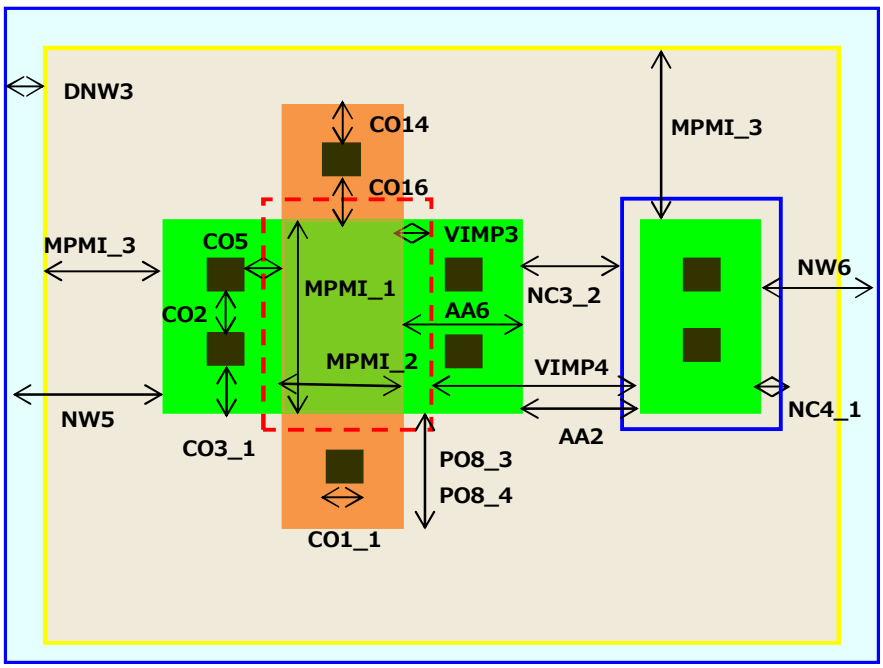
3.4 MPN ・・・ Pch Native Vt MOS Transistor（N+Polycide gate)

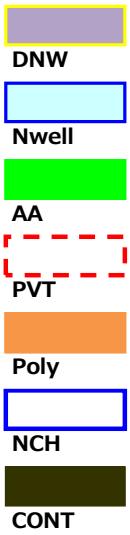
Rule No.	Description		class	Layout Rule (um)
MPN_1a	Transistor Width		min	3.30
MPN_1b			max	100.00
MPN_2a	Transistor Length		min	0.70
MPN_2b			max	100.00
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



3.5 MPMI ・・・ Isolated Type Pch Medium Vt MOS Transistor（N+Polycide gate）

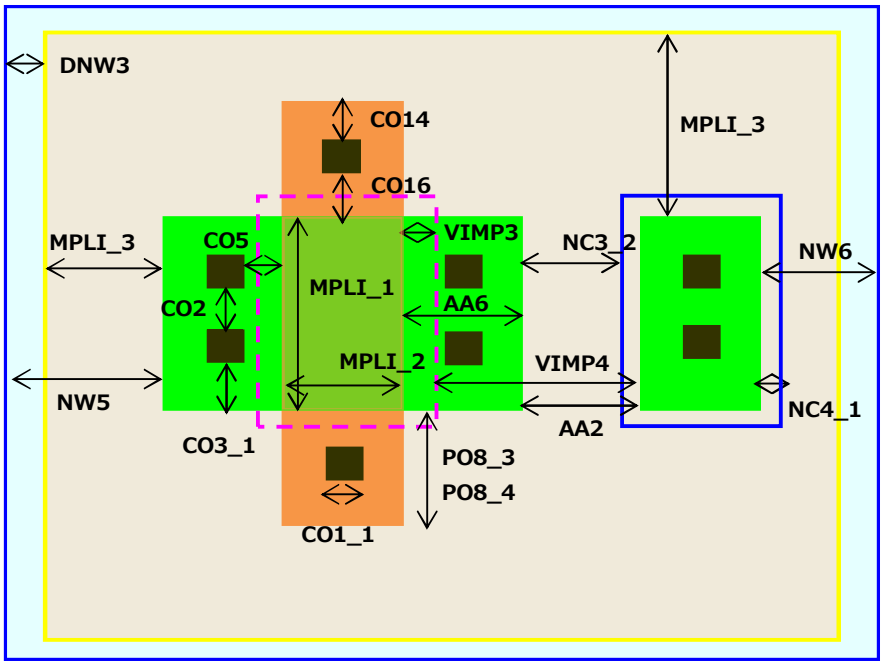
Rule No.	Description		class	Layout Rule (um)
MPMI_1a	Transistor Width		min	3.30
MPMI_1b			max	100.00
MPMI_2a	Transistor Length		min	0.70
MPMI_2b			max	100.00
MPMI_3	DNW enclosure of AA		min	0.35
DNW3	NWELL extension beyond DNW		min	1.50
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

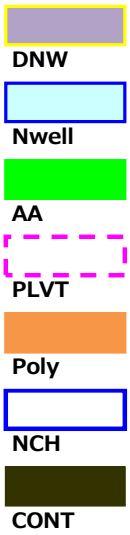




3.6 MPLI ・・・ Isolated Type Pch Low Vt MOS Transistor（N+Polycide gate）

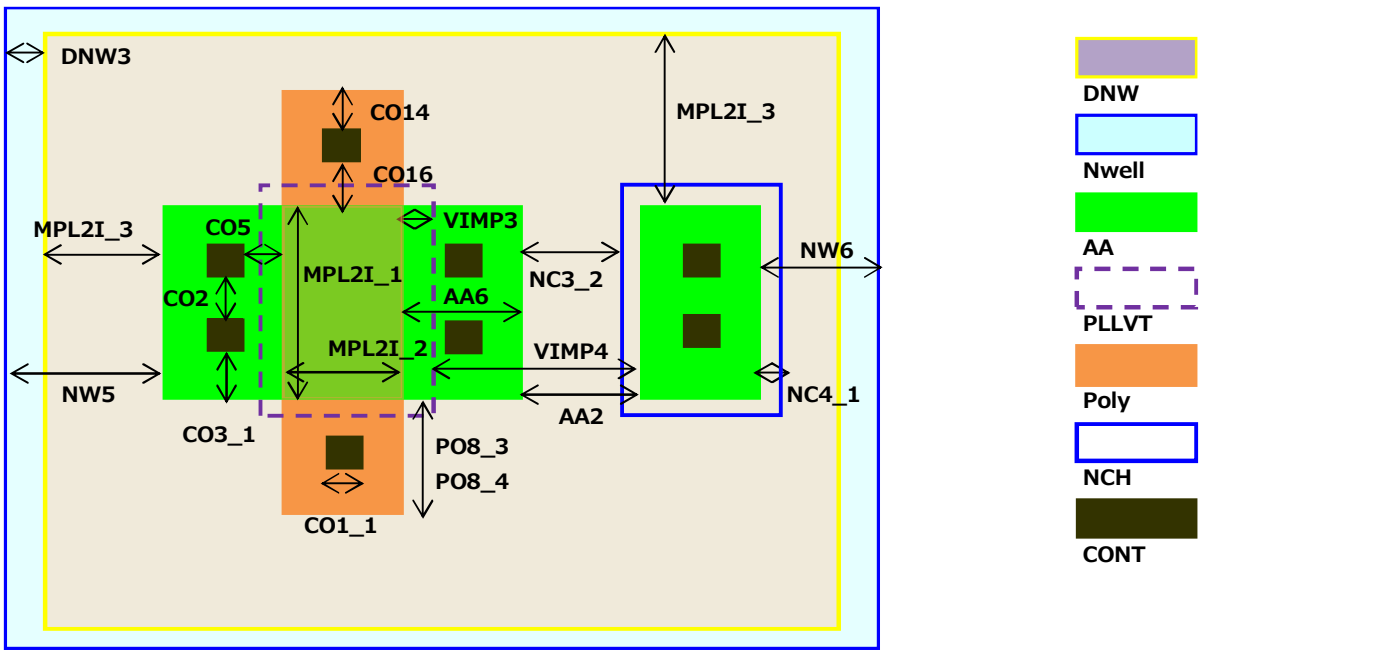
Rule No.	Description		class	Layout Rule (um)
MPLI_1a	Transistor Width		min	3.30
MPLI_1b			max	100.00
MPLI_2a	Transistor Length		min	0.80
MPLI_2b			max	100.00
MPLI_3	DNW enclosure of AA		min	0.35
DNW3	NWELL extension beyond DNW		min	1.50
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29





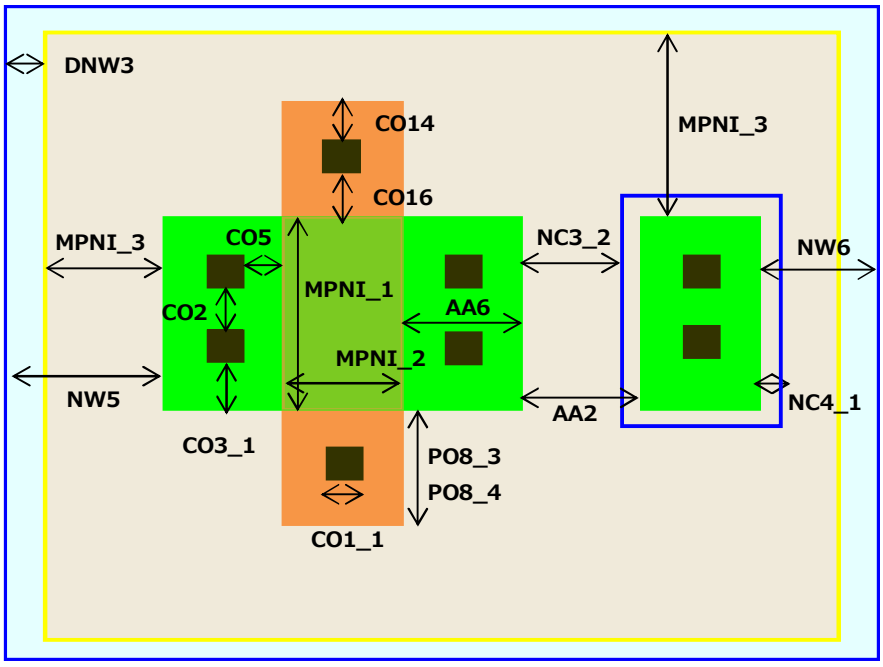
3.7 MPL2I ・・・ Isolated Type Pch Very Low Vt MOS Transistor（N+Polycide gate）

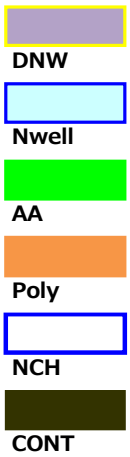
Rule No.	Description		class	Layout Rule (um)
MPL2I_1a	Transistor Width		min	3.30
MPL2I_1b			max	100.00
MPL2I_2a	Transistor Length		min	1.00
MPL2I_2b			max	100.00
MPL2I_3	DNW enclosure of AA		min	0.35
DNW3	NWELL extension beyond DNW		min	1.50
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



3.8 MPNI ・・・ Isolated Type Pch Native Vt MOS Transistor（N+Polycide gate)

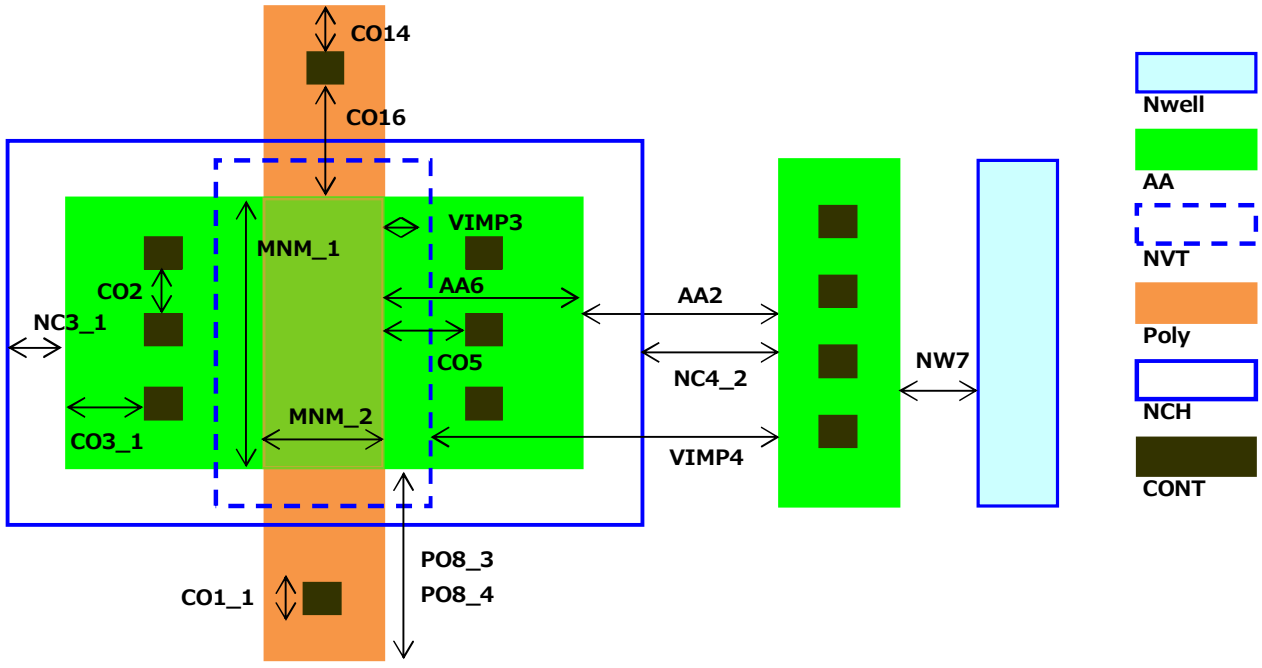
Rule No.	Description		class	Layout Rule (um)
MPNI_1a	Transistor Width		min	3.30
MPNI_1b			max	100.00
MPNI_2a	Transistor Length		min	0.70
MPNI_2b			max	100.00
MPNI_3	DNW enclosure of AA		min	0.35
DNW3	NWELL extension beyond DNW		min	1.50
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29





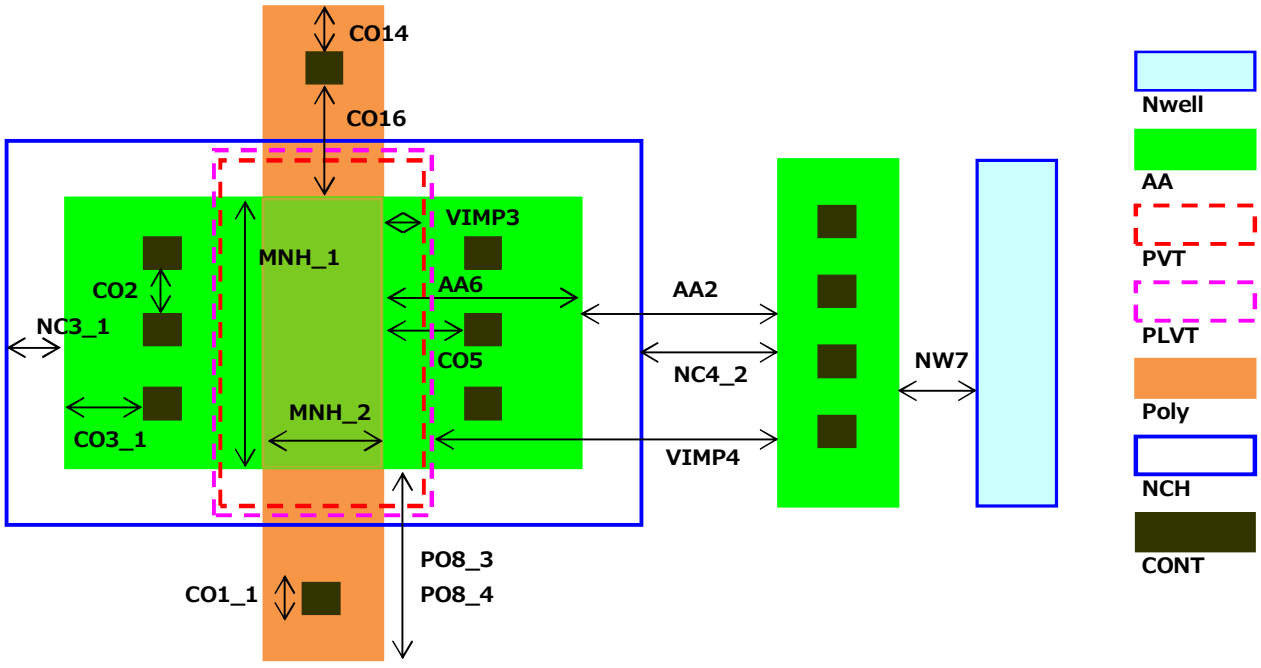
3.9 MNM ・・・ Nch Medium Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNM_1a	Transistor Width		min	3.30
MNM_1b			max	100.00
MNM_2a	Transistor Length		min	0.70
MNM_2b			max	100.00
NW7	NWELL spacing to AA(p+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



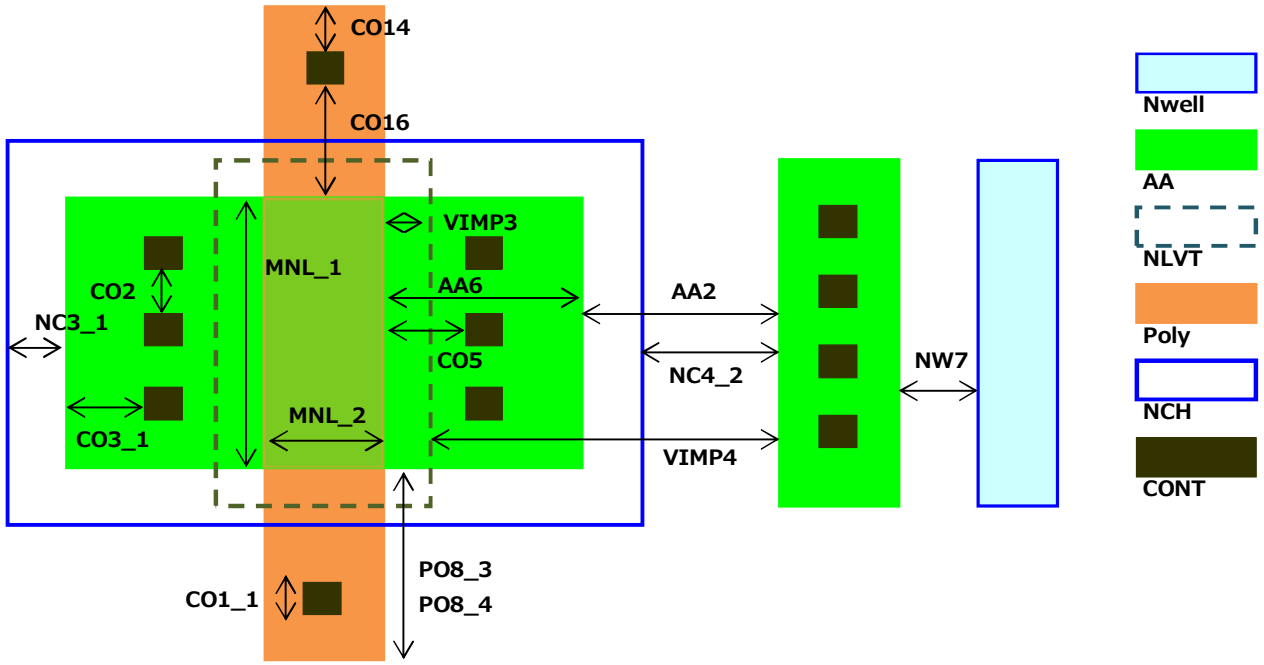
3.10 MNH ・・・ Nch High Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNH_1a	Transistor Width		min	3.30
MNH_1b			max	100.00
MNH_2a	Transistor Length		min	0.70
MNH_2b			max	100.00
NW7	NWELL spacing to AA(p+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



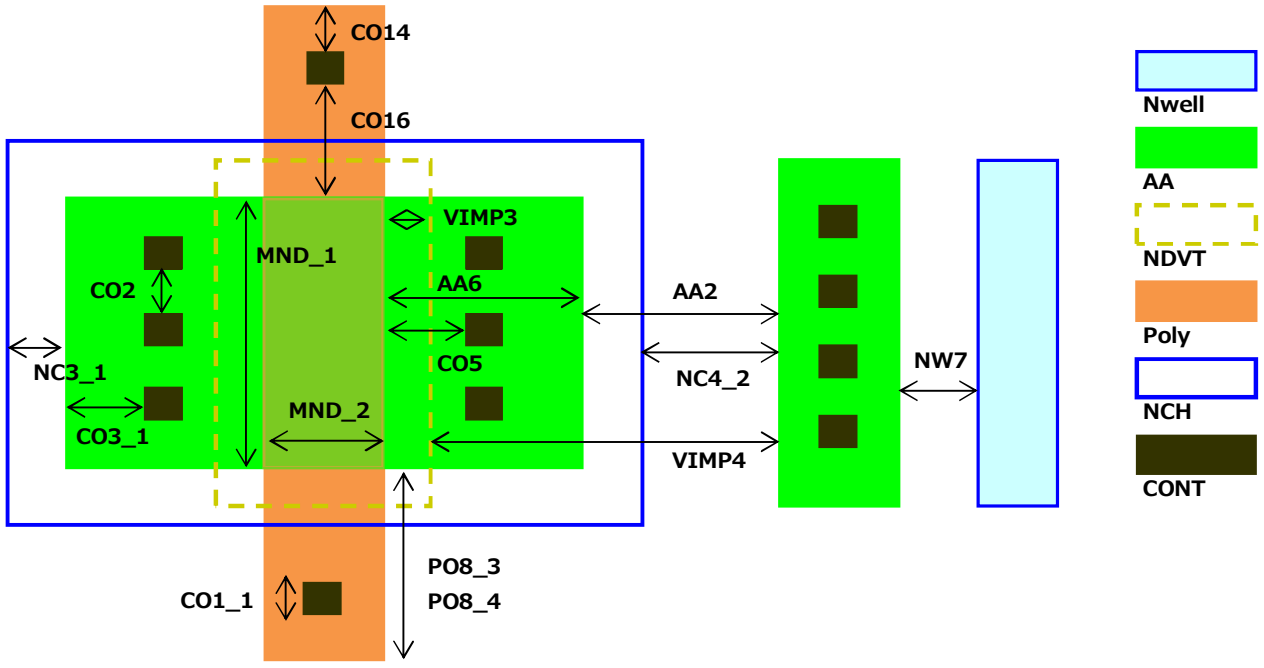
3.11 MNL ・・・ Nch Low Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNL_1a	Transistor Width		min	3.30
MNL_1b			max	100.00
MNL_2a	Transistor Length		min	0.80
MNL_2b			max	100.00
NW7	NWELL spacing to AA(p+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



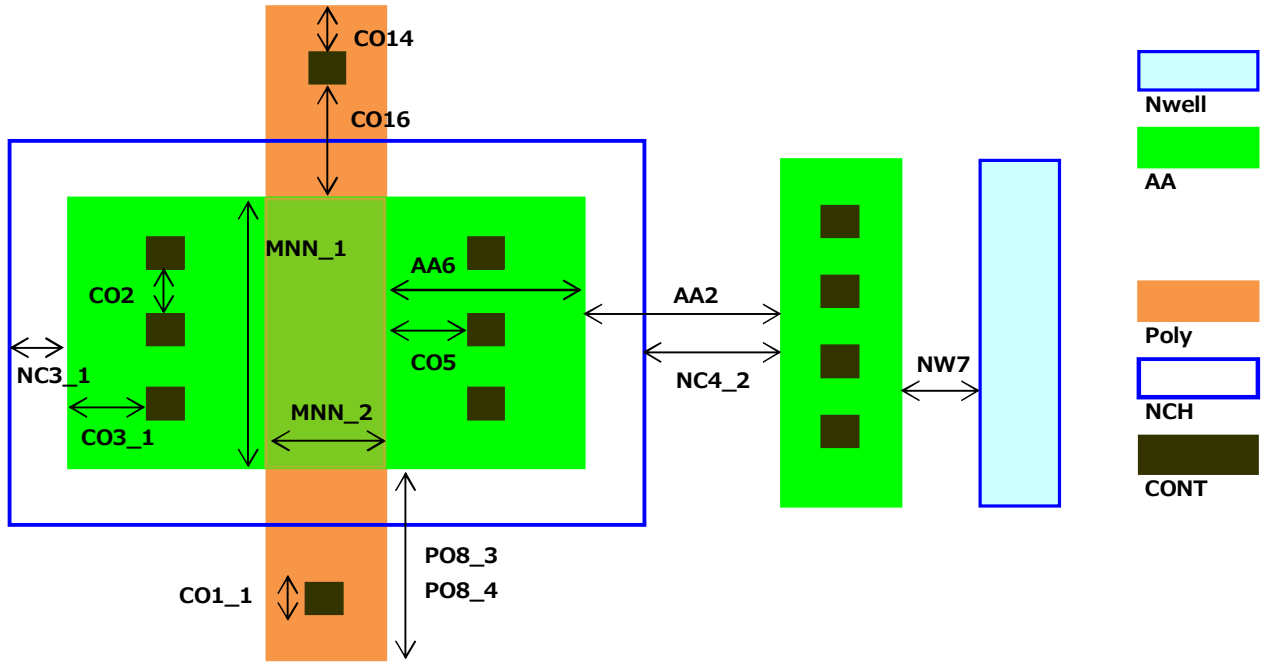
3.12 MND・・・ Nch Depletion Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MND_1a	Transistor Width		min	3.30
MND_1b			max	100.00
MND_2a	Transistor Length		min	2.00
MND_2b			max	100.00
NW7	NWELL spacing to AA(p+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



3.13 MNN・・・ Nch Native Vt MOS Transistor（N+Polycide gate）

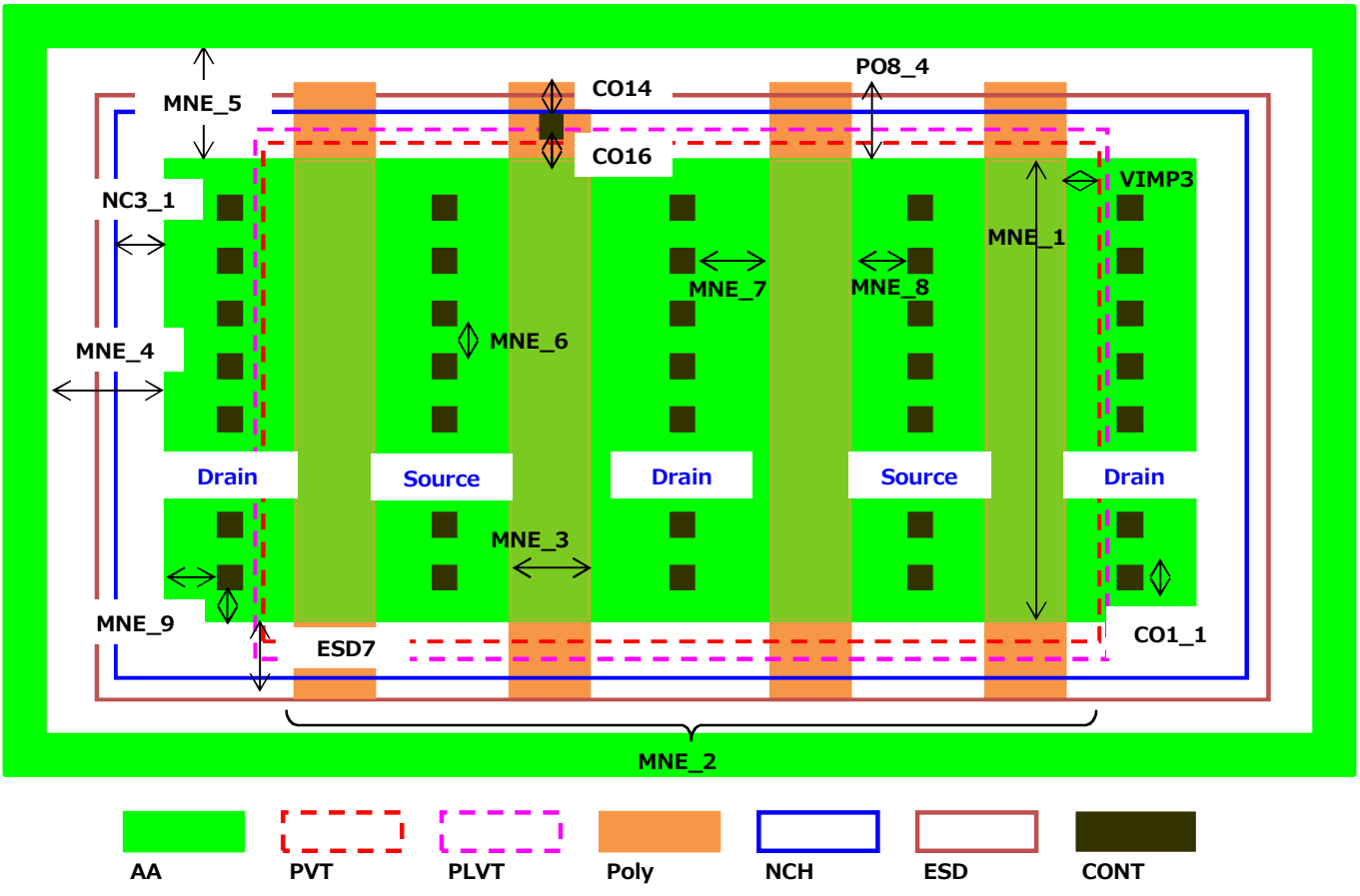
Rule No.	Description		class	Layout Rule (um)
MNN_1a	Transistor Width		min	3.30
MNN_1b			max	100.00
MNN_2a	Transistor Length		min	1.00
MNN_2b			max	100.00
NW7	NWELL spacing to AA(p+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



3.14 MNE_LC/MNE_PC ・・・ Nch ESD Protection MOS Transistor（N+Polycide gate）

MNE_LC(8 finger)、MNE_PC(10 finger)

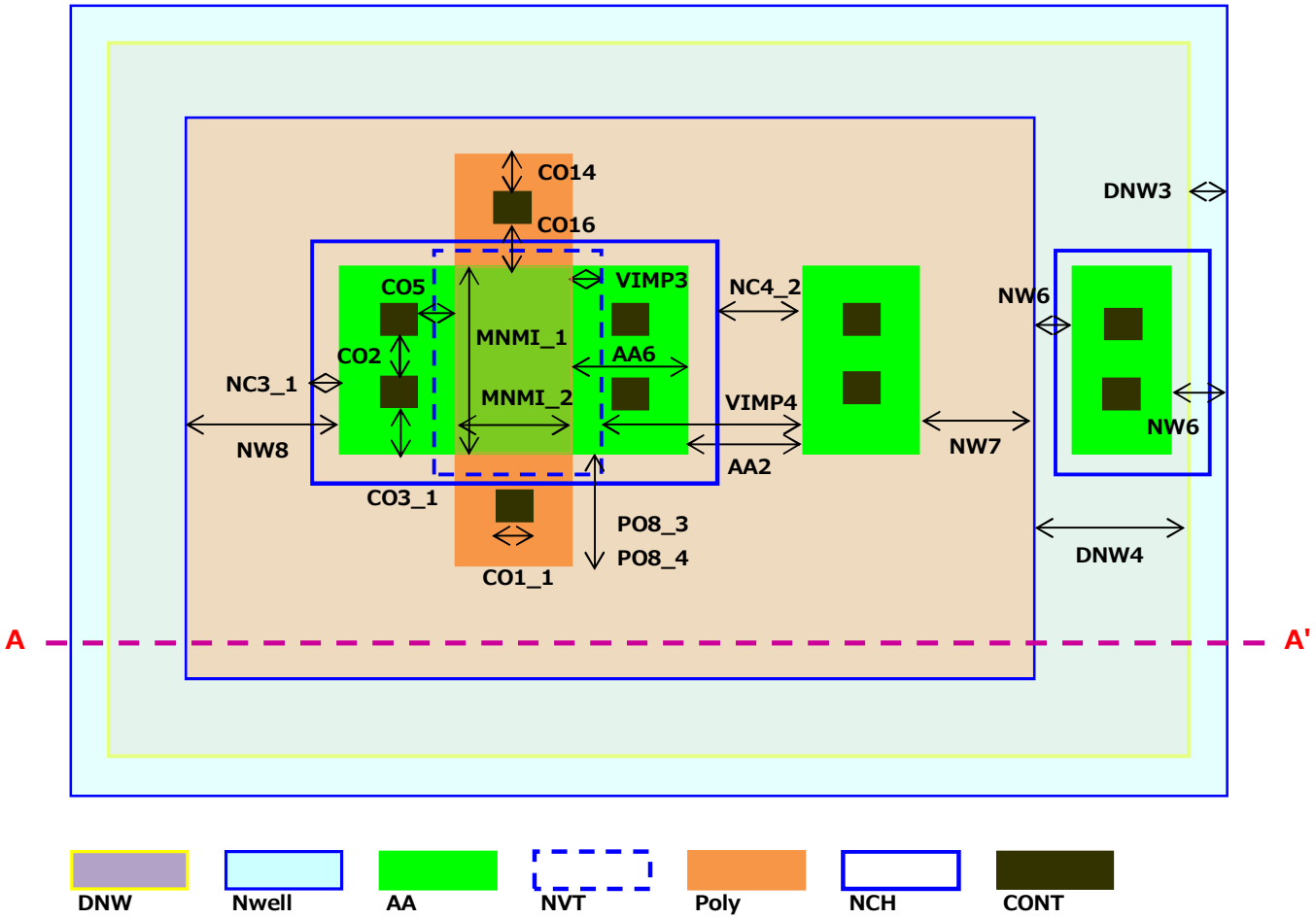
Rule No.	Description		class	Layout Rule (um)
MNE_1	Transistor Width per Finger		fix	60.00
MNE_2a	Transistor Finger	MNE_LC (Local Cramp)	fix	8 finger
MNE_2b		MNE_PC (Power Cramp)	fix	10 finger
MNE_3	Transistor Length		fix	2.00
MNE_4	space AA(P+) to AA(N+)	TR Length side	fix	2.00
MNE_5		TR Width side	fix	4.50
MNE_6	CONT space		fix	0.60
MNE_7	space CONT to Poly	Source Side	min	2.00
MNE_8		Drain side	min	2.00
MNE_9	Drain Contact to Locos		min	1.50
MNE_10	Both outer AA(N+) must be Drain		-	-
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
ESD7	ESD enclosure of AA		min	0.30
CO1	standard CONT size1		fix	0.40x0.40
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



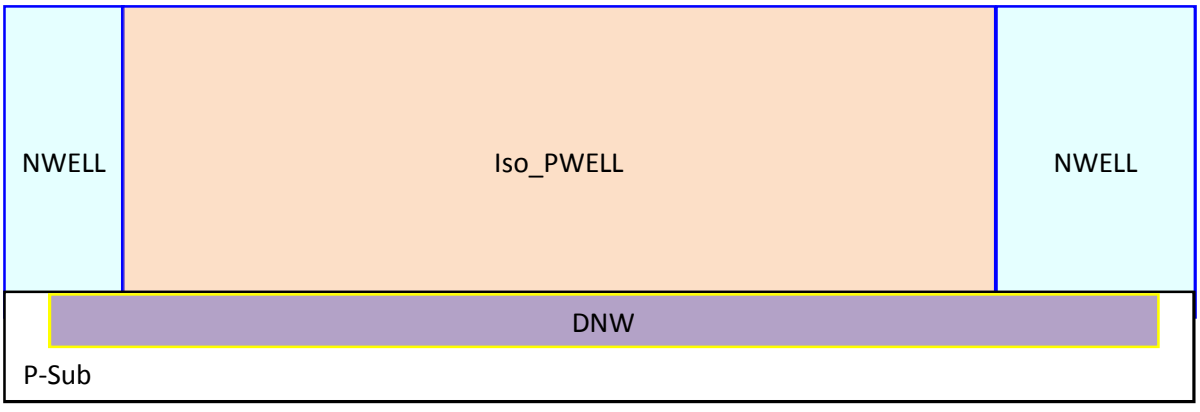
3.15 MNMI ・・・ Isolated Type Nch Medium Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNMI_1a	Transistor Width		min	3.30
MNMI_1b			max	100.00
MNMI_2a	Transistor Length		min	0.70
MNMI_2b			max	100.00
DNW3	NWELL extension beyond DNW		min	1.50
DNW4	NWELL overlap to DNW		min	1.50
NW6	NWELL enclosure of AA(n+tap)		min	0.45
NW7	NWELL spacing to AA(p+tap)		min	0.45
NW8	NWELL spacing to AA(n+)		min	1.00
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

MNMI ・・・ Isolated Type Nch Medium Vt MOS Transistor（N+Polycide gate）



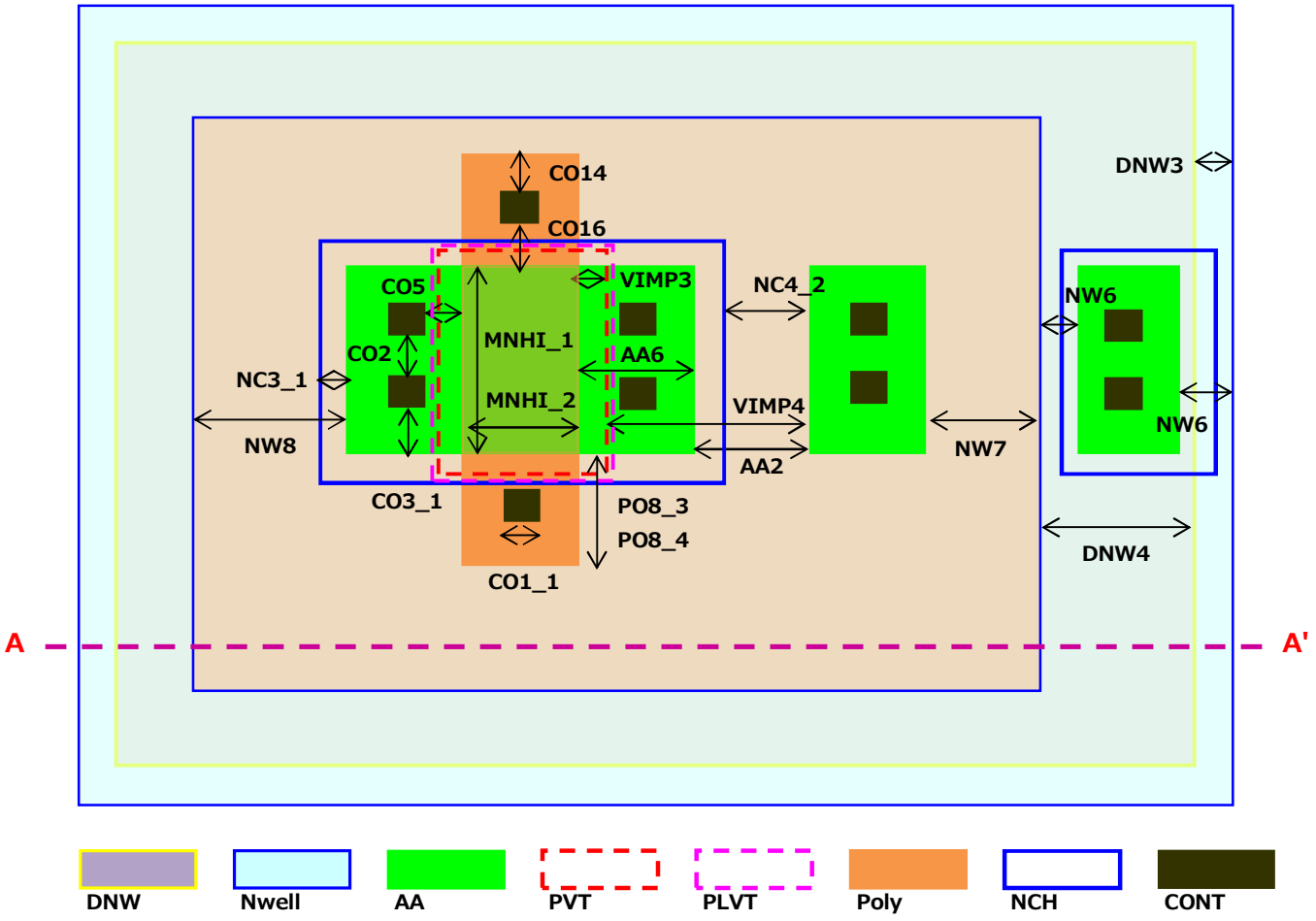
Sectional view in A-A'



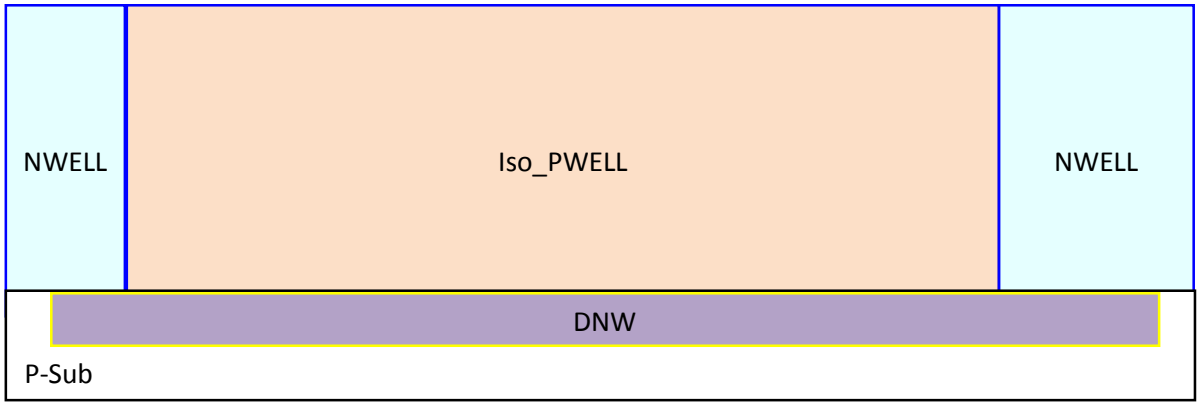
3.16 MNHI ・・・ Isolated Type Nch High Vt MOS Transistor（N+Polycide gate)

Rule No.	Description		class	Layout Rule (um)
MNHI_1a	Transistor Width		min	3.30
MNHI_1b			max	100.00
MNHI_2a	Transistor Length		min	0.70
MNHI_2b			max	100.00
DNW3	NWELL extension beyond DNW		min	1.50
DNW4	NWELL overlap to DNW		min	1.50
NW6	NWELL enclosure of AA(n+tap)		min	0.45
NW7	NWELL spacing to AA(p+tap)		min	0.45
NW8	NWELL spacing to AA(n+)		min	1.00
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

MNHI ・・・ Isolated Type Nch High Vt MOS Transistor（N+Polycide gate）



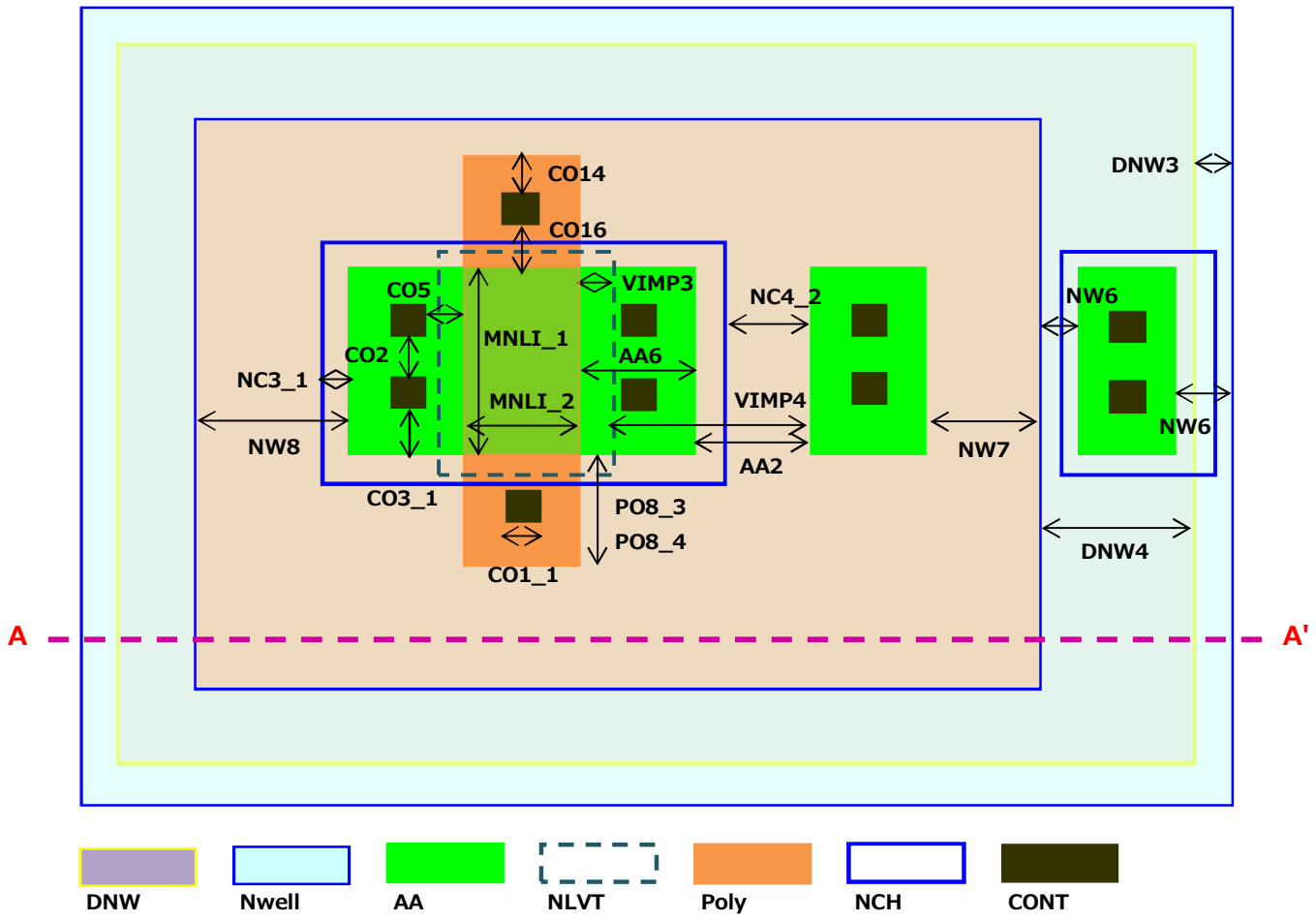
Sectional view in A-A'



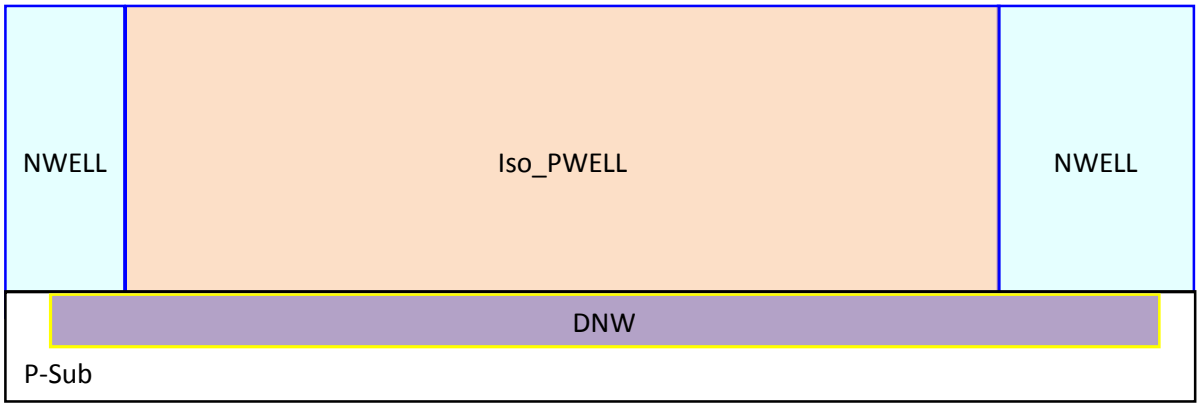
3.17 MNLI ・・・ Isolated Type Nch Low Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNLI_1a	Transistor Width		min	3.30
MNLI_1b			max	100.00
MNLI_2a	Transistor Length		min	0.80
MNLI_2b			max	100.00
DNW3	NWELL extension beyond DNW		min	1.50
DNW4	NWELL overlap to DNW		min	1.50
NW6	NWELL enclosure of AA(n+tap)		min	0.45
NW7	NWELL spacing to AA(p+tap)		min	0.45
NW8	NWELL spacing to AA(n+)		min	1.00
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

MNLI ・・・ Isolated Type Nch Low Vt MOS Transistor（N+Polycide gate)



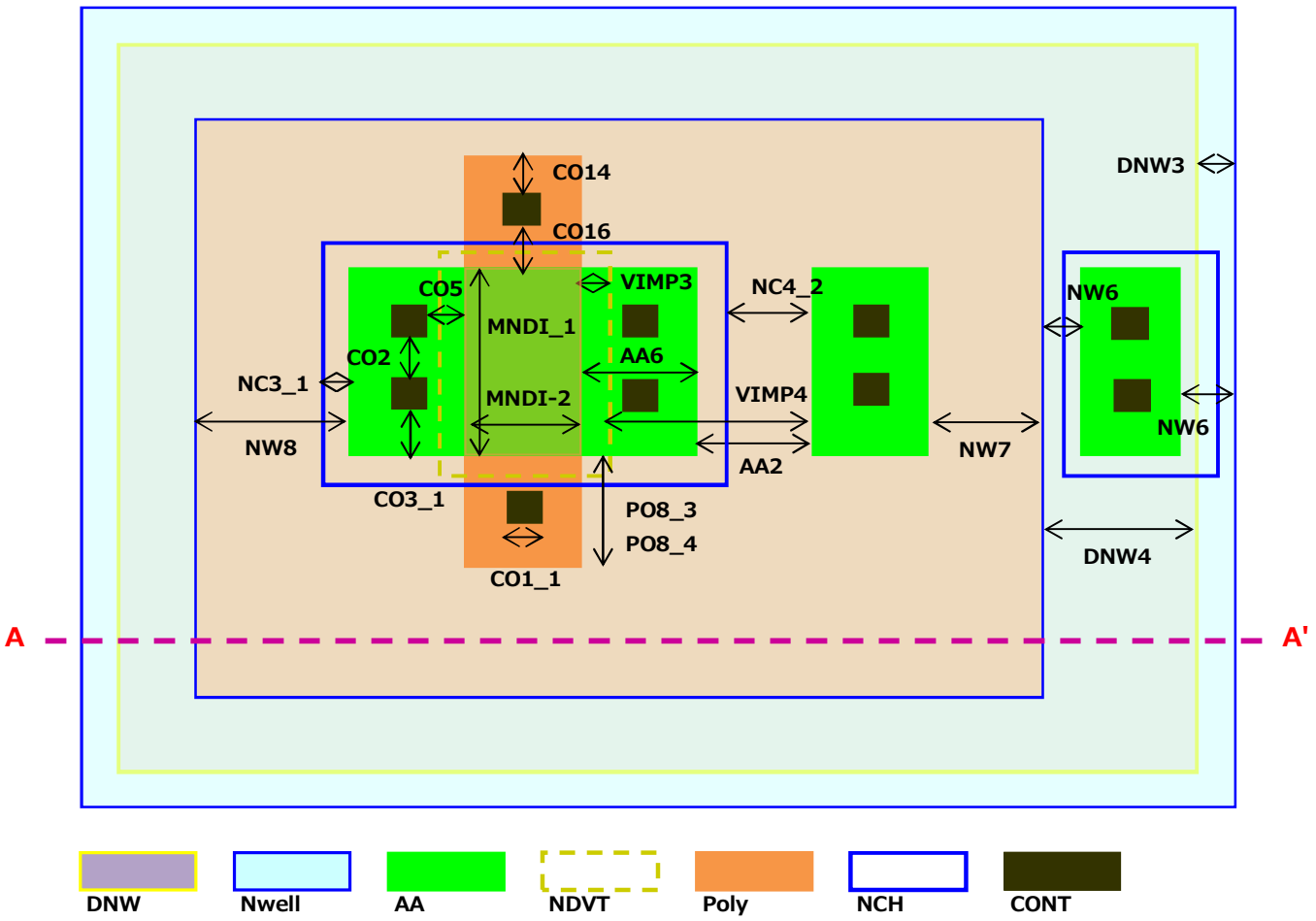
Sectional view in A-A'



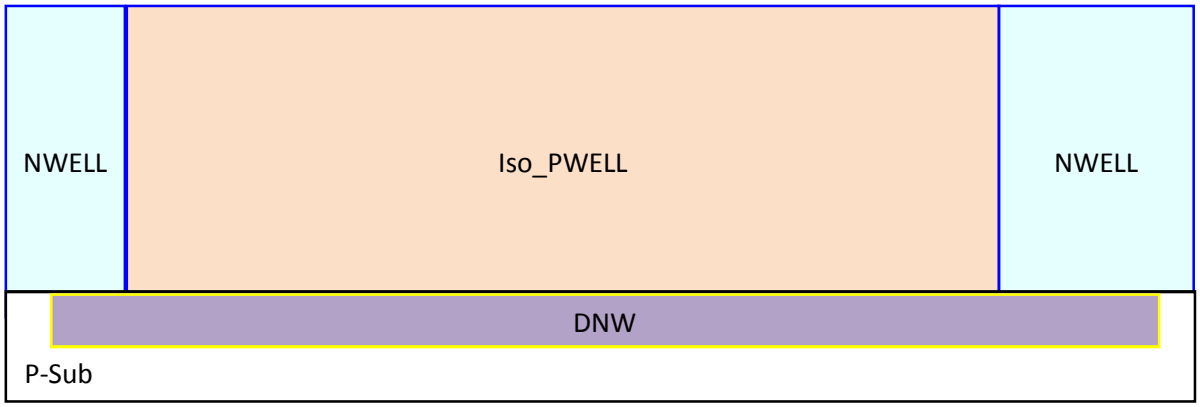
3.18 MNDI ・・・ Isolated Type Nch Depletion Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNDI_1a	Transistor Width		min	3.30
MNDI_1b			max	100.00
MNDI_2a	Transistor Length		min	2.00
MNDI_2b			max	100.00
DNW3	NWELL extension beyond DNW		min	1.50
DNW4	NWELL overlap to DNW		min	1.50
NW6	NWELL enclosure of AA(n+tap)		min	0.45
NW7	NWELL spacing to AA(p+tap)		min	0.45
NW8	NWELL spacing to AA(n+)		min	1.00
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
VIMP4	VIMP spacing to AA (excluding Tap AA)		min	0.30
PO8_3	POLY extension beyond AA @ 0.5um=<POLY width<1.2um		min	0.38
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

MNDI ・・・ Isolated Type Nch Depletion Vt MOS Transistor（N+Polycide gate）



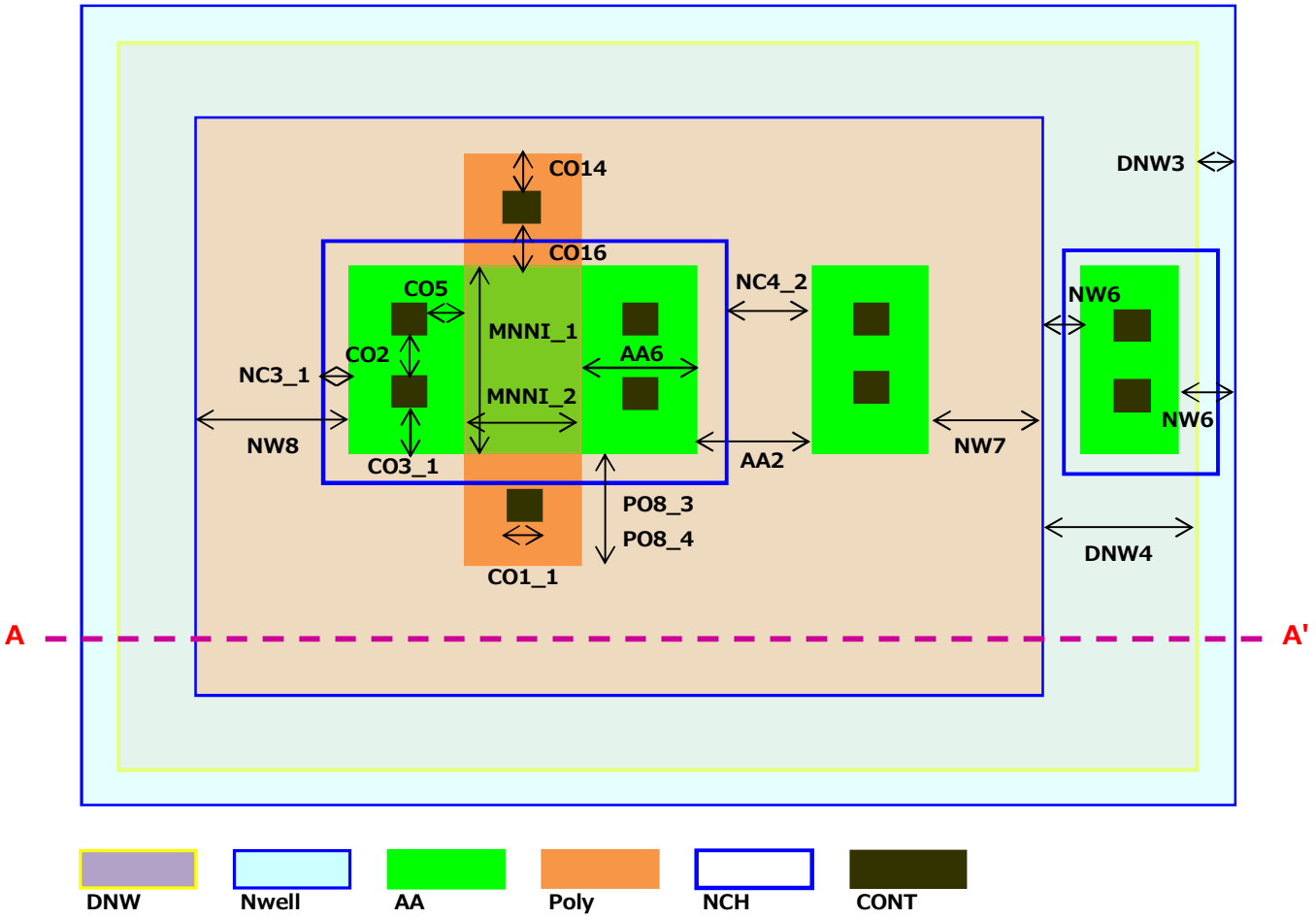
Sectional view in A-A'



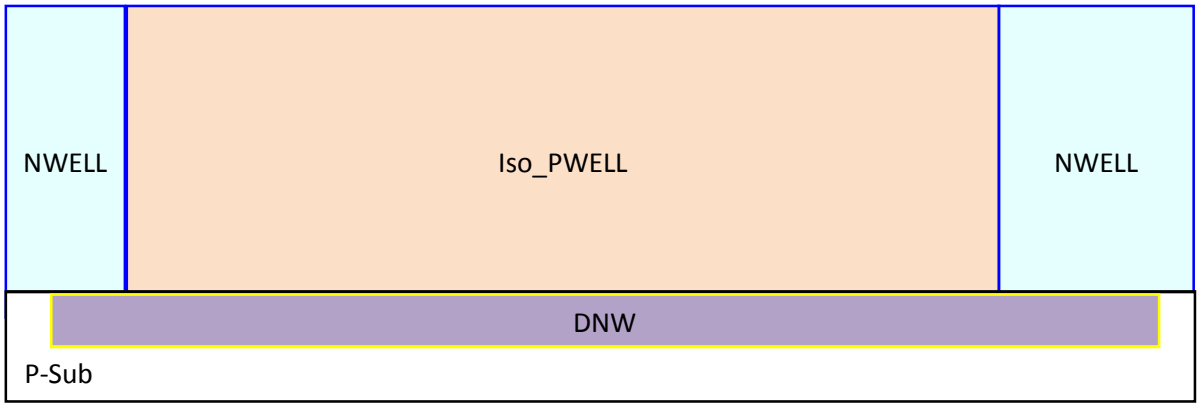
3.19 MNNI ・・・ Isolated Type Nch Native Vt MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
MNNI_1a	Transistor Width		min	3.30
MNNI_1b			max	100.00
MNNI_2a	Transistor Length		min	1.00
MNNI_2b			max	100.00
DNW3	NWELL extension beyond DNW		min	1.50
DNW4	NWELL overlap to DNW		min	1.50
NW6	NWELL enclosure of AA(n+tap)		min	0.45
NW7	NWELL spacing to AA(p+tap)		min	0.45
NW8	NWELL spacing to AA(n+)		min	1.00
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.69
AA2_2		same node	min	0.50 or butting
AA6	AA extension beyond gate		min	0.65
PO8_3	POLY extension beyond AA	@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

MNNI ・・・ Isolated Type Nch Native Vt MOS Transistor（N+Polycide gate）



Sectional view in A-A'

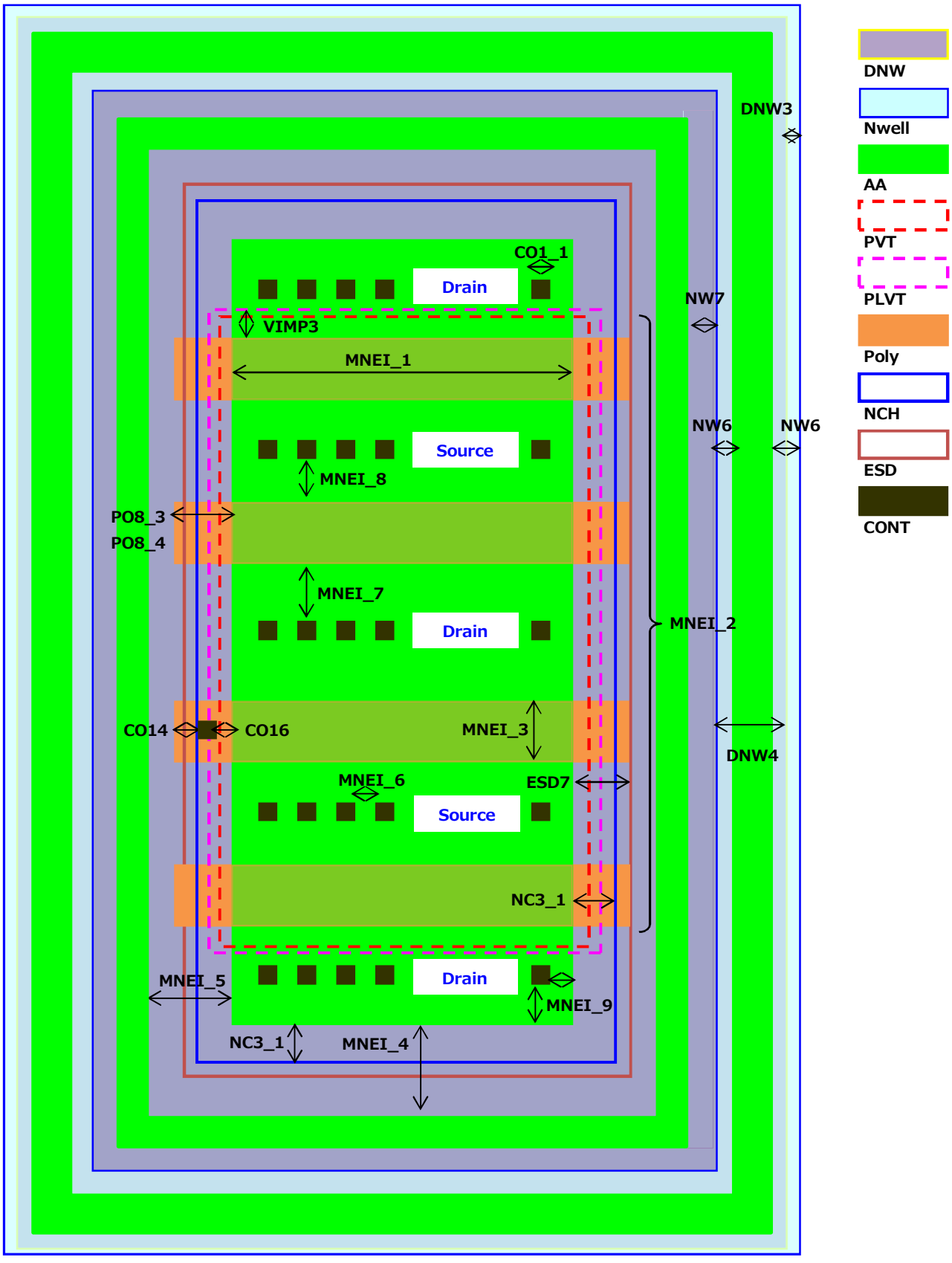


3.20 MNEI_LC/MNEI_PC ・・・ Isolated Type Nch ESD Protection MOS Transistor（N+Polycide gate）

MNEI_LC(8 finger)、MNEI_PC(10 finger)

Rule No.	Description		class	Layout Rule (um)
MNEI_1	Transistor Width		fix	60.00
MNEI_2a	Transistor Finger	MNEI_LC (Local Cramp)	fix	8 finger
MNEI_2b		MNEI_PC (Power Cramp)	fix	10 finger
MNEI_3	Transistor Length		fix	2.00
MNEI_4	space AA(P+) to AA(N+)	TR Length side	fix	2.00
MNEI_5		TR Width side	fix	4.50
MNEI_6	CONT space		fix	0.60
MNEI_7	space CONT to Poly	Source Side	min	2.00
MNEI_8		Drain side	min	2.00
MNEI_9	Drain Contact to Locos		min	1.50
MNEI_10	Both outer AA(N+) must be Drain		-	-
DNW3	NWELL extension beyond DNW		min	1.50
DNW4	NWELL overlap to DNW		min	1.50
NW6	NWELL enclosure of AA(n+tap)		min	0.45
NW7	NWELL spacing to AA(p+tap)		min	0.45
VIMP3	VIMP enclosure of gate (POLY and AA)		min	0.30
PO8_4	@ POLY width>=1.2um		min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
ESD7	ESD enclosure of AA		min	0.30
CO1	standard CONT size1		fix	0.40x0.40
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29

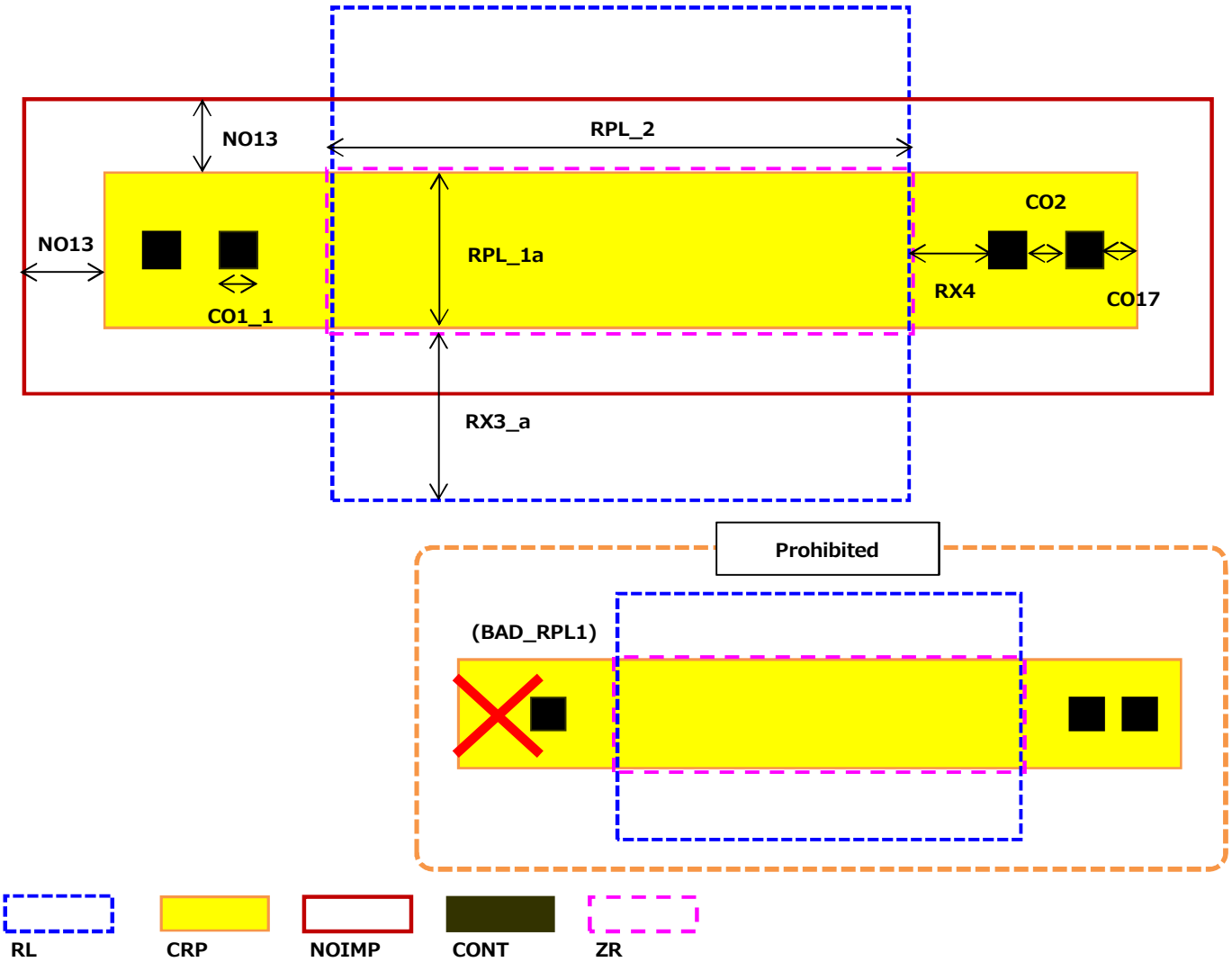
MNEI_LC/MNEI_PC ・・・ Isolated Type Nch ESD Protection MOS Transistor（N+Polycide gate）



3.21 RPL ・・・ Low Resistance Poly-Si Resistor (95ohm/s)

Rule No.	Description	class	Layout Rule (um)
RPL_1a	RPL Width	min	1.30
RPL_2a	RPL Length	min	30.00
RPL_2b		max	100.00
RX3_a	RL extension beyond CRP for RPL	min	4.00
RX4	RX spacing to CONT for RPL,RPM,RPH	fix	0.56
NO13	NOIMP enclosure of CRP for RPL,RPM,RPH	min	0.48
CO1	standard CONT size1	fix	0.40x0.40
CO2	CONT spacing	min	0.40
CO17	CRP enclosure of CONT	min	0.45
BAD_RPL1	Single CONT is prohibited between CRP and 1METAL.		

＊Place the ZR layer in the resistance recognition part (Flush with the overlapping part between CRP and RL).【Please refer to the figure below.】

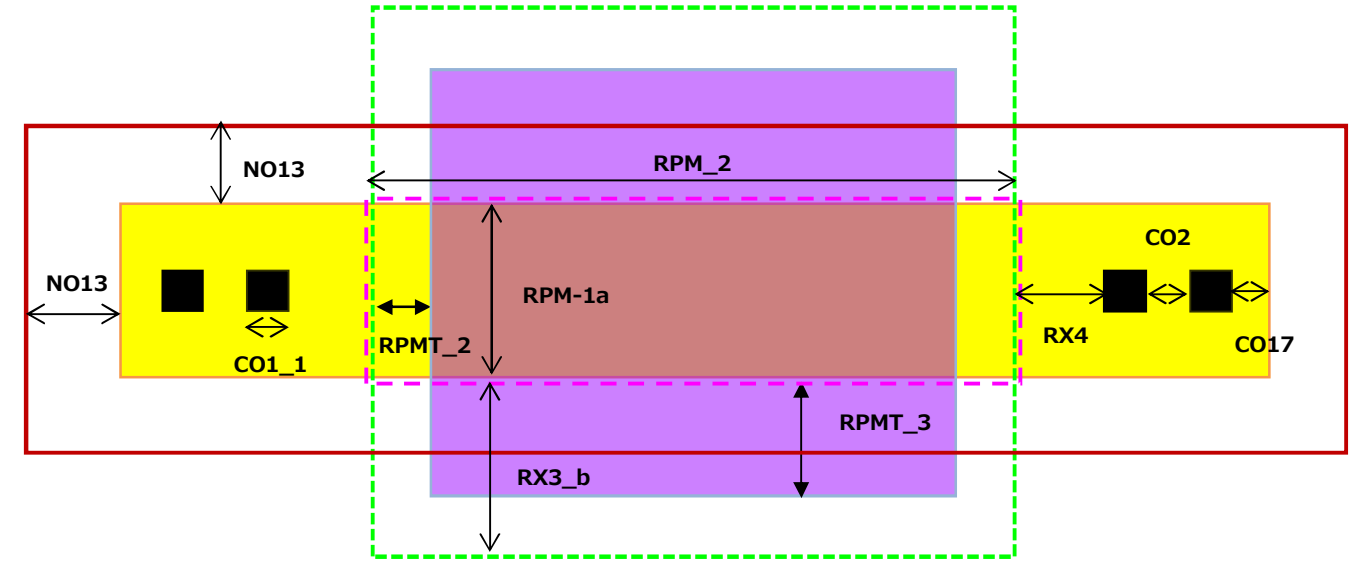


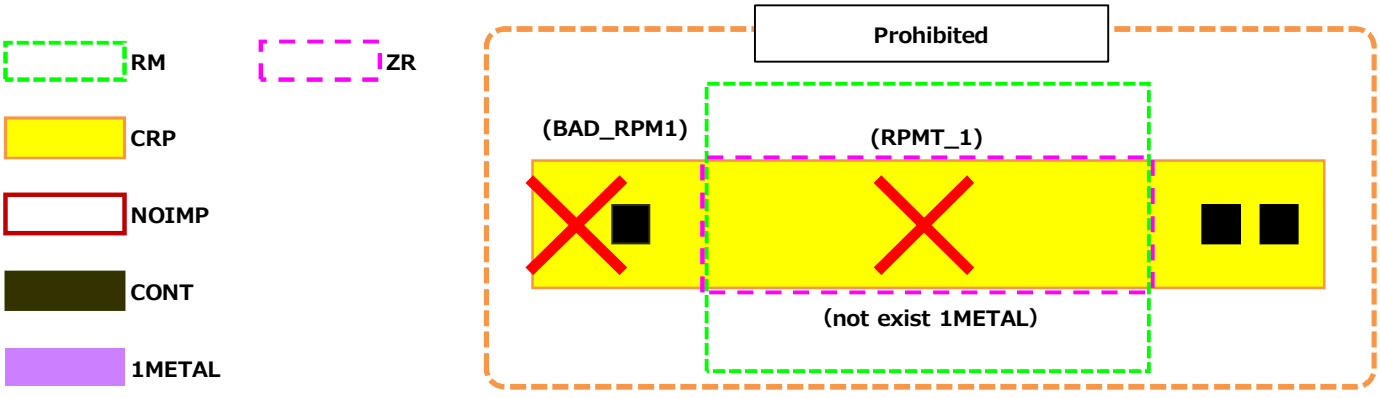
3.22 RPM ・・・ Medium Resistance Poly-Si Resistor (330ohm/s)

Rule No.	Description	class	Layout Rule (um)
RPM_1a	RPM Width	min	1.30
RPM_2a	RPM Length	min	30.00
RPM_2b		max	100.00
RPMT_1	1METAL must cover on RPM, RPH area		
RPMT_2	RM, RH overlap to 1METAL for RPM, RPH length direction	fix	0.23
RPMT_3	1METAL overlap to CRP for RPM, RPH	min	6.00
RX3_b	RM, RH extension beyond CRP for RPM,RPH	min	8.00
RX4	RX spacing to CONT for RPL,RPM,RPH	fix	0.56
NO13	NOIMP enclosure of CRP for RPL,RPM,RPH	min	0.48
CO1	standard CONT size1	fix	0.40x0.40
CO2	CONT spacing	min	0.40
CO17	CRP enclosure of CONT	min	0.45
BAD_RPM1	Single CONT is prohibited between CRP and 1METAL.		

＊Place the ZR layer in the resistance recognition part (Flush with the overlapping part between CRP and RM).【Please refer to the figure below.】

＊1METAL Cover should be hand-drawn.(T-Cell is not supported.)





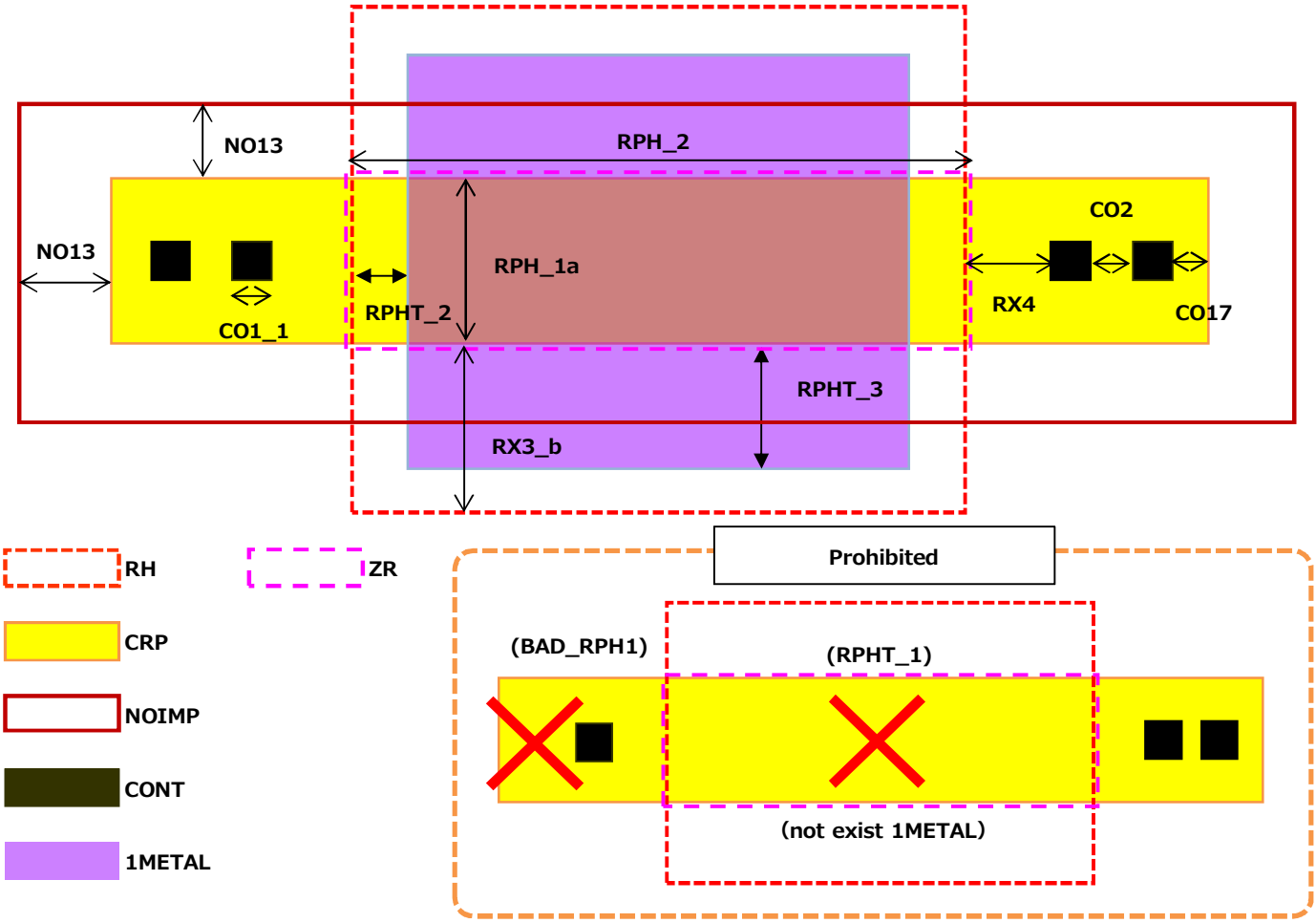
3.23 RPH/RPH2 ・・・ High Resistance Poly-Si Resistor RPH(5Kohm/s)、RPH2(8Kohm/s)

＊Don't use RPH and RPH 2 at the same time.

Rule No.	Description	class	Layout Rule (um)
RPH_1a	RPH Width	min	1.30
RPH_2a	RPH Length	min	30.00
RPH_2b		max	100.00
RPHT_1	1METAL must cover on RPM, RPH area		
RPHT_2	RM, RH overlap to 1METAL for RPM, RPH length direction	fix	0.23
RPHT_3	1METAL overlap to CRP for RPM, RPH	min	6.00
RX3_b	RM, RH extension beyond CRP for RPM,RPH	min	8.00
RX4	RX spacing to CONT for RPL,RPM,RPH	fix	0.56
NO13	NOIMP enclosure of CRP for RPL,RPM,RPH	min	0.48
CO1	standard CONT size1	fix	0.40x0.40
CO2	CONT spacing	min	0.40
CO17	CRP enclosure of CONT	min	0.45
BAD_RPH1	Single CONT is prohibited between CRP and 1METAL.		

＊Place the ZR layer in the resistance recognition part (Flush with the overlapping part between CRP and RH).【Please refer to the figure below.】

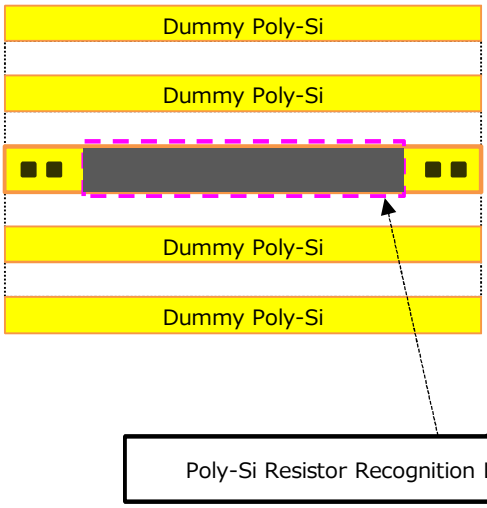
＊1METAL Cover should be hand-drawn.(T-Cell is not supported.)



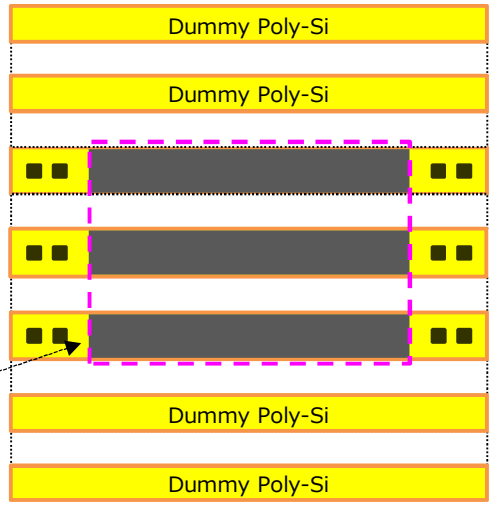
3.24 Ladder Poly-Si Resistor Layout Rule

In order to reduce resistance variation, please place them on both sides for a single Poly-Si resistor. When multiple resistors are in parallel, please arrange two dummy Poly on the each outside of the Poly area of the resistance area as shown on the figure.

・Single Poly-Si Resistor Case

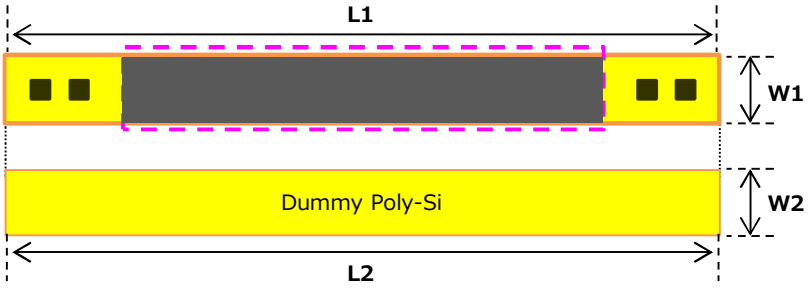


・Multi Poly-Si Resistors Case



The layout rule around Poly-Si resistor is applied to the body pattern including Poly-Si resistor and it is not applicable to dummy pattern.

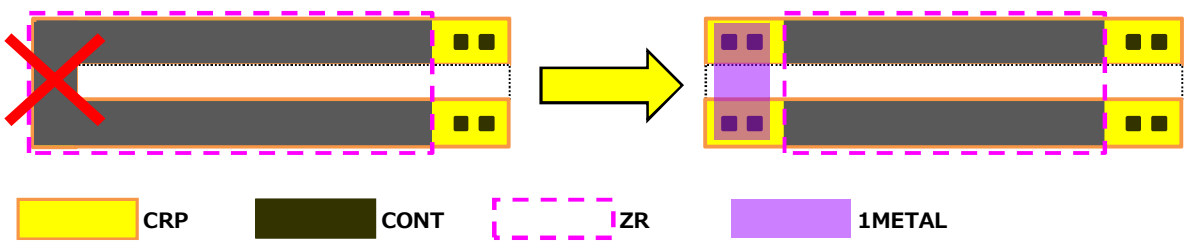
Make the dimensions of dummy pattern same as Poly-Si Resistor.



L1 = L2

W1 = W2

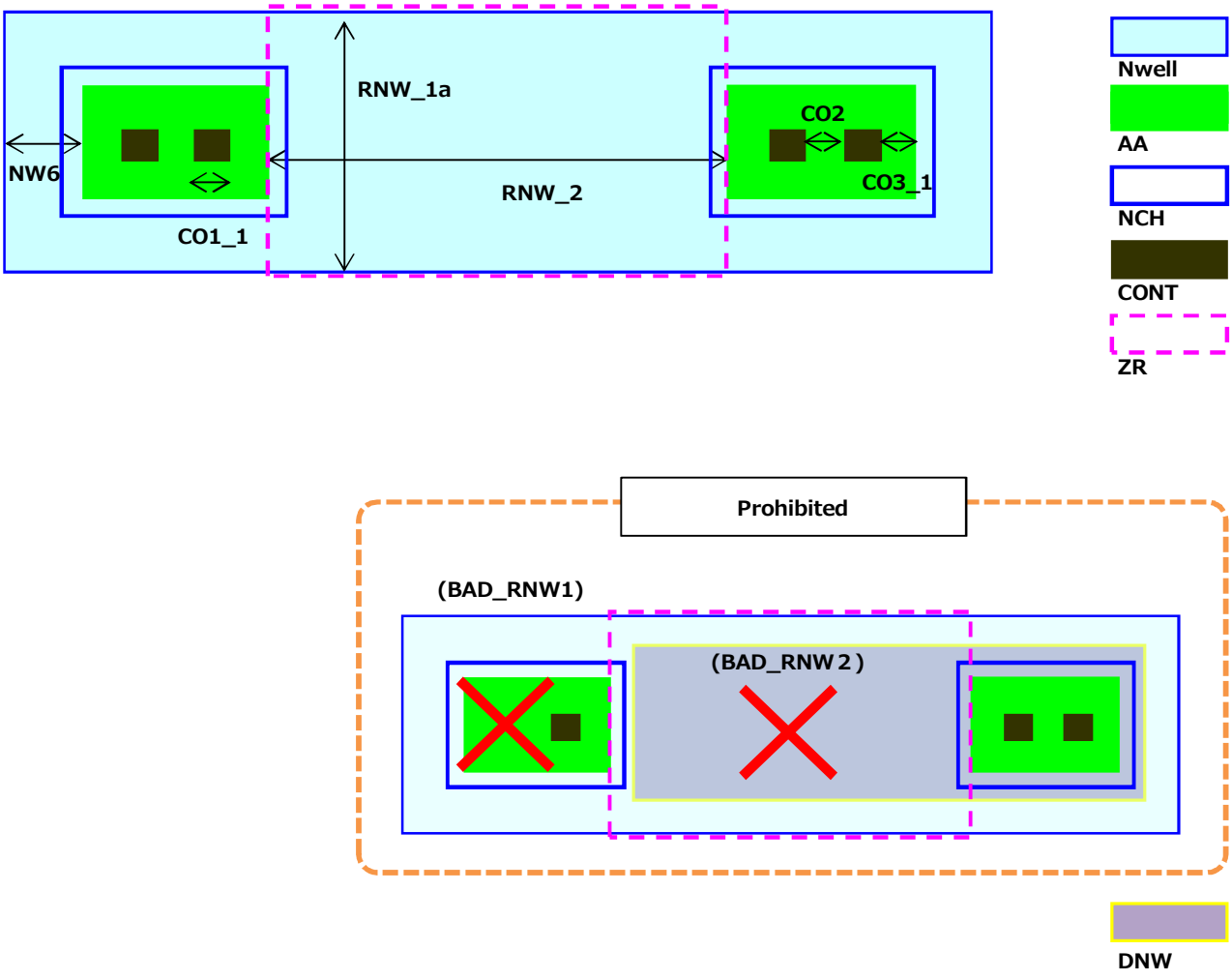
Folding of Poly-Si resistor is prohibited.
Place in a straight line and connect a metal wiring between the Poly-Si resistors.



3.25 RNW ・・・ Nwell Diffusion Resistor

Rule No.	Description		class	Layout Rule (um)
RNW_1a	RNW Width		min	3.00
RNW_2a	RNW Length		min	10.00
RNW_2b			max	100.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
BAD_RNW1	Single CONT is prohibited between RNW and 1METAL.			
BAD_RNW2	NWELL of RNW overlap DNW is prohibited			

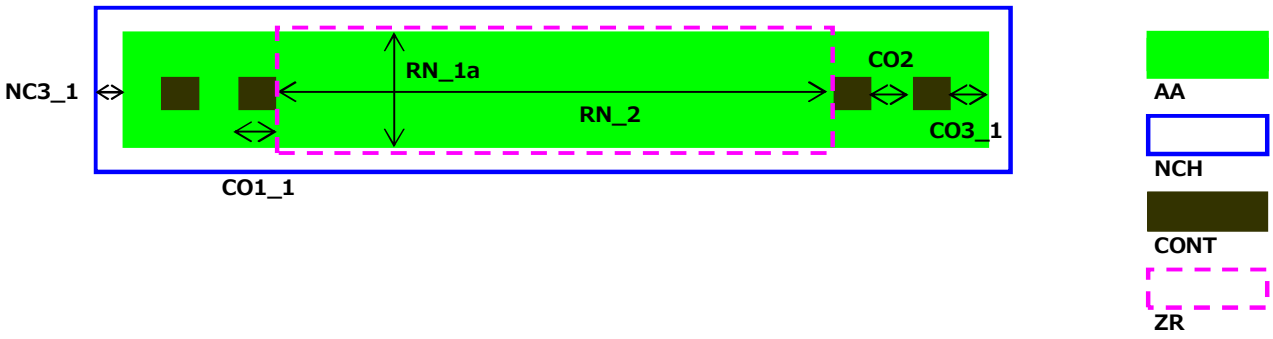
＊Place the ZR layer in the resistance recognition part(Width direction: NW edge, Length direction: flush with AA edge）.【Please refer to the figure below.】

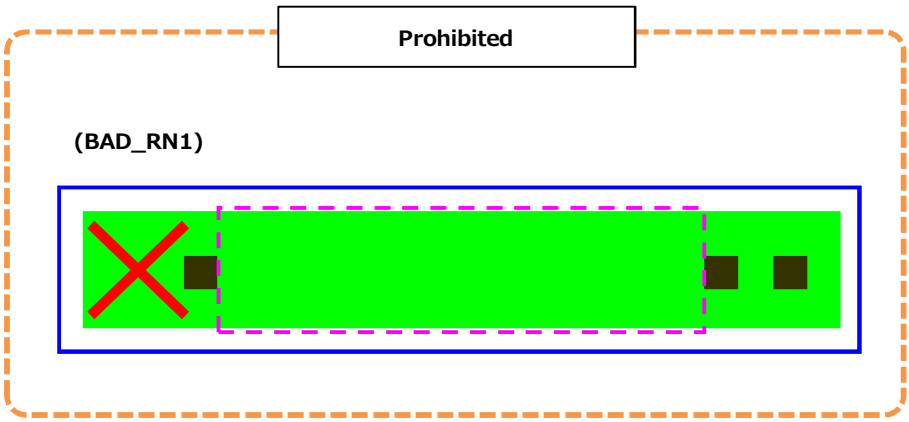


3.26 RN ・・・ N+ Diffusion Resistor

Rule No.	Description		class	Layout Rule (um)
RN_1a	RN Width		min	1.00
RN_2a	RN Length		min	10.00
RN_2b			max	100.00
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
BAD_RN1	Single CONT is prohibited between RN and 1METAL.			

＊Place the ZR layer in the resistance recognition part(Width direction: AA edge、Length direction: flush with CONT edge).【Please refer to the figure below.】

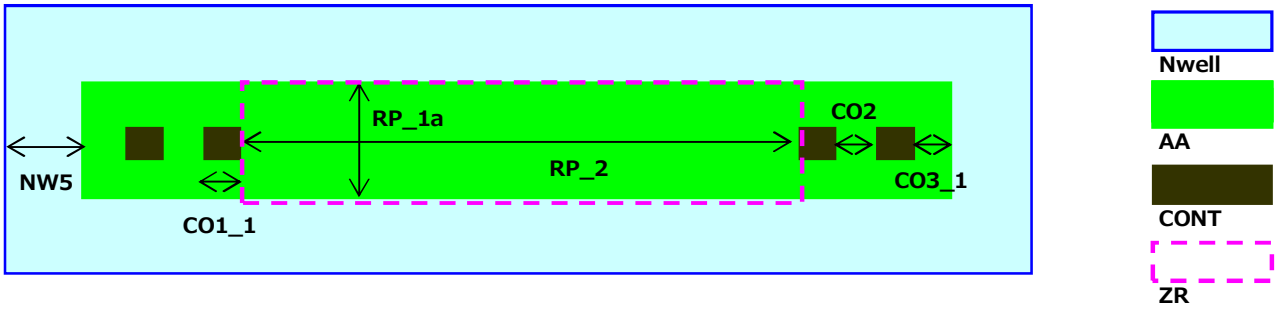


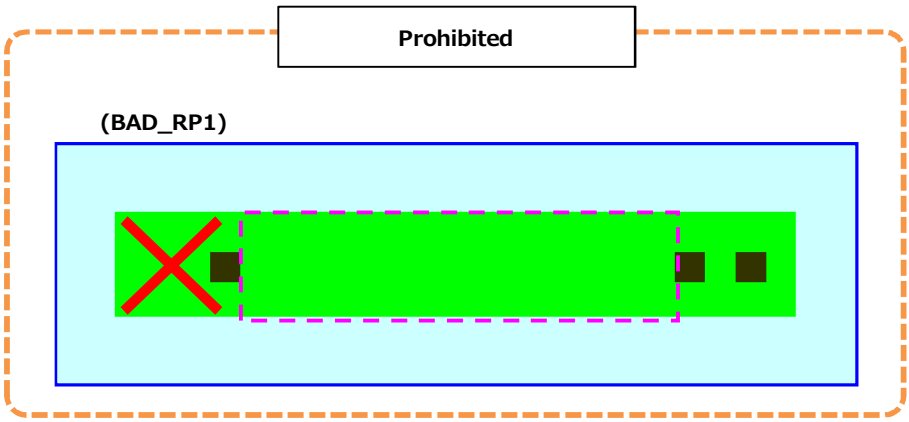


3.27 RP ・・・ P+ Diffusion Resistor

Rule No.	Description		class	Layout Rule (um)
RP_1a	RP Width		min	1.00
RP_2a	RP Length		min	10.00
RP_2b			max	100.00
NW5	NWELL enclosure of AA(p+)		min	1.00
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
BAD_RP1	Single CONT is prohibited between RP and 1METAL.			

＊Place the ZR layer in the resistance recognition part(Width direction: AA edge、Length direction: flush with CONT edge）.【Please refer to the figure below.】

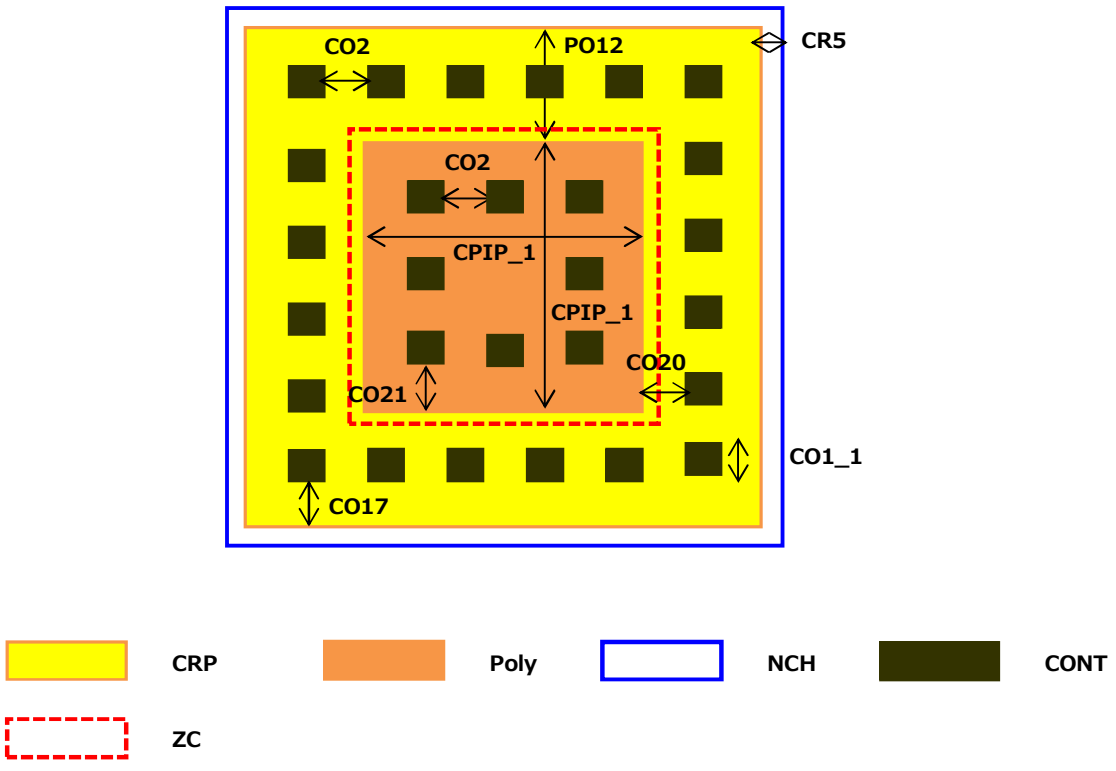




3.28 CPIP・・・ PIP Capacitor

Rule No.	Description	class	Layout Rule (um)
CPIP_1a	CPIP Size	min	10x10
CPIP_1b		max	100x100
CR5	NCH enclosure of CRP (only for CPIP)	min	0.48
PO12	CRP enclosure of POLY	min	0.60
CO1	standard CONT size1	fix	0.40x0.40
CO2	CONT spacing	min	0.40
CO17	CRP enclosure of CONT	min	0.45
CO20	CONT spacing to POLY (on CRP)	min	0.47
CO21	POLY enclosure of CONT (on upper plate)	min	0.47

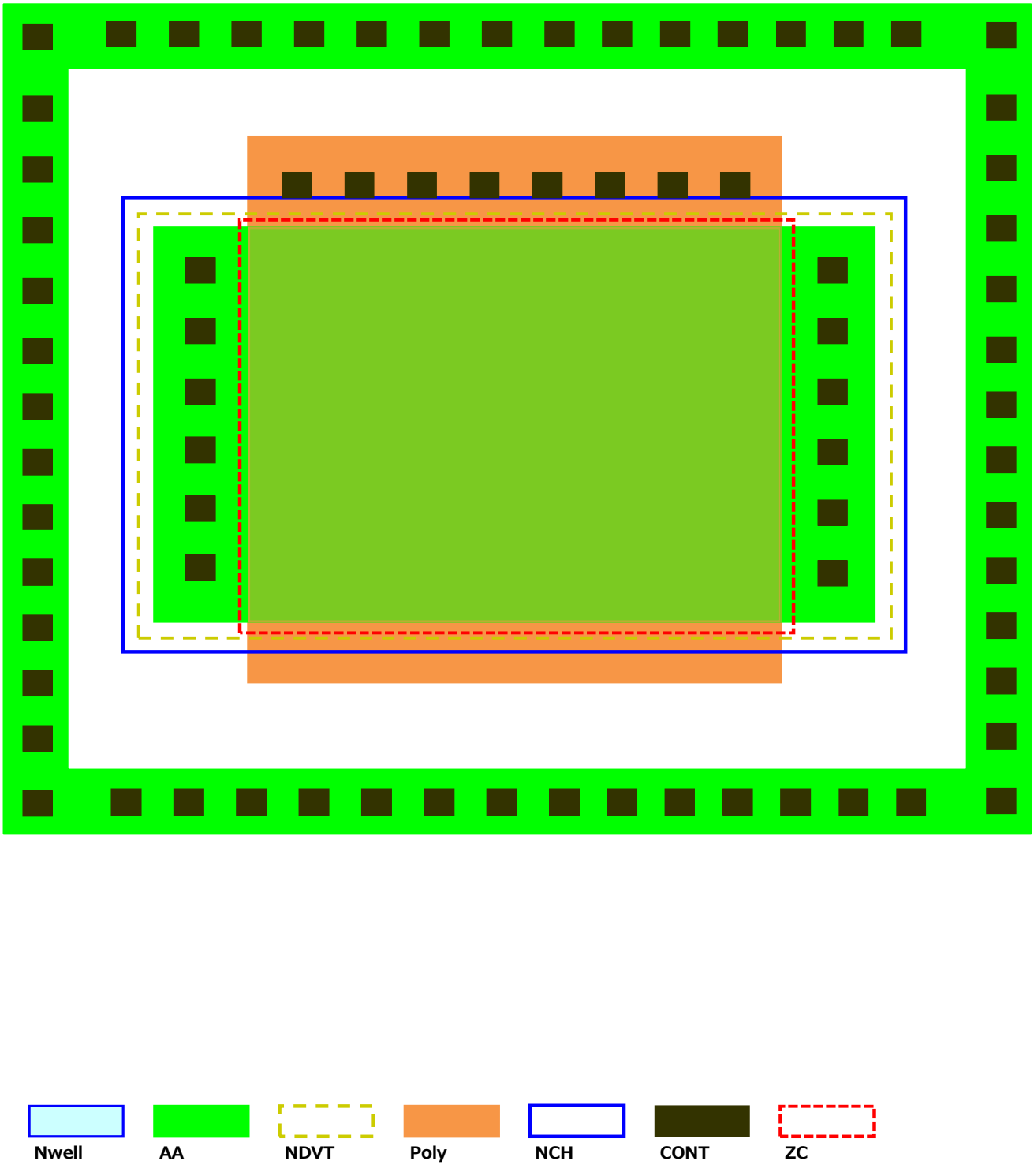
＊Place the ZC layer in the capacity recognition part (Flush with the overlapping part between CRP and POLY).【Please refer to the figure below.】



3.29　CND・・・ Nch Depletion Vt MOS Capacitor（N+Polycide gate）

＊Place the ZC layer in the capacity recognition part(Channel Active: AA and Poly).
【Please refer to the figure below.】

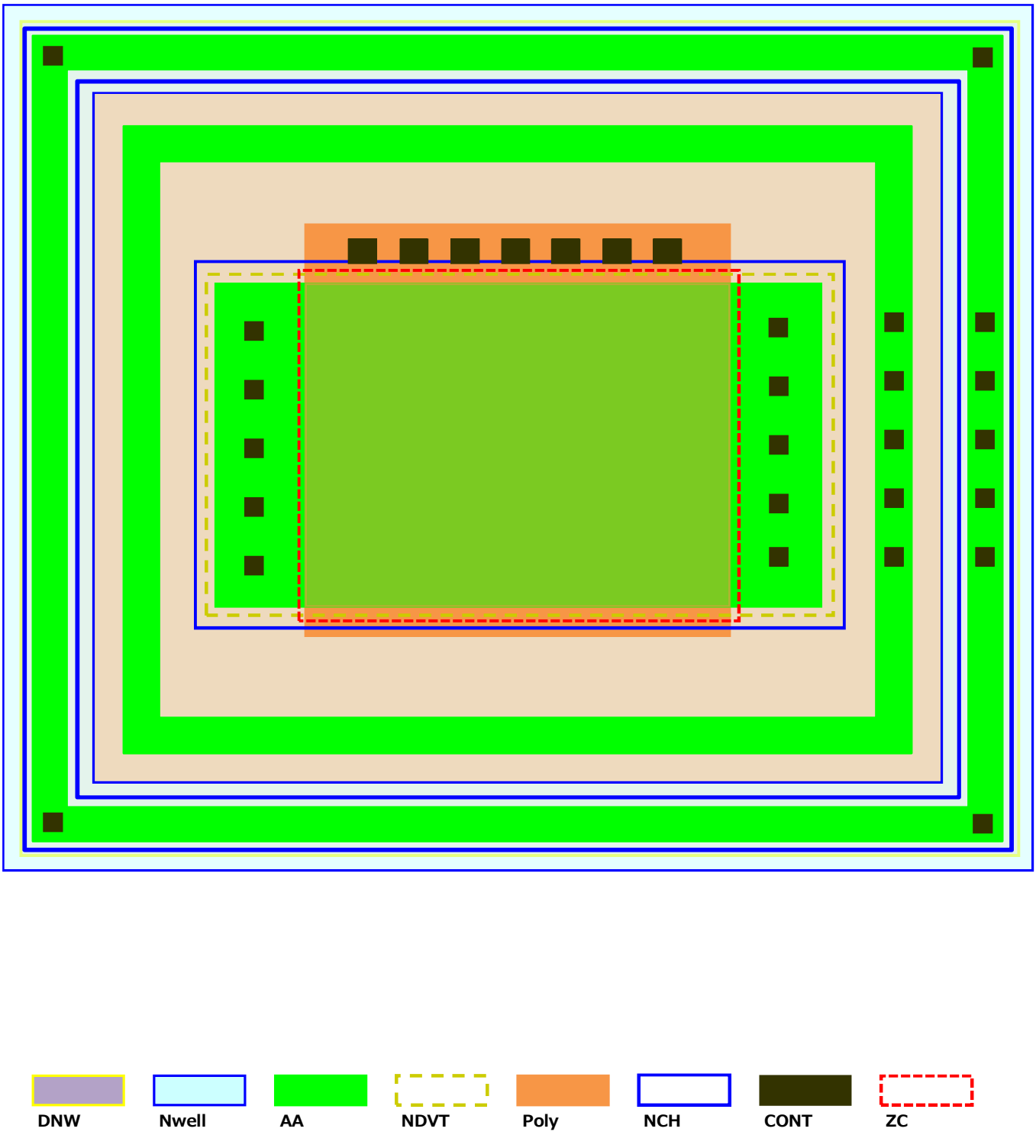
Other Rules >
Please refer to a page of MND device rule for each structural parameter.



3.30　CNDI ・・・ Isolated Type Nch Depletion Vt MOS Capacitor（N+Polycide gate）

＊Place the ZC layer in the capacity recognition part(Channel Active: AA and Poly).
【Please refer to the figure below.】

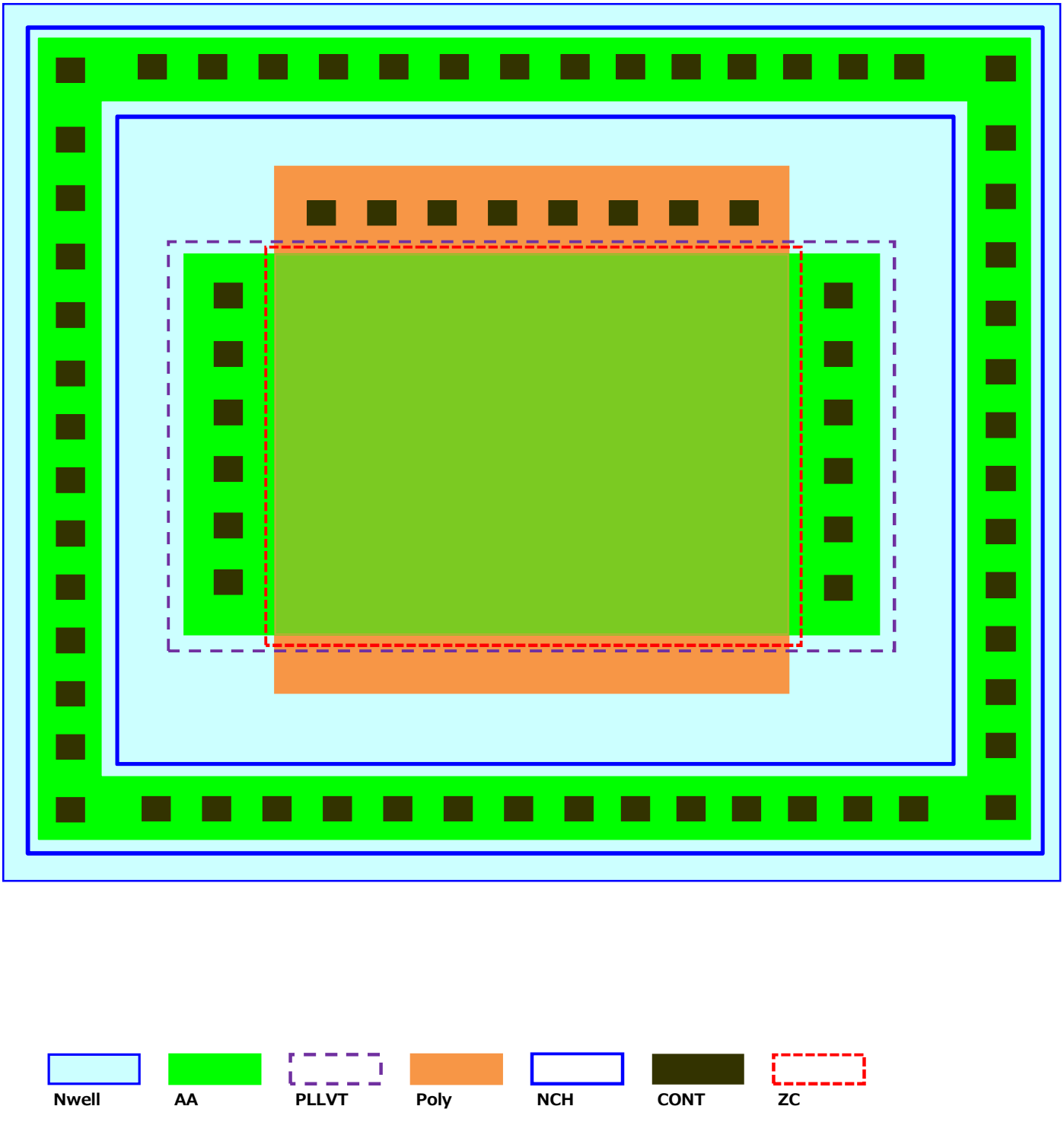
Other Rules >
Please refer to a page of MNDI & CND device rule for each structural parameter.



3.31　CPL2･･･ Pch Very Low Vt MOS Capacitor（N+Polycide gate）

＊Place the ZC layer in the capacity recognition part(Channel Active: AA and Poly).
【Please refer to the figure below.】

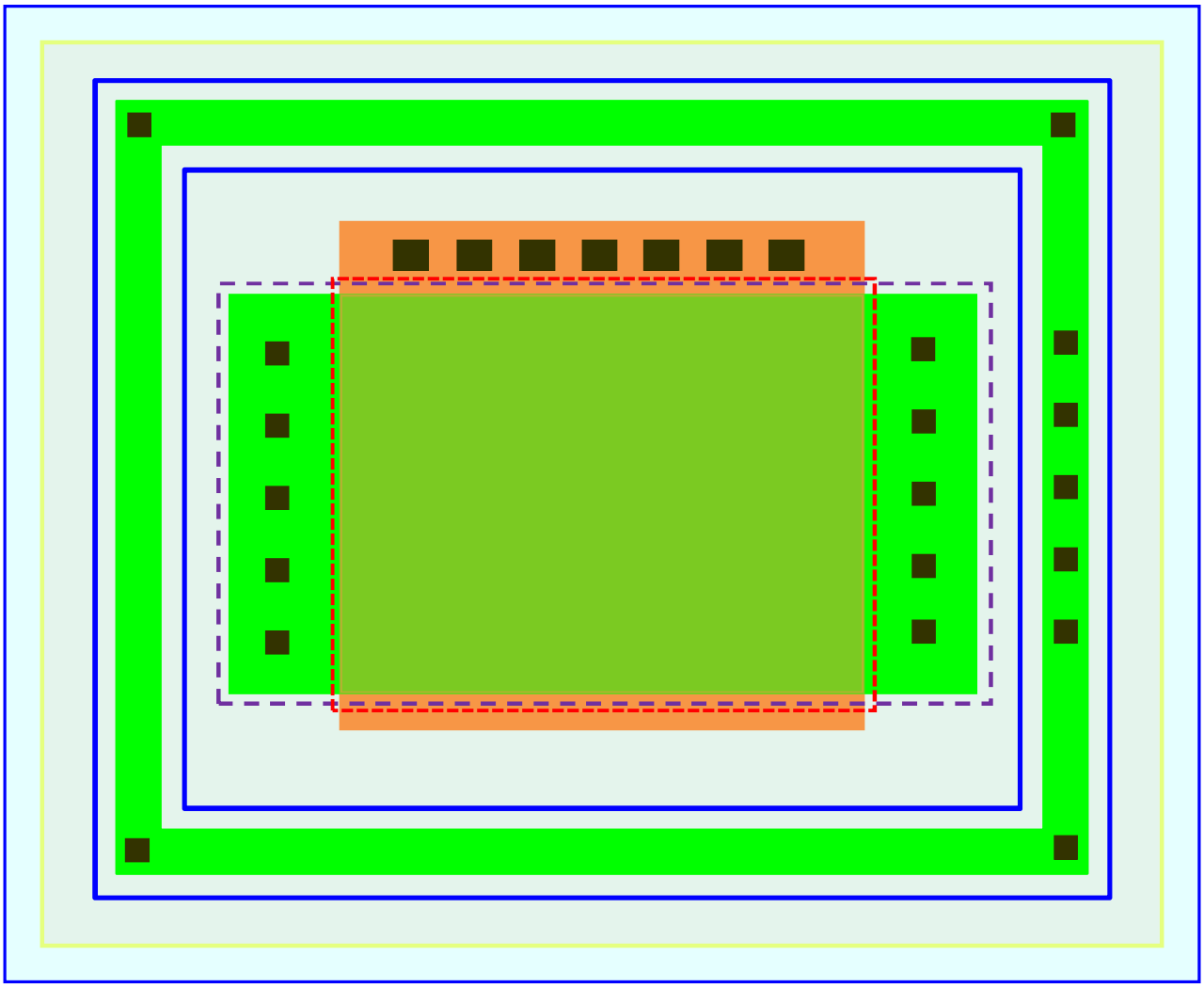
Other Rules >
Please refer to a page of MPL2 device rule for each structural parameter.



3.32　CPL2I ・・・ Isolated Type Pch Very Low Vt MOS Capacitor（N+Polycide gate）

＊Place the ZC layer in the capacity recognition part(Channel Active: AA and Poly).
【Please refer to the figure below.】

Other Rules >
Please refer to a page of MPL2I & CPL device rule for each structural parameter.



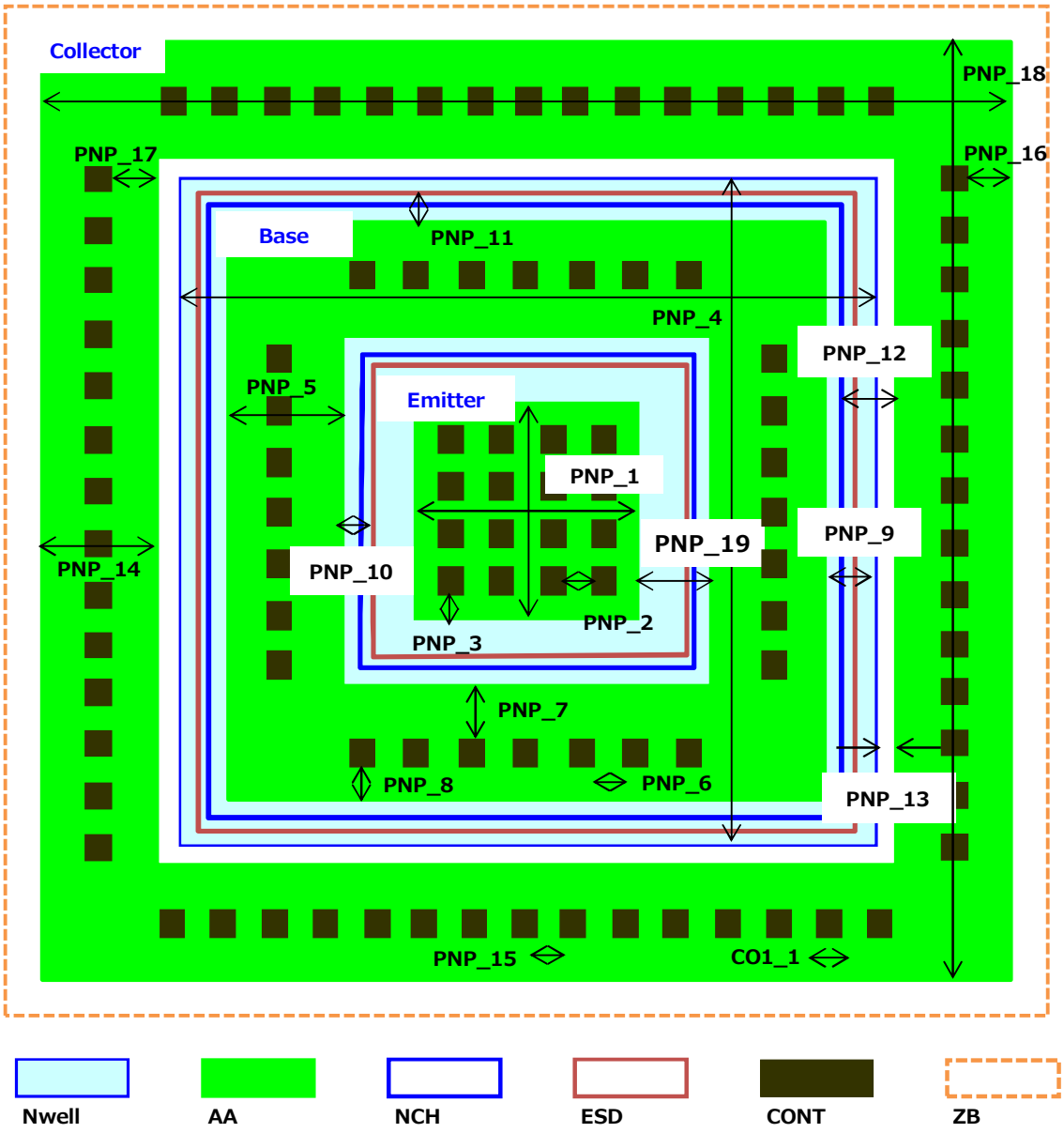
3.33 PNP・・・ vertical PNP (P+/NW/Psub)

Rule No.	Description	class	Layout Rule (um)
CO1	standard CONT size1	fix	0.40x0.40
PNP_1	Emitter Area Size	fix	5.00x5.00
PNP_2	Contact space in Emitter Area	fix	0.60
PNP_3	AA enclosure of Contact in Emitter Area	fix	0.80
PNP_4	Base Area Size	fix	19.00x19.00
PNP_5	Base AA width(n+tap) in Nwell	fix	2.00
PNP_6	Contact space in Base Area	min	0.40
PNP_7	AA enclosure of Contact(Emitter side) in Base Area	fix	1.00
PNP_8	AA enclosure of Contact(Collector side) in Base Area	fix	0.60
PNP_9	NW enclosure of AA	fix	2.00
PNP_10	NCH & ESD enclosure of AA(Emitter side) in Base Area	fix	1.00
PNP_11	NCH & ESD enclosure of AA(Collector side) in Base Area	fix	1.00
PNP_12	space NCH & ESD to AA(ptap)	fix	2.00
PNP_13	space Nwell to AA(ptap)	fix	1.00
PNP_14	Collector AA width(p+tap) in Pwell/Psub	fix	2.00
PNP_15	Contact space in Collector Area	min	0.40
PNP_16	AA enclosure of Contact(Outer) in Collector Area	fix	0.80
PNP_17	AA enclosure of Contact(Inner) in Collector Area	fix	0.80
PNP_18	Collector Area Size	fix	25.00x25.00
PNP_19	space Emitter AA(p+) to Base AA(n+)	fix	3.00

＊Place the ZB layer in the PNP recognition part (Flush with the outer edge of the collector area (AA)). 【Please refer to the next page.】

＊Base / Collector must be wired as diode.（Can not be used as transistor）.

PNP・・・ vertical PNP (P+/NW/Psub)



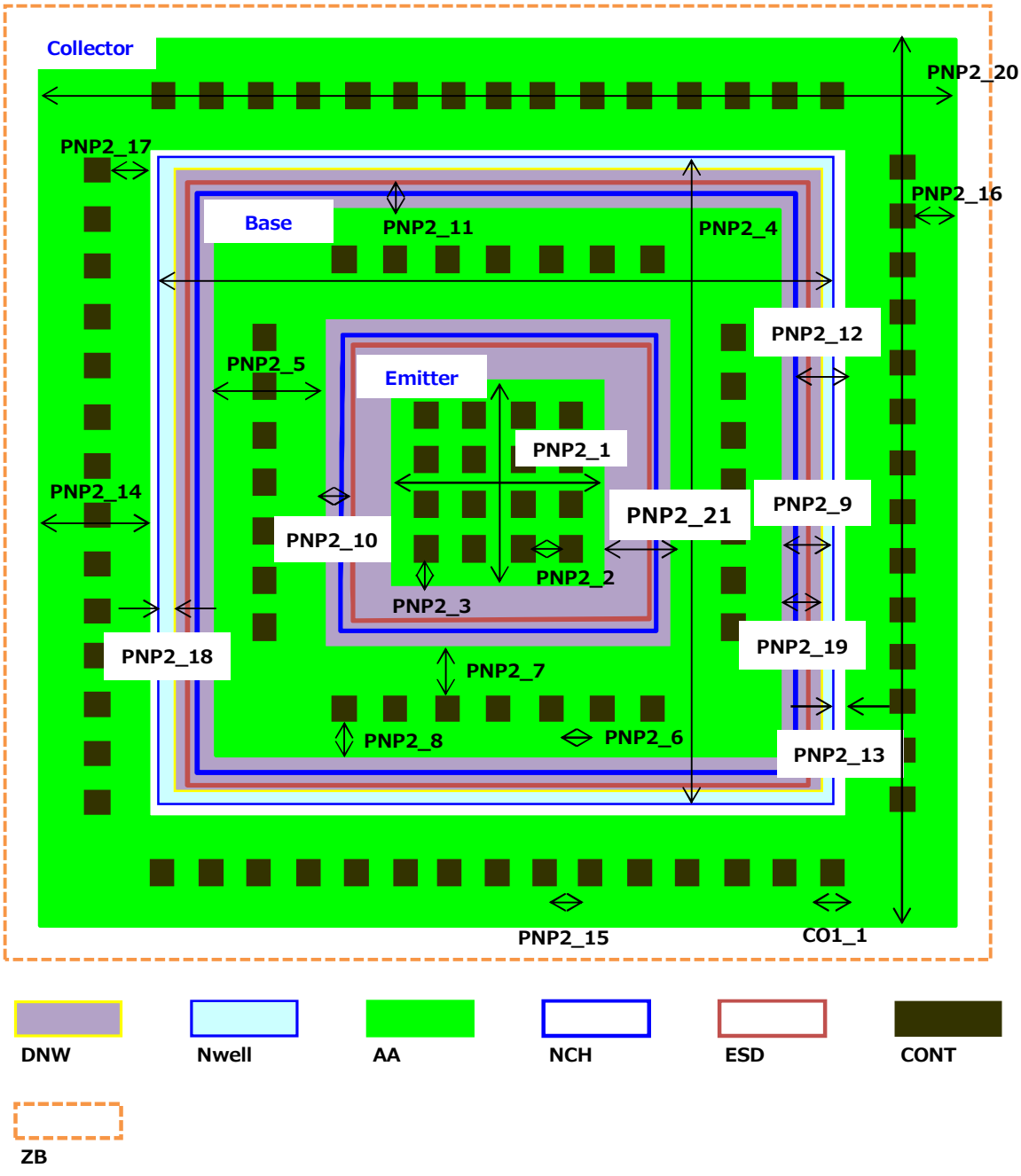
3.34 PNP2・・・ vertical PNP (P+/NW+DNW/Psub)

Rule No.	Description	class	Layout Rule (um)
CO1	standard CONT size1	fix	0.40x0.40
PNP2_1	Emitter Area Size	fix	5.00x5.00
PNP2_2	Contact space in Emitter Area	fix	0.60
PNP2_3	AA enclosure of Contact in Emitter Area	fix	0.80
PNP2_4	Base Area Size	fix	19.00x19.00
PNP2_5	Base AA width(n+tap) in Nwell	fix	2.00
PNP2_6	Contact space in Base Area	min	0.40
PNP2_7	AA enclosure of Contact(Emitter side) in Base Area	fix	1.00
PNP2_8	AA enclosure of Contact(Collector side) in Base Area	fix	0.60
PNP2_9	NW enclosure of AA	fix	2.00
PNP2_10	NCH & ESD enclosure of AA(Emitter side) in Base Area	fix	1.00
PNP2_11	NCH & ESD enclosure of AA(Collector side) in Base Area	fix	1.00
PNP2_12	space NCH & ESD to AA(ptap)	fix	2.00
PNP2_13	space Nwell to AA(ptap)	fix	1.00
PNP2_14	Collector AA width(p+tap) in Pwell/Psub	fix	2.00
PNP2_15	Contact space in Collector Area	min	0.40
PNP2_16	AA enclosure of Contact(Outer) in Collector Area	fix	0.80
PNP2_17	AA enclosure of Contact(Inner) in Collector Area	fix	0.80
PNP2_18	NW enclosure of DNW	fix	2.00
PNP2_19	AA enclosure of DNW	fix	0.00
PNP2_20	Collector Area Size	fix	25.00x25.00
PNP2_21	space Emitter AA(p+) to Base AA(n+)	fix	3.00

＊Place the ZB layer in the PNP recognition part (Flush with the outer edge of the collector area (AA)). 【Please refer to the next page.】

＊Base / Collector must be wired as diode.（Can not be used as transistor）.

PNP2・・・ vertical PNP (P+/NW+DNW/Psub)



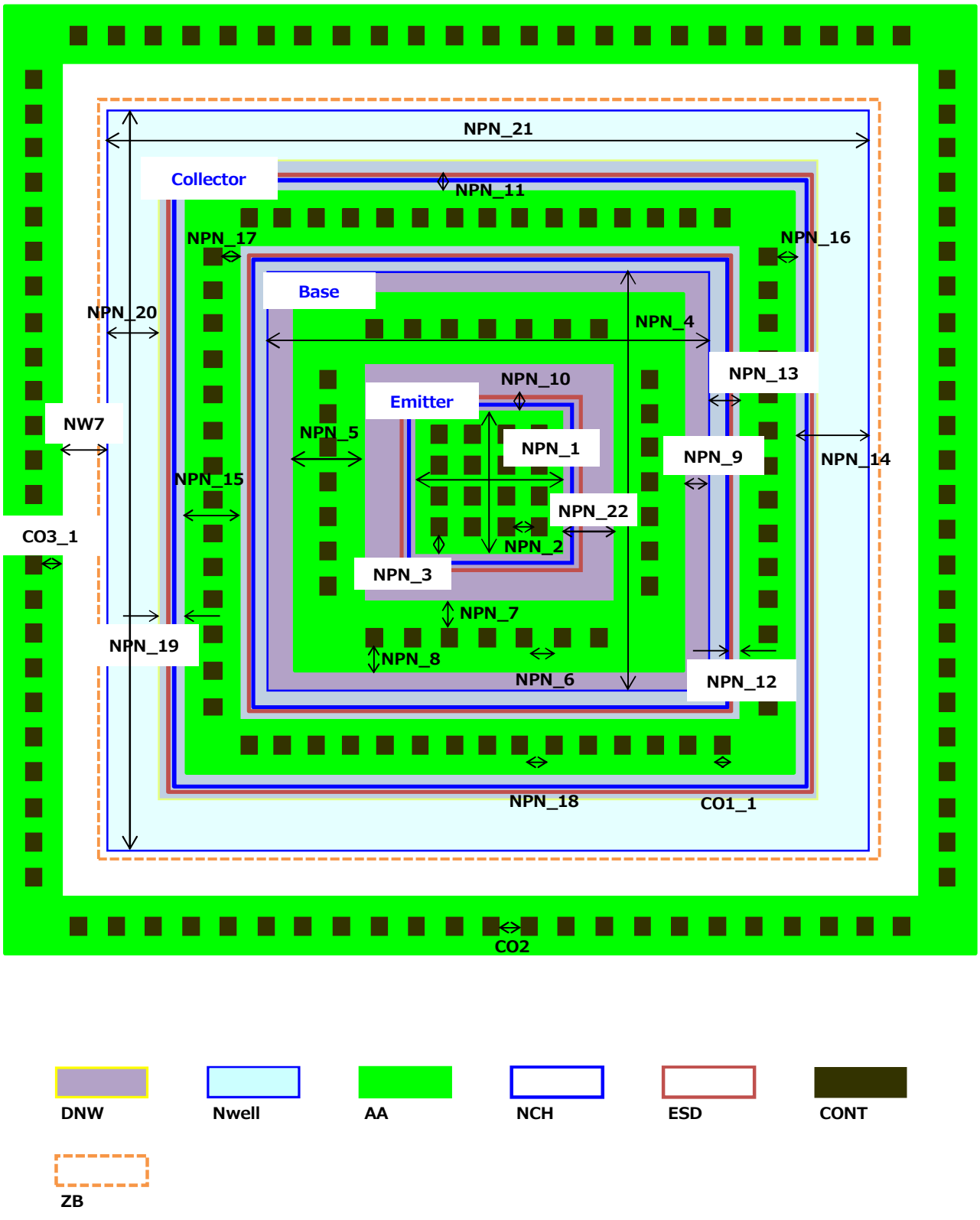
3.35 NPN・・・ vertical NPN (N+/PW/DNW)

Rule No.	Description		class	Layout Rule (um)
CO1	standard CONT size1		fix	0.40x0.40
NPN_1	Emitter Area Size		fix	5.00x5.00
NPN_2	Contact space in Emitter Area		fix	0.60
NPN_3	AA enclosure of Contact in Emitter Area		fix	0.80
NPN_4	Base Area Size		fix	19.00x19.00
NPN_5	Base AA width(p+tap) in Pwell		fix	2.00
NPN_6	Contact space in Base Area		min	0.40
NPN_7	AA enclosure of Contact(Emitter side) in Base Area		fix	1.00
NPN_8	AA enclosure of Contact(Collector side) in Base Area		fix	0.60
NPN_9	space AA(p+tap) to Nwell		fix	2.00
NPN_10	NCH & ESD enclosure of AA in Emitter Area		fix	1.00
NPN_11	NCH & ESD enclosure of AA(outside) in Collector Area		fix	1.00
NPN_12	NCH & ESD enclosure of AA(Base side) in Collector Area		fix	1.00
NPN_13	NW enclosure of AA(n+tap) *Base side		fix	1.00
NPN_14	NW enclosure of AA(n+tap) *Outside		fix	2.00
NPN_15	Collector AA width(n+tap) in Nwell		fix	2.00
NPN_16	AA enclosure of Contact(Outer) in Collector Area		fix	0.80
NPN_17	AA enclosure of Contact(Inner) in Collector Area		fix	0.80
NPN_18	Contact space in Collector Area		min	0.40
NPN_19	DNW enclosure of Collector AA		fix	0.50
NPN_20	NW enclosure of DNW		fix	1.50
NPN_21	Collector Area Size		fix	29.00x29.00
NPN_22	space Emitter AA(n+) to Base AA(p+)		fix	3.00
NW7	NWELL spacing to AA(p+tap)		min	0.45
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15

＊Place the ZB layer in the NPN recognition part (Flush with the outer edge of the Collector area (NW)).【Please refer to the next page.】

＊Base / Collector must be wired as diode.（Can not be used as transistor）.

NPN･･･ vertical NPN (N+/PW/DNW)

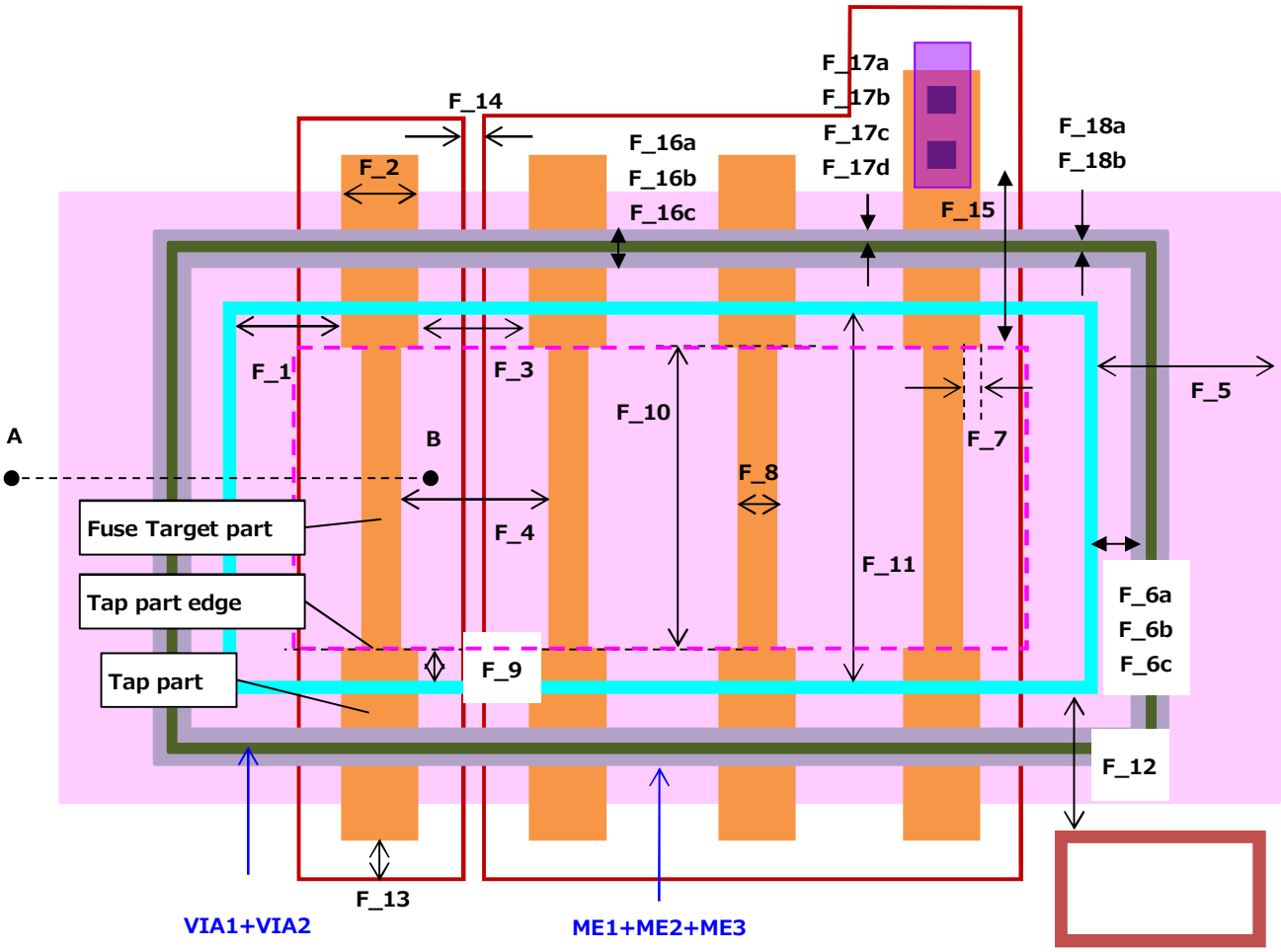


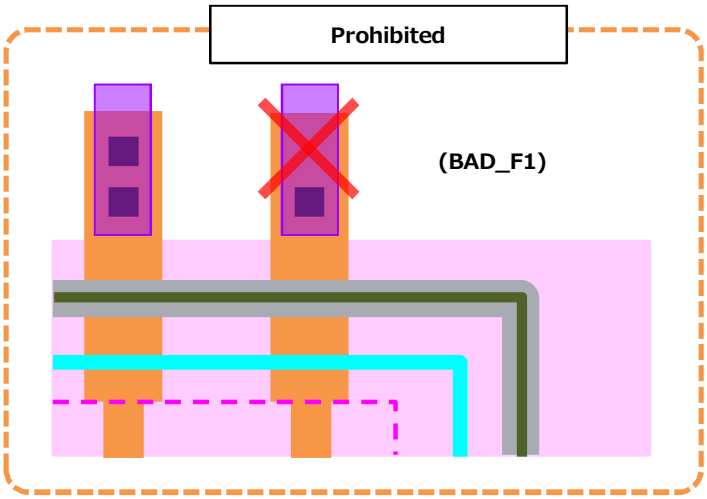
3.36 RFS・・・ Poly-Si Laser Trimming Fuse　　* T-cell is NOT supported for this device.

Rule No.	Description	class	Layout Rule (um)
F_1	space FUSE to Fuse Poly	min	4.00
F_2	Fuse Poly Width	fix	2.00
F_3	space Fuse Poly to Fuse Poly @Tap part	min	2.80
F_4	@Fuse Target part	min	3.20
F_5	PI overlap to FUSE	min	4.00
F_6a	space FUSE to Fuse Guardring 1Metal	fix	3.00
F_6b	space FUSE to Fuse Guardring 2Metal	fix	3.00
F_6c	space FUSE to Fuse Guardring 3Metal	fix	3.00
F_7	Fuse Target part extended into Fuse Tap part	fix	0.20
F_8	Fuse Target part Poly width	fix	1.60
F_9	FUSE overlap to Fuse Poly Tap part	fix	1.00
F_10	the narrow part length of Fuse Poly	fix	6.00
F_11	FUSE opening size	fix	8.00
F_12	space FUSE to Pad	min	34.00
F_13	NOIMP overlap to POLY	min	1.00
F_14	space NOIMP to NOIMP	min	2.00 or Merge
F_15	space Fuse Tap to CONT	fix	6.40
F_16a	Fuse Guardring 1Metal width	fix	1.50
F_16b	Fuse Guardring 2Metal width	fix	1.50
F_16c	Fuse Guardring 3Metal width	fix	1.50
F_17a	Fuse Guardring 1Metal overlap to VIA1	fix	0.52
F_17b	Fuse Guardring 2Metal overlap to VIA1	fix	0.52
F_17c	Fuse Guardring 2Metal overlap to VIA2	fix	0.50
F_17d	Fuse Guardring 3Metal overlap to VIA2	fix	0.50
F_18a	Fuse Guardring VIA1 width	fix	0.46
F_18b	Fuse Guardring VIA2 width	fix	0.50
BAD_F1	Single CONT is prohibited between Fuse Tap and 1METAL.		

＊The FUSE part should be covered with ZR layer, but the length direction should be flushed with the TAP edge.【Please refer to the figure below.】

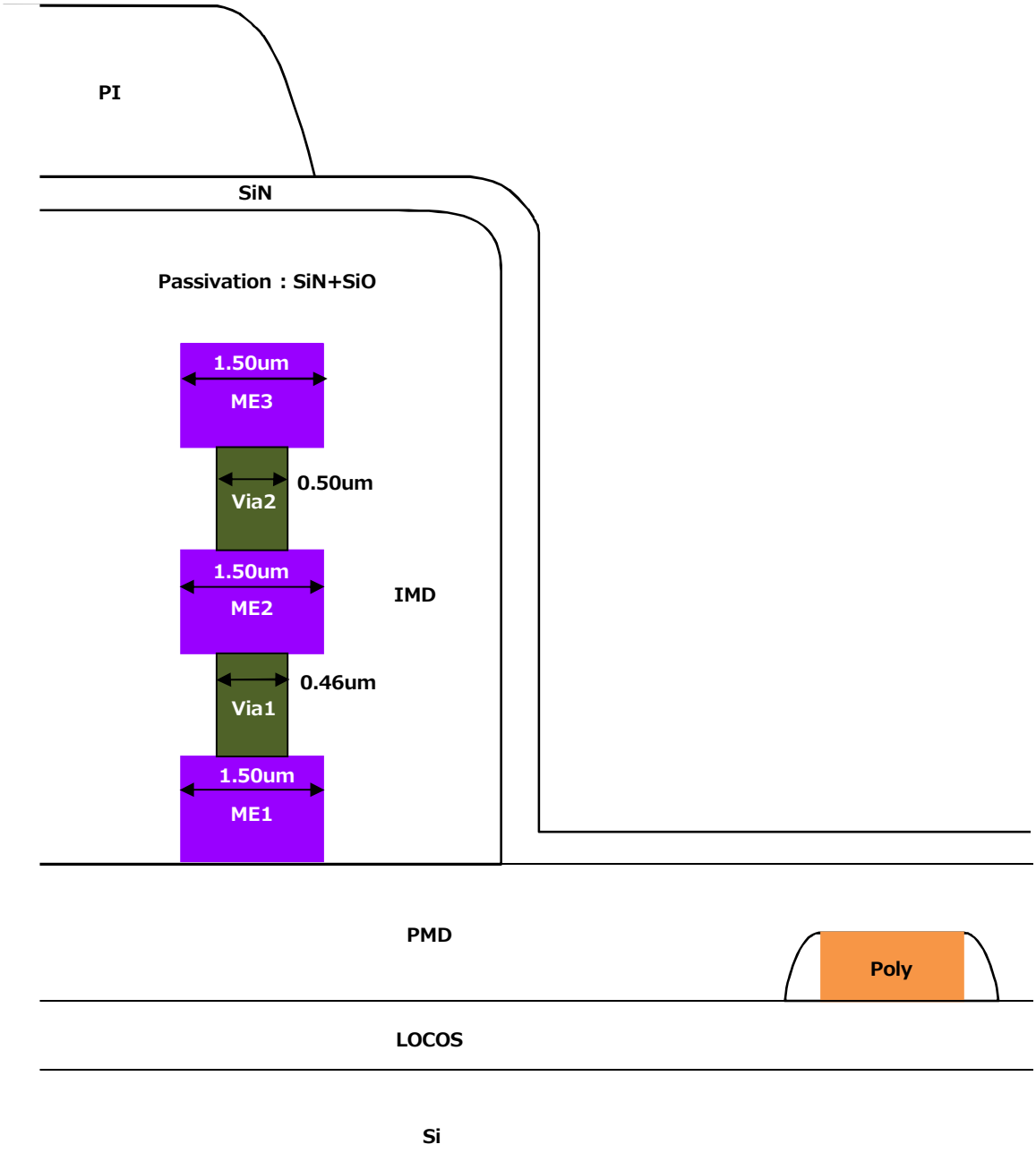
RFS・・・ Poly-Si Laser Trimming Fuse





Poly CONT ME1 FUSE PAD PI NOIMP ZR

Poly-Si Laser Trimming Fuse ・・・ Cross Section （A-B）

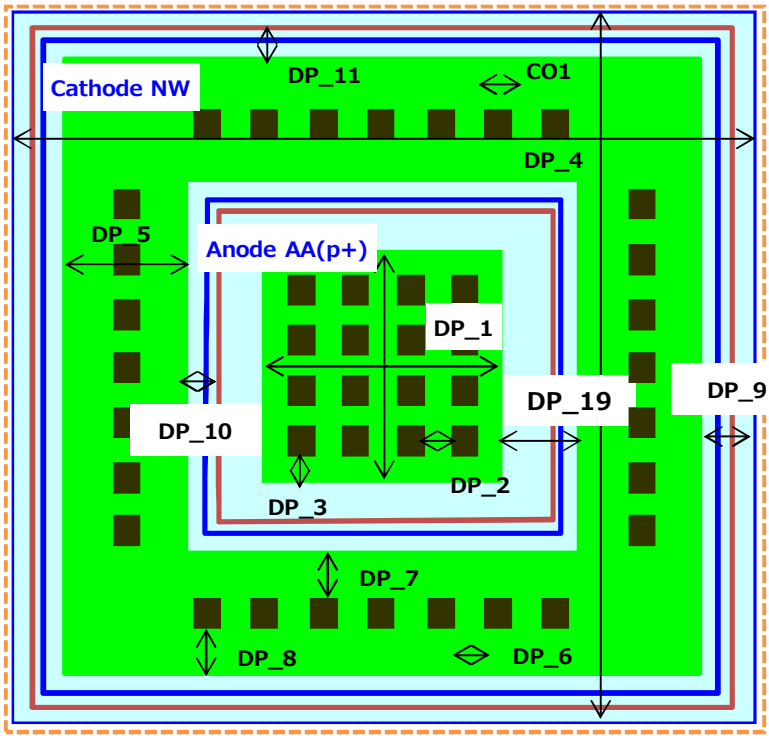


3.37 DP・・・ P+/Nwell Diode

Rule No.	Description	class	Layout Rule (um)
CO1	standard CONT size1	fix	0.40x0.40
DP_1	Anode AA(p+) Area Size	fix	5.00x5.00
DP_2	Contact space in Anode AA(p+) Area	fix	0.60
DP_3	AA enclosure of Contact in Anode AA(p+) Area	fix	0.80
DP_4	Cathode NW Area Size	fix	19.00x19.00
DP_5	Cathode AA width(n+tap) in Nwell	fix	2.40
DP_6	Contact space in Cathode AA(n+tap) Area	min	0.40
DP_7	AA enclosure of Contact(Inner side) in Cathode AA(n+tap) Area	fix	1.00
DP_8	AA enclosure of Contact(Outer side) in Cathode AA(n+tap) Area	fix	1.00
DP_9	NW enclosure of AA	fix	1.60
DP_10	NCH & ESD enclosure of AA(Inner side) in Cathode AA(n+tap) Area	fix	1.00
DP_11	NCH & ESD enclosure of AA(Outer side) in Cathode AA(n+tap) Area	fix	1.00
DP_19	space Anode AA(p+) to Cathode AA(n+tap)	fix	3.00

＊Place the ZD layer in the DP recognition part (Flush with the outer edge of the Cathode area (NW)). 【Please refer to the next page.】

DP・・・ P+/Nwell Diode

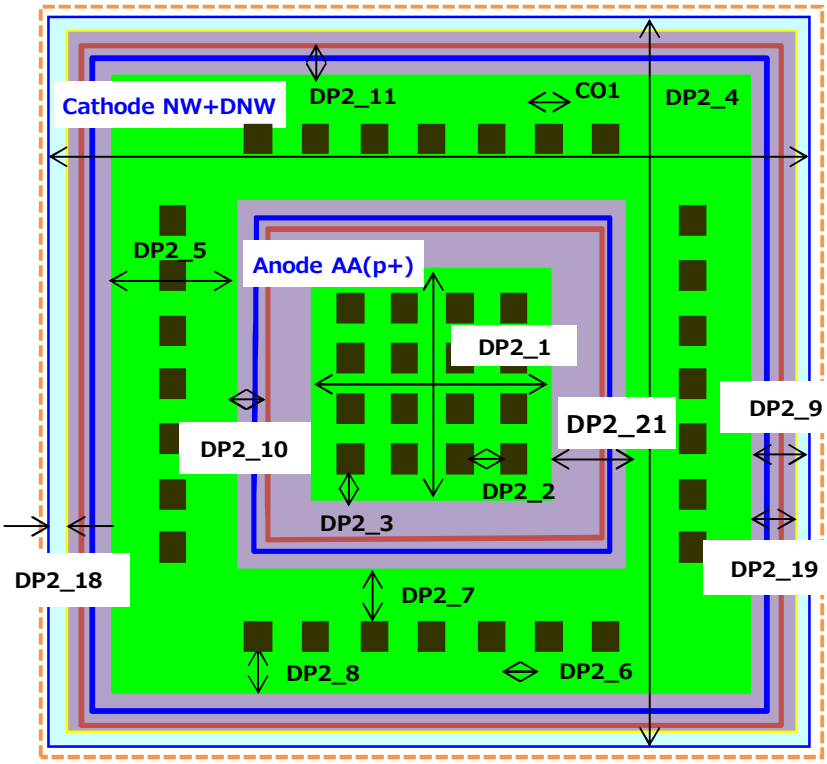


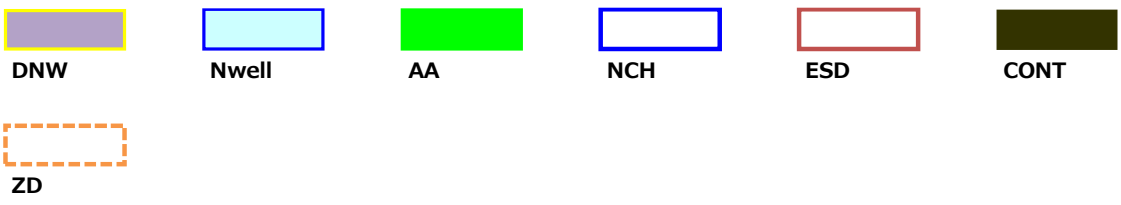
3.38 DP2・・・ P+/Nwell in Niso Diode

Rule No.	Description	class	Layout Rule (um)
CO1	standard CONT size1	fix	0.40x0.40
DP2_1	Anode AA(p+) Area Size	fix	5.00x5.00
DP2_2	Contact space in Anode AA(p+) Area	fix	0.60
DP2_3	AA enclosure of Contact in Anode AA(p+) Area	fix	0.80
DP2_4	Cathode NW Area Size	fix	19.00x19.00
DP2_5	Cathode AA width(n+tap) in Nwell	fix	2.40
DP2_6	Contact space in Cathode AA(n+tap) Area	min	0.40
DP2_7	AA enclosure of Contact(Inner side) in Cathode AA(n+tap) Area	fix	1.00
DP2_8	AA enclosure of Contact(Outer side) in Cathode AA(n+tap) Area	fix	1.00
DP2_9	NW enclosure of AA	fix	1.60
DP2_10	NCH & ESD enclosure of AA(Inner side) in Cathode AA(n+tap) Area	fix	1.00
DP2_11	NCH & ESD enclosure of AA(Outer side) in Cathode AA(n+tap) Area	fix	1.00
DP2_18	NW enclosure of DNW	fix	1.60
DP2_19	Cathode AA(n+tap) enclosure of DNW	fix	0.00
DP2_21	space Anode AA(p+) to Cathode AA(n+tap)	fix	3.00

＊Place the ZD layer in the DP2 recognition part (Flush with the outer edge of the Cathode area (NW)). 【Please refer to the next page.】

DP2・・・ P+/Nwell in Niso Diode



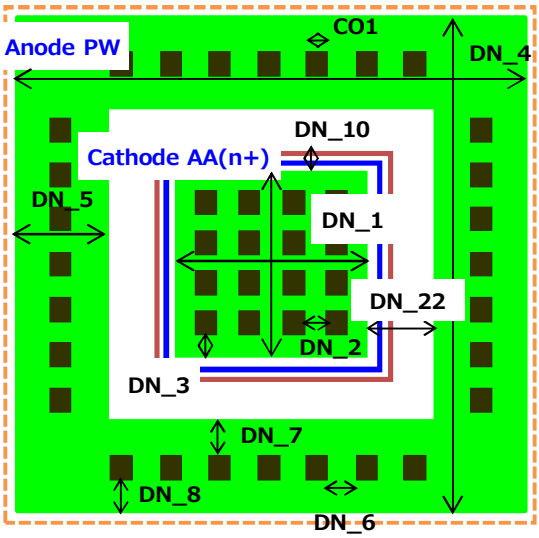


3.39 DN・・・ N+/Pwell Diode

Rule No.	Description	class	Layout Rule (um)
CO1	standard CONT size1	fix	0.40x0.40
DN_1	Cathode AA(n+) Area Size	fix	5.00x5.00
DN_2	Contact space in Cathode AA(n+) Area	fix	0.60
DN_3	AA enclosure of Contact in Cathode AA(n+) Area	fix	0.80
DN_4	Anode AA(p+tap) Area Size	fix	15.80x15.80
DN_5	Anode AA width(p+tap) in Pwell	fix	2.40
DN_6	Contact space in Anode AA(p+tap) Area	min	0.40
DN_7	AA enclosure of Contact(Inner side) in Anode AA(p+tap) Area	fix	1.00
DN_8	AA enclosure of Contact(Outer side) in Anode AA(p+tap) Area	fix	1.00
DN_10	NCH & ESD enclosure of AA in Cathode AA(n+) Area	fix	1.00
DN_22	space Cathode AA(n+) to Anode AA(p+tap)	fix	3.00

＊Place the ZD layer in the DN recognition part (Flush with the outer edge of the Anode area (AA)).【Please refer to the next page.】

DN・・・ N+/Pwell Diode

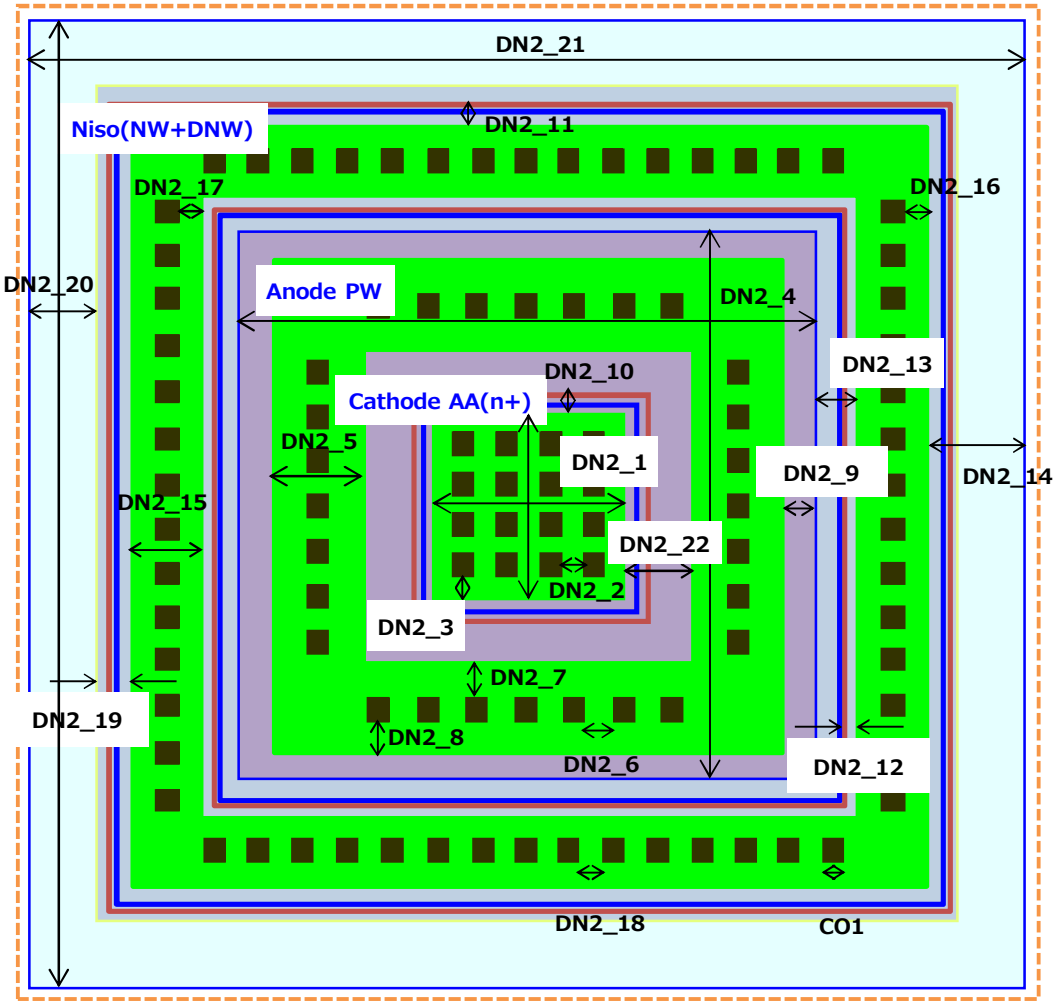


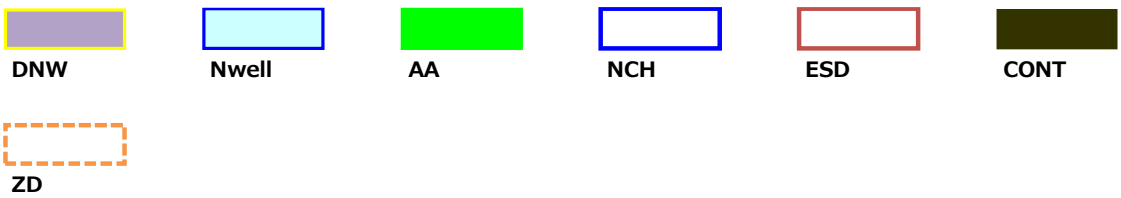
3.40 DN2・・・ N+/Pwell in Niso Diode

Rule No.	Description	class	Layout Rule (um)
CO1	standard CONT size1	fix	0.40x0.40
DN2_1	Cathode AA(n+) Area Size	fix	5.00x5.00
DN2_2	Contact space in Cathode AA(n+) Area	fix	0.60
DN2_3	AA enclosure of Contact in Cathode AA(n+) Area	fix	0.80
DN2_4	Anode PW Area Size	fix	19.00x19.00
DN2_5	Anode AA width(p+tap) in Pwell	fix	2.40
DN2_6	Contact space in Anode AA(p+tap) Area	min	0.40
DN2_7	AA enclosure of Contact(Inner side) in Anode AA(p+tap) Area	fix	1.00
DN2_8	AA enclosure of Contact(Outer side) in Anode AA(p+tap) Area	fix	1.00
DN2_9	space AA(p+tap) to Nwell	fix	1.60
DN2_10	NCH & ESD enclosure of AA in Cathode AA(n+) Area	fix	1.00
DN2_11	NCH & ESD enclosure of AA(Outer side) in Niso Area	fix	1.00
DN2_12	NCH & ESD enclosure of AA(Inner side) in Niso Area	fix	1.00
DN2_13	NW enclosure of AA(n+tap) *Inner side	fix	1.00
DN2_14	NW enclosure of AA(n+tap) *Outer side	fix	2.00
DN2_15	Niso AA width(n+tap) in Nwell	fix	2.00
DN2_16	AA enclosure of Contact(Outer side) in Niso Area	fix	0.80
DN2_17	AA enclosure of Contact(Inner side) in Niso Area	fix	0.80
DN2_18	Contact space in Niso Area	min	0.40
DN2_19	DNW enclosure of Niso AA	fix	0.50
DN2_20	NW enclosure of DNW	fix	1.50
DN2_21	Niso Area Size	fix	29.00x29.00
DN2_22	space Cathode AA(n+) to Anode AA(p+tap)	fix	3.00

＊Place the ZD layer in the DN2 recognition part (Flush with the outer edge of the Niso area (NW)).【Please refer to the next page.】

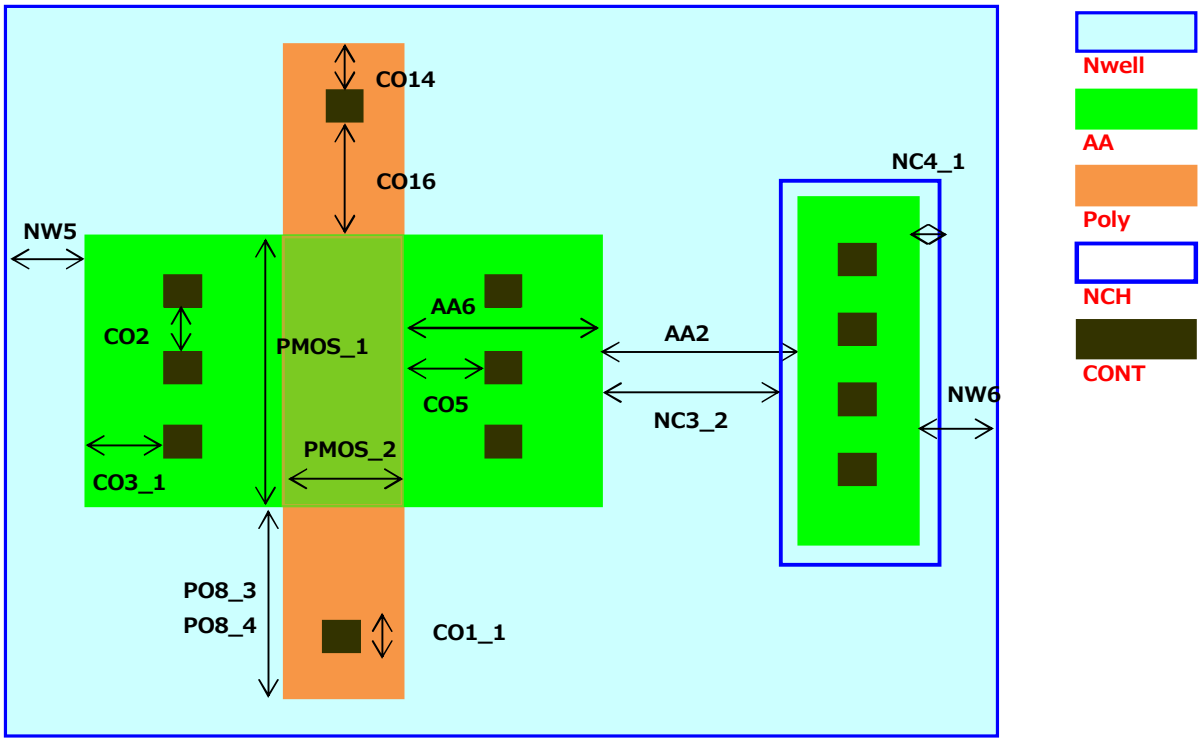
DN2・・・ N+/Pwell in Niso Diode





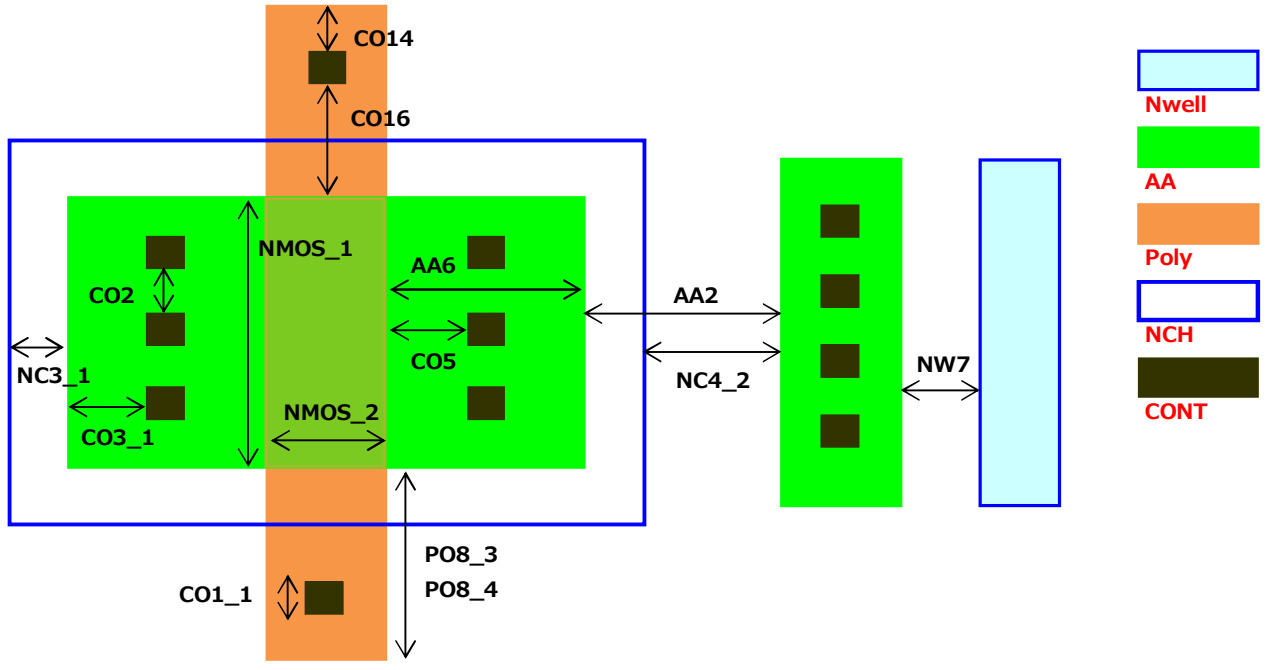
3.41 P··· 3.3V Pch MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
PMOS_1	Transistor Width		min	0.60
PMOS_2	Transistor Length		min	0.39
NW5	NWELL enclosure of AA(p+)		min	1.00
NW6	NWELL enclosure of AA(n+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.55
AA2_2		same node @ L≧7.0um	min	0.55
AA2_3		@ L<7.0um	min	0.45
AA6	AA extension beyond gate		min	0.63
PO8_1	POLY extension beyond AA	@ POLY width<0.5, AA-POLY space<0.44	min	0.76
PO8_2		@ POLY width<0.5, 0.44≦AA-POLY space	min	0.40
PO8_3		@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_2	NCH spacing to AA(p+) in NWELL		min	0.30
NC4_1	NCH extension beyond AA(n+tap) in NWELL		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



3.42 N··· 3.3V Nch MOS Transistor（N+Polycide gate）

Rule No.	Description		class	Layout Rule (um)
NMOS_1	Transistor Width		min	0.50
NMOS_2	Transistor Length		min	0.39
NW7	NWELL spacing to AA(p+tap)		min	0.45
AA2_1	AA(p+) spacing to AA(n+)	different node	min	0.55
AA2_2		same node @ L≧7.0um	min	0.55
AA2_3		@ L<7.0um	min	0.45
AA6	AA extension beyond gate		min	0.63
PO8_1	POLY extension beyond AA	@ POLY width<0.5, AA-POLY space<0.44	min	0.76
PO8_2		@ POLY width<0.5, 0.44≦AA-POLY space	min	0.40
PO8_3		@ 0.5um=<POLY width<1.2um	min	0.38
PO8_4		@ POLY width>=1.2um	min	0.33
NC3_1	NCH extension beyond AA(n+) in pwell		min	0.30
NC4_2	NCH spacing to AA(p+tap) in pwell		min	0.15
CO1	standard CONT size1		fix	0.40x0.40
	standard CONT size2 (Allowed on AA, L>0.40um)		min	0.40xL(rectangle)
CO2	CONT spacing		min	0.40
CO3_1	AA enclosure of CONT	CONT size=0.40x0.40	min	0.15
CO3_2		CONT size=0.40xL (rectangle)	min	0.30
CO5_1	CONT spacing to POLY	CONT size=0.40x0.40	min	0.27
CO5_2		CONT size=0.40xL (rectangle)	min	0.42
CO14	POLY enclosure of CONT		min	0.20
CO16	CONT spacing to AA		min	0.29



4. Antenna Rule

Gate oxide may be damaged by plasma discharge in wafer manufacturing process.
Antenna rules must be applied for poly and metal to prevent the above damage.

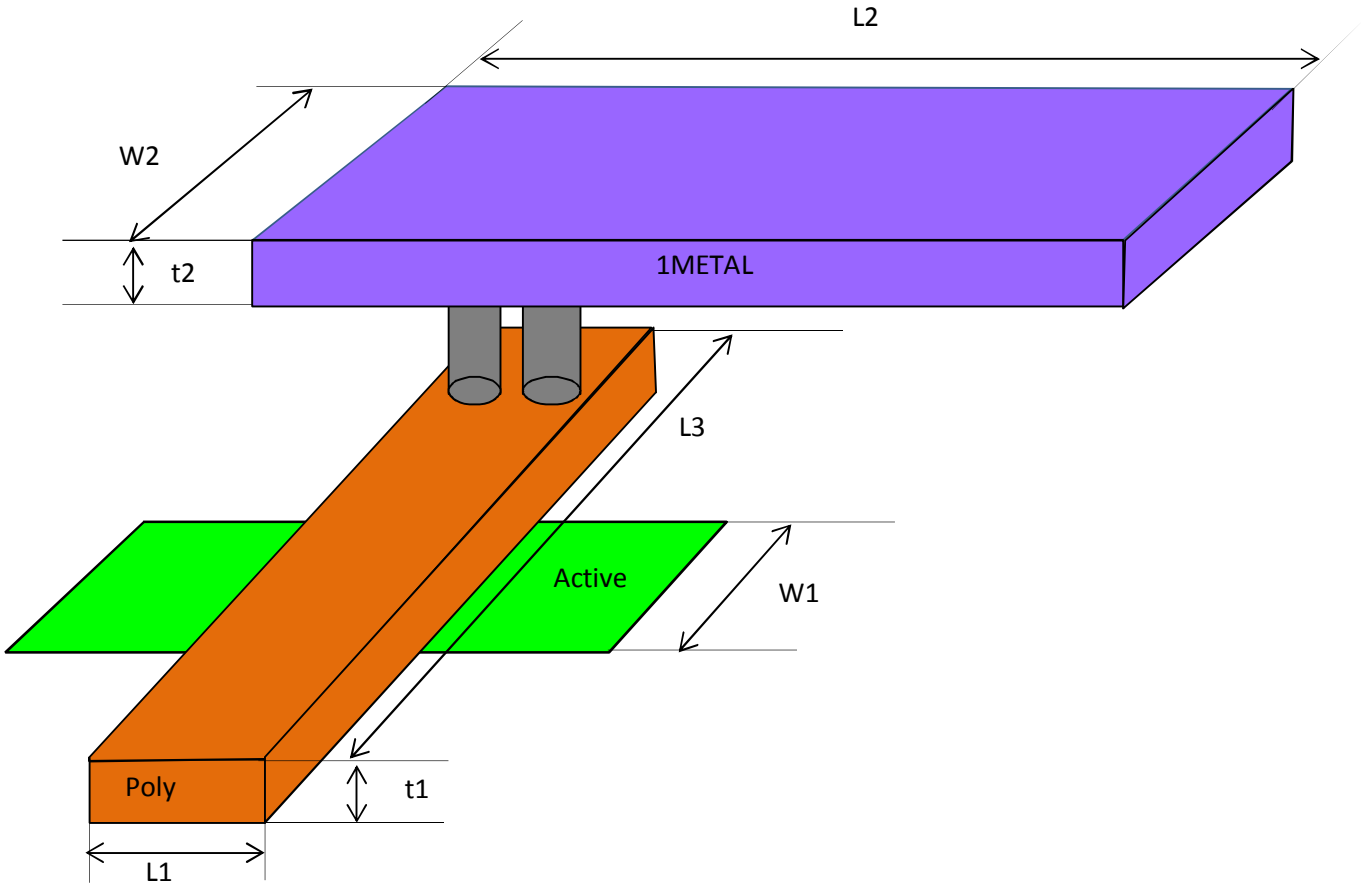
Rule No.	Description	class	Layout Rule (-)
AN-1	Maximum ratio of poly perimeter area to active gate area	max	200
AN-2	Maximum ratio of 1METAL perimeter area to active gate area	max	400
AN-3	Maximum ratio of 2METAL perimeter area to active gate area	max	400
AN-4	Maximum ratio of 3METAL perimeter area to active gate area	max	400

The definition of antenna ratio is expressed the following formula,

For poly Ratio = poly perimeter(*sidewall*) area / active gate area
= 2 x (L1 + L3) x t1 / (W1 x L1)

For metal Ratio = metal perimeter*(sidewall)* area / active gate area
= 2 x (L2+W2) x t2 / (W1 x L1)

L1 : connected transistor channel length
W1 : connected transistor channel width
t1 : poly thickness *t1 =0.34um
L2 : floating METAL length connected to gate
W2 : floating METAL width connected to gate
t2 : metal thickness *t2 =0.57um(1METAL), 0.59um(2METAL), 0.86um(3METAL)
L3 : Gate poly length



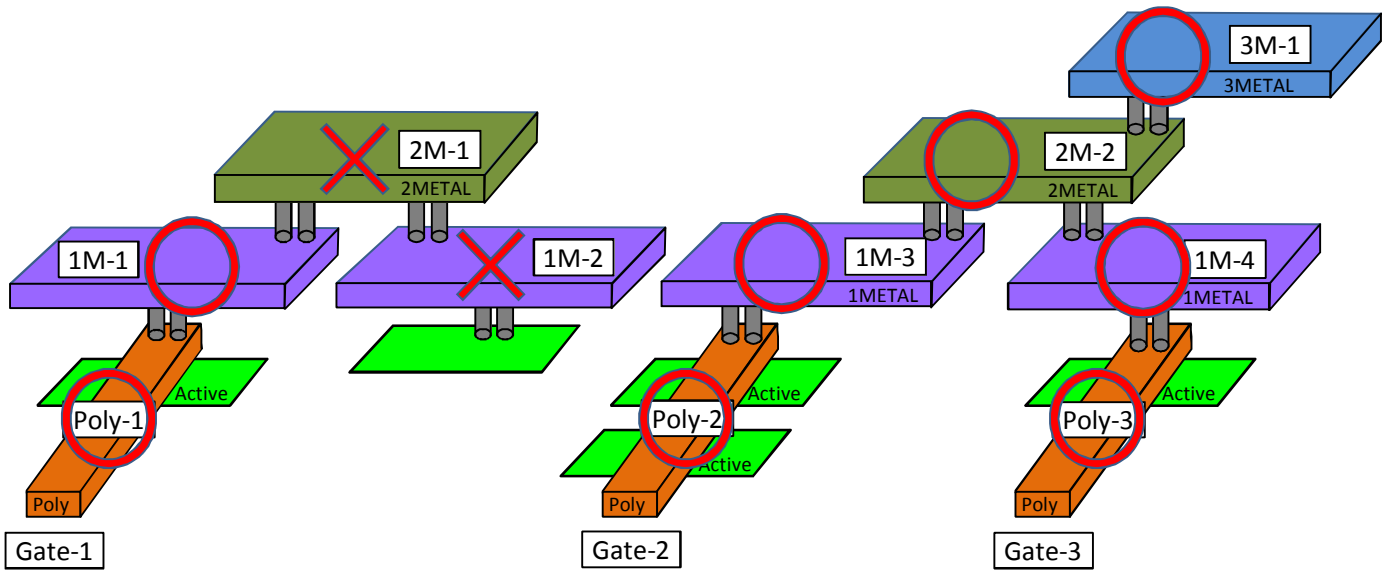
4. Antenna Rule ~ continued ~

Floating POLY / METAL connected to GATE is subject to the rule.
Antenna ratio is calculated for each layer.
Gate_area as the sum of the Gate area connected.

For poly	Ratio = poly perimeter(sidewall) area / active gate area
For 1METAL	Ratio = 1METAL perimeter(sidewall) area / active gate area
For 2METAL	Ratio = 2METAL perimeter(sidewall) area / active gate area
For 3METAL	Ratio = 3METAL perimeter(sidewall) area / active gate area

【Example below】

Gate-1	target Routing->	Poly-1, 1M-1
Gate-2	target Routing->	Poly-2, 1M-3, 2M-2, 3M-1
Gate-3	target Routing->	Poly-3, 1M-4, 2M-2, 3M-1
1M-1	target Gate->	Gate-1
1M-2	target Gate->	none
1M-3	target Gate->	Gate-2
1M-4	target Gate->	Gate-3
2M-1	target Gate->	none
2M-2	target Gate->	Gate-2 + Gate-3
3M-1	target Gate->	Gate-2 + Gate-3



5. Maximum Current Density Rule (Electromigration Rule)

Maximum current density (Jmax) with temperature rating is shown in the table below.

<Jmax for various temperature>

*Life time > 10years for 0.01% cumulative failure

*Current acceleration factor; n=-2

Layer	Hole Size (um)	Ea (eV)	Jmax				unit
			85℃	105℃	125℃	150℃	
1METAL	-	0.6	5.0	3.0	1.9	1.1	[mA/um]
2METAL	-	0.6	5.0	3.0	1.9	1.1	[mA/um]
3METAL	-	0.6	6.9	4.1	2.6	1.5	[mA/um]
CONT	0.40	1.0	3.1	1.3	0.6	0.25	[mA/hole]
1VIA	0.46	1.0	2.6	1.1	0.51	0.21	[mA/hole]
2VIA	0.50	1.0	3.1	1.3	0.61	0.25	[mA/hole]

6. Character Rule

Creating characters such as product type names in the chip, please follow the rules below.

6.1 Drawing Layers

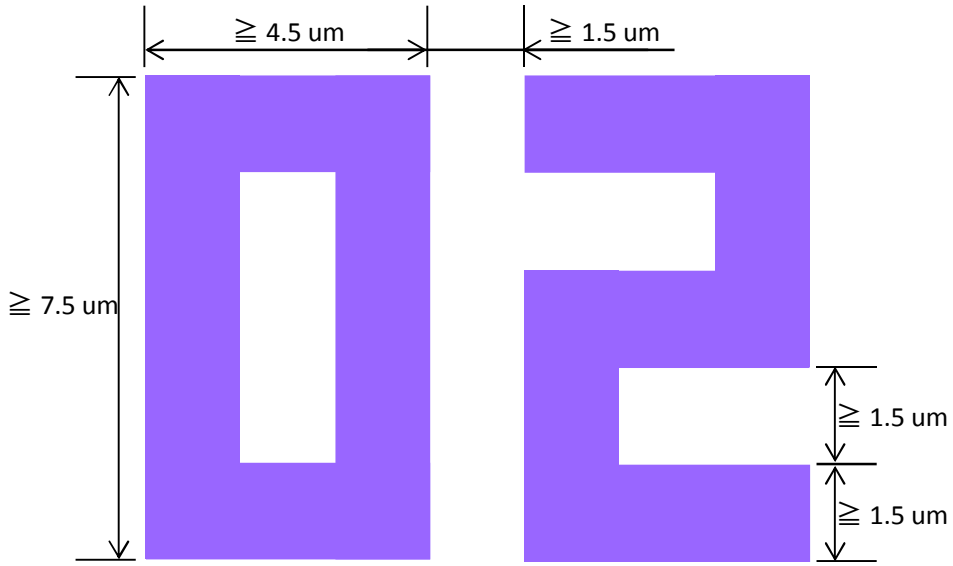
・Basically, please draw with AA layer or METAL layers.
・Drawing with PAD / FUSE / PI layer is prohibited.

6.2 Drawing Rules

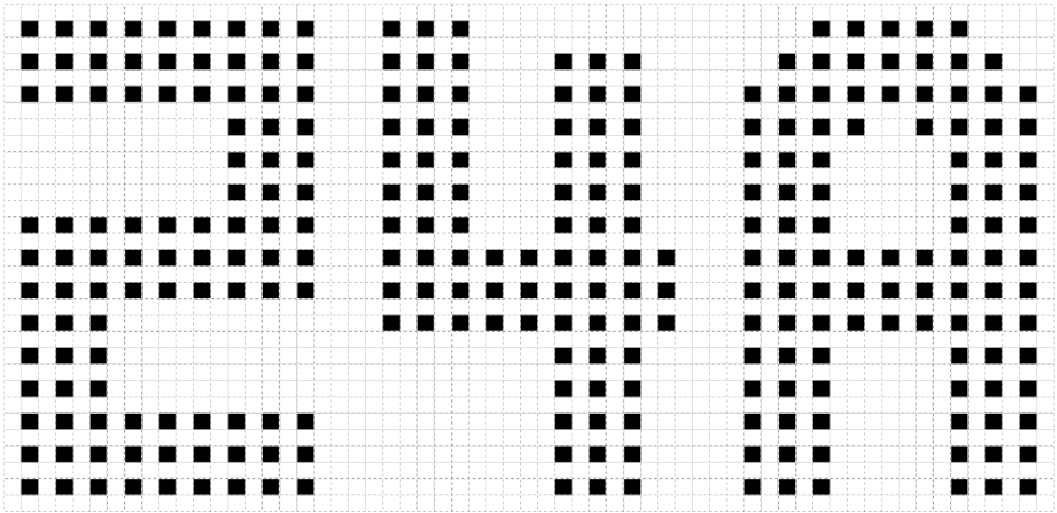
・Please observe Layer Rules for both minimum width and minimum spacing.
・Diagonal 45 degree pattern is acceptable. However, sharp patterns are prohibited.
・Font size shown in 6.3_Drawing_Example is the smallest size.

6.3 Drawing Example

・AA, 1METAL, 2METAL, 3METAL



・CONT, 1VIA, 2VIA



制定日 ver.0.0	2017.02.07

保管先	技術1課

Approval	Check	Issue
技術グループ 2017/07/04 栗原	PDK 29/07/04 喜多川	PDKﾌﾟﾛｼﾞｪｸﾄ '17.07.04 大川

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
0.0	2017/2/7	Originated from merging Document "PK35BT_LayoutRules_v006_161220.docx" and "PK35_DeviceRule_p05.xlsx".	Kitagawa
1.0	2017/4/18	Contents Add 1.5 Definition of the Layout Geometry Add Device CDN,CDNI,CPL2, CPL2I Change contents order 1 Layer information Change Layer Name order and some description Change Design Grid of PAD,FUSE,PI in 1.1 Correct 1.4 Device to Layer Mapping Matrix Add 1.5 Definition of the Layout Geometry 2. Layer Rules, 3. Device Rules Implemented overall review , Change description of geometry according to 1.5, other description, and rules. Add diagrams for all rules Complete 2.22 Seal-Ring Structure and related definition	Ohkawa Mitsuzono Kitagawa
1.1	2017/7/4	cover Assign management number Header, Footer Correction 1.1 Midium → Medium Typo correction 1.3 300ohm/s → 330ohm/s Error correction AA add "AA11" and "AA12" rule POLY add "BAD_POLY2" rule 2METAL(2) Illustration correction 2METAL(3) sheet addition (Illustration correction for merge of CRP)	Ohkawa (Nakajima) Kitagawa kurihara

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.1	2017/7/4	Metal Slit 880um → 800um Error correction Metal Slit(diagram) sheet addition（Add application examples） PI PI2 20.00 → 20.00 or Merge correction PI3 min → fix correction RPM, RPH Add a hand-drawn notice on the 1METAL cover NPN,PNP,PNP2 Add the notice of Base / Collector connection (Only use diode) Poly FUSE Fixed how to cover ZR recognition layer * The contents of following page were translated into English. + cover (p.0) + 1.2 Mask specifications (p.4) + 2.14 2METAL (p.23,24,25) + Wide Metal (p.28,29) + Metal Slit (p.30,31) + PAD (p.32) + RPL (p.62) + RPM (p.63) + RPH (p.64) + RNW (p.66) + RN (p.67) + RP (p.68) + CPIP (p.69) + CND (p.70) + CNDI (p.71) + CPL2 (p.72) + CPL2I (p.73) + PNP (p.74) + PNP2 (p.76) + NPN (p.78) + Poly FUSE (p.80,81) + 4. revision history (p.84) * Add "3.24 Ladder Poly-Si_Resistor" page.(p.65) * The color of characters changed to the black. *Correction of MNE and MNEI + contents (p.2) + 1.3 Device Description (p.5) + 1.4 Device to Layer Mapping Matrix (p.6) + 3.14 MNE_LC/MNE_PC (p.49) + 3.20 MNEI_LC/MNEI_PC (p.60,61)	Ohkawa (Nakajima) Kitagawa kurihara

7. Revision History

Rev.	Date	Description of change		Issue Check Approval
1.2	2017/7/21	contents	add "2.23 chip area"	Ohkawa
		contents(2)	add "4. Antenna Rule"	
		DNW	add "PMOS" and "NMOS" to figure	PDKプロジェクト '17.07.21 大川
		RX	RX2 RX spacing → same RX spacing 0.80 or abutted → 0.80 correction	
		NOIMP	NO1 0.76 → 0.80 correction	
			NO2 0.76 → 0.80 correction	
		ESD	ESD1 0.76 → 0.80 correction	
			ESD2 0.76 → 0.80 correction	Kitagawa
		1VIA	add "VI6" rule	
		2VIA	add "SV5" rule	
		PAD	delete "P_14" rule	PDK pj 29/07/21 喜多川
			add "P_19" and "P_20" rule	
			add "BAD_PAD2" and "BAD_PAD3" rule	
			add "Anything(※) definition	
			Illustration correction.	
			(extended PAD metals to Seal-Ring edge)	kurihara
			(PAD_Metal area,METAL routing)	
		Sealring	Add a hand-drawn notice of Seal-Ring	
			Add a notice of SRING layer	技術グループ 2017/07/21 栗原
			Add Rule_No. SR1,SR2,,,SR20 and SR21	
		chip area	add "2.23 chip area" page	
		all MOS	insert "AA2_2" rule	
		Iso_PMOS	add "DNW enclosure of AA" rule	
		Iso_NMOS	insert "NW8" rule	
		RNW	add "BAD_RNW1" and "BAD_RNW2" rule	
		RN	add "NC3_1" and "BAD_RN1" rule	
		RP	add "BAD_RP1" rule	
		PNP	PNP_16 0.85 → 0.80, PNP_17 0.75 → 0.80	
		PNP(diagram)	delete corner Cont at guard ring	
		PNP2	PNP2_16 0.85 → 0.80, PNP2_17 0.75 → 0.80	
		PNP2(diagram)	delete corner Cont at guard ring	
		NPN	NPN_16 0.85 → 0.80, NPN_17 0.75 → 0.80	
			insert "NW7","CO2" and "CO3_1" rule	
		NPN(diagram)	add Sub_Tap	
			Illustration correction. (Sub_Tap)	
			delete corner Cont at guard ring	
		Poly_FUSE	add "BAD_F1" rule	
			Illustration correction. (ZR,BAD_F1)	
		4.antenna	add "4. Antenna Rule" page	
		5.revision history	Change chapter.4 → chaper.5	

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.3	2017/8/17	All pages　Change format of header 名称 → Document name 管理番号 → Document number 版 → Rev. 頁 → Page 5.revision history(4) Page addition. (total pages 87 → 88)	Ohkawa PDKプロジェクト '17.08.17 大川 Kitagawa PDK pj 29/08/17 喜多川 kurihara 技術グループ 2017/08/17 栗原
1.4	2017/12/11	cover　Total Page 88 → 92 (add "4.Antenna Rule continued" Page.85) (add "5.Maximum Current Density Rule" Page.86) (add "6.Character Rule" Page.87) (add "7.Revision History" Page.92) Contents　add "5.Maximum Current Density Rule" add "6.Character Rule" 5.Revision History → 7.Revision History 1.1 Layer definitions PAD Design Grid 0.05 → 0.005 correction FUSE Design Grid 0.05 → 0.005 correction PI Design Grid 0.05 → 0.005 correction Seal_ring identification for DRC exception → Seal_ring identification for Extraction RX　RX3_a,RX3_b,RX4　add "for RPL,RPM,RPH" RX5　add "for RPL,RPM,RPH,PiP" Delete "RX6" rule add "RX7" rule Illustration correction. (delete "RX6","NOIMP") (add "RX7","POLY")	Ohkawa PDKプロジェクト '17.12.11 大川 Kitagawa PDK pj 29/12/13 喜多川 kurihara 技術グループ 2017/12/13 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.4		NOIMP Illustration correction. (add "NO13" on CRP width direction) POLY(gate_interconnect) Change specification of dogbone_rule 2METAL delete "SM2_2" rule Illustration correction. (delete example of Dogbone_rule) Wide Metal "Caution 1" → 【Metal routing containing oblique line】 (change Description and Illustration) PAD P_13 53.00 → 65.00 correction Illustration correction. (End point of arrow P_13 from SealringEdge to ScribelineEdge) Chip area add ＊Place the WAKU layer in the Chip area .. Illustration correction.(add "WAKU") MPMI,MPLI,MPL2I,MPNI DNW_enclosure_of_AA 1.00 → 0.35 correction RPL,RPM,RPH delete Width_max rule delete "RX6" rule Illustration correction. (delete "RX6") (add "NO13" for width side) ("RPL_1" → "RPL_1a") ("RPM_1" → "RPM_1a") ("RPH_1" → "RPH_1a") RNW,RN,RP delete Width_max rule Illustration correction. ("RNW_1" → "RNW_1a") ("RN_1" → "RN_1a") ("RP_1" → "RP_1a") 4.antenna poy → poly Typo correction W1 → L3 Error correction foating → floating Typo correction add "L3 : Gate poly length" Illustration correction. (add "L3") 4.antenna ~ continued ~ (Page.85) sheet addition 5. Maximum Current Density Rule (Page.86) sheet addition 6. Character Rule (Page.87) sheet addition 7.revision history (Page.92) sheet addition	Ohkawa PDKプロジェクト '17. 12. 11 大川 Kitagawa PDK pj 29/12/13 喜多川 kurihara 技術グループ 2017/12/13 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.5	2018/1/12	cover Total Page 92 → 93 (add "7.revision_history(6)" Page.93) RX RX3_a "for RPL,RPM,RPH" → "for RPL" RX3_b "for RPL,RPM,RPH" → "for RPM,RPH" RX5,RX7 2.00 → 3.50 correction POLY(PIP upper plate) delete "PO15","PO16","PO17" rule add "PO18" rule Illustration correction. (delete "PO15","PO16","PO17") (add "PO18") ESD delete "ESD3" rule Illustration correction. (delete "ESD3") 2METAL SM2_3 "width>20um" → "width>5um" Wide Metal "(W is 20μm for 2M..)" → "(W is 5μm for 2M..)" Metal slit (Page.30) , Metal slit diagram (Page.31) "area Re" → "region Re" correction RPL,RPM,RPH Illustration correction. (changed width "NO13">"RX3" to "NO13"<"RX3") RPL RX3_a "for RPL,RPM,RPH" → "for RPL" RPM RPMT_3 add "for RPM, RPH" RX3_b "for RPL,RPM,RPH" → "for RPM,RPH" RPH RPHT_3 add "for RPM, RPH" RX3_b "for RPL,RPM,RPH" → "for RPM,RPH" 7.revision history（Page.93） sheet addition	Ohkawa PDKﾌﾟﾛｼﾞｪｸﾄ '18.01.12 大川 Kitagawa PDK pj 2018/1/12 喜多川 kurihara 技術グループ 2018/01/15 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.6	2018/2/16	cover Total Page 93 → 96 contents add "1.3 Process Mask table" 1.4、1.5、1.6 change chapter number 1.2 Mask Specifications "NCH""PCH Memo correction 1.3 Process Mask table sheet addition 1.4、1.5、1.6 change chapter number AA AA4 0.69 → 0.60 correction AA5 0.69 → 0.60 correction VIMP VIMP3 VIMP enclosure of "AA" → "gate" VIMP4 add "(excluding Tap AA)" Illustration correction. NOIMP NO14 0.76 → "0.76 or butting" correction POLY(PIP upper plate) PO12 0.93 → 0.60 correction NCH NC9、NC10、BAD_NC1 add "in AA" CONT CO18 0.29 → 0.25 correction CO22 0.38 → 0.25 correction 1METAL add "A wide 1METAL definition is referred to 2.17 Wide Metal Definition" 1VIA VI2_2 on Wide 1METAL > 5um : min 0.40 → on Wide 1METAL > 5um : min 0.20 → on Wide 1METAL >10um : min 0.40 BAD_1V2 add "(1VIA spacing to the nearest 1VIA must be within 10 um)" add "A wide 1METAL definition is referred to 2.17 Wide Metal Definition" Illustration correction. 2METAL "*A wide 2METAL definition is same as TM2_3 definition." → "A wide 2METAL definition is referred to 2.17 Wide Metal Definition" 2VIA SV1 0.51x0.51 → 0.50x0.50 correction SV2 0.54 → 0.50 correction SV3_1 0.22 → 0.20 correction SV3_2 on Wide 2METAL > 5um : min 0.42 → on Wide 2METAL > 5um : min 0.20 → on Wide 2METAL >10um : min 0.42 BAD_2V2 add "(2VIA spacing to the nearest 2VIA must be within 10 um)" add "A wide 2METAL definition is referred to 2.17 Wide Metal Definition" Illustration correction.	Ohkawa PDKプロジェクト '18. 02. 16 大川 Kitagawa PDK pj 2018/2/16 喜多川 kurihara 技術グループ 2018/02/16 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.6	2018/2/16	3METAL TM2_1 0.60 → 0.55 correction TM2_3 either/both 5um<3METAL width<15um : min 0.90 → delete either/both 15um≦3METAL : min 2.00 → either/both 10um<3METAL : min 1.00 add "A wide 3METAL definition is referred to 2.17 Wide Metal Definition" Wide Metal change the definition of wide METAL. Sealring SR8 0.99 → 1.00 correction SR9 0.51 → 0.50 correction PolyFUSE F1 5.00 → 4.00 correction F5 4.71 → 4.00 correction F_6a 3.005 → 3.00 correction F_6b delete "3Metal" add "F_6c" rule F_12 35.00 → 34.00 correction F_16b delete "3Metal" 1.51 → 1.50 correction add "F_16c" rule F_17b 0.525 → 0.52 correction F_17c delete "3Metal" add "F_17d" rule F_18b 0.51 → 0.50 correction PolyFUSE(2) Illustration correction. (add "F_6c","F_16c","F_17d") PolyFUSE(crosssection) Illustration correction. (ME2:1.51 → 1.50, Via2:0.51 → 0.50, ME3:1.51 → 1.50)) 5.Current Density 2VIA Hole size and Jmax correction 7.revision history(7) sheet addition 7.revision history(8) sheet addition	Ohkawa PDKプロジェクト '18.02.16 大川 Kitagawa PDK pj 2018/2/16 喜多川 kurihara 技術グループ 2018/02/16 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.7	2018/3/15	cover Total Page 96 → 105 contents(2) add "3.37 DP" "3.38 DP2" "3.39 DN" "3.40 DN2" 1.1 Layer definitions add ZD 1.4 Device Description add DP, DP2, DN, DN2 1.5 Device to Layer Mapping Matrix add DP, DP2, DN, DN2, ZD 3.37 DP, DP (diagram) sheet addition 3.38 DP2, DP2 (diagram) sheet addition 3.39 DN, DN (diagram) sheet addition 3.40 DN2, DN2 (diagram) sheet addition 7.revision history(9) sheet addition	Mitsuzono PDK pj 2018/03/16 満園 Kitagawa PDK pj 2018/3/16 喜多川 kurihara 技術グループ 2018/03/16 栗原
1.8	2018/4/20	1.1 Layer Definitions add TEXT layer 2.3 AA AA11 AA(n+) → gate correction AA12 AA(p+) → gate correction Add *Definition of gate is (POLY and AA). 2.13 1VIA VI2_2 on Wide 1METAL>10um 0.40 → 0.22 correction 2.17 Wide Metal definition ~continued~ Slit shapes of 10μm or less are virtually filled, even other metal put inside slit. ↓ When the same metal is in the slit, virtual filling of the slit is not performed. 2.20 FUSE FU2 30.00 → 8.00 correction	Ohkawa PDKプロジェクト '18.04.20 大川 Kitagawa PDK pj 2018/4/24 喜多川 kurihara 鹿児島工場 2018/04/24 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
1.9	2018/9/26	cover Total Page 105 → 106 1.1 Layer Definitions Add "ZRMET1", "ZRMET2", "ZRMET3" and "ZPSUB2" 2.4 VIMP VIMP3 gate -> gate (POLY and AA) 3.1-3, 5-7, 9-12, 14-18 and 20 VIMP3 gate -> gate (POLY and AA) Illustration correction. (Corrected VIMP3 to enclosure of gate) 7.revision history(10) sheet addition	Ohkawa PDKプロジェクト '18.09.26 大川 Kitagawa PDK pj 2018/9/27 喜多川 kurihara 鹿児島工場 2018/09/27 栗原
2.0	2019/6/7	■Upgraded Rev.1.9 to Rev.2.0 by adding 3.3V rules. cover Total Pages 106 → 113 Contents Add "2.24 GO" Contents(2) Add "3.41 P" and "3.42 N". 1.1 Layer Definitions Add "5V" to Description of PVT, PLVT, PLLVT, NVT, NLVT, NDVT and ESD. 1.1 Layer Definitions ~ continued ~ Sheet addition. Add Layer GO, NL3, NL5, PL3, RECOGR, Boundary, TEXT, MTEXT1_10, MTEXT2_10 and MTEXT3_10. 1.2 Mask Specifications Add Layer GO, NL3, NL5 and PL3. Add "5V" to Memo of PVT, PLVT, PLLVT, NVT, NLVT, NDVT and ESD. 1.3 Process Mask table Add Mask PVT3, NVT3, GOX, NLD3, NLD5 and PLD3. Add "5V" to comment of PVT, PLVT, PLLVT, NVT, NLVT, NDVT and ESD. 1.4 Device Description Add Device "P" (3.3V PMOS) and "N" (3.3V NMOS) Add "5V" to Description of all PK35 MOS transistors.	Ohkawa 技術1課 '19.05.31 大川 Kitagawa 技術1課 2019/6/3 喜多川 Takenaka 技術1課 2019/06/07 竹中 Kurihara 鹿児島工場 '19.06.07 栗原

7. Revision History

Rev.	Date	Description of change	Issue Check Approval
2.0	2019/6/7	1.5 Device to Layer Mapping Matrix Add Device "P" (3.3V PMOS) and "N" (3.3V NMOS) Add Layer "GO" 2.2 NWELL Add Rule NW4_2 and illustration. 2.3 AA Add Layout Rule of 3.3V MOS. Add Rule AA2_3 and AA10_2 to 3.3V MOS. Illustration correction. (add illustration of Rule AA2) 2.8 POLY (for polycide gate and interconnect polycide) Add Rule PO4, PO8_1 and PO8_2. 2.24 GO sheet addition. (Layer Rules and illustration) 2.24 GO ~continued~ sheet addition. (GO example of layout) 2.24 GO ~continued(2)~ sheet addition. 3.41 P sheet addition. 3.42 N sheet addition. ■Other changes 2.17 Wide Metal definition Update definition and illustration of metal routing containing oblique line. 3.15 MNMI, 3.16 MNHI, 3.17 MNLI, 3.18 MNDI, 3.19 MNNI Add Sectional view in A-A'.	Ohkawa 技術1課 '19.05.31 大川 Kitagawa 技術1課 2019/6/3 喜多川 Takenaka 技術1課 2019/06/07 竹中 Kurihara 鹿児島工場 '19.06.07 栗 原