



3. Tool 설치 및 사용

논리로 실습

부경대 컴퓨터·인공지능공학부 최필주

- Tool 설치
- ModelSim을 이용한 Simulation
- Quartus II를 이용한 FPGA 구현



Tool 설치

Tool 내려받기

- 내려받을 tool
 - ModelSim: Siemens사의 simulation 프로그램
 - Quartus II web edition: Intel altera사의 FPGA 칩 사용에 필요

Tool 내려받기

- Quartus ii로 검색

The screenshot shows a Google search interface with the query 'quartus ii'. Below the search bar are tabs for '이미지', '동영상', '13.0 sp1 download', '뉴스', '쇼핑', '도서', '지도', '항공편', and '금융'. The search results are displayed below the tabs, showing three results. The first result is from Inje University, the second is from Yonsei University, and the third is from Intel. The Intel result is highlighted with a red border.

Google

quartus ii

이미지 동영상 13.0 sp1 download 뉴스 쇼핑 도서 지도 항공편 금융

검색결과 약 2,220,000개 (0.31초)

Inje University
http://airlab.inje.ac.kr > dsmc_lab1 > Quartus_2...
<Quartus II 설치 및 사용 manual>
본 실험에서는 'ALTERA'社의 FPGA를 사용한 실험을 하게 된다. 이 소자를 사용하기 위한 Tool
이 필요하며, 여기서는 'ALTERA'社에서 제공하는 'Quartus II'를 사용할 ...
페이지 24개

Yonsei University
http://csys.yonsei.ac.kr > emhw > hw-quartus2-13
Quartus-II 13.0 사용법
Altera(현재 Intel)의 FPGA를 위한 FPGA 설계 소프트웨어. • 설계 입력: VerilogHDL, VHDL,
AHDL, 또는 schematic을 사용. • Quartus II v9 이전.
페이지 33개

Intel
https://www.intel.com > content > www > software-kit > i...
Intel® Quartus® II Web Edition Design Software Version ...
The Intel® Quartus® II Web Edition Design Software, Version 13.1 is subject to removal from
the web when support for all devices in this release are available ...

Tool 내려받기

● 클릭했을 때 나오는 화면

The screenshot shows the Intel website's download center for Quartus II. The Intel logo is on the left, followed by navigation links: PRODUCTS, SUPPORT, SOLUTIONS, DEVELOPERS, and PARTNERS. On the right, there are links for user account, language (ENGLISH), and a search bar. Below the navigation is a link to the 'FPGA Software Download Center'. The main content area has a dark blue background with the title 'Intel® Quartus® II Web Edition Design Software Version 13.1 for Windows'. Below the title is a table with three columns: ID, Date, and Version. The table contains one row with the ID '666221', the date '11/3/2013', and a dropdown menu for the version '13.1 (Latest)'.

ID	Date	Version
666221	11/3/2013	13.1 (Latest) ▼

Users should upgrade to the latest version of the Intel® Quartus® II Design Software. The selected version does not include the latest functional and security updates. If you must use this version of software, follow the [technical recommendations](#) to help improve security. For critical support requests, please contact our [support team](#).

The Intel® Quartus® II Web Edition Design Software, Version 13.1 is subject to removal from the web when support for all devices in this release are available in a newer version, or all devices supported by this version are obsolete. If you would like to receive customer notifications by e-mail, please subscribe to our [subscribe to our customer notification mailing list](#).

This archived version does not include the latest functional and security updates. For a supported version of Quartus, upgrade to the latest version. If your device family is not compatible with the latest version, contact your Intel field rep or the support team about migrating to the latest device family. See [here](#) for device family compatibility. If you must use this version of software, follow the [technical recommendations](#) to help improve security.

You may be exposed to a vulnerability issue if you have installed or plan to install Intel® Quartus® II Design Software from version 11.0 to version 18.0 to a location with space(s) in the path. See this [KDB solution](#) for more details.

To find software versions that support specific device families:

- Refer to the [Device Support List](#)
- Use the [Software Selector](#)

Tool 내려받기

- Individual Files 선택 후 software 다운로드 받기

Downloads

[Multiple Download](#)[Individual Files](#)[Additional Software](#)[DVD Files](#)[Updates](#)

Intel® Quartus® Software

ModelSim-Intel® Edition (includes Starter Edition)

Download
ModelSimSetup-13.1.0.162.exe

Size: 822.8 MB

SHA1: 061feacbbc342df28cfee8be72438720ea51b6dd

Intel® Quartus® II Software (includes Nios® II EDS)

Download
QuartusSetupWeb-13.1.0.162.exe

Size: 1.5 GB

SHA1: 58121f29614878fb81d27dec3eb914331cbaebb5

Tool 내려받기

- Individual Files 선택 후 device support 다운로드 받기

Devices

Intel® Cyclone® III, Intel® Cyclone® IV Device Support (includes all variations)

Download
cyclone_web-13.1.0.162.qdz

Size: 548.4 MB
SHA1: 83a5cc8d8d65198bb7830ed22f39cda86a709446

Intel® MAX® II, Intel® MAX® V Device Support

Download
max_web-13.1.0.162.qdz

Size: 6.1 MB
SHA1: ba90ec11ba266c67de6b931513ebe25c20b991c5

Intel® Arria® II Device Support

Download
arria_web-13.1.0.162.qdz

Size: 466.5 MB
SHA1: 15d7f4febd8e9e7f280829f67c3295d463a35638

Intel® Cyclone® V Device Support (includes all variations)

Download
cyclonev-13.1.0.162.qdz

Size: 810.4 MB
SHA1: 42effa35fed2df509420193d49a2057df65e9379

Tool 내려받기

- Software License Agreement

- Download할 때마다 나오는 페이지
- Accept 선택



Software License Agreement

Legal Disclaimer

PLEASE NOTE: This version of software ("Software") does not contain the latest functional and security updates. In order to use this version, you must first acknowledge the following term, which supplements and supersedes any inconsistent provision in the version of the Intel® FPGA Software License Subscription Agreement for the product (e.g., Intel® Quartus® Prime Software, Intel® HLS Compiler, Intel® FPGA SDK for OpenCL™, DSP Builder for Intel® FPGAs, or Advanced Link Analyzer) with which you use the Software:

Intel does not give or enter into any condition, warranty, or other term:

- i. with respect to any malfunctions or other errors in its Software caused by virus, infection, worm or similar malicious code not developed or introduced by Intel; or
- ii. to the effect that any Software will protect against all possible security threats, including intentional misconduct by third parties. Intel is not liable for any downtime or service interruption, for any lost or stolen data or systems, or for any other damages arising out of or relating to any such actions or intrusions or resulting from use of Software. Intel does not give or enter into any condition, warranty, or other term with respect to interoperability.

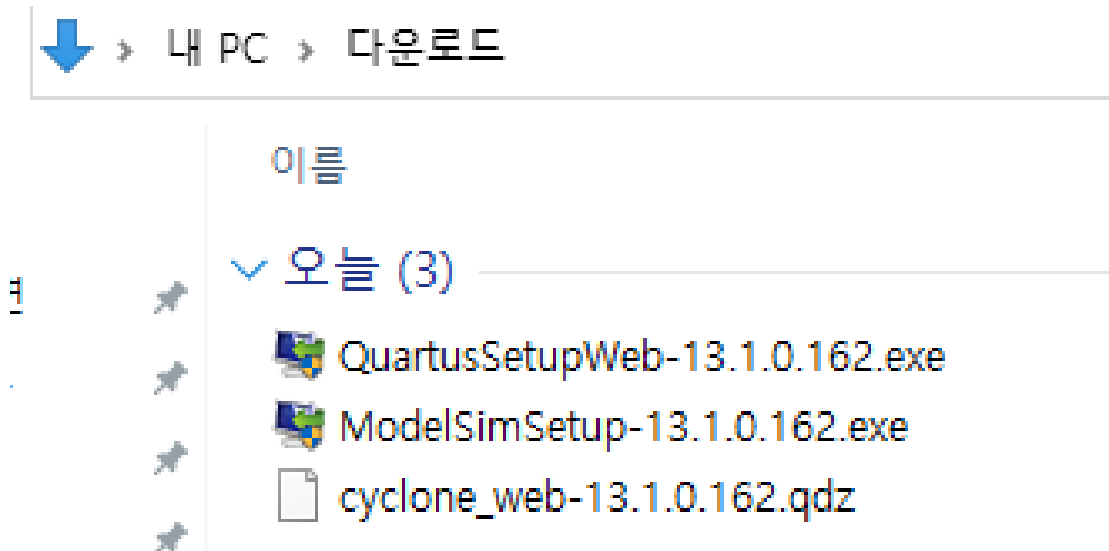
Intel does not warrant or assume responsibility for the accuracy or completeness of any information, text, graphics, links or other items within the Software. Please click "Accept" below to continue the download process.

Accept

Reject

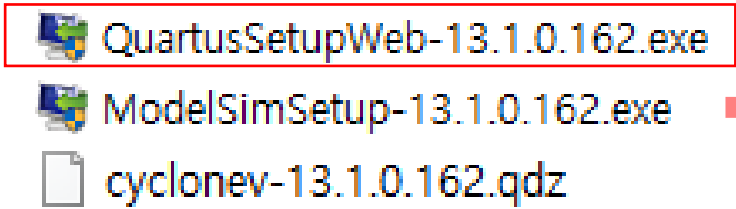
Tool 내려받기

- 내려받은 파일



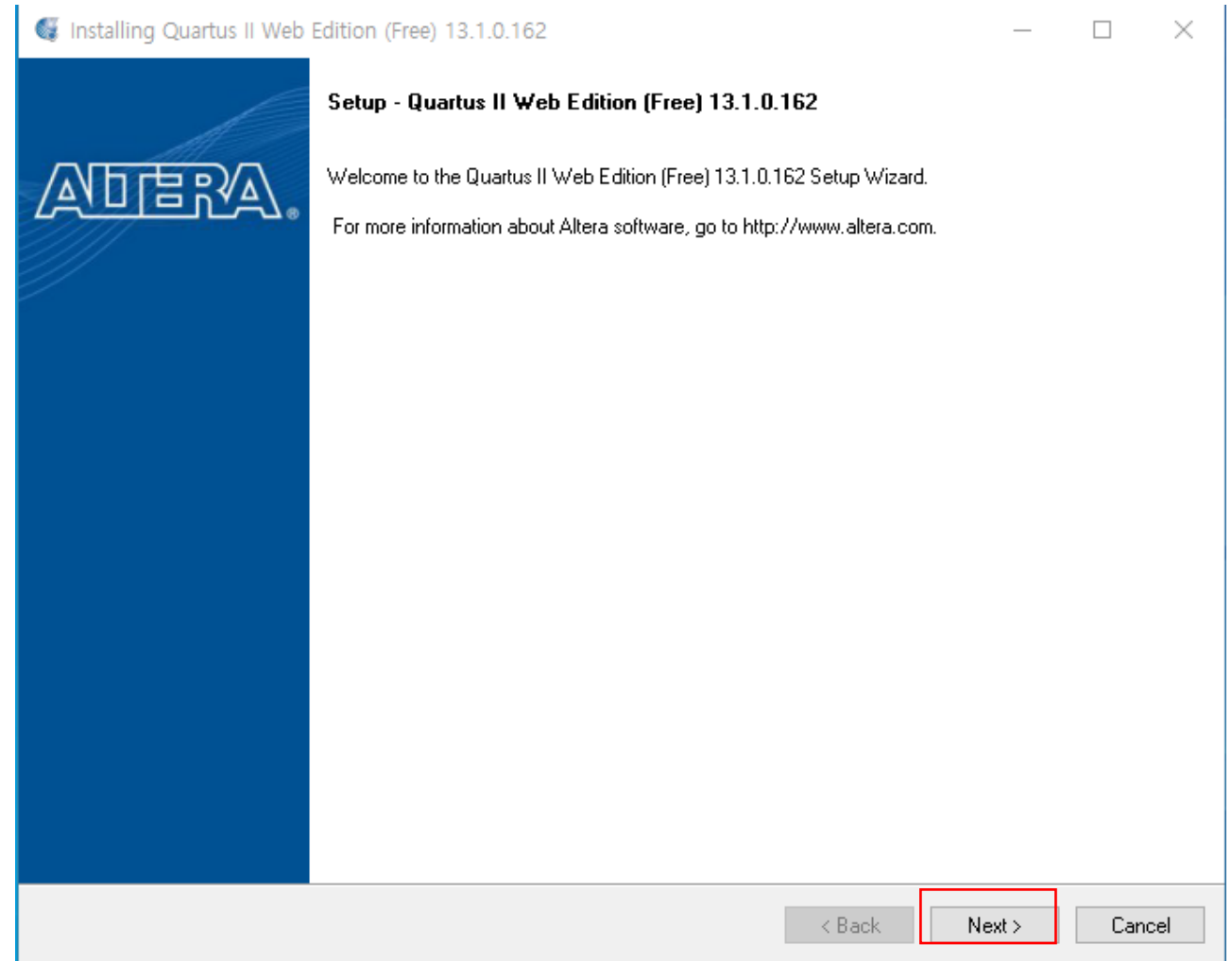
Quartus II web edition 설치

- QuartusSetup 파일 실행



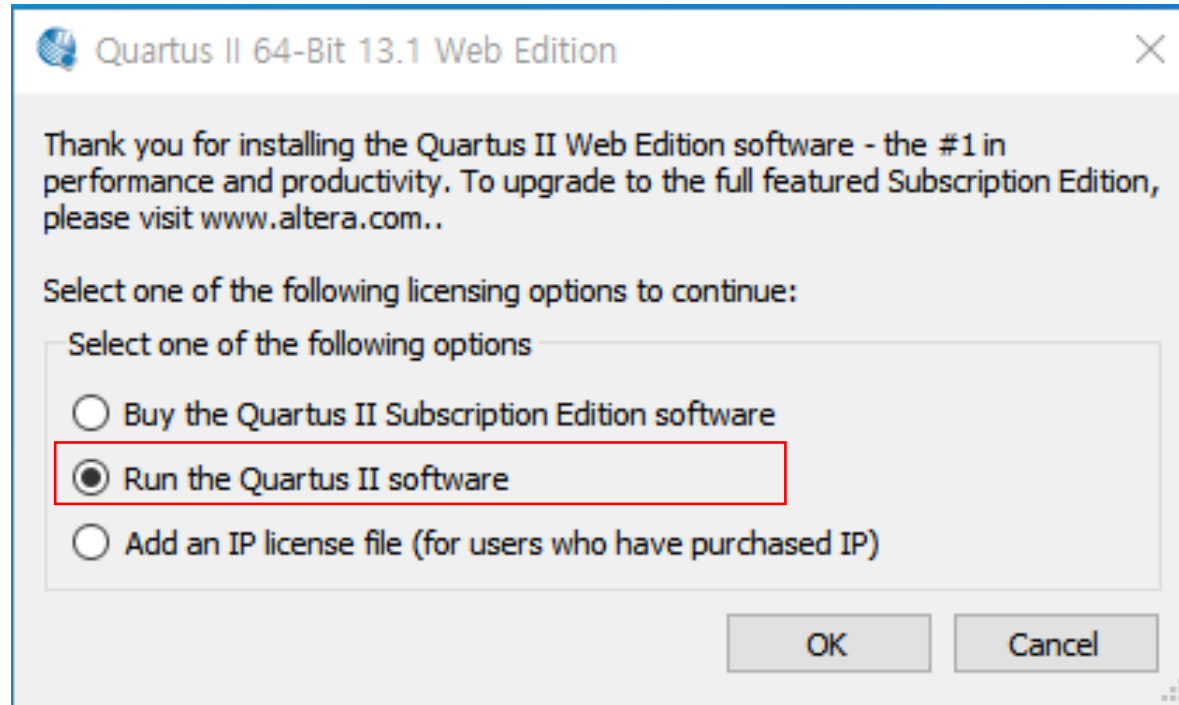
- 이후 나오는 창들

- License Agreement
 - I accept the agreement ➔ Next
- Installation directory: Next
- Select Components: Next
 - Check: Modelsim, cyclone V
- Ready to Install: Next
- 설치 완료 후: Finish



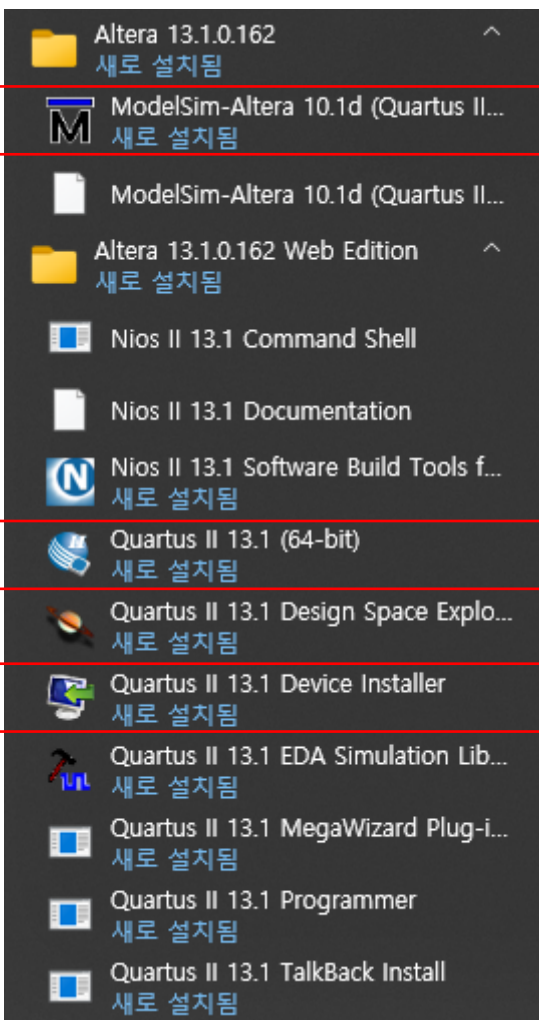
Quartus II web edition 설치

- 설치 후 나오는 창



설치 후 화면

- Window키를 눌렀을 때



ModelSim: simulation에 사용

Quartus II: FPGA 구현에 사용

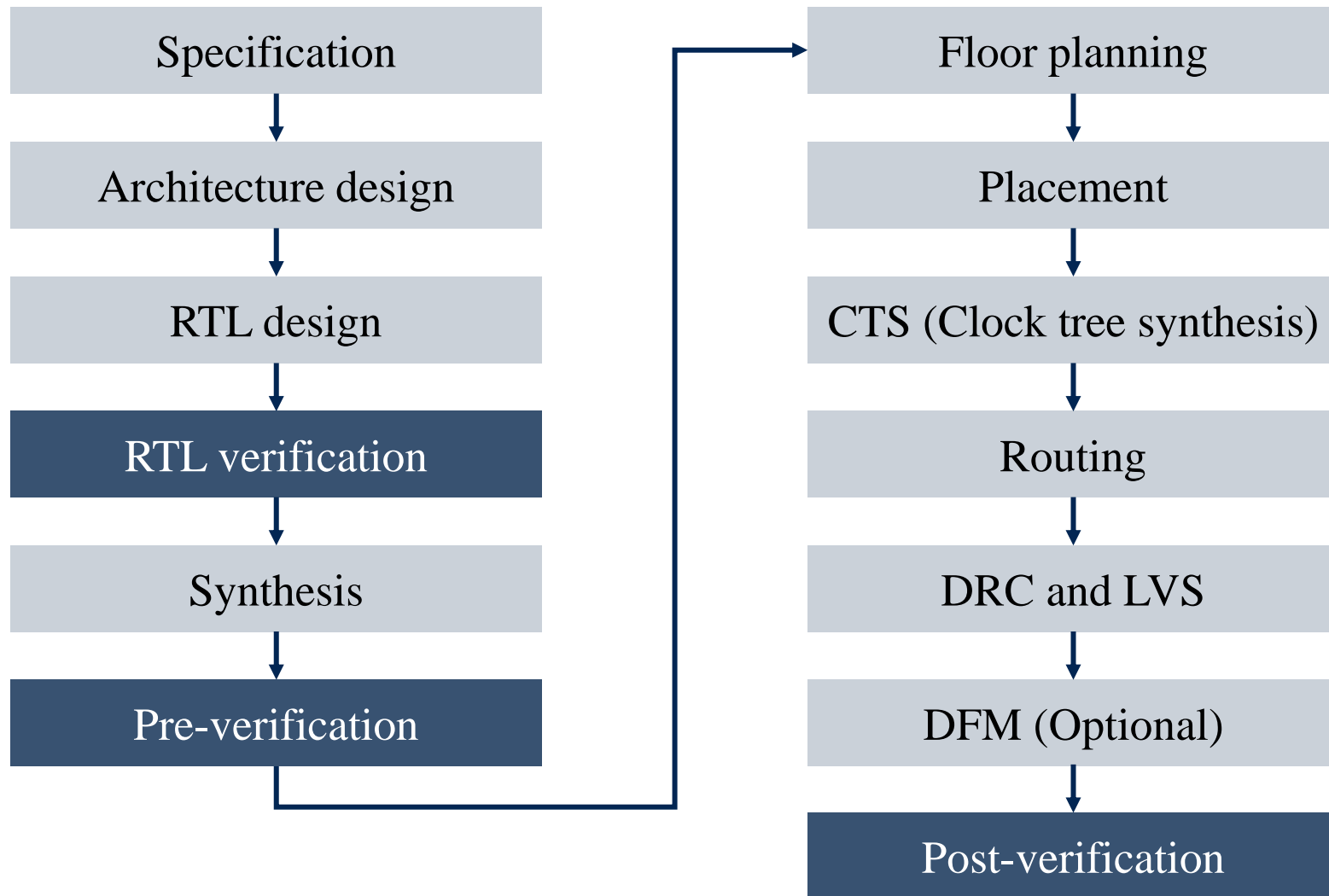
Quartus II Device Installer: Quartus II에 기기 추가 시 사용



ModelSim을 이용한 Simulation

Simulation 개요

- 디지털 설계에서의 시뮬레이션이 필요한 부분



Simulation 개요

- 비교) C 프로그래밍 과정

- 프로젝트 생성 → 프로젝트에 포함된 c 파일 빌드(컴파일 과정 포함)
→ 실행 파일의 실행
- 가장 먼저 실행되는 것은 main 함수

Simulation 개요

- 비교) C 프로그래밍 과정

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→ 실행 파일의 실행
- 가장 먼저 실행되는 것은 main 함수

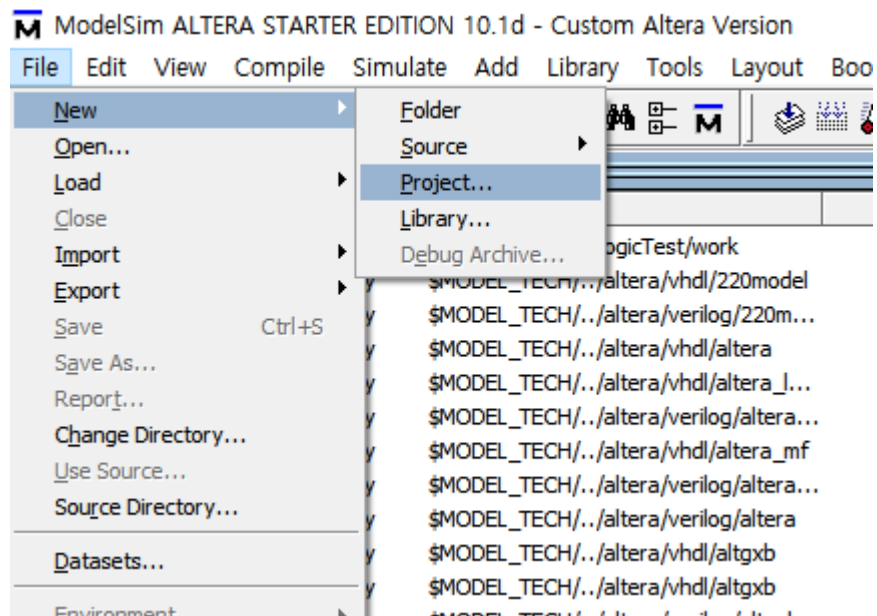
- Modelsim을 이용한 시뮬레이션 과정

- 프로젝트 생성 → 프로젝트에 포함된 Verilog 파일(.v) 컴파일
→ 시뮬레이션 수행
- 가장 상위 모듈은?? ➔ testbench

프로젝트 생성

- 생성 방법

- File – New – Project 클릭



프로젝트 생성

- 정보 입력

- 프로젝트 이름과 프로젝트가 저장될 경로(Project Location) 설정

- Project Location

- 프로젝트 생성 시 관련 파일이 생성되는 위치를 뜻함
- **Browser**를 눌러 반드시 폴더를 변경
 - 변경 없이 사용 시 오류 나는 경우가 많음
 - 모델심 설치 폴더 외부에 폴더 생성하여 사용
 - ✓ 모델심 내부에 폴더 생성/사용 시 'Loading Module Error' 발생 가능
 - 경로에 한글이 포함되지 않도록 함

Create Project

Project Name
logicTest

Project Location
C:/Research/SIM/logicTest Browse...

Default Library Name
work

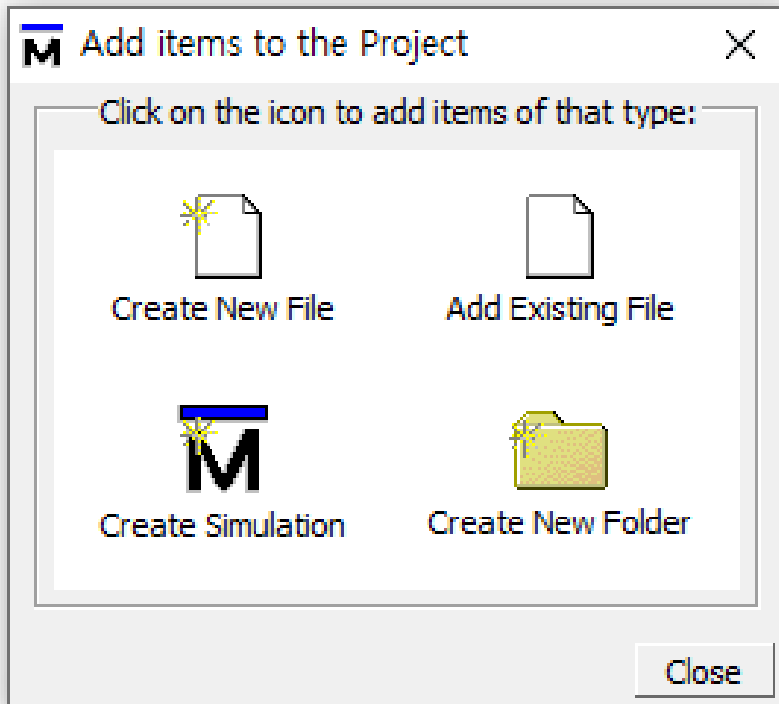
Copy Settings From
1/modelsim_ase/modelsim.ini Browse...

☒ Copy Library Mappings ☐ Reference Library Mappings

OK Cancel

- 파일 추가

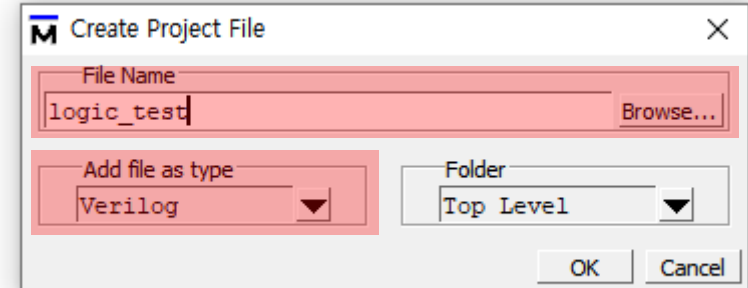
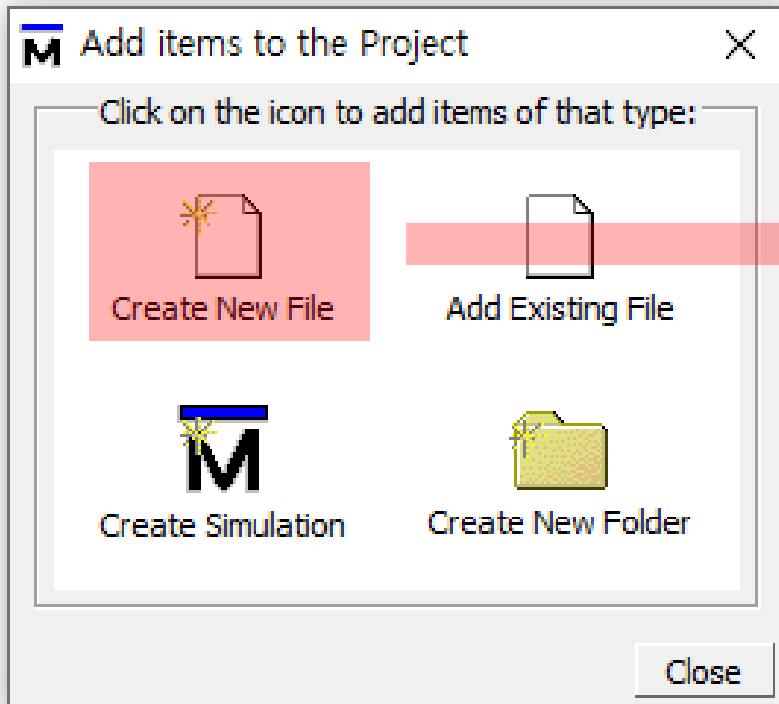
- 프로젝트에 포함될 파일을 새로 만들 경우: Create New File
- 기존 파일을 추가할 경우: Add Existing File



프로젝트 생성

● 파일 추가

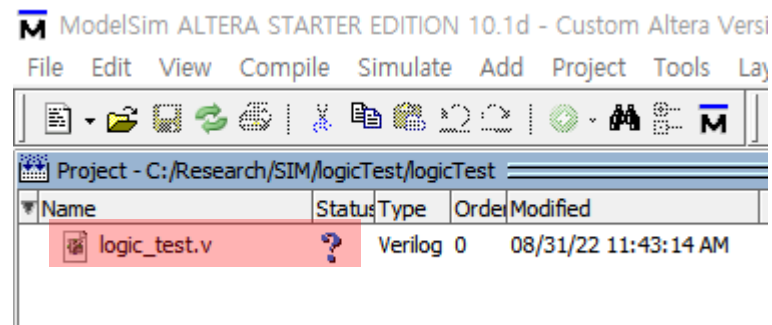
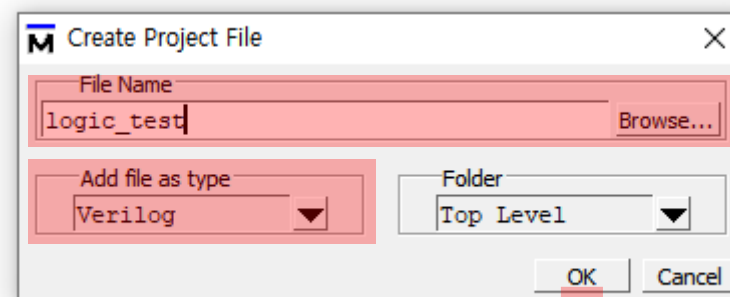
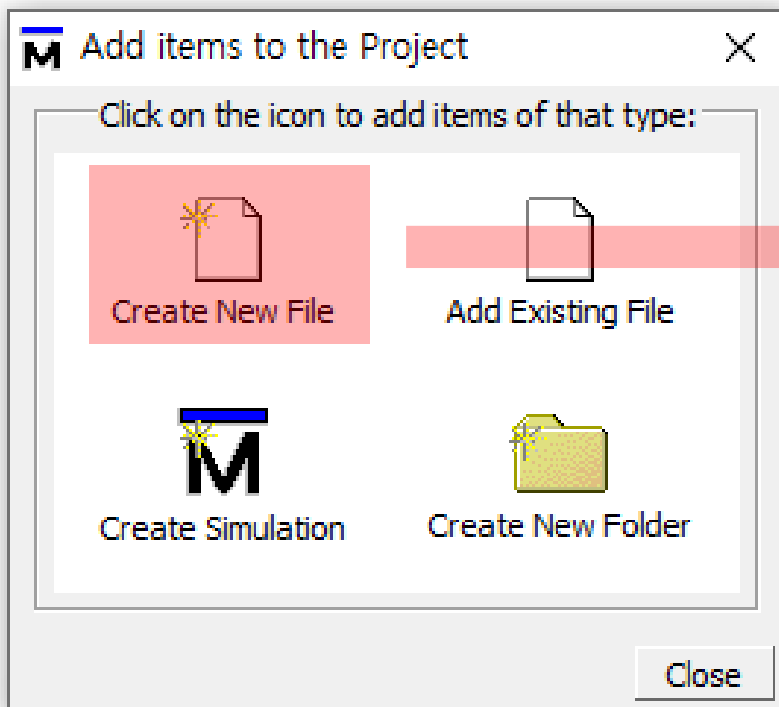
- 새로 만들 경우(Create New File을 눌렀을 때)
 - File Name: 새로 생성할 파일의 이름 및 폴더 지정
 - 저장 위치를 지정하지 않으면 프로젝트 폴더 내에 파일이 생성됨
 - Add file as type: **Verilog로 변경**



프로젝트 생성

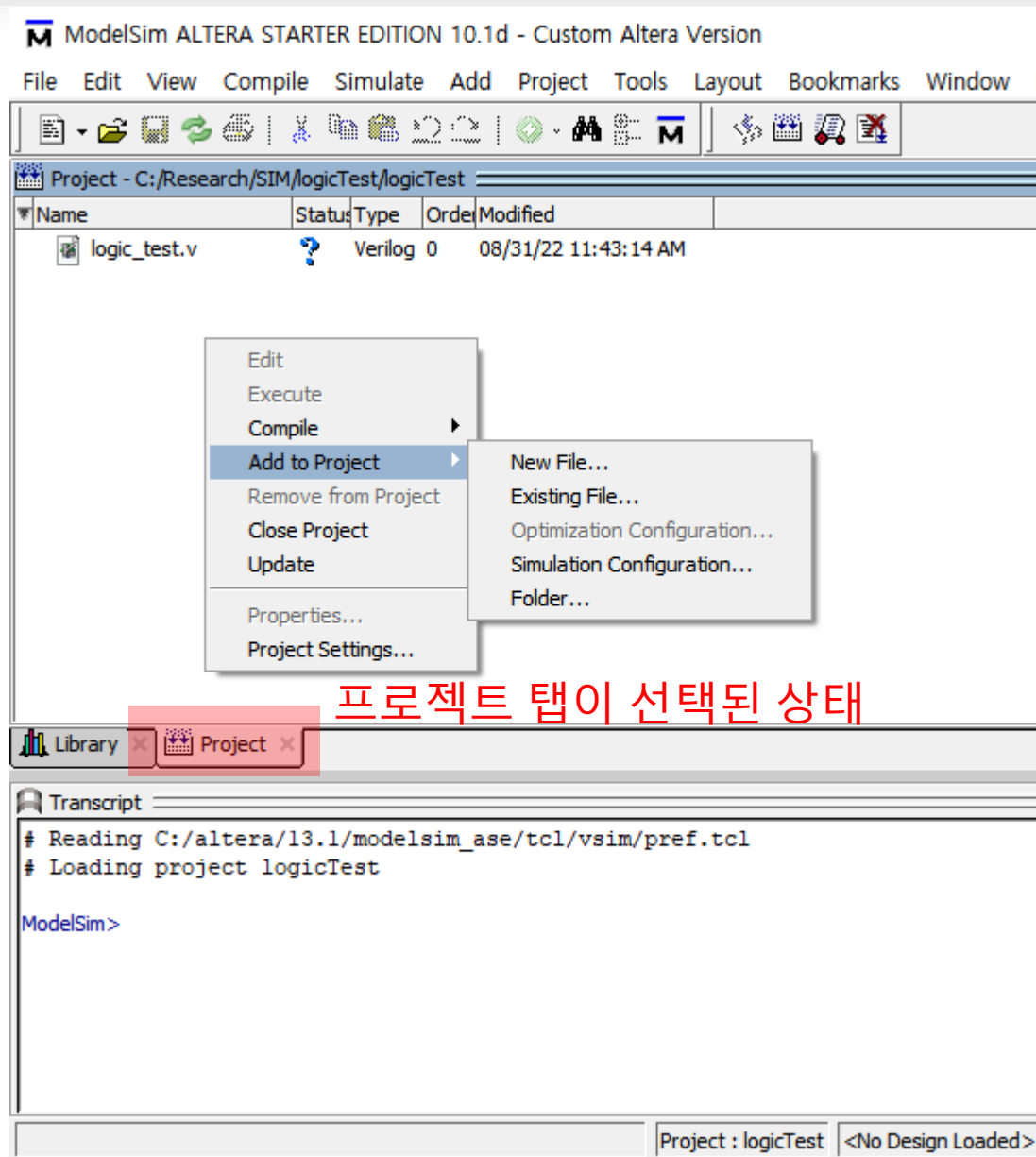
- 파일 추가

- 새로 만들 경우(Create New File을 눌렀을 때)
 - OK를 누르면 Project 창에 생성한 파일이 추가됨



프로젝트 생성

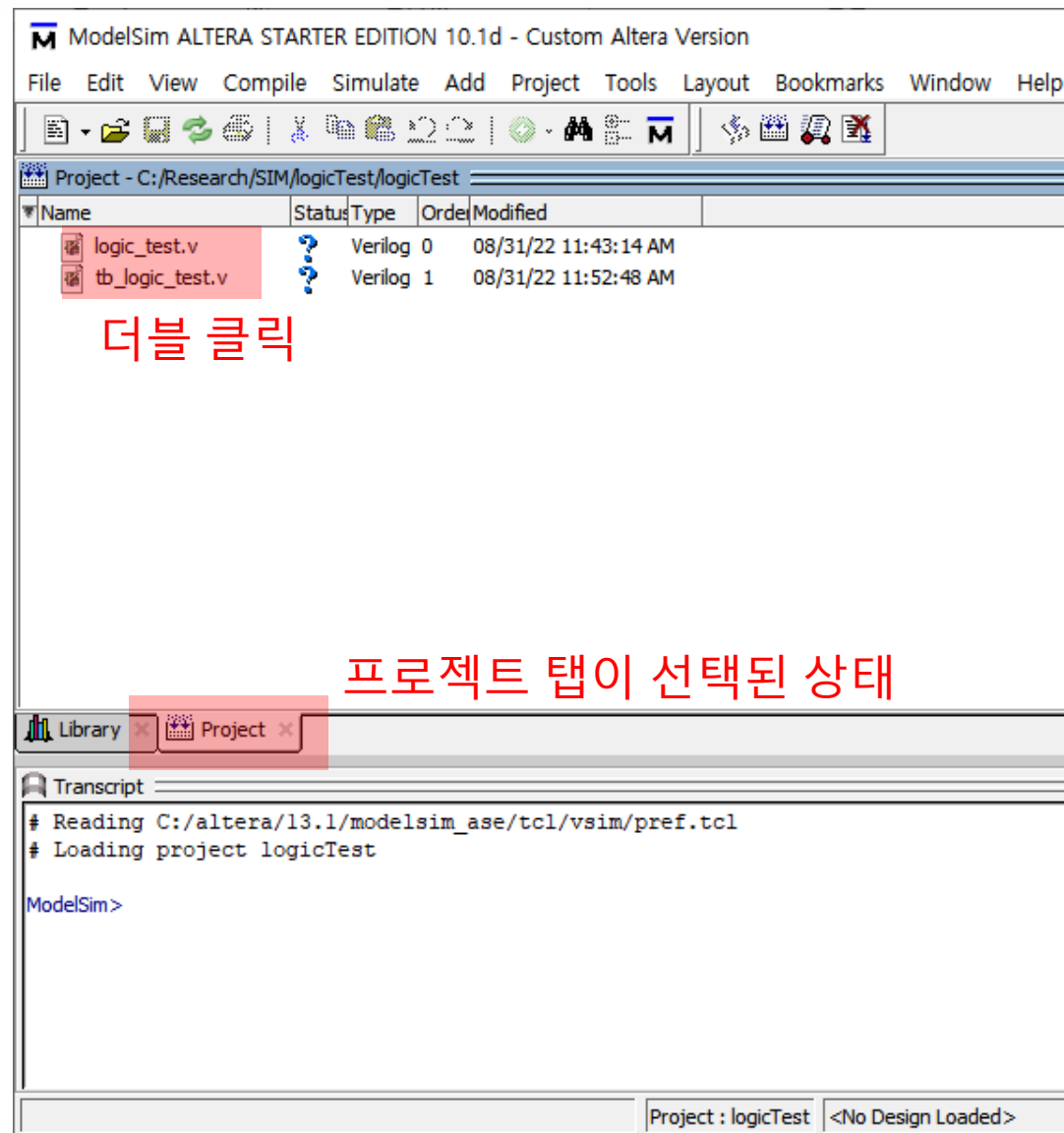
- 참고) 나중에 파일을 추가할 때
 - 프로젝트 탭이 선택된 상태에서
흰 바탕 오른쪽 버튼 클릭
→ Add to Project



파일 수정하기

● 파일 보기

- 프로젝트 탭이 선택된 상태에서
- 파일을 **더블 클릭** 또는
오른쪽 버튼 → Edit
하면 edit 창이 열림
- 수정 사항 바로 반영 X.
반드시 **저장 후 컴파일** 해야 함



파일 수정하기

tb_logic_test.v

```
module tb_logic_test;
reg LT_i_0;
reg LT_i_1;
wire LT_o_AND;
wire LT_o_OR;
wire LT_o_NOT;
wire LT_o_XOR;

logic_test U0(LT_i_0, LT_i_1, LT_o_AND, LT_o_OR,
              LT_o_NOT, LT_o_XOR);

initial
begin
    LT_i_0 = 0; LT_i_1 = 0;
    #10 LT_i_0 = 0; LT_i_1 = 1;
    #10 LT_i_0 = 1; LT_i_1 = 0;
    #10 LT_i_0 = 1; LT_i_1 = 1;

end
endmodule
```

logic_test.v

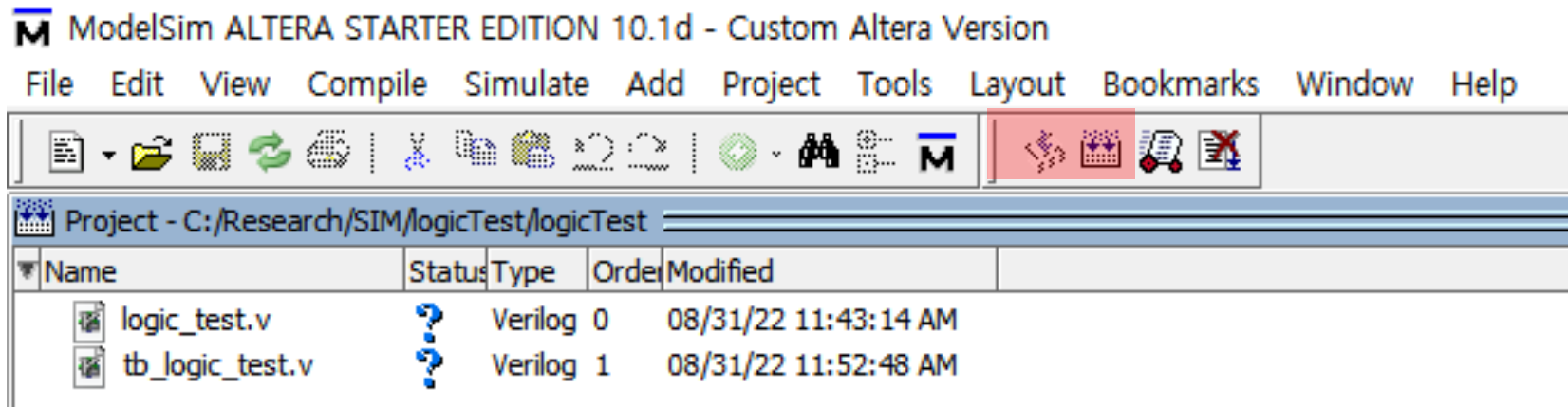
```
module logic_test(i_0, i_1, o_AND, o_OR, o_NOT, o_XOR);
input i_0;
input i_1;
output o_AND;
output o_OR;
output o_NOT;
output o_XOR;




assign o_AND = i_0 & i_1;
assign o_OR = i_0 | i_1;
assign o_NOT = ~i_0;
assign o_XOR = i_0 ^ i_1;

endmodule
```

Compile

- Compile 관련 버튼



-  : 선택된 파일 컴파일하기
-  : 수정사항 발생한(새롭게 저장된) 파일만 컴파일하기(Optional)
-  : 모든 파일 컴파일하기

Compile

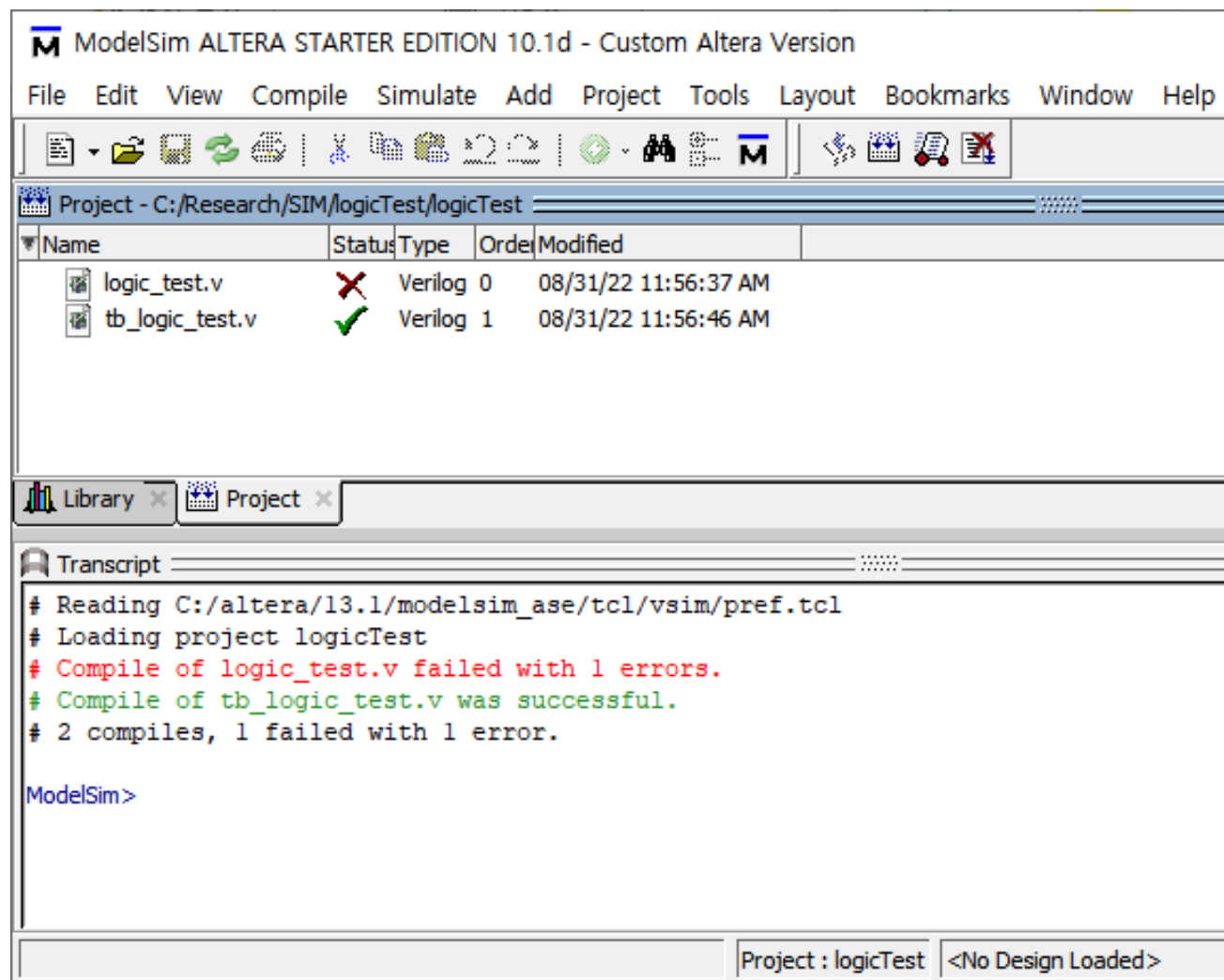
- 수행 결과

- Project 창

- ❌ : 오류 발생
 - ✅ : 성공

- Transcript 창

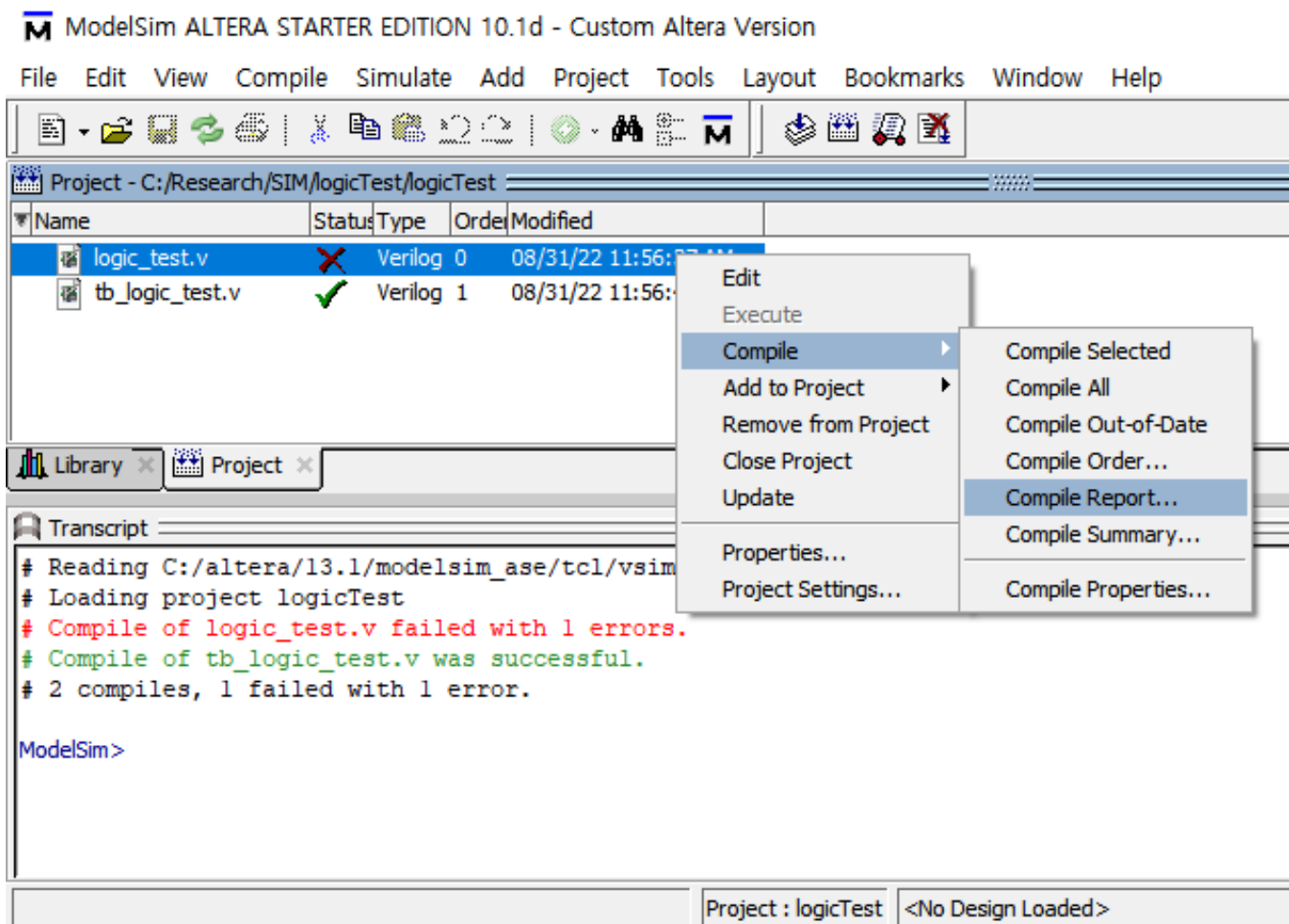
- 자세한 메시지 출력



Compile

- 오류 확인

- 파일 선택 후 마우스 오른쪽 버튼 → Compile → Compile Report



Compile

● 오류 확인 예시

```
M ...cTest/logic_test.v -- Unsuccessful Compile
vlog -work work C:/Research/SIM/logicTest/logic_test.v
Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
-- Compiling module logic_test
** Error: C:/Research/SIM/logicTest/logic_test.v(2): near "input": syntax error,
unexpected input, expecting ';'

```

```
C:/Research/SIM/logicTest/logic_test.v - Default
Ln#
1  module logic_test(i_0, i_1, o_AND, o_OR, o_NOT, o_XOR)
2  input i_0;
3  input i_1;
4  output o_AND;
5  output o_OR;
6  output o_NOT;
7  output o_XOR;
8

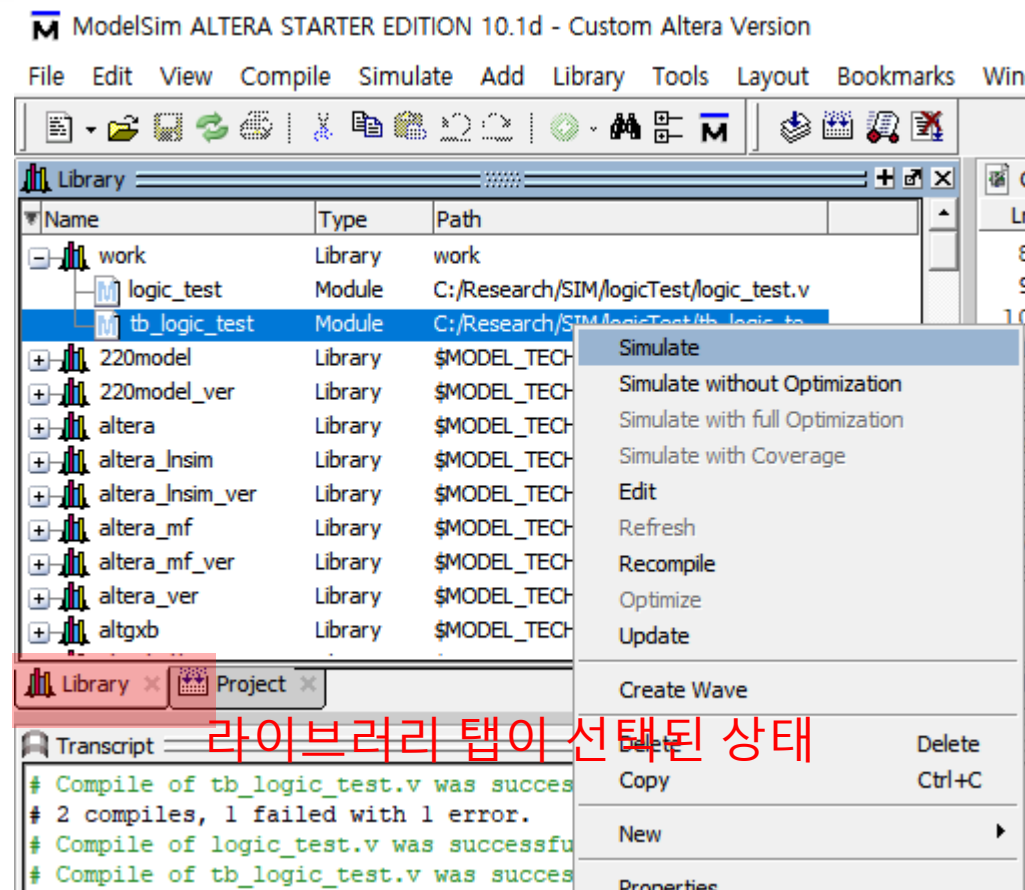
```

- logic_test.v(2) → 오류 난 줄 번호(2번째 줄)을 알려주고 있음
- syntax error, unexpected input, expecting ‘;’ or ‘,’.
→ 세미콜론(;)이 빠졌다는 오류 메시지

Simulation

● 시작 방법1

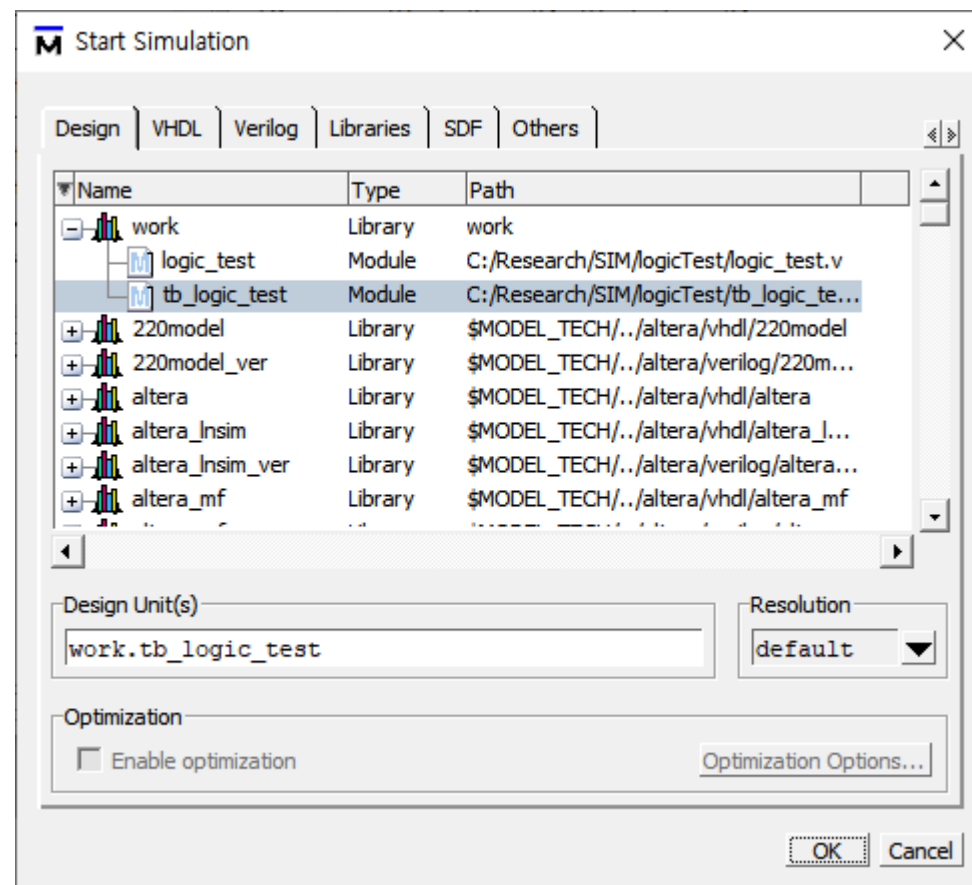
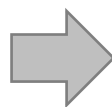
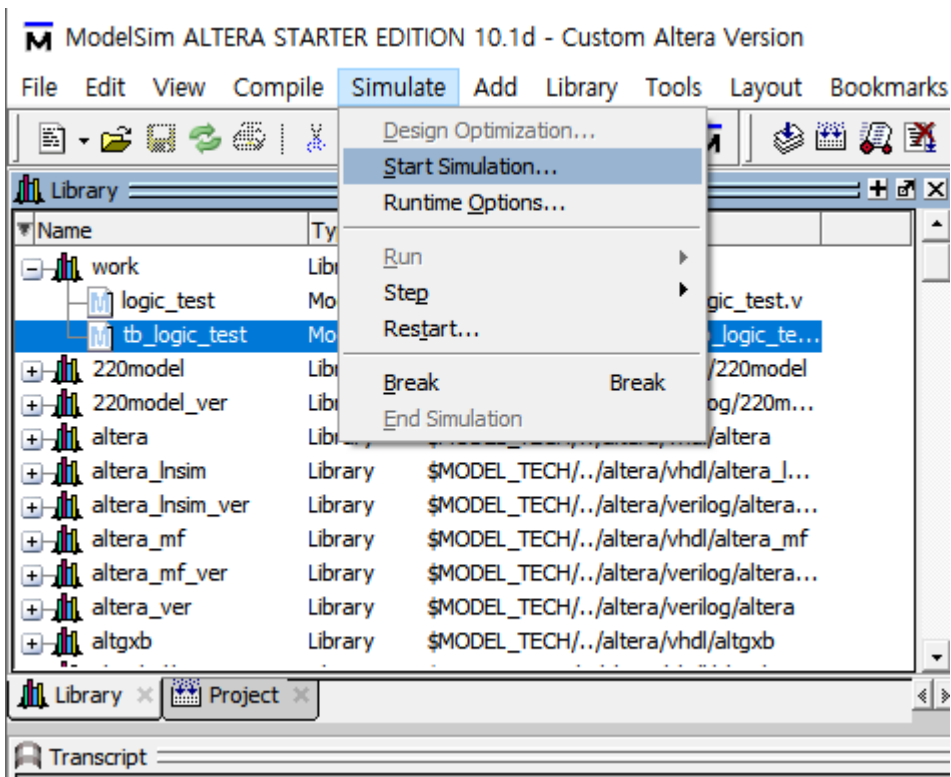
- 라이브러리 탭 선택 →
work 안의 최상위(top) 모듈 선택 →
오른쪽 버튼 → Simulate 선택
- 최상위 모듈
 - 테스트 벤치 (tb_logic_test)
 - SW 프로그래밍에서 main 함수 역할
- work 폴더
 - 컴파일된 모듈이 포함되어 있음



Simulation

시작 방법2

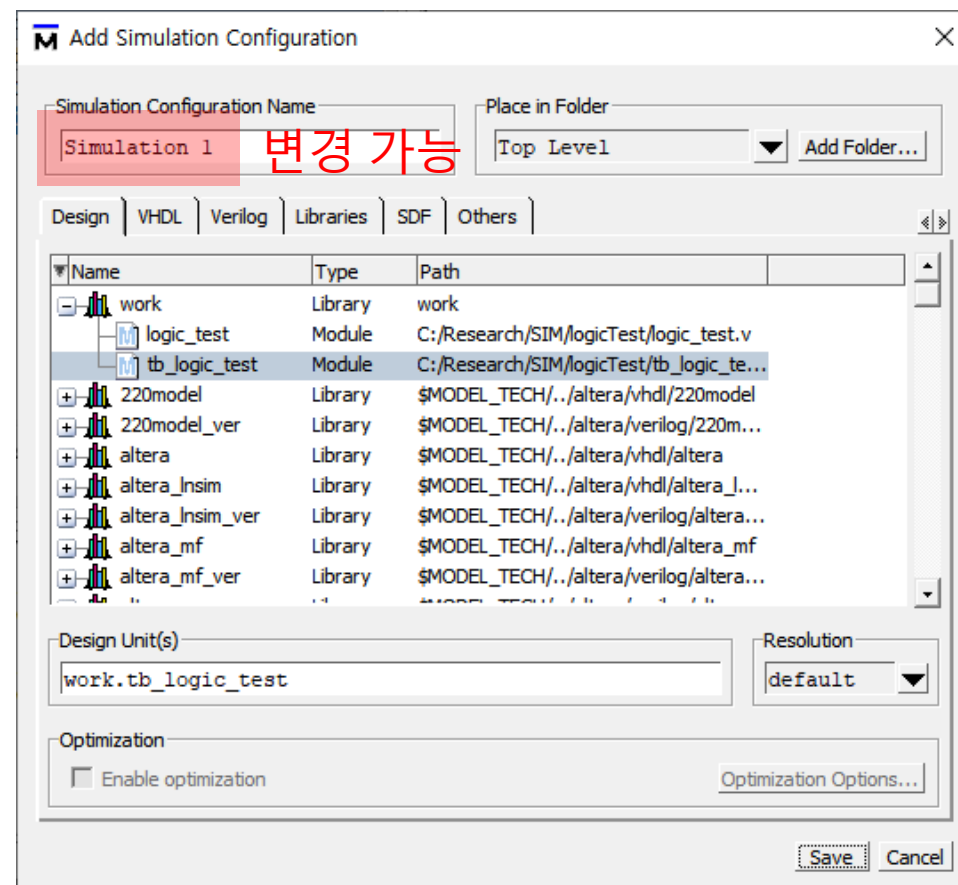
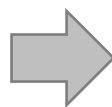
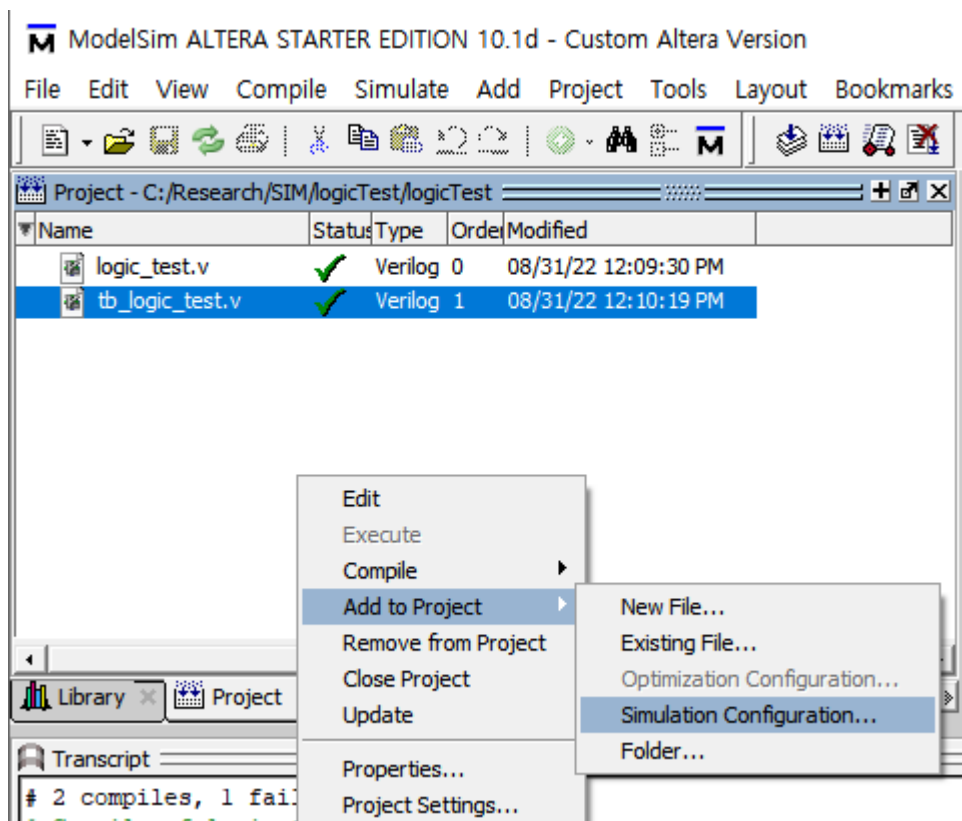
- Menu – Simulate – Start simulation... 선택
- Start Simulation 창의 work에서 최상위 모듈 선택 후 OK



Simulation

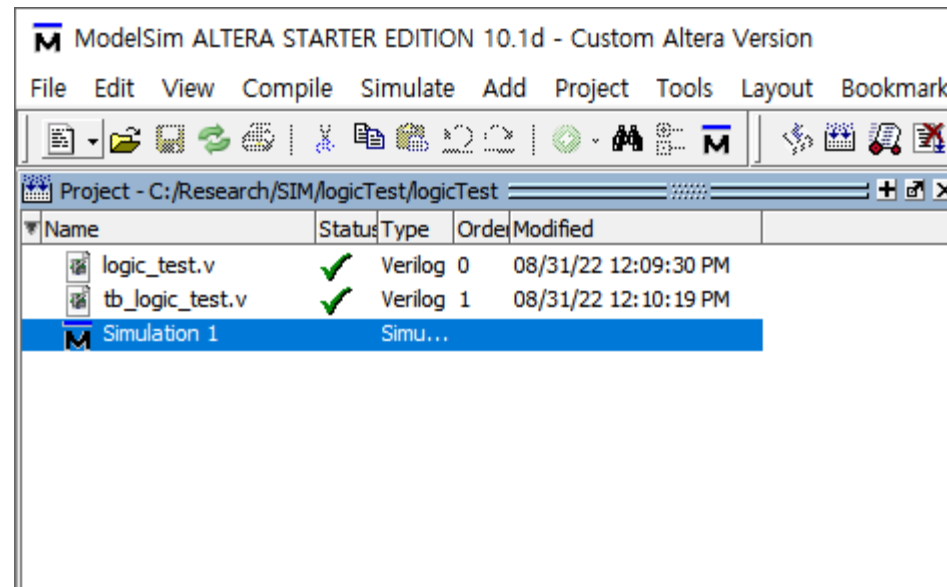
시작 방법3

- Project 창 선택 → Add to Project 선택 → Simulation Configuration 선택
- Add Simulation Configuration 창의 work에서 최상위 모듈 선택 후 Save



● 시작 방법3

- Project 창 선택 → Add to Project 선택 → Simulation Configuration 선택
- Add Simulation Configuration 창의 work에서 최상위 모듈 선택 후 Save
- Project 창에 Simulation 버튼 생성: 더블 클릭 시 시뮬레이션 시작
 - 추후 시뮬레이션 시 top module을 선택하는 등의 설정 불필요



Simulation

● 제대로 시작된 경우

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

sim - Default

Instance	Design unit	Design
tb_logic_test	tb_logic_test	Module
U0	logic_test	Module
#INITIAL #11	tb_logic_test	Process
#vsim_capacity#		Capacit

Objects

Name	Value
LT_i_0	x
LT_i_1	x
LT_o_AND	StX
LT_o_NOT	StX
LT_o_OR	StX
LT_o_XOR	StX

Processes (Active)

Name	Type (filter)
#ASSIGN #9	Assign
#ASSIGN #10	Assign
#ASSIGN #11	Assign
#ASSIGN #12	Assign
#INITIAL #11	Initial

Wave - Default

Now 0 ps

Cursor 1 0 ps

0 ps 500 ps 1000 ps 1500 ps

새로 생김

Transcript

```
# vsim work.tb_logic_test
# Loading work.tb_logic_test
# Loading work.logic_test

VSIM 2>
```

0 ps to 1769 ps Ln: 13 Col: 0 Project : logicTest Now: 0 ps Delta: 0 sim:/tb_logic_test

Simulation

● 오류 발생 시

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

sim - Default

Instance Design unit Design

Instance	Design unit	Design
tb_logic_test	tb_logic_test	Module
U0	logic_test	Module
#INITIAL #11	tb_logic_test	Process
#vsim_capacity#		Capacit

Objects

Name	Value
LT_i_0	x
LT_i_1	y
LT_o_AND	
LT_o_NOT	
LT_o_OR	
LT_o_XOR	

Processes (Active)

Name	Value
#ASSIGN #9	Assign
#ASSIGN #10	Assign
#ASSIGN #11	Assign
#ASSIGN #12	Assign
#INITIAL #11	Initial

Wave - Default

Msgs

Now 0 ps

Cursor 1 0 ps

0 ps 500 ps 1000 ps 1500 ps

0 ps to 1769 ps

Ln: 13 Col: 0

Project : logicTest

Now: 0 ps Delta: 0

sim:/tb_logic_test

Transcript

```
# vsim work.tb_logic_test
# Loading work.tb_logic_test
# Loading work.logic_test
VSIM 2>
```

오류 발생 시 시뮬레이션이 되지 않음

오류가 발생하는 경우

- 연결하려는 하위 모듈이 없는 경우
(파일 추가 안 했거나 컴파일 시 오류가 난 경우)
- 연결하려는 하위 모듈의 입출력 포트의 개수가 맞지 않는 경우 등

오류 발생 시 메시지 확인 필요

Simulation

● 창 설명

The screenshot shows the ModelSim ALTERA STARTER EDITION 10.1d interface. The main window is titled 'sim - Default'. The menu bar includes File, Edit, View, Compile, Simulate, Add, Wave, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and viewing. The left pane shows a project tree with 'tb_logic_test' selected. The middle pane shows the 'Objects' window with a list of objects including 'LT_i_0', 'LT_i_1', 'LT_o_AND', 'LT_o_NOT', 'LT_o_OR', and 'LT_o_XOR'. The bottom pane shows the 'Processes (Active)' window with a list of processes including '#ASSIGN#9', '#ASSIGN#10', '#ASSIGN#11', '#ASSIGN#12', and '#INITIAL#11'. The right pane shows a waveform window with multiple vertical lines representing signals.

- Library, Project, Simulation 탭 중 하나 선택 가능
- Simulation 탭 창은 계층 구조를 확인할 수 있음
- Objects 창
- Simulation 탭 창에서 선택한 모듈이 사용하는 신호
- Processes 창
- 불필요(X눌러 닫기)
- Wave 창: 파형이 표시됨
- **주의:** Modelsim 설치 후 첫 시뮬레이션 시에는 wave 창이 자동으로 보이지 않음. 이 경우 Menu - View - Wave 선택

Ln: 13 Col: 0 Project : logicTest Now: 0 ps Delta: 0 sim:/tb_logic_test

Simulation

- 창 설명 - 참고) 불필요한 단추 없애기

The screenshot shows the ModelSim ALTERA STARTER EDITION 10.1d interface. The main window is titled 'sim - Default'. The menu bar includes File, Edit, View, Compile, Simulate, Add, Structure, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and viewing. The left pane shows the 'Objects' and 'Processes (Active)' lists. The right pane shows the 'Wave - Default' window with a signal trace. A context menu is open over the Wave window, listing various options: Standard, Bookmarks, Changelog, Compile, Coverage, Layout, Mode, Objectfilter, Process, Profile, Simulate, Source, Step, Wave, Wave Compare, Wave Cursor, Wave Edit, Wave Expand Time, Zoom, and Reset. A red text box is overlaid on the Wave window, containing the text: '마우스 오른쪽 버튼 누른 후 Standard, Compile, Simulate을 제외한 모든 단추 해제하기'.

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

sim - Default

Instance Design unit Design

Instance	Design unit	Design
tb_logic_test	tb_logic_test	Module
U0	logic_test	Module
#INITIAL#11	tb_logic_test	Process
#vsim_capacity#		Capacit

Objects

Name	Value
LT_i_0	x
LT_i_1	x
LT_o_AND	StX
LT_o_NOT	StX
LT_o_OR	StX
LT_o_XOR	StX

Processes (Active)

Name	Type (filter)
#ASSIGN#9	Assign
#ASSIGN#10	Assign
#ASSIGN#11	Assign
#ASSIGN#12	Assign
#INITIAL#11	Initial

Wave - Default

Msgs

Now 0 ps

Cursor 1 0 ps

0 ps 500 ps 1500 ps

마우스 오른쪽 버튼 누른 후
Standard, Compile, Simulate을
제외한 모든 단추 해제하기

Library Project sim

Transcript

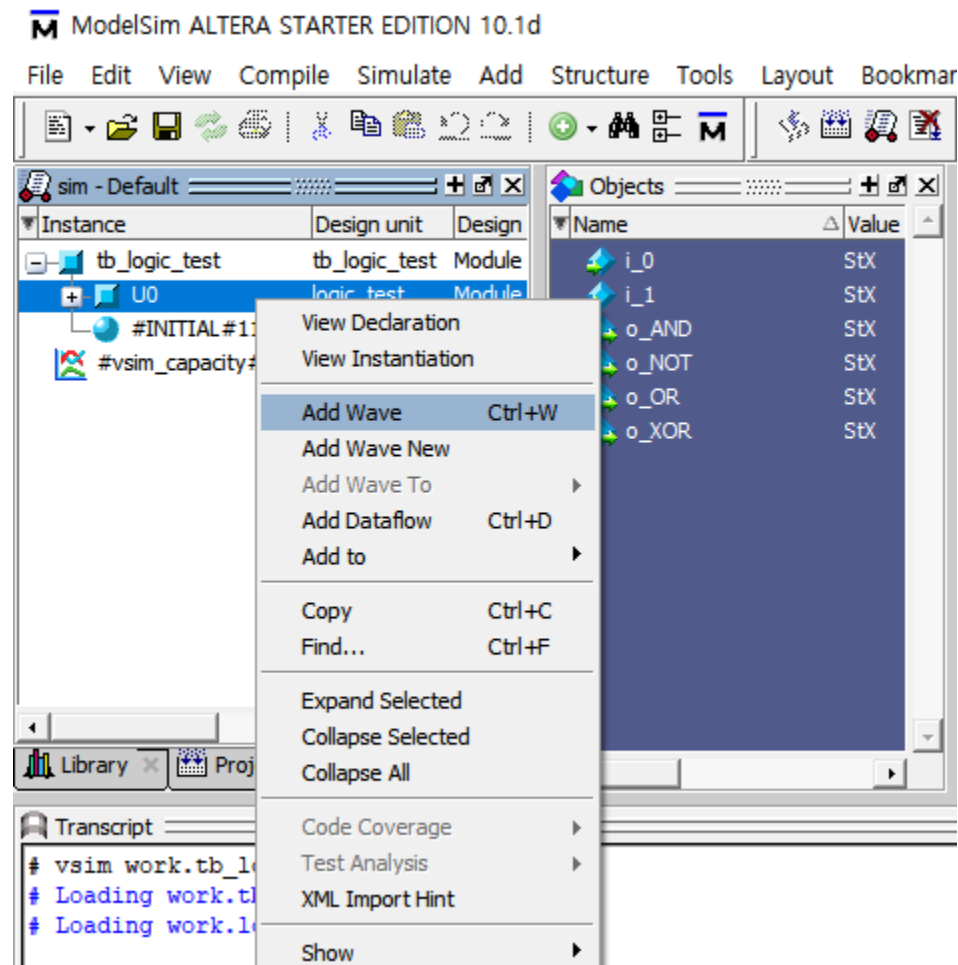
```
# vsim work.tb_logic_test
# Loading work.tb_logic_test
# Loading work.logic_test

VSIM 2>
```

0 ps to 1769 ps Ln: 13 Col: 0 Project : logicTest Now: 0 ps Delta: 0 logic_test

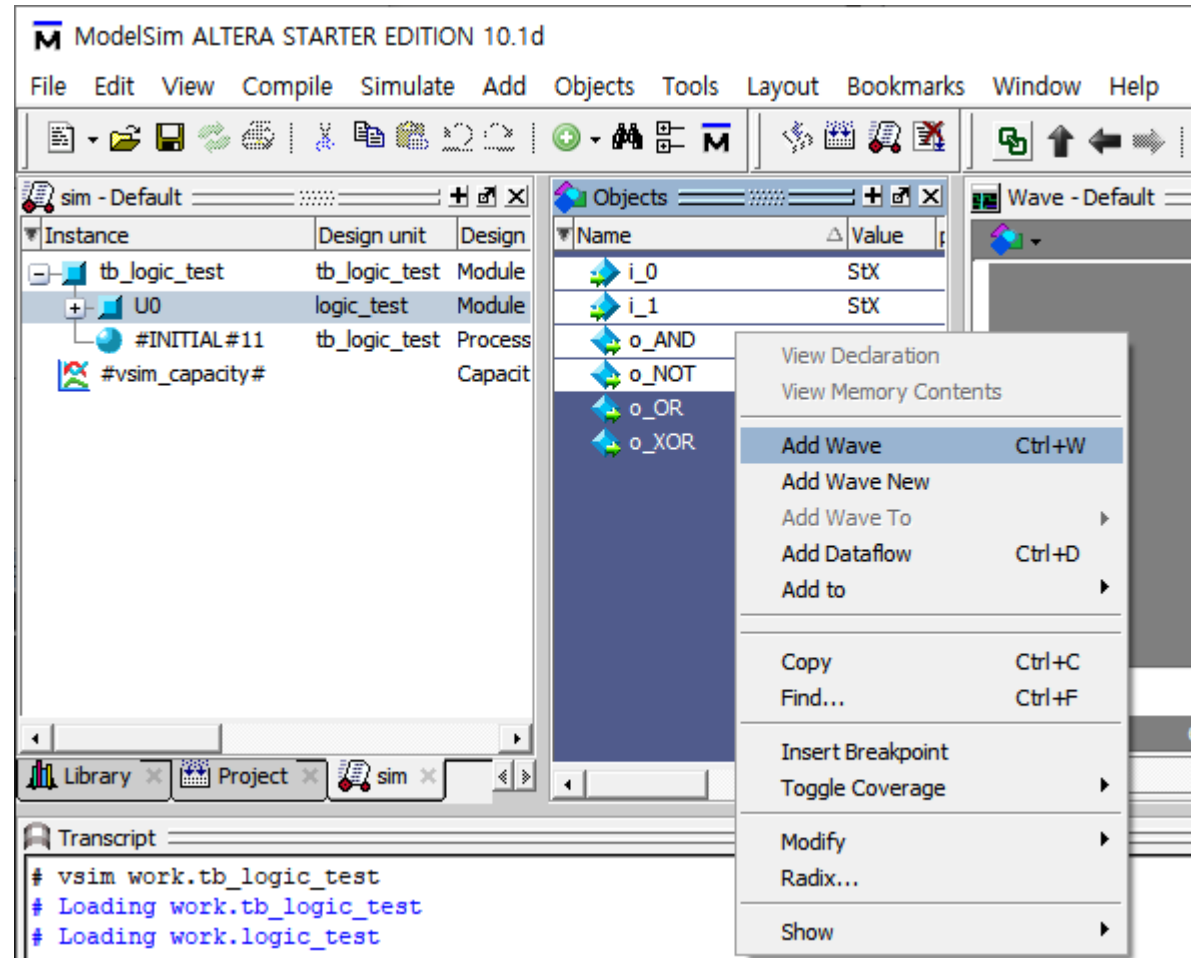
Simulation

- Wave에 신호 추가하기1 - 특정 모듈의 신호 모두 추가하기
 - 시뮬레이션 탭에서 모듈 선택 후
 - 방법1) 오른쪽 버튼 ➡ Add Wave
 - 방법2) 마우스로 wave 창으로 drag



Simulation

- Wave에 신호 추가하기2 - 일부 신호만 선택하여 추가하기
 - 시뮬레이션 탭에서 모듈 선택
→ Objects 창에서 신호 선택 후
 - 방법1) 오른쪽 버튼 → Add Wave
 - 방법2) 마우스로 wave 창으로 drag



Simulation

- U0의 모든 신호가 추가된 상태

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

다음 슬라이스에서 설명

sim - Default

Instance	Design unit	Design
tb_logic_test	tb_logic_test	Module
U0	logic_test	Module
#INITIAL#11	tb_logic_test	Process
#vsim_capacity#		Capacit

Objects

Name	Value
i_0	StX
i_1	StX
o_AND	StX
o_NOT	StX
o_OR	StX
o_XOR	StX

Wave - Default

Msgs
/tb_logic_test/U0/i_0
/tb_logic_test/U0/i_1
/tb_logic_test/U0/o_AND
/tb_logic_test/U0/o_OR
/tb_logic_test/U0/o_NOT
/tb_logic_test/U0/o_XOR


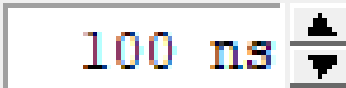




Now 0 ps
Cursor 1 502 ps

500 ps 1000 ps
502 ps

Transcript

```
add wave -position end sim:/tb_logic_test/U0/o_AND  
add wave -position end sim:/tb_logic_test/U0/o_OR
```


- Simulation 관련 버튼

- : restart (처음부터 run하고 싶을 때, 보통 수정사항 발생 시 사용)
- : run length
- : Run (run length 시간 만큼 진행됨)
- : ContinueRun
- : Run -all (시간 제한 없이 run, \$stop, \$finish 등을 만나면 멈춤)
- : Break (진행 중인 run을 멈추고 싶을 때 사용)

Simulation

● 100 ps run한 결과

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

sim - Default

Objects

Name	Value
i_0	St1
i_1	St1
o_AND	St1
o_NOT	St0
o_OR	St1
o_XOR	St0

Wave - Default

Msgs

Signal	Value
/tb_logic_test/U0/i_0	St1
/tb_logic_test/U0/i_1	St1
/tb_logic_test/U0/o_AND	St1
/tb_logic_test/U0/o_OR	St1
/tb_logic_test/U0/o_NOT	St0
/tb_logic_test/U0/o_XOR	St0

노란선은 마우스 클릭한 곳으로 변경 가능

노란색 선 부분의 값 표시

Now 100 ps
Cursor 1 36 ps

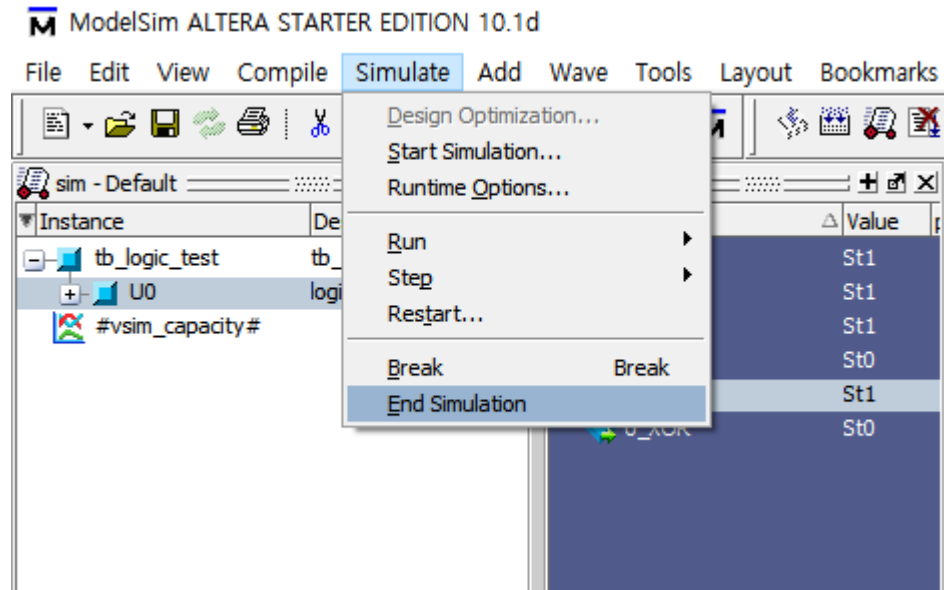
Transcript

```
add wave -position end sim:/tb_logic_test/U0/o_NOT  
add wave -position end sim:/tb_logic_test/U0/o_XOR
```

- 녹색 신호: 정상 신호
- 붉은 신호(X): unknown (신호 충돌, 정의되지 않은 신호, timing 문제 등의 이유로 값을 명확히 알 수 없는 경우)
- 파란 신호(Z): high impedance (신호가 연결되어 있지 않은 경우)

Simulation

- 종료하기
 - Menu – Simulate – End Simulation





Quartus II를 이용한 FPGA 구현

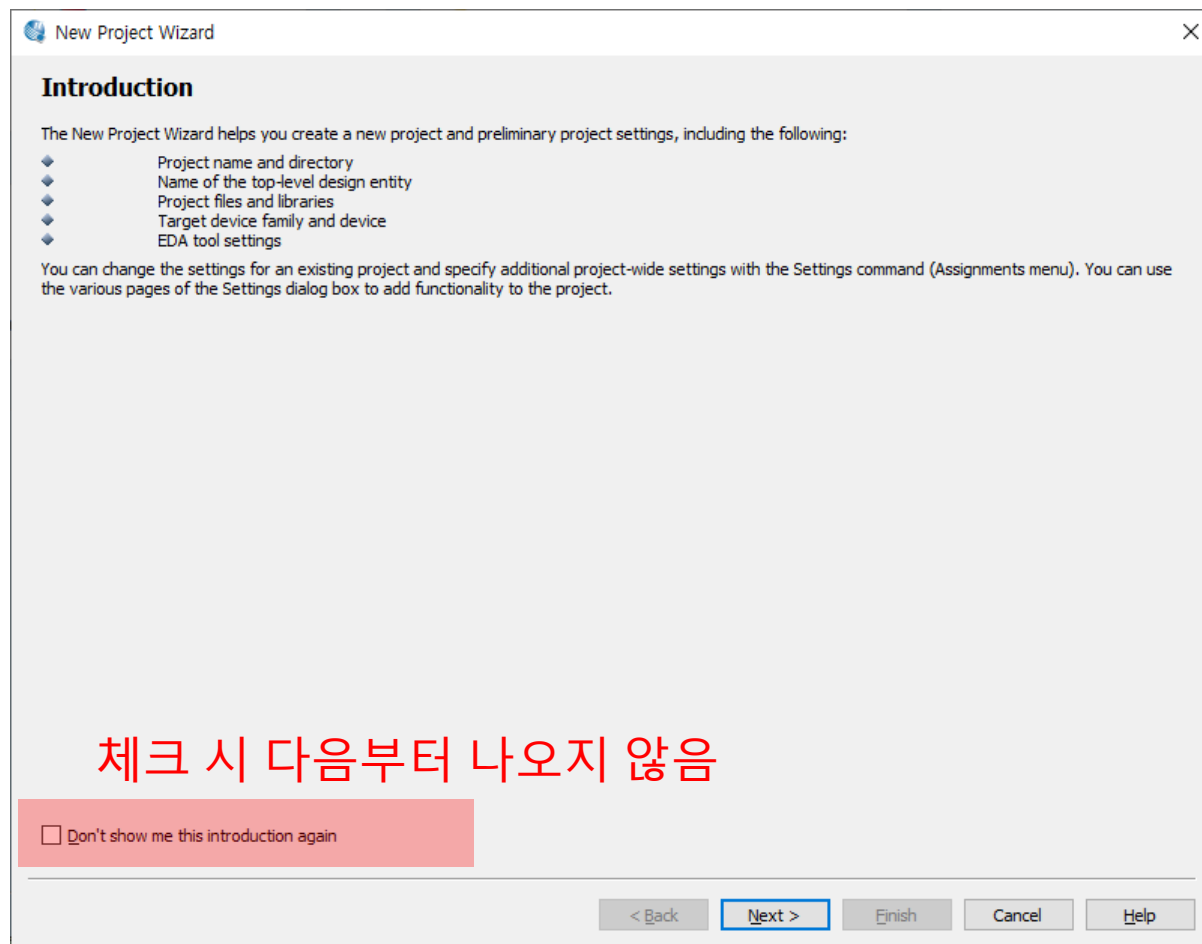
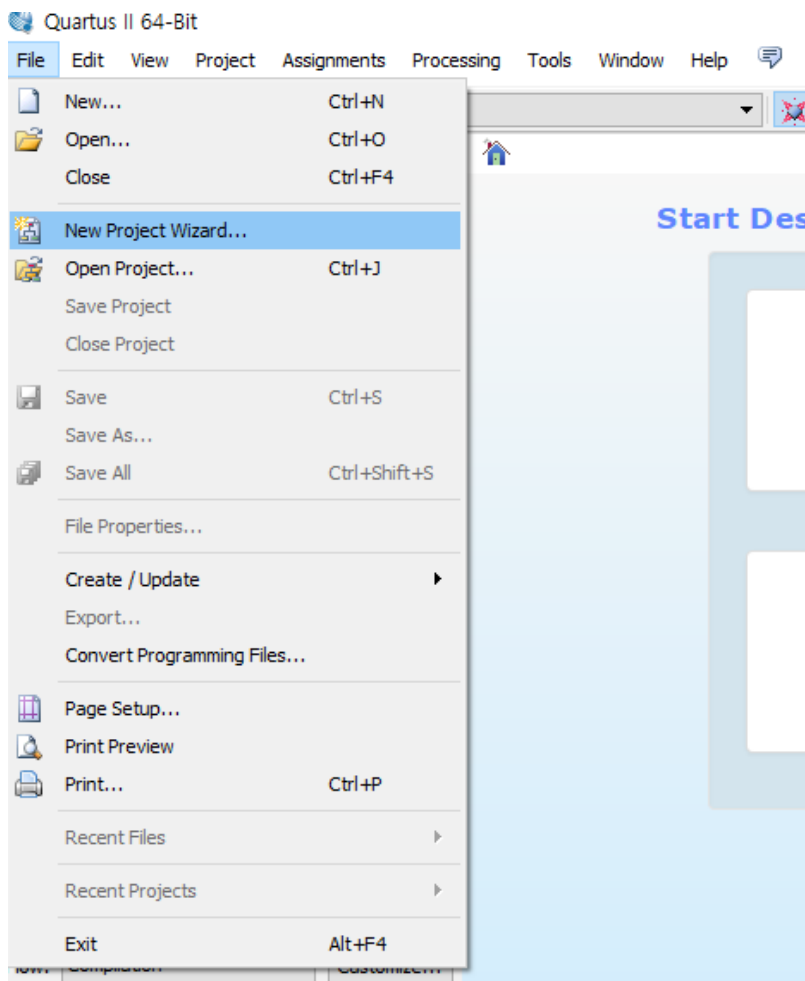
FPGA 구현 개요

- Quartus II를 이용한 FPGA 구현 과정
 - 프로젝트 생성: 프로젝트 이름 설정, 파일 추가, 기기 선택
 - Timing Constraints 설정
 - Pin 설정: 논리적 핀과 물리적 핀 매핑
 - Compile: 합성 및 PnR 수행
 - Program: FPGA에 compile된 결과 전송

프로젝트 생성

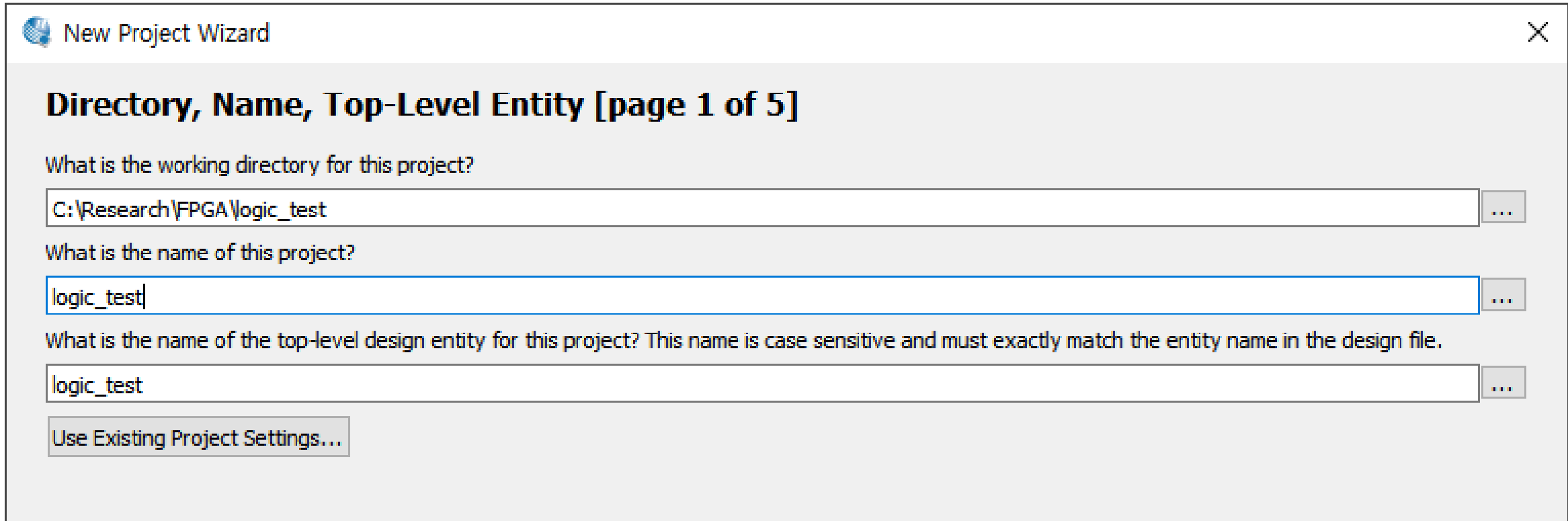
● 생성 방법

■ File – New Project Wizard 클릭



프로젝트 생성

- 프로젝트 폴더/이름, Top module 이름 설정
 - 설정 후 Next



New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

C:\Research\FPGA\logic_test

What is the name of this project?

logic_test

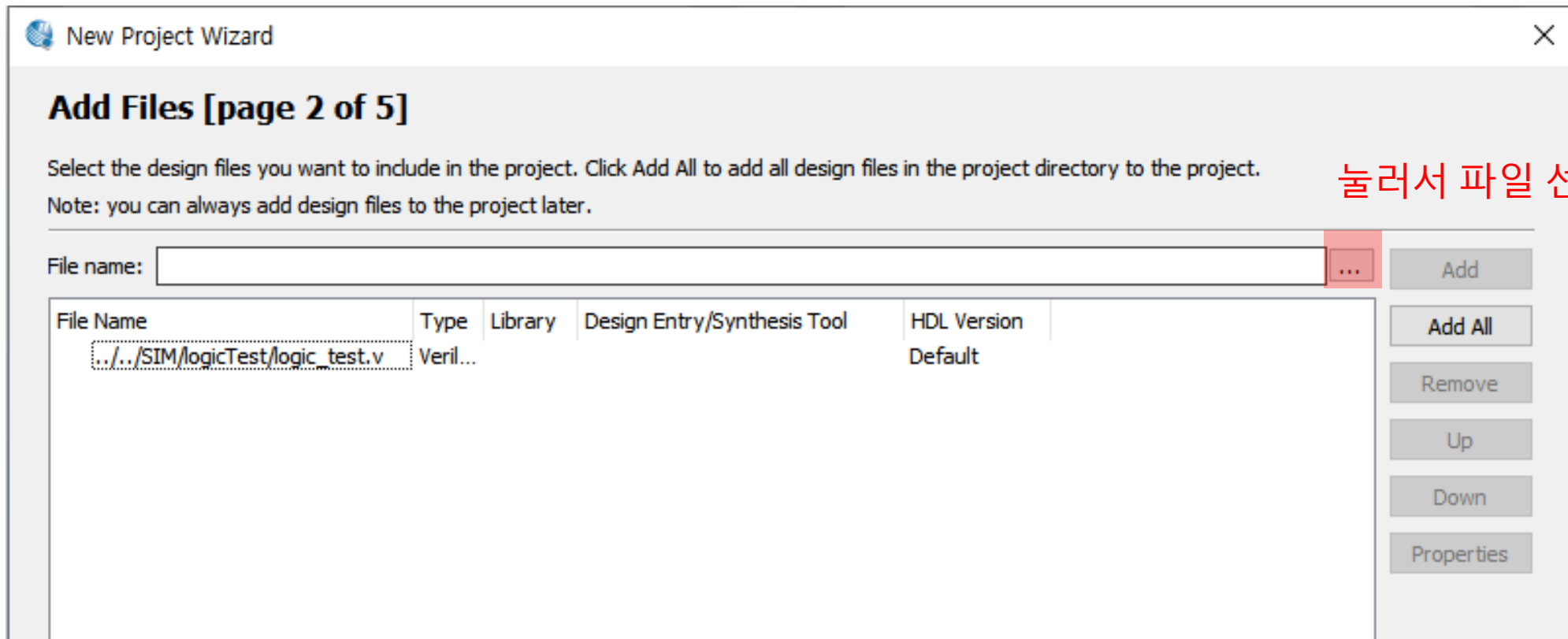
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

logic_test

Use Existing Project Settings...

- Add Files

- Verilog(Testbench 파일은 제외), SDC 파일 추가



프로젝트 생성

- Family & Device Settings

- 사용할 칩 모델명은 FPGA 칩 표면이나 매뉴얼에서 확인 가능



New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family: **Cyclone V (E/GX/GT/SX/SE/ST)**

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter: **5CSEMA5F31C6**

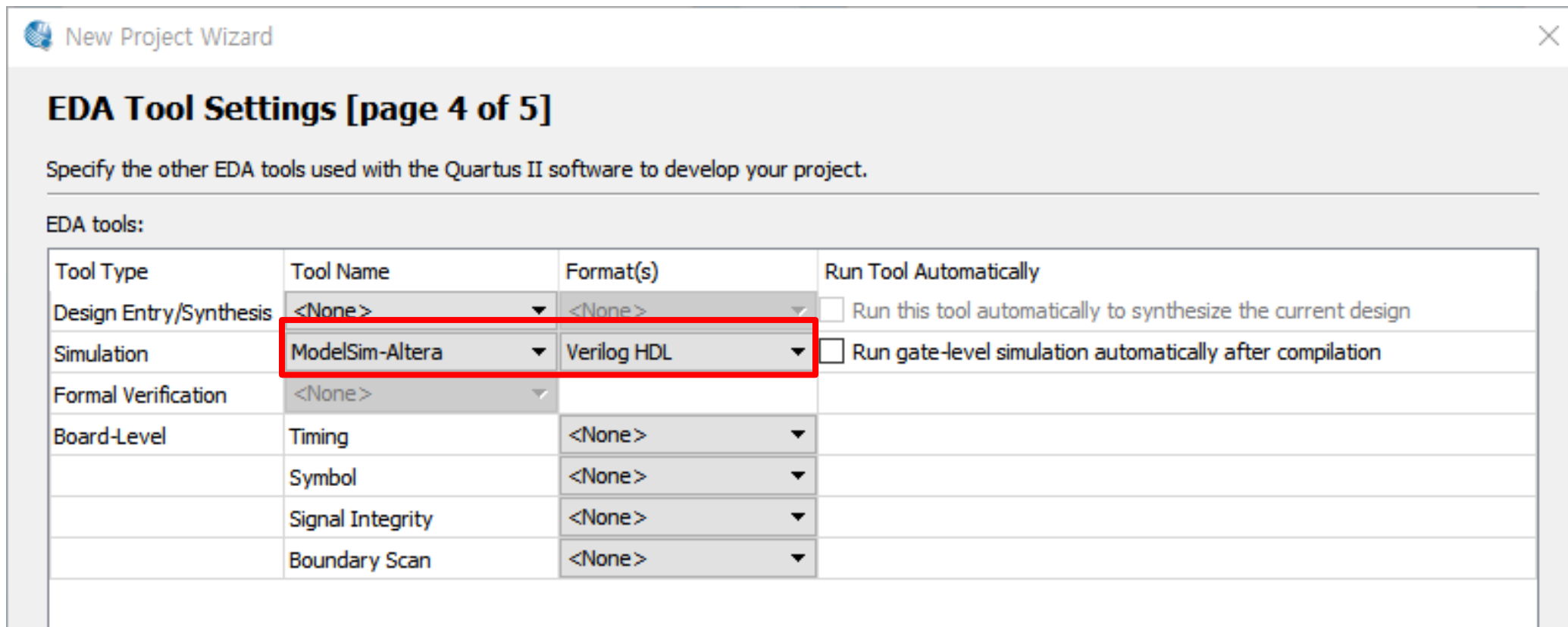
☒ Show advanced devices

Available devices:

Name	Core Voltage	ALMs	User I/Os	GXB Channel PMA	GXB Channel PCS	PCIe (PIPE) Hard IP Blocks
5CSEMA5F31C6	1.1V	32070	457	0	0	0

- Tool Settings

- Simulation: modelsim-Alter & Verilog HDL로 설정 후 Next

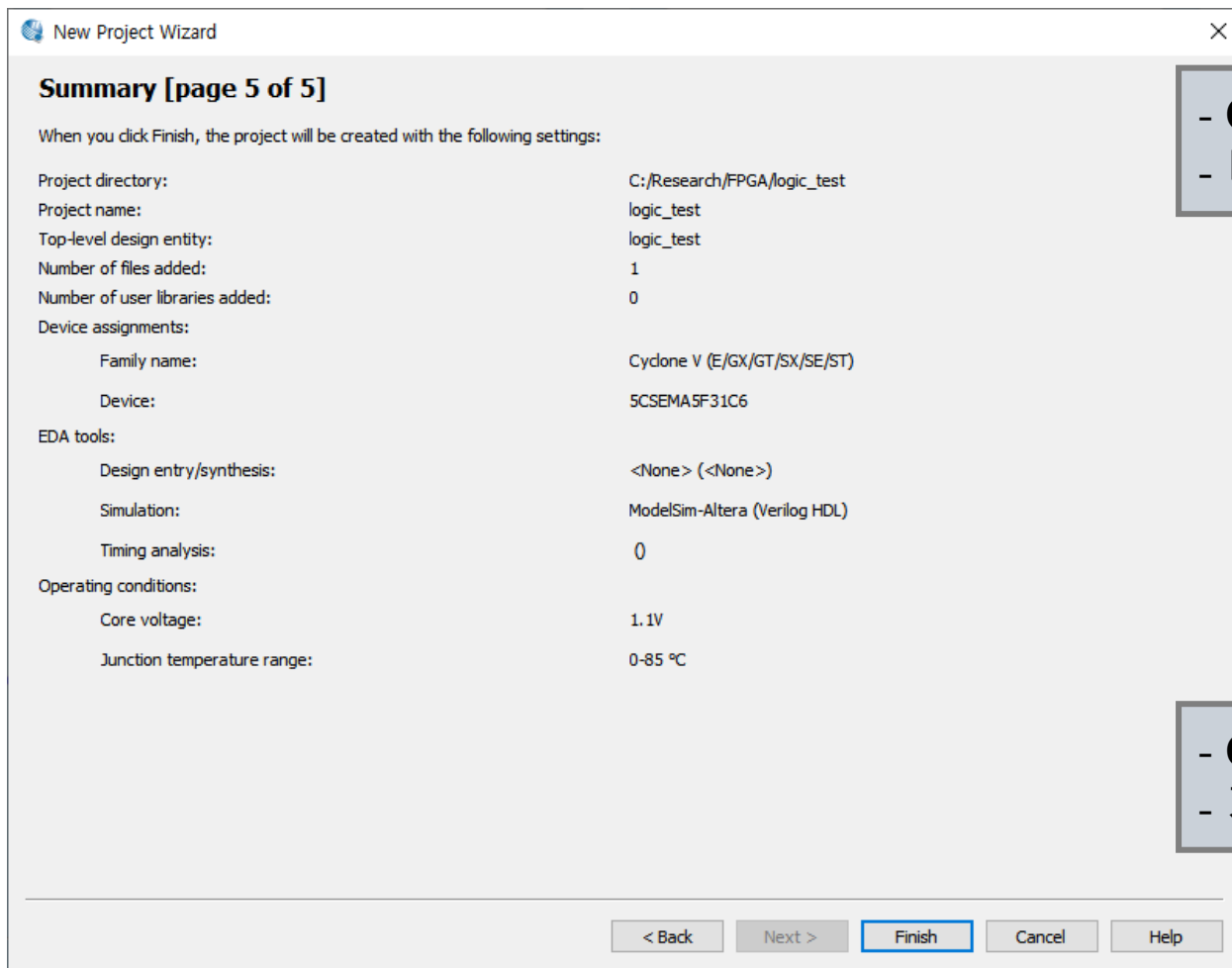


The screenshot shows the 'New Project Wizard' window, specifically the 'EDA Tool Settings' page (page 4 of 5). The window title is 'New Project Wizard' with a close button. The main heading is 'EDA Tool Settings [page 4 of 5]'. Below the heading is a descriptive text: 'Specify the other EDA tools used with the Quartus II software to develop your project.' The section is titled 'EDA tools:'. It contains a table with four columns: 'Tool Type', 'Tool Name', 'Format(s)', and 'Run Tool Automatically'. The 'Simulation' row is highlighted with a red rectangle, showing 'ModelSim-Altera' as the tool name and 'Verilog HDL' as the format. To the right of the table, there are two checkboxes: 'Run this tool automatically to synthesize the current design' and 'Run gate-level simulation automatically after compilation', both of which are currently unchecked.

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

● Summary

■ 정보 확인 후 Finish

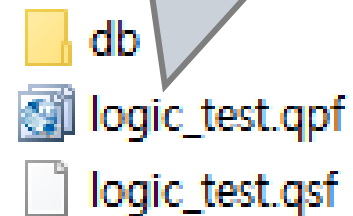


- Quartus Project File

- 더블 클릭 시 해당 프로젝트로 Quartus II가 열림



이름

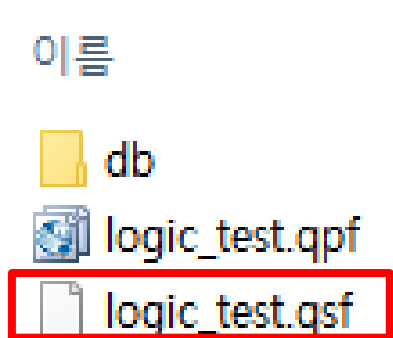


- Quartus Setting File

- 기기 정보 등의 설정 정보가 포함되어 있음

프로젝트 생성

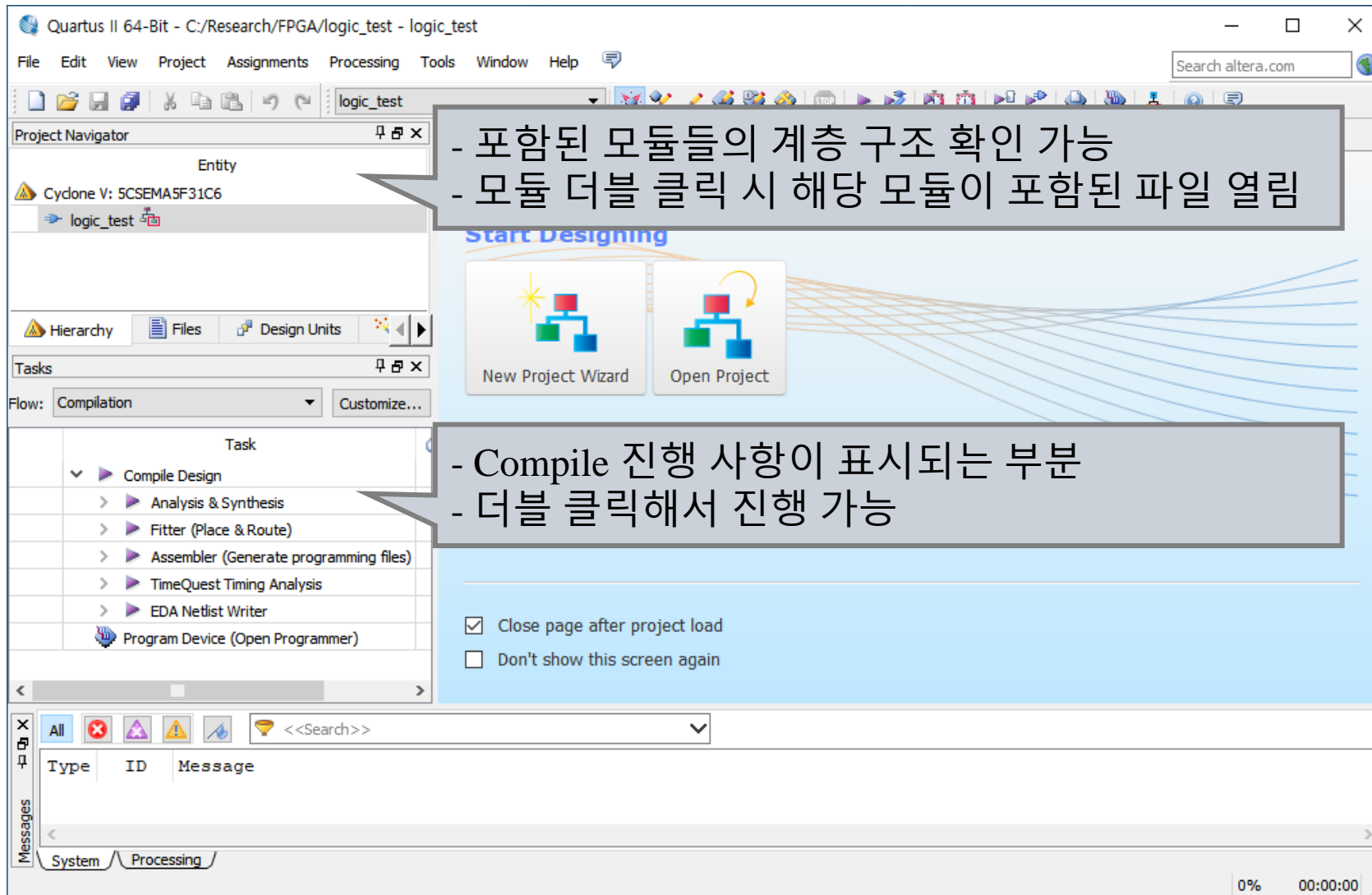
- 프로젝트 생성 후 qsf 파일의 내용



```
38
39 set_global_assignment -name FAMILY "Cyclone V"
40 set_global_assignment -name DEVICE 5CSEMA5F31C6
41 set_global_assignment -name TOP_LEVEL_ENTITY logic_test
42 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 13.1
43 set_global_assignment -name PROJECT_CREATION_TIME_DATE "17:14:24 AUGUST 31, 2022"
44 set_global_assignment -name LAST_QUARTUS_VERSION 13.1
45 set_global_assignment -name VERILOG_FILE ../../SIM/logicTest/logic_test.v
46 set_global_assignment -name PROJECT_OUTPUT_DIRECTORY output_files
47 set_global_assignment -name MIN_CORE_JUNCTION_TEMP 0
48 set_global_assignment -name MAX_CORE_JUNCTION_TEMP 85
49 set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 256
50 set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim-Altera (Verilog)"
51 set_global_assignment -name EDA_OUTPUT_DATA_FORMAT "VERILOG HDL" -section_id eda_simulation
~
~
```

프로젝트 생성

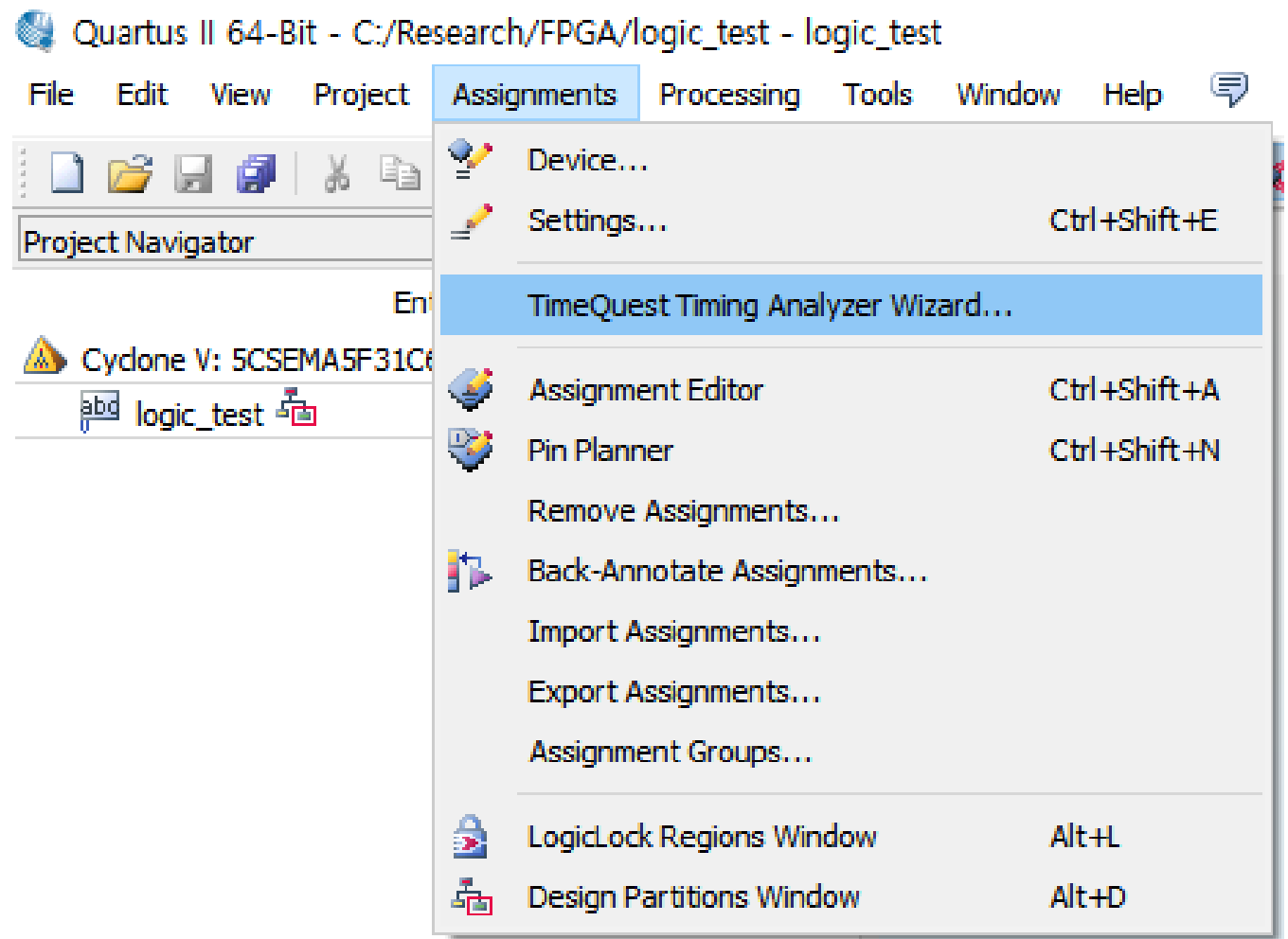
● 완료 후 창



Timing Constraints 설정

- TimeQuest Timing Analyzer Wizard

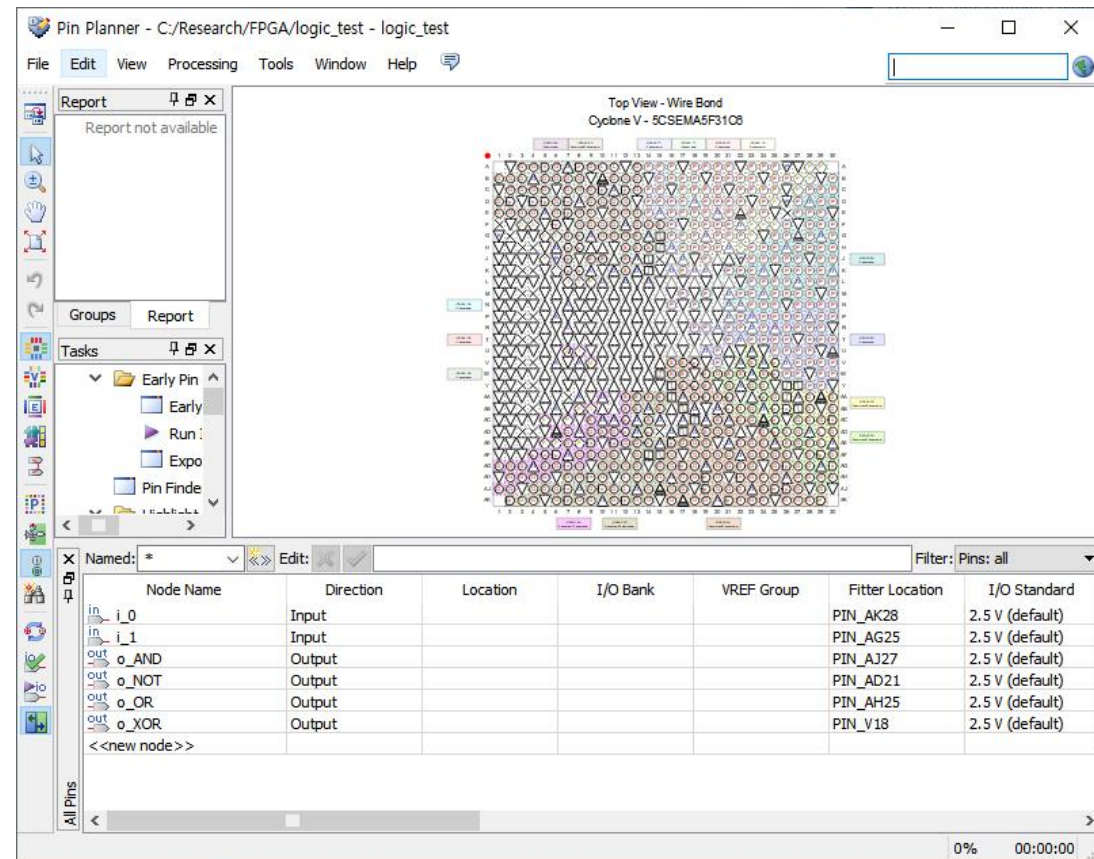
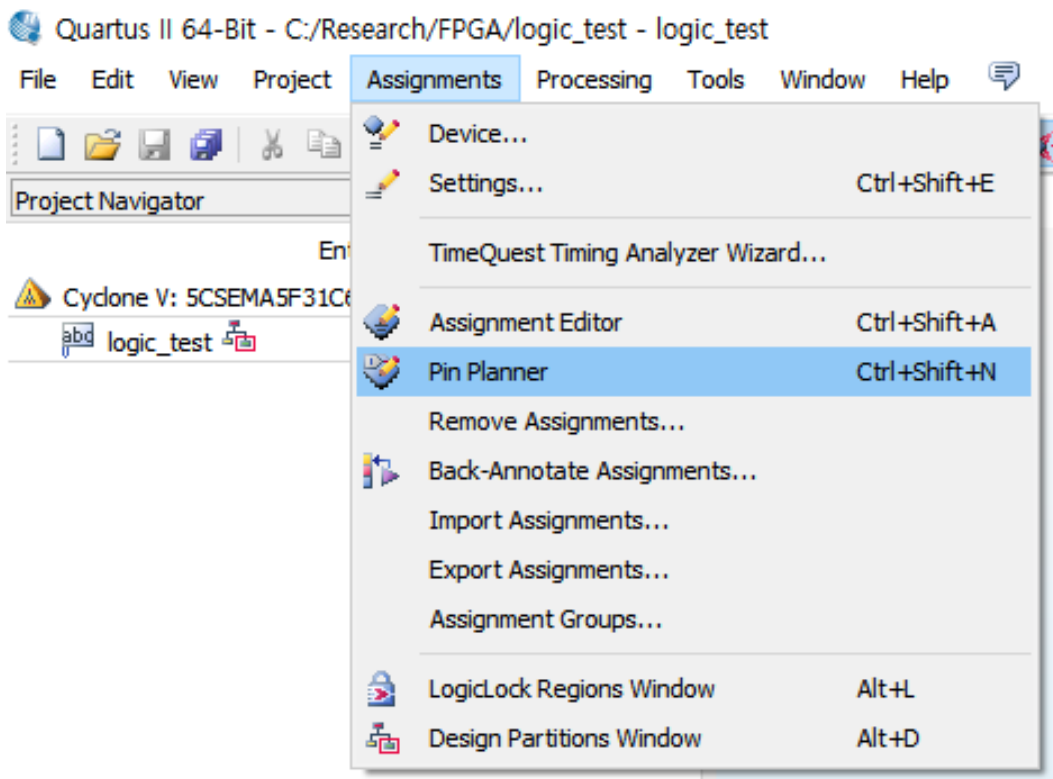
- Sequential logic의 경우
 설정 필요
- 추후 설명 예정



Pin 설정

● Pin Planner 시작 방법

- Assignments – Pin Planner 클릭



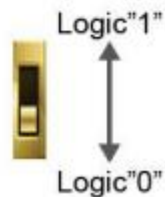
Pin 설정

- 참고) Switch 정보



Table 3-6 Pin Assignments for Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW[0]	PIN_AB12	Slide Switch[0]	3.3V
SW[1]	PIN_AC12	Slide Switch[1]	3.3V
SW[2]	PIN_AF9	Slide Switch[2]	3.3V
SW[3]	PIN_AF10	Slide Switch[3]	3.3V
SW[4]	PIN_AD11	Slide Switch[4]	3.3V
SW[5]	PIN_AD12	Slide Switch[5]	3.3V
SW[6]	PIN_AE11	Slide Switch[6]	3.3V
SW[7]	PIN_AC9	Slide Switch[7]	3.3V
SW[8]	PIN_AD10	Slide Switch[8]	3.3V
SW[9]	PIN_AE12	Slide Switch[9]	3.3V



Pin 설정

- 참고) LED 정보



Table 3.8 Pin Assignments for LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR[0]	PIN_V16	LED [0]	3.3V
LEDR[1]	PIN_W16	LED [1]	3.3V
LEDR[2]	PIN_V17	LED [2]	3.3V
LEDR[3]	PIN_V18	LED [3]	3.3V
LEDR[4]	PIN_W17	LED [4]	3.3V
LEDR[5]	PIN_W19	LED [5]	3.3V
LEDR[6]	PIN_Y19	LED [6]	3.3V
LEDR[7]	PIN_W20	LED [7]	3.3V
LEDR[8]	PIN_W21	LED [8]	3.3V
LEDR[9]	PIN_Y21	LED [9]	3.3V

Pin 설정

● Location 설정

Table 3-6 Pin Assignments for Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW[0]	PIN_AB12	Slide Switch[0]	3.3V
SW[1]	PIN_AC12	Slide Switch[1]	3.3V
SW[2]	PIN_AF9	Slide Switch[2]	3.3V
SW[3]	PIN_AF10	Slide Switch[3]	3.3V
SW[4]	PIN_AD11	Slide Switch[4]	3.3V
SW[5]	PIN_AD12	Slide Switch[5]	3.3V
SW[6]	PIN_AE11	Slide Switch[6]	3.3V
SW[7]	PIN_AC9	Slide Switch[7]	3.3V
SW[8]	PIN_AD10	Slide Switch[8]	3.3V
SW[9]	PIN_AE12	Slide Switch[9]	3.3V

Table 3-8 Pin Assignments for LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR[0]	PIN_V16	LED [0]	3.3V
LEDR[1]	PIN_W16	LED [1]	3.3V
LEDR[2]	PIN_V17	LED [2]	3.3V
LEDR[3]	PIN_V18	LED [3]	3.3V
LEDR[4]	PIN_W17	LED [4]	3.3V
LEDR[5]	PIN_W19	LED [5]	3.3V
LEDR[6]	PIN_Y19	LED [6]	3.3V
LEDR[7]	PIN_W20	LED [7]	3.3V
LEDR[8]	PIN_W21	LED [8]	3.3V
LEDR[9]	PIN_Y21	LED [9]	3.3V

Named: *

Edit:

Filter: Pins: all

	Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
<div>in</div> <div></div>	i_0	Input	PIN_AB12	3A	B3A_N0	PIN_AK28	2.5 V (default)
<div>in</div> <div></div>	i_1	Input	PIN_AC12	3A	B3A_N0	PIN_AG25	2.5 V (default)
<div>out</div> <div></div>	o_AND	Output	PIN_V16	4A	B4A_N0	PIN_AJ27	2.5 V (default)
<div>out</div> <div></div>	o_NOT	Output	PIN_W16	4A	B4A_N0	PIN_AD21	2.5 V (default)
<div>out</div> <div></div>	o_OR	Output	PIN_V17	4A	B4A_N0	PIN_AH25	2.5 V (default)
<div>out</div> <div></div>	o_XOR	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V (default)

- Location 설정 - 변경된 qsf 파일

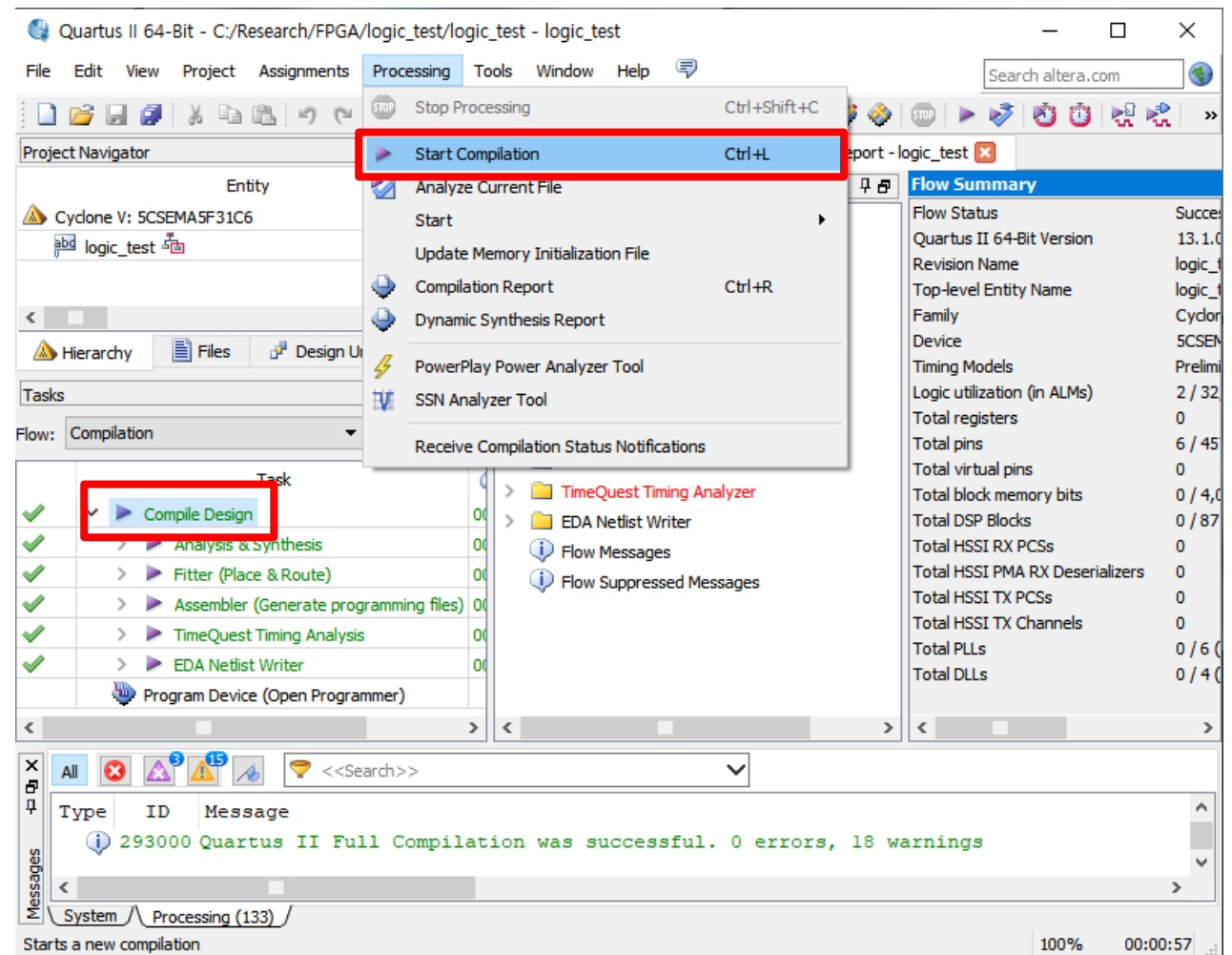
```
57 set_location_assignment PIN_AB12 -to i_0
58 set_location_assignment PIN_AC12 -to i_1
59 set_location_assignment PIN_U16 -to o_AND
60 set_location_assignment PIN_W16 -to o_NOT
61 set_location_assignment PIN_U17 -to o_OR
62 set_location_assignment PIN_U18 -to o_XOR
```

- 핀 정보가 추가됨
- Pin planner 없이 qsf 파일 수정만으로도 설정 가능

Compile

- Compile 방법

- Compile 창에서 더블 클릭
- Processing – Start Compilation 클릭



Compile

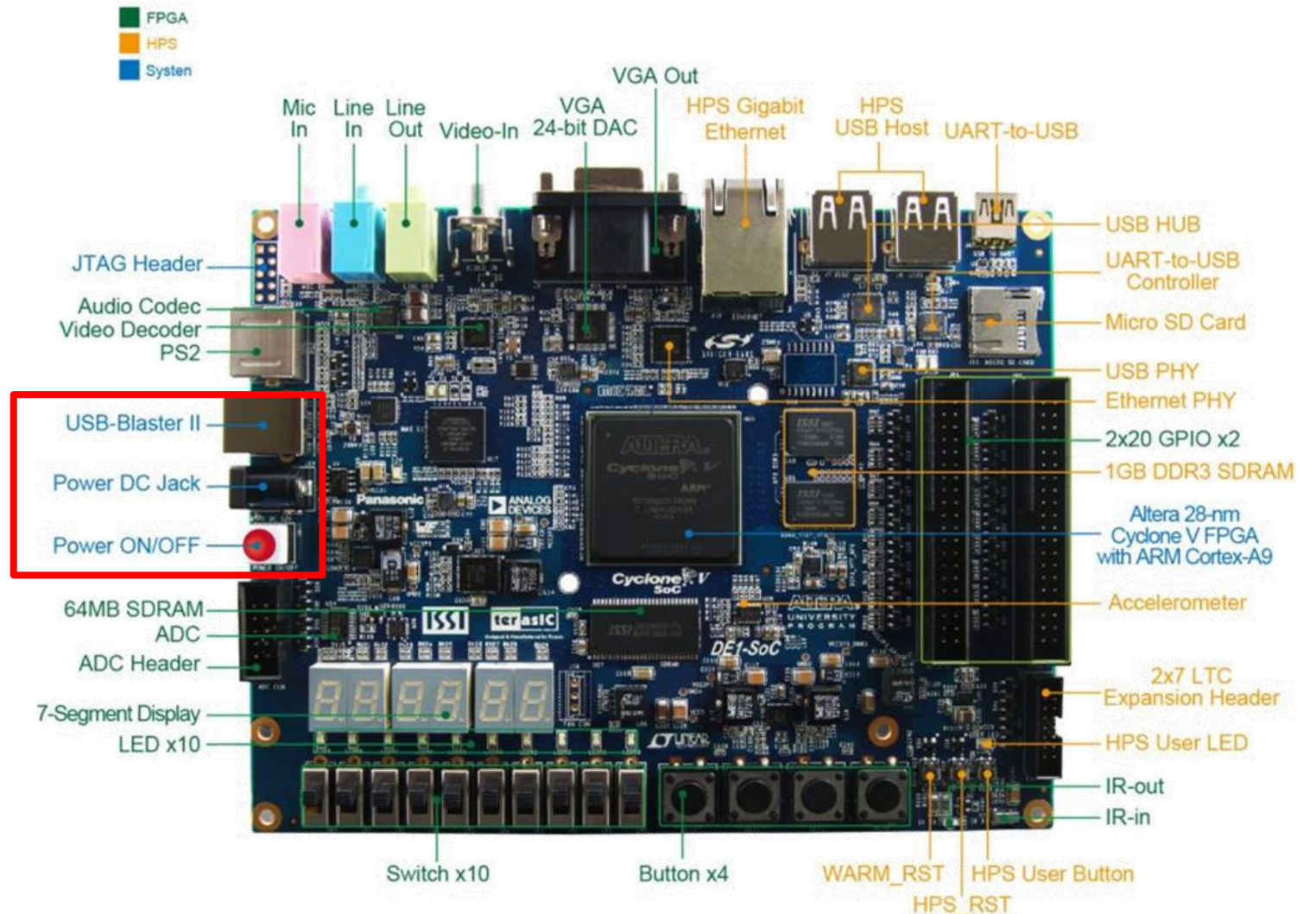
- 완료 후 화면
 - 사용 자원량 등이 보고됨

Flow Summary

Flow Status	Successful - Wed Aug 31 17:27:04 2022
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Web Edition
Revision Name	logic_test
Top-level Entity Name	logic_test
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Preliminary
Logic utilization (in ALMs)	2 / 32,070 (< 1 %)
Total registers	0
Total pins	6 / 457 (1 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI TX Channels	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

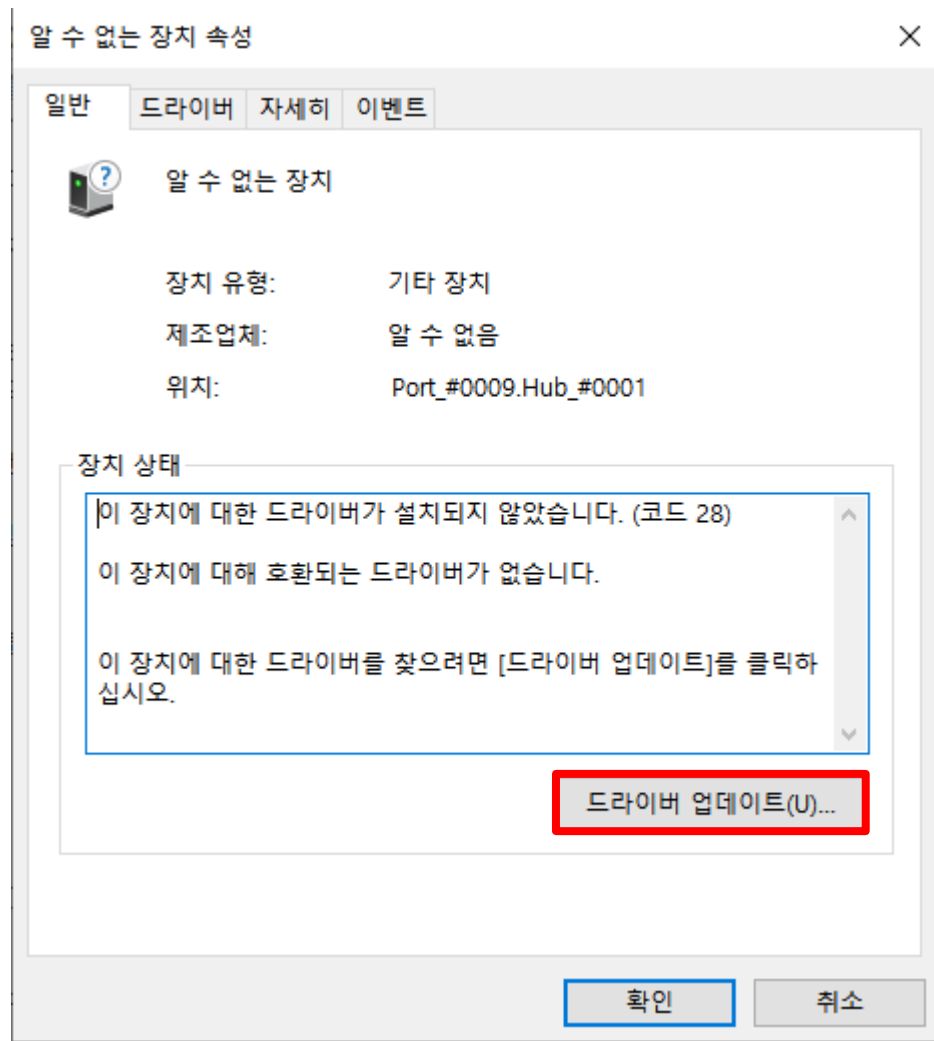
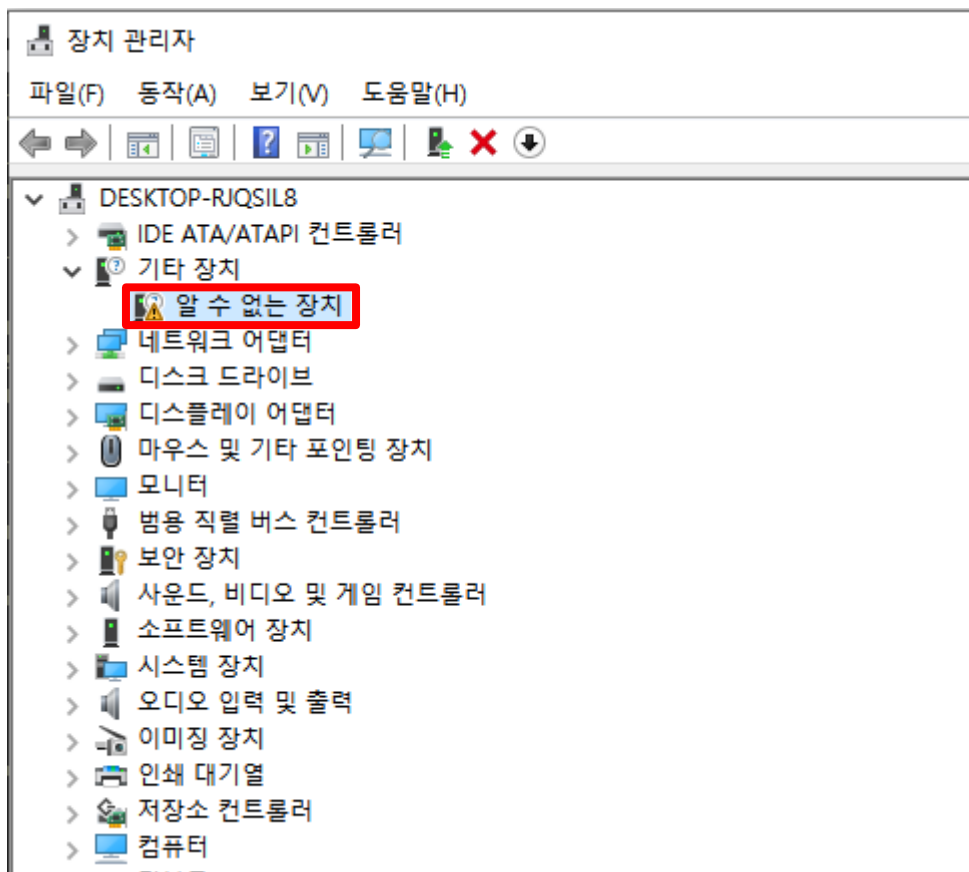
Program Device

- FPGA 설정
 - 전원 연결
 - USB-Blaster II 연결
 - 전원 ON



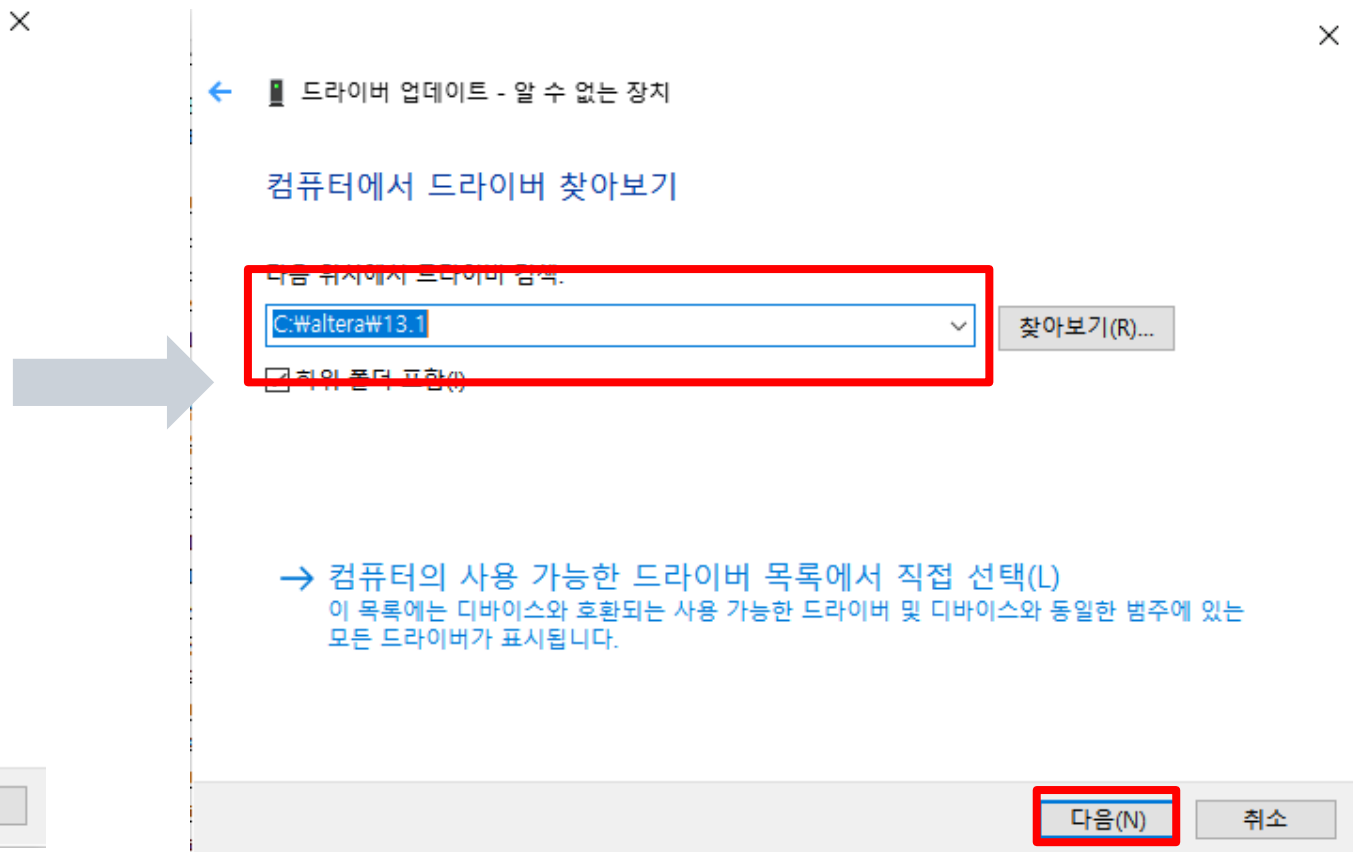
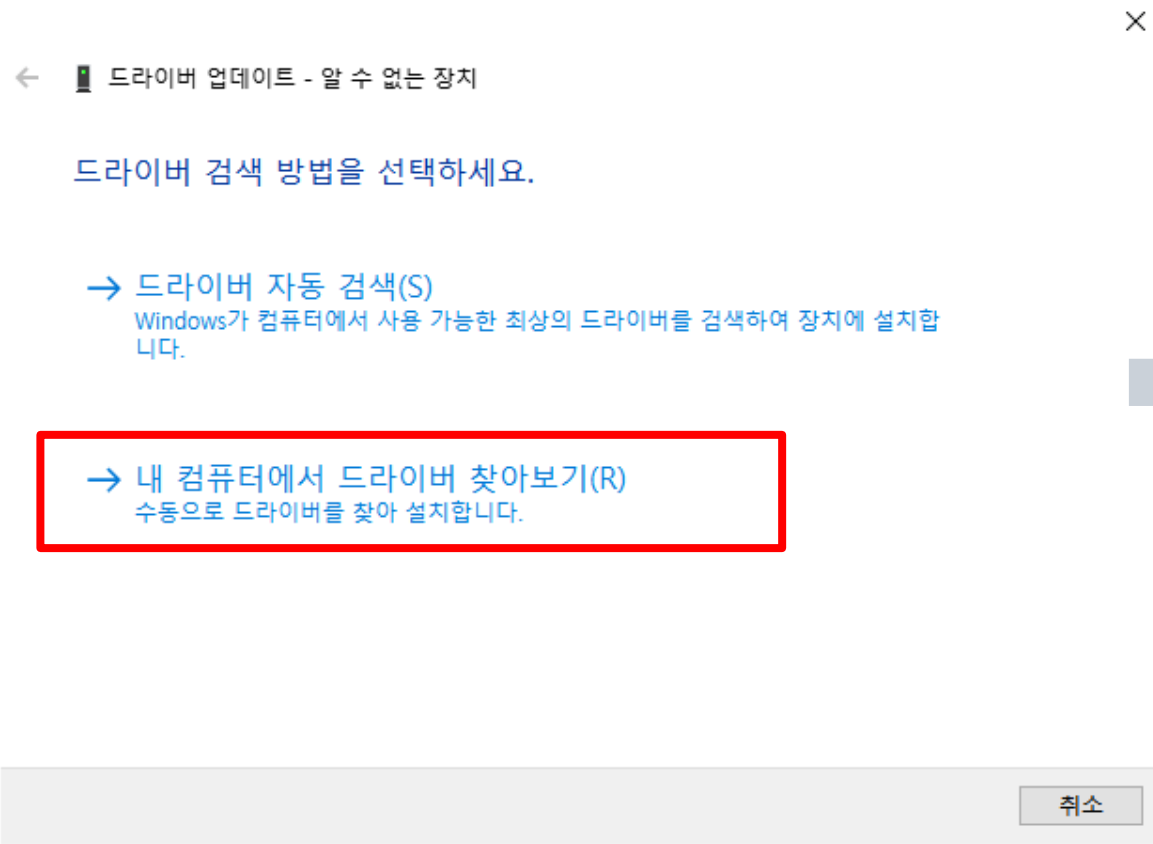
Program Device

● USB-Blaster 설치



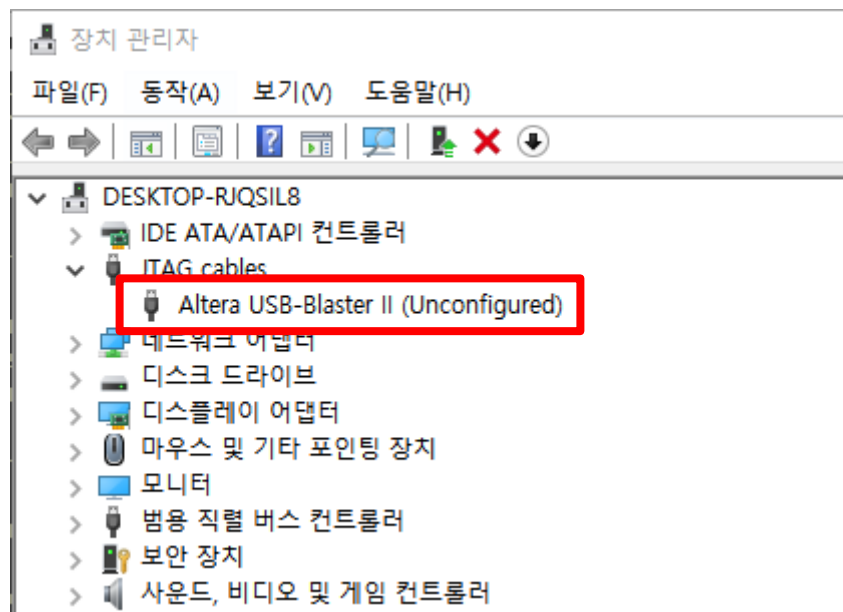
Program Device

● USB-Blaster 설치



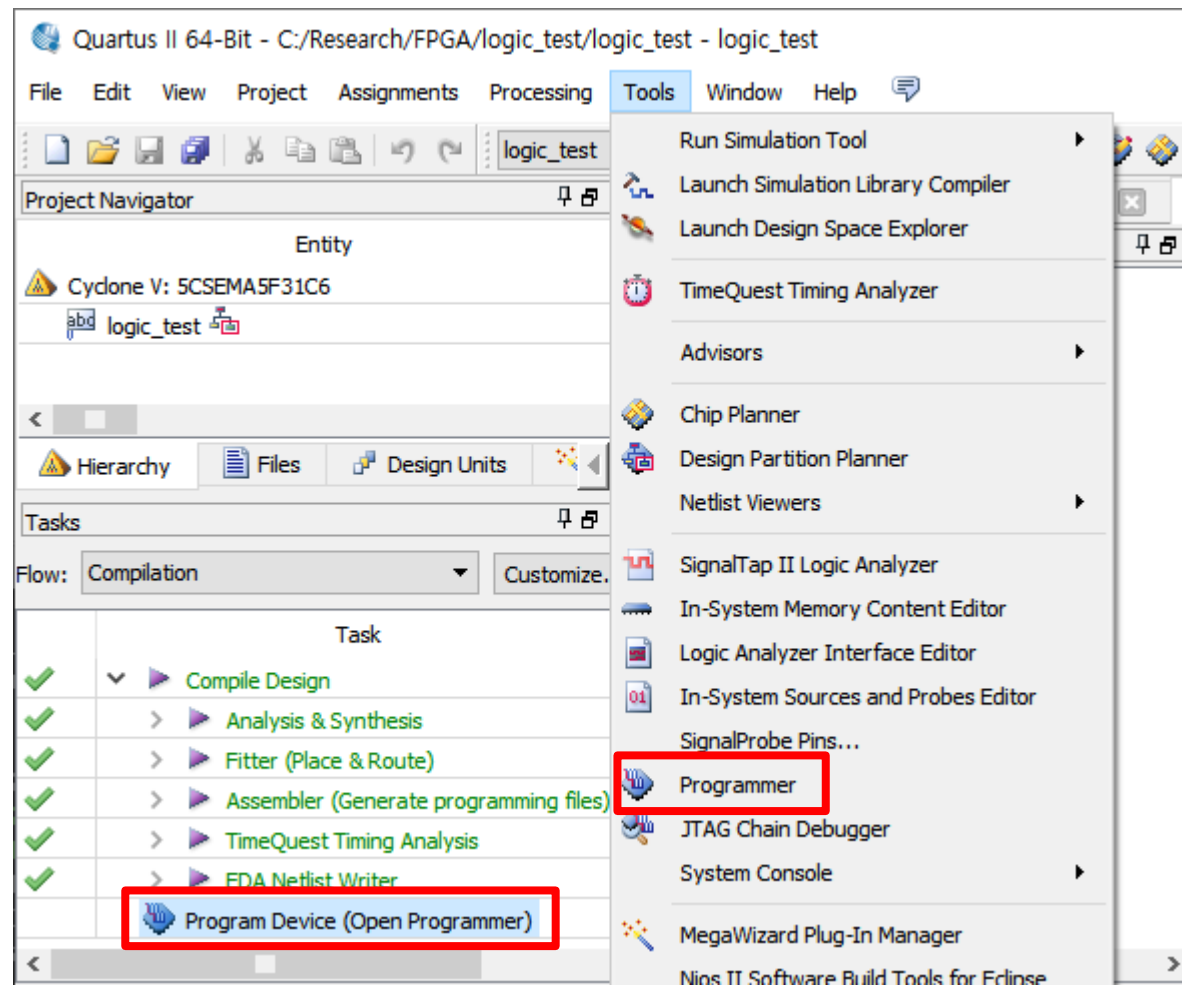
Program Device

- USB-Blaster 설치 - 완료 후



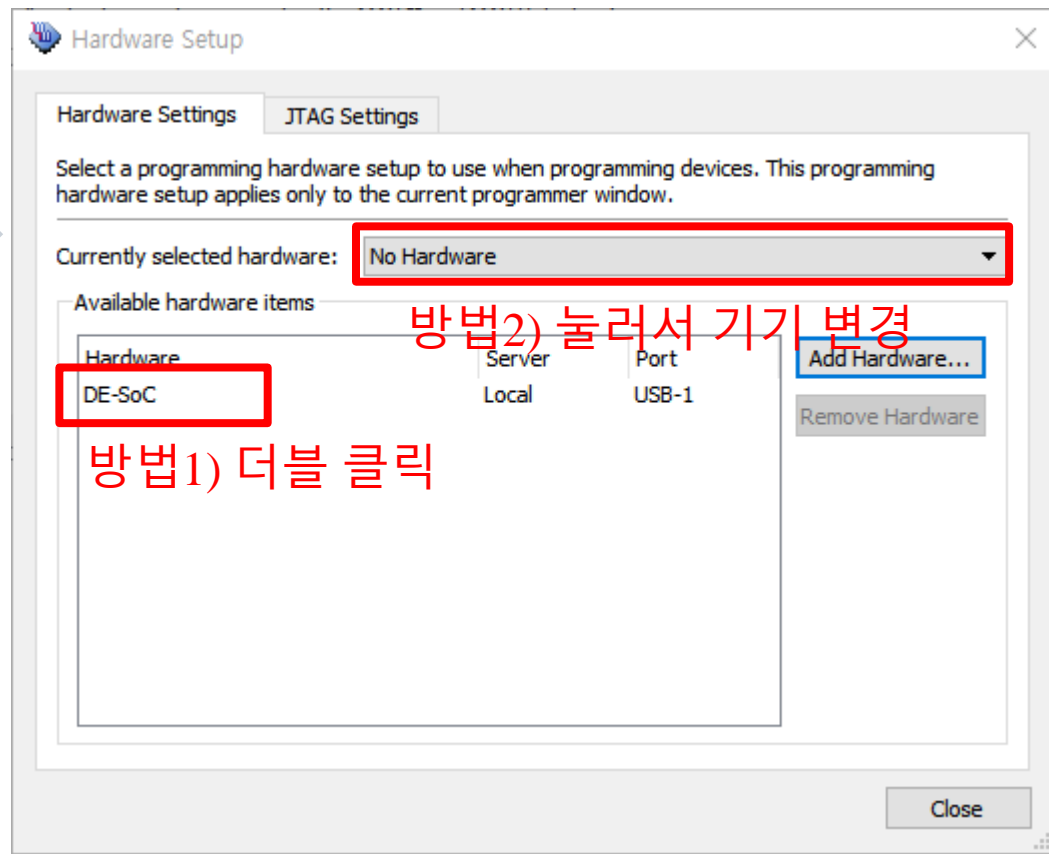
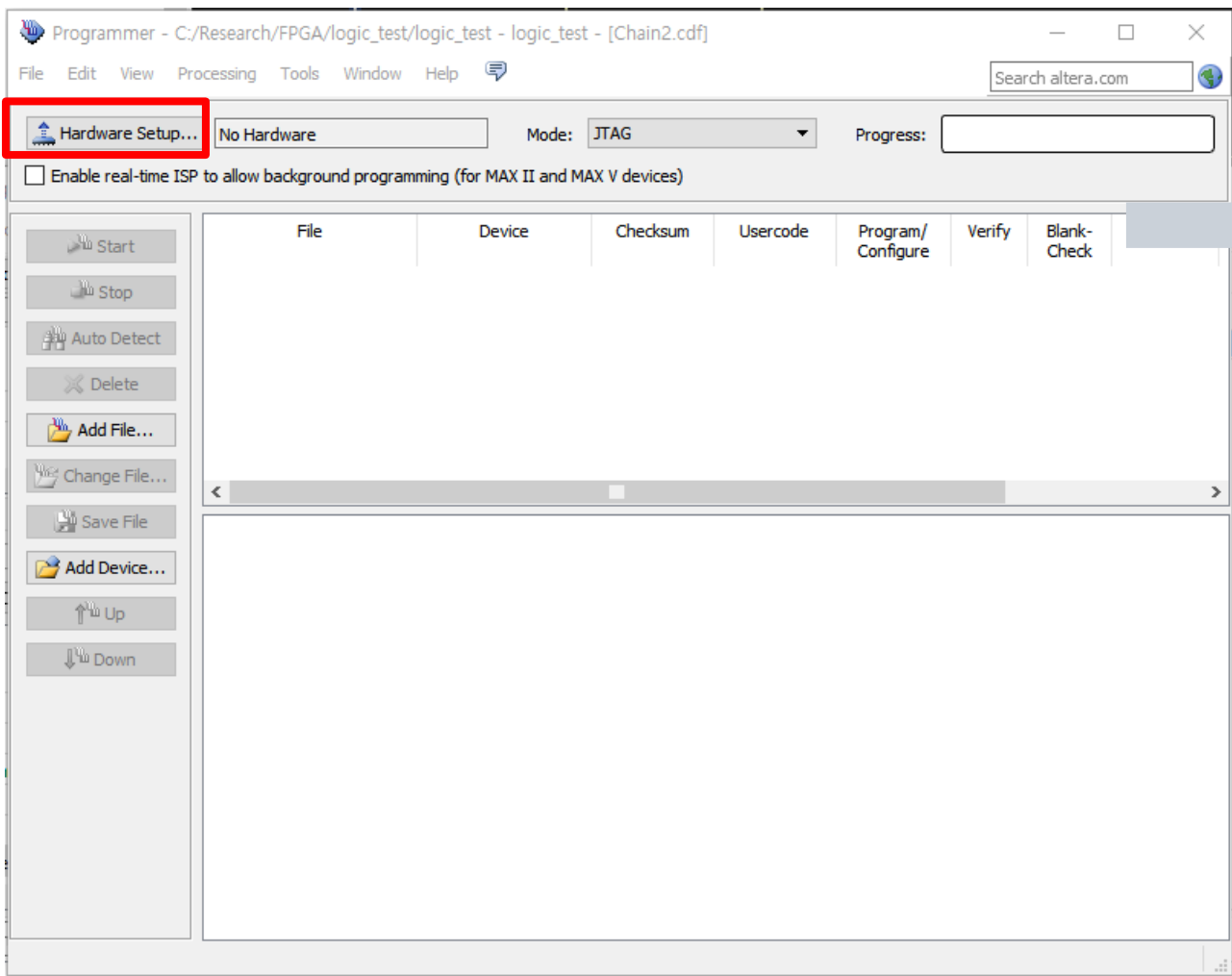
Program Device

- Programmer 실행 방법
 - Compile 창에서 Program Device 더블 클릭
 - Tools – Programmer 클릭



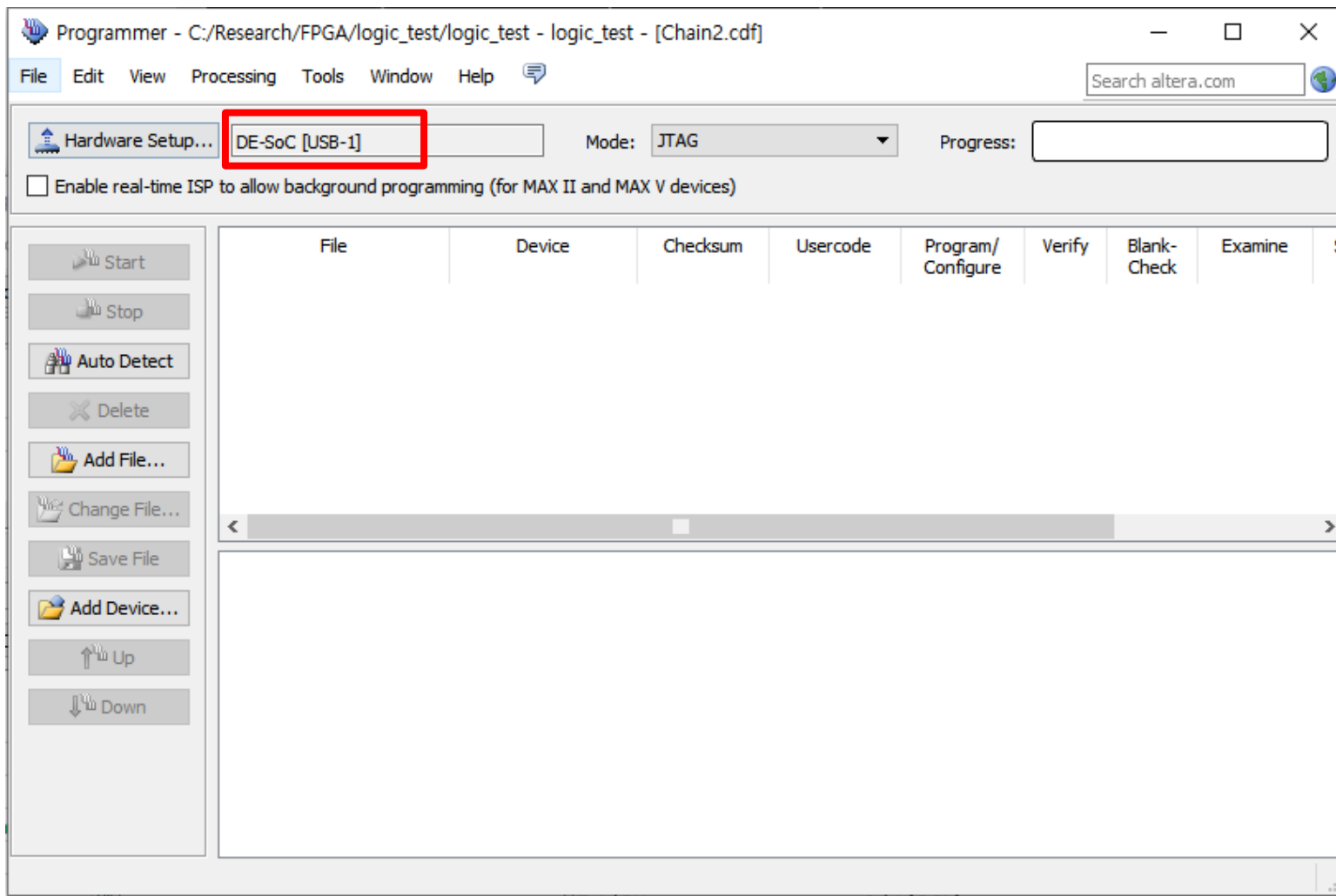
Program Device

● Hardware Setup



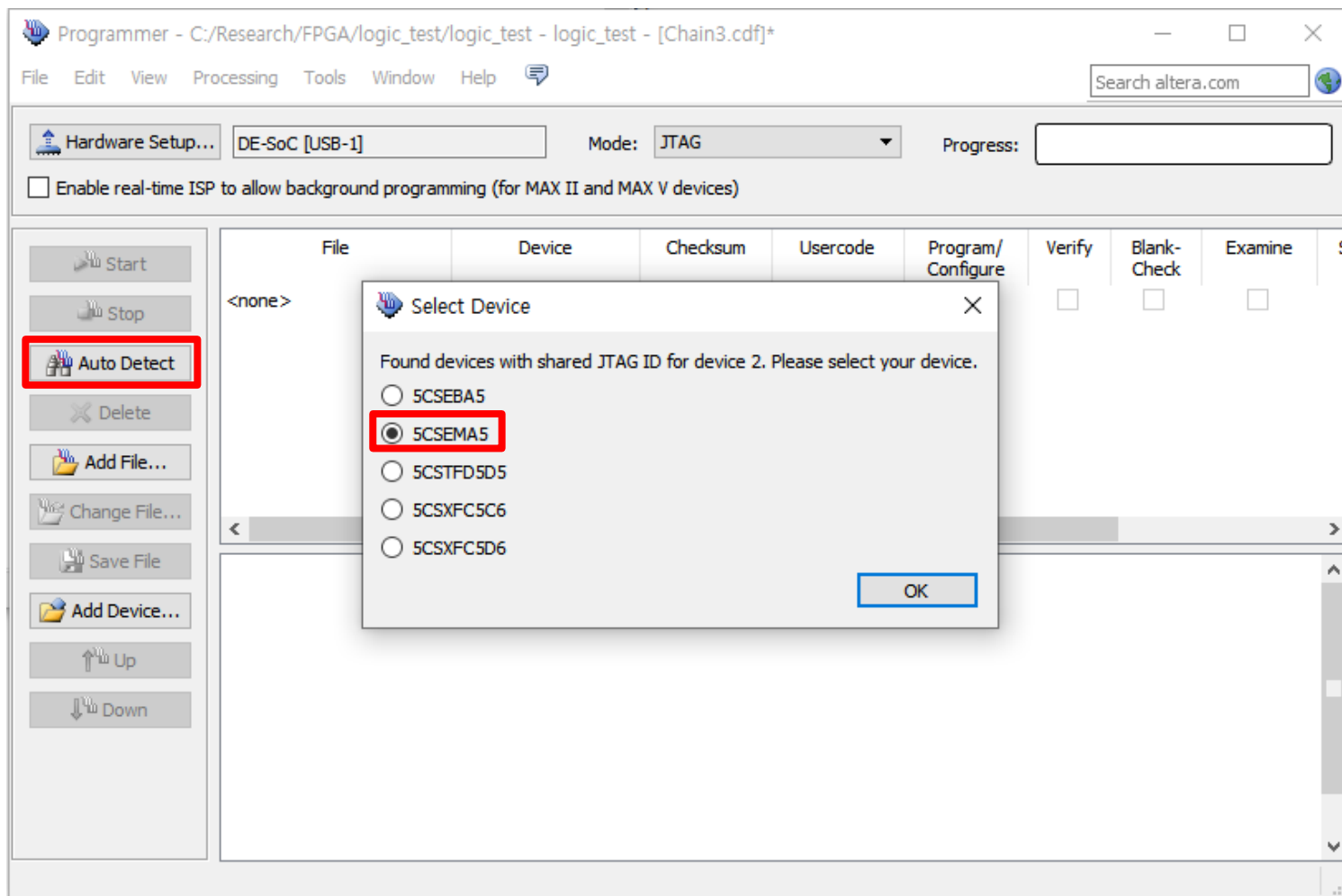
Program Device

- Hardware Setup - 완료 후 화면



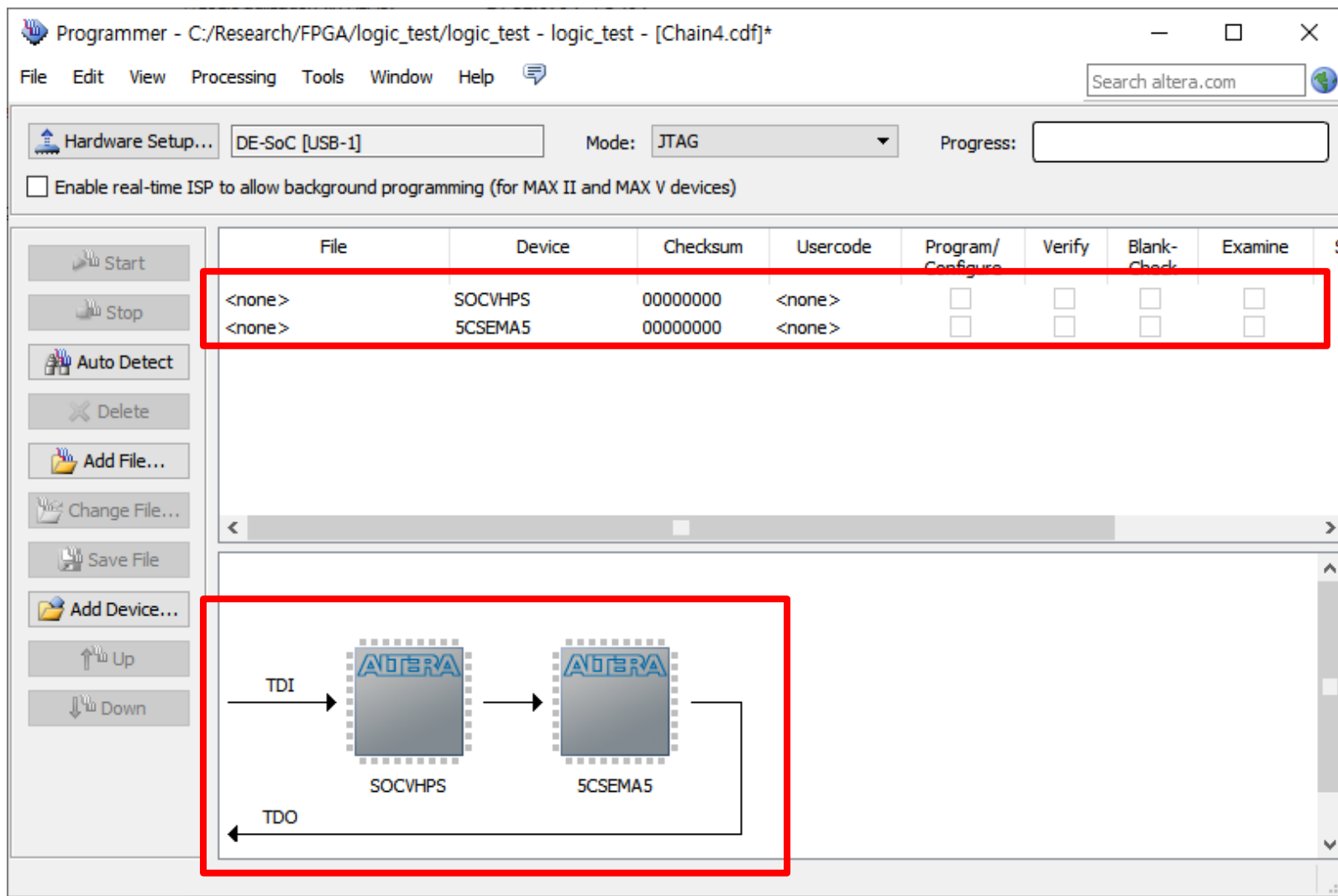
Program Device

- 연결된 보드에서의 칩셋 선택
 - Auto Detect → 5CSEMA5



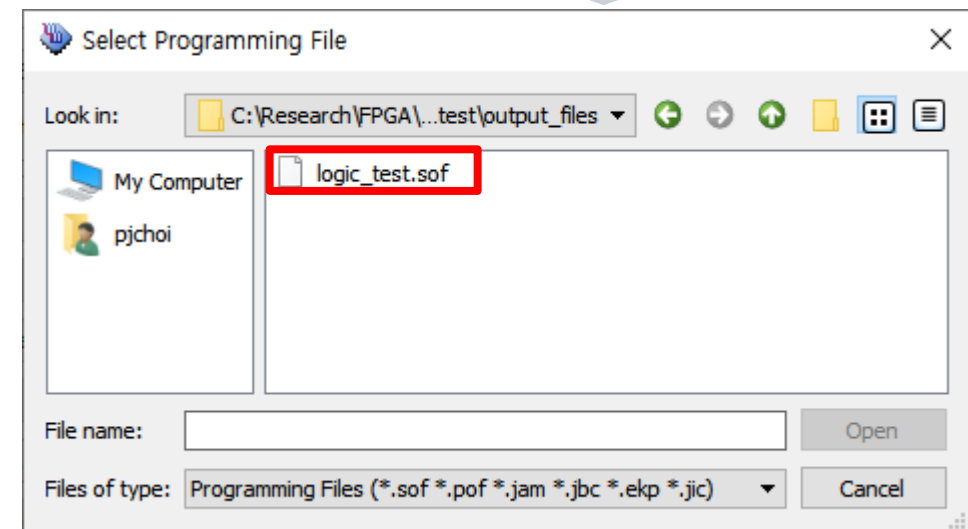
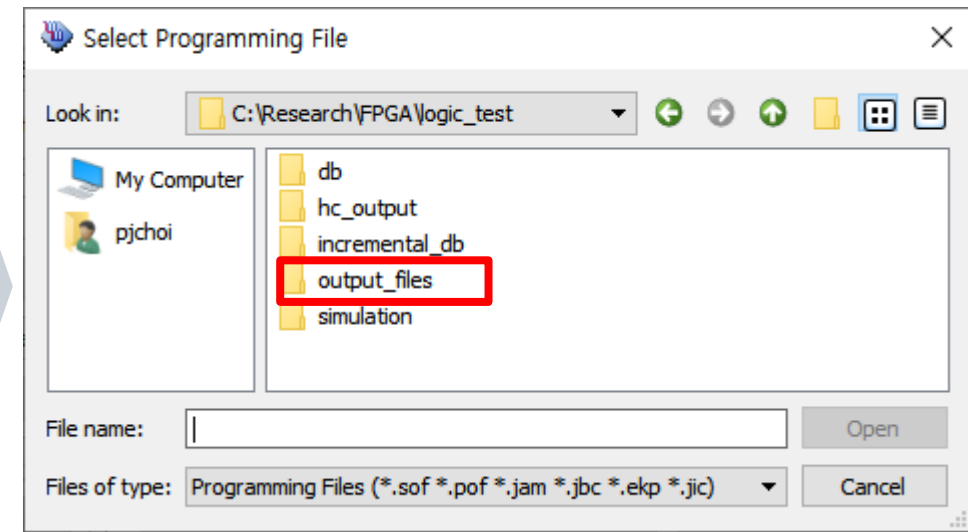
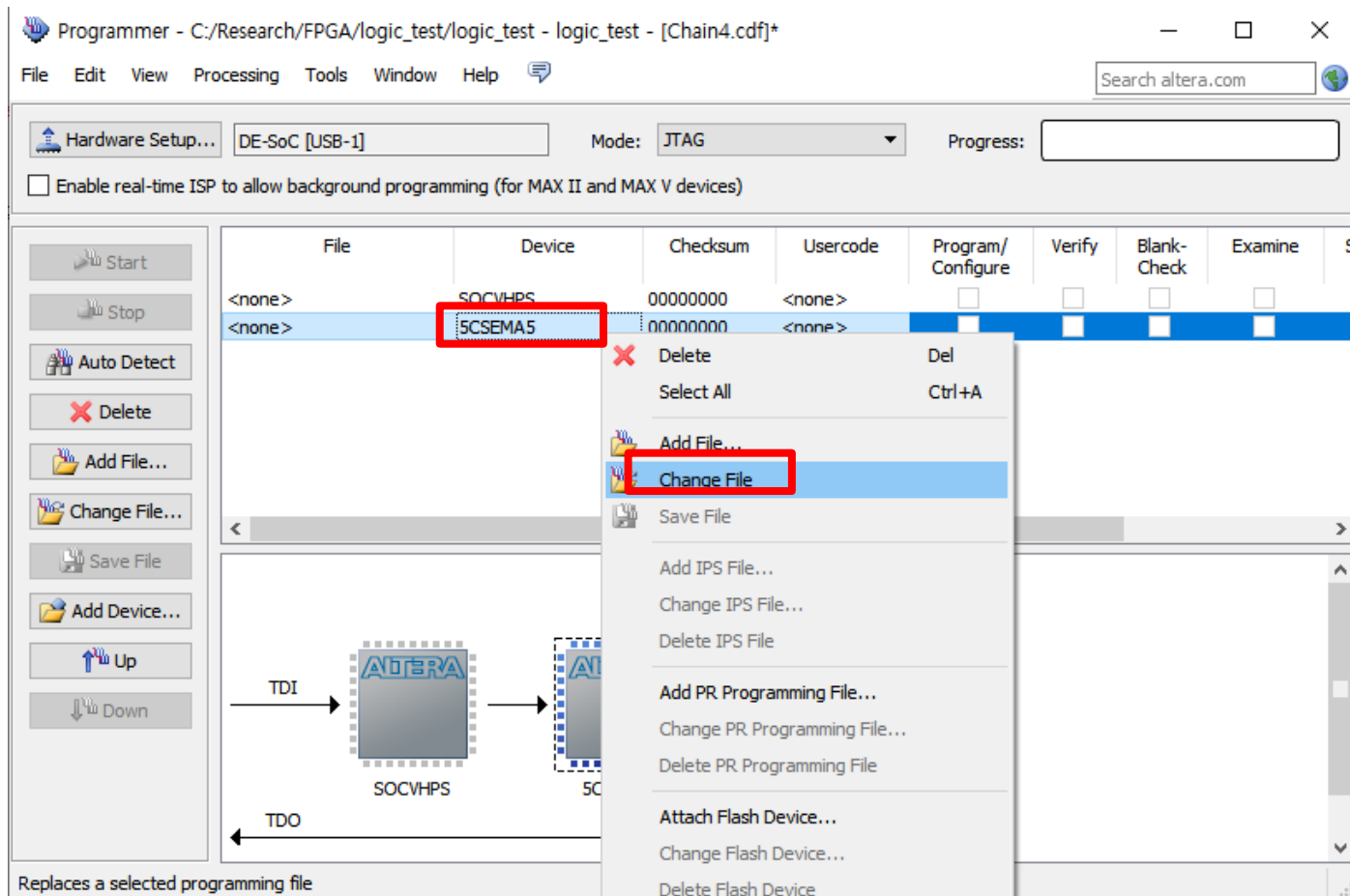
Program Device

- 연결된 보드에서의 칩셋 선택 – 완료 후 화면



Program Device

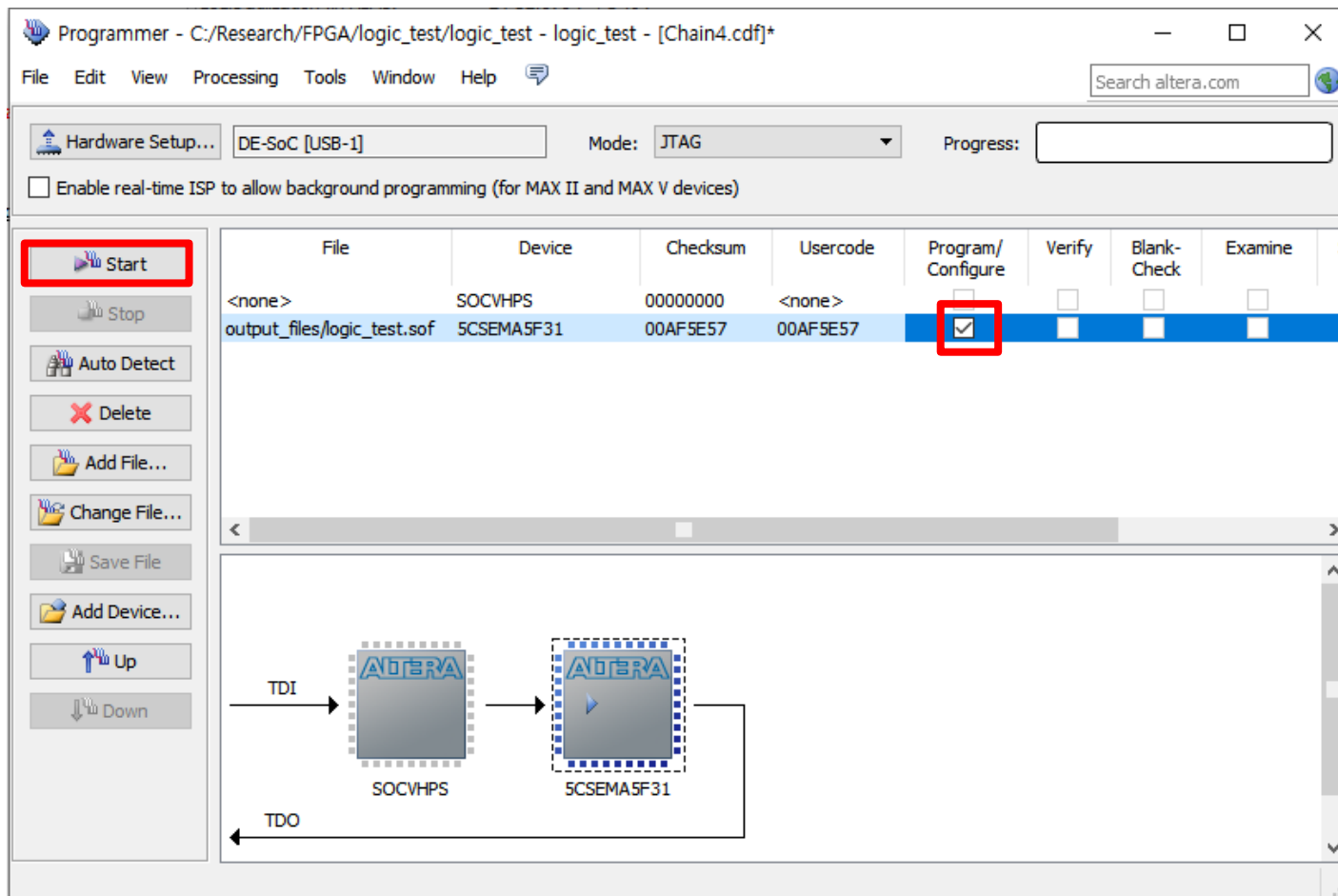
- Program할 파일 선택
 - 5CSEMA5 선택 → Change File



Program Device

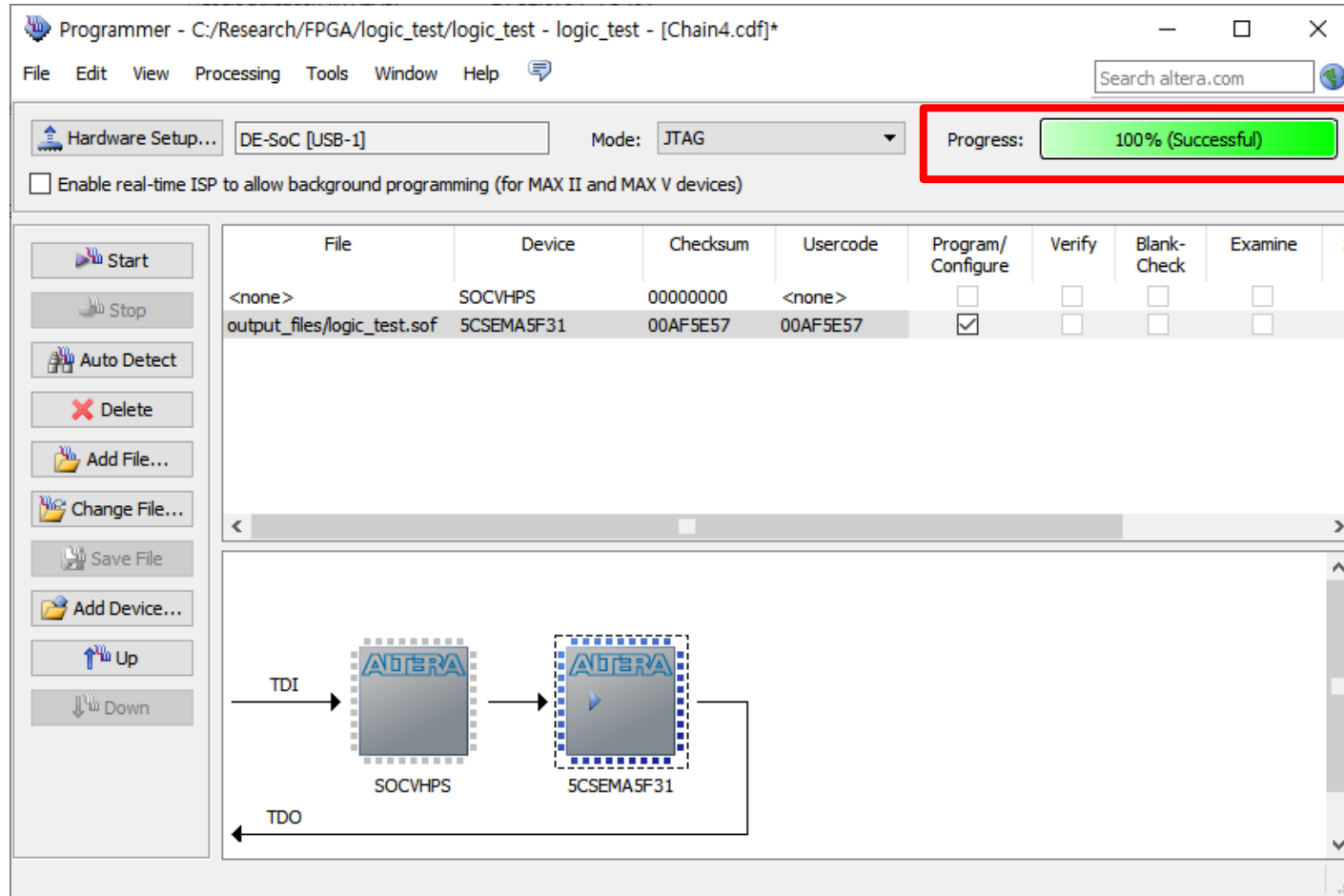
- Program

- Program/Configure 체크 ➔ Start



Program Device

- Program - 성공한 경우 화면



➔ FPGA를 직접 제어하면서 동작 확인