Apt 110, 402 Northwestern
West Lafayette, IN – 47906
Contact Number: (765) 772 8212
Email: sekale@purdue.edu

Siddhant Ekale

Github: https://github.com/sekale
LinkedIn:www.linkedin.com/in/siddhantekale
Personal: https://sekale.github.io/

Education

Purdue University — Senior, Computer Engineering — GPA: 3.52/4.00

Work Experience

Software Engineering Intern — Lutron Electronics, Coopersburg, PA — June 6th – Aug 12th, 2016

- Optimized firmware update algorithms to support up to a 2x speed improvement. Worked on ICD Cold-Fire microcontroller device specific code (in 'C') and integrated it with a Win-forms application.
- Win-forms application developed for firmware update support, with approved code architecture (.NET 4.5, VS 2015)
- Led weekly design and code reviews, accomplished two internal releases for the application (built from scratch).

Teaching Assistant — Purdue (Computer Architecture) — Fall 2016

- Assisted students in debugging design specific questions for MIPS 32 bit single/pipelined/cached/multicore processor

Teaching Assistant — Purdue (Introduction to C) — Spring 2015

- Led a lab of 30 students, setting assignments, and briefing important concepts (mainly arrays and pointers).

Engineering Intern — Extentia Information Technology, Pune — July 10th – Aug 10th, 2014

- Developed (from scratch) Windows Phone 8.0/8.1 applications for client. (.NET 4.5)
- OCR Integration using a proprietary library into current functioning project. (WP 8.1 App)

Projects

Team — Hackathon: *(Intel, First Prize)* — UIUC 2016

- Built a server side game controller by integrating it with Intel Edison processor, interfaced with accelerometer.
- Role: Calibrating the accelerometer by writing code to interpret <x, y, z> values and set appropriate flags to interface with JavaScript game app as well as helping Django server configurations.

Team — MIPS 32-bit Processor Design — Purdue 2016

- Single Cycle Design and Implementation (Individual)
- Pipelined design for parallel execution of instructions (Hazard Detection and Branch Prediction)
- Cache Interface (I-Cache & D-Cache), *Multicore* processor implementation with coherence controller. *(MSI Protocol)*
- My Contribution (Design and Implementation): Pipelined data-path, Cached interface, Branch prediction.

Individual — Project Glass — Purdue 2016

- Wearable gear designed for displaying Android Notifications on an OLED projected in front of the eye.
- Weather data extraction using API, SPI interfaced for OLED, Bluetooth LE interfaced for duplex communication

Team — Purdue SOC Design Team — Purdue 2016

- Worked on implementing a Platform Level Interrupt Controller for a RISC-V core implementation
- Wrote UART software driver for the SOC equipped with interrupt handlers and call back functions.

Team — Compiler Design — Purdue 2016

- Built a fully functional compiler using ANTLR, for custom "LITTLE" language.
- Wrote code for converting Intermediate Code to MIPS Assembly, register allocation using dataflow analysis.

Leadership and Academic Achievements

- Semester Honors (Fall '13, Spring '14, Fall '14, Fall '15, Spring '16)
- EPICS: Lead Lafayette Crisis Center Project (Developed database architecture for maintaining employee records)

Relevant Coursework: Algorithms, Compilers, Computer Architecture, Signals and Systems

Skills and Tools: C, C++, C#, Java, Python, Bash, System Verilog, VC using Git, JIRA