# Aleksandar N. **Vuković**

Design Engineer · Analog RF/mmwave IC

*Belgrade, Republic of Serbia*

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## Education

**School of Electrical Engineering, University of Belgrade** — *Belgrade, Serbia*

M.Sc. in Computer Science and Engineering — *Oct 2018 - Sep 2021*

- Master's thesis: All-digital RF Transceiver Based on Parallel and Approximative DSM

**School of Electrical Engineering, University of Belgrade** — *Belgrade, Serbia*

B.Sc. in Computer Science and Engineering — *Oct 2014 - Sep 2018*

- Bachelor's thesis: 1 GHz Low Noise Phase-Frequency Detector and Charge Pump

## Skills

| | |
|---|---|
| **Programming languages/scripting** | C/C++, Python, TeX, *nix shell |
| **NI AWR Design Environment** | Microwave Office |
| **Cadence Custom IC** | Virtuoso Platform, schematic entry, custom layout, physical verification, extraction |
| **Cadence Spectre X** | Simulator, RF Option, APS |
| **Cadence EM simulator** | EMX Planar 3D Solver |
| **Mentor Graphics** | Calibre IC Verification: nmDRC, nmLVS, xRC |
| **Keysight PathWave Design** | Momentum |
| **Operating systems** | GNU/Linux, Microsoft Windows |
| **Languages** | Serbian, English |

## Projects

**Flash Analog Digital Converter** — *Ethernet IEEE 802.3*

TSMC 40 nm LP CMOS technology — *Jun 2023 - Sep 2023*

- Redesign of 250 MS/s ADC to have more supply voltage
- Verification of ADC and comparator redesign, Monte Carlo ENOB
- LDO transient simulations, under current load

**LC Class C Voltage Controlled Oscillator (6.3 - 13.7 GHz )** — *LO block VCO*

TSMC 40 nm CMOS technology — *Sep 2022 - Dec 2022*

- Improving phase noise and frequency pushing. Consists of two cores to cover the LO range
- Gate voltage control feedback ensuring oscillation start up and class C operation

**Ku-band 4 Output Active Power Divider (APD)** — *Ku and Ka band TX - LO distribution*

TSMC 55 nm technology — *May 2021 - Apr 2022*

- Design of both one-stage and two-stage APDs and comparison on schematic level
- Simulated as part of transmitter chain's LO distribution for isolation between outputs
- KuKa-band One Input Two Output Balun for LO Mixer Ku and Ka inputs
- Parts of passive layout structures simulated using both EMX and ADS simulators

**All-digital RF Transceiver Based on Parallel and Approximative DSM** — *All-Digital Delta-Sigma Modulators*

python scripts — *Jun 2021 - Oct 2021*

- Behaviour and application of parallel and approximative DSMs is tested using python language
- Parallel and approximative DSMs can generate RF signals on significantly higher frequencies comparing to the conventional DSM, with minimal signal degradation
- All-digital transceivers, delta-sigma modulation (DSM)

**Active-RC Filter and its Operational Amplifier** — *Ku and Ka band TX - Low Pass Filter*

TSMC 55 nm technology — *Dec 2020 - May 2021*

- Design of High Unity Gain-Bandwidth Operational Amplifier on schematic level
- Simulating different operational amplifiers in active-RC filter topologies like Rauch and Ackerberg-Mossberg with bandwith of 250 MHz
- Comparison of different topoologies in noise performance and limitations of the finality of uGBW

### 8 GHz Low Noise Phase Frequency Detector based on Gilbert cell

*Phase Detector*

IHP SiGe 130 nm BiCMOS technology

*Aug 2020 - Sep 2020*

- Simulation of different Gilbert cell based Phase Detectors and different frequency locking techniques on schematic level

### 57 GHz - 64 GHz Voltage Controlled Oscillator

*Radar*

IBM (GF) SiGe 130 nm BiCMOS technology

*Dec 2019 - Mar 2020*

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

### 57 GHz - 64 GHz Active Power Divider

*Radar*

IBM (GF) SiGe 130 nm BiCMOS technology

*Apr 2019 - Nov 2019*

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

### 28 GHz Active Phase Shifter - Vector Modulator

*School project*

IHP SiGe 130 nm BiCMOS technology

*Jan 2019 - Jun 2019*

- Band around 28 GHz (from 26.5 GHz to 29.5 GHz) and controlled by 8-bit ADC simulated on schematic level in Cadence Virtuoso
- Parts of design (all-pass filter, matching networks) EM simulated using ADS Momentum

### 1 GHz Low Noise Phase-Frequency Detector and Charge Pump

*PLL block*

IHP 130 nm BiCMOS technology

*May 2018 - Nov 2018*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

### Phase-Frequency detector, CP and Divider as blocks of MDLL

*Multiplying Delay Locked Loop*

TSMC CMOS i think

*Oct 2018 - Dec 2018*

- Schematic and layout redesign of PFD, CP, divider with surrounding circuits

### High Gain Operational Transconductance Amplifier

*OTA*

IHP 130 nm BiCMOS technology

*Mar 2018 - May 2018*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

### Small Signal GSM 1800 MHz Amplifier

*Wi-Fi Band Amplifier*

Microstrip technology

*Dec 2017 - Jan 2018*

- Schematic design using Microwave office
- Layout design using Altium Designer
- Verification via measurement

### Custom IC layout for the Configurable IIR Filter

*Digital Circuitry*

TSMC 180 nm technology

*Mar 2017 - May 2017*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

## Work Experience

### Novelic

*Belgrade, Serbia*

Junior Design Engineer

*February 2018 - 2021*

- First year internship, schematic design, verification, layouting and post-layout verification
- Internal projects, feasibility studies, commercial projects, analog IC design at first, RF/mmwave design later

### Nirsen

*Belgrade, Serbia*

Design Engineer

*2021 - PRESENT*

- Mostly commercial projects both analog IC and RF/mmwave design