Aleksandar N. **Vuković**

Design Engineer · Analog RF/mmwave IC

Belgrade, Republic of Serbia

(+381) 616920298 | aleksandarvukovic@tutanota.com | aleksandar-vuković

Education

School of Electrical Engineering, University of Belgrade

Belgrade, Serbia

M.Sc. in Computer Science and Engineering, module Electronics

Oct 2018 - Sep 2021

- GPA : 10.0/10.0
- Master's thesis: All-digital RF Transceiver Based on Parallel and Approximative Delta Sigma Modulators
- Relevant subjects: Integrated Circuits for Communication Systems, Hardware and Software Signal Processing, Power Electronics 2, Millimeter waves,

School of Electrical Engineering, University of Belgrade

Belgrade, Serbia

B.Sc. in Computer Science and Engineering, module Electronics

Oct 2014 - Sep 2018

- GPA : 8.8/10.0
- Bachelor's thesis: 1 GHz Low Noise Phase-Frequency Detector and Charge Pump
- Relevant subjects: Analog Electronics, Power Electronics, Integrated Circuits Design, Microwave Electronics, Microwave technology

Skills

Programming languages/scripting	Python, TeX, *nix shell
NI AWR Design Environment	Microwave Office
Cadence Custom IC	Virtuoso, schematic entry, custom layout, physical verification, Quantus QRC extraction
Cadence Spectre X	Simulator, RF Option, APS
Functional Modeling	Verilog-A
Mentor Graphics	Calibre IC Layout Verification: nmDRC, nmLVS, xRC
Cadence EM simulator	EMX Planar 3D Solver
Keysight PathWave Design	Momentum
Operating systems	GNU/Linux, Microsoft Windows
Languages	Serbian(native), English(professional)

Projects

Colpitts class B Voltage Controlled Oscillator (6-8 GHz)

PLL

IHP SiGe 130 nm BiCMOS technology

Oct 2023 - Nov 2024

- Cascode VCO class B, resistive biasing for low noise
- Robust amplitude control for VCO output
- Simulating residual phase noise for PLL as closed loop using verilogA VCO model

Flash Analog Digital Converter

Ethernet IEEE 802.3

TSMC 40 nm LP CMOS technology

Jun 2023 - Sep 2023

- Redesign of 250 MS/s ADC to have higher supply voltage
- Verification of ADC and comparator redesign, Monte Carlo ENOB
- LDO transient simulations, under current load

LC Class C Voltage Controlled Oscillator (6.3 - 13.7 GHz)

LO block VCO

TSMC 40 nm CMOS technology

Sep 2022 - Dec 2022

- Improving phase noise and frequency pushing. Consists of two cores to cover the LO range
- Gate voltage control feedback ensuring oscillation start up and class C operation

Ku-band 4 Output Active Power Divider (APD)

Ku and Ka band TX - LO distribution

TSMC 55 nm CMOS technology

May 2021 - Apr 2022

- Design of both one-stage and two-stage APDs and comparison on schematic level
- Simulated as part of transmitter chain's LO distribution for isolation between outputs
- KuKa-band One Input Two Output Balun for LO Mixer Ku and Ka inputs
- Parts of passive layout structures simulated using both EMX and ADS simulators

All-digital RF Transceiver Based on Parallel and Approximative DSM

All-Digital Delta-Sigma Modulators

PYTHON SCRIPTS

Jun 2021 - Oct 2021

- Behavior and application of parallel and approximative DSMs is tested using python language
- Parallel and approximative DSMs generate RF signals on significantly higher frequencies
- Comparison with the conventional DSM, with minimal signal degradation

Active-RC Filter and its Operational Amplifier

Ku and Ka band TX - Low Pass Filter

TSMC 55 NM CMOS TECHNOLOGY

Dec 2020 - May 2021

- Design of High Unity Gain-Bandwidth Operational Amplifier on schematic level
- Simulating different operational amplifiers in active-RC filter different
- Topologies Rauch and Ackerberg-Mossberg with bandwith of 250 MHz
- Comparison of different topologies in noise performance and limitations of the finality of uGBW

8 GHz Low Noise Phase Frequency Detector based on Gilbert cell

Phase Detector

IHP SiGe 130 NM BiCMOS TECHNOLOGY

Aug 2020 - Sep 2020

- Simulation of different Gilbert cell based Phase Detectors and different frequency locking techniques on schematic level

57 - 64 GHz Voltage Controlled Oscillator and Active Power Divider

Radar

IBM (GF) SiGe 130 NM BiCMOS TECHNOLOGY

Apr 2019 - Mar 2020

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

28 GHz Active Phase Shifter - Vector Modulator

School project

IHP SiGe 130 NM BiCMOS TECHNOLOGY

Jan 2019 - Jun 2019

- Band around 28 GHz (from 26.5 GHz to 29.5 GHz) and controlled by 8-bit ADC simulated on schematic level in Cadence Virtuoso
- Parts of design (all-pass filter, matching networks) EM simulated using ADS Momentum

1 GHz Low Noise Phase-Frequency Detector and Charge Pump

PLL block

IHP SiGe 130 NM BiCMOS TECHNOLOGY

May 2018 - Nov 2018

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

Phase-Frequency detector, CP and Divider as blocks of MDLL

Multiplying Delay Locked Loop

TSMC 55 NM CMOS TECHNOLOGY

Oct 2018 - Dec 2018

- Schematic and layout redesign of PFD, CP, divider with surrounding circuits

High Gain Operational Transconductance Amplifier

OTA

IHP SiGe 130 NM BiCMOS TECHNOLOGY

Mar 2018 - May 2018

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L/XL on a QRC-extracted model

Small Signal GSM 1800 MHz Amplifier

School Project - Wi-Fi Band Amplifier

MICROSTRIP TECHNOLOGY

Dec 2017 - Jan 2018

- Schematic design using Microwave office
- Layout design using Altium Designer
- Verification via measurement

Custom IC layout for the Configurable IIR Filter

School project - Digital Circuitry

TSMC 180 NM TECHNOLOGY

Mar 2017 - May 2017

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L/XL on a QRC-extracted model

Work Experience

Novelic

Belgrade, Serbia

JUNIOR DESIGN ENGINEER

February 2018 - 2021

- First year internship, schematic design, verification, custom layout and post-layout verification
- Internal projects, feasibility studies, commercial projects, analog IC design at first, RF/mmwave design later

Nirsen

Belgrade, Serbia

DESIGN ENGINEER

2021 - PRESENT

- Mostly commercial projects both analog IC and RF/mmwave design as presented in experience section