Aleksandar N. **Vuković**

Design Engineer · Analog IC

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Education

School of Electrical Engineering, University of Belgrade — *Belgrade, Serbia*

M.Sc. in Computer Science and Engineering — *Oct 2018 - Sep 2021*

- Master's thesis:

School of Electrical Engineering, University of Belgrade — *Belgrade, Serbia*

B.Sc. in Computer Science and Engineering — *Oct 2014 - Sep 2018*

- Bachelor's thesis:

Skills

Programming languages/scripting	C/C++, Python, TeX, *nix shell
NI AWR Design Environment	Microwave Office
Cadence Custom IC	Virtuoso Platform, schematic entry, custom layout, physical verification, extraction
Cadence Spectre X	Simulator, RF Option, APS
Cadence EM simulator	EMX Planar 3D Solver
Mentor Graphics	Calibre IC Verification: nmDRC, nmLVS, xRC
Keysight PathWave Design	Momentum
Operating systems	GNU/Linux, Microsoft Windows
Languages	Serbian, English

Projects

All-digital RF Transceiver Based on Parallel and Approximative DSM — *All-Digital Delta-Sigma Modulators*

IHP SiGe 130 nm BiCMOS technology — *Jun 2021 - Oct 2021*

- Behaviour and application of parallel and approximative DSMs is tested using python language
- Parallel and approximative DSMs can generate RF signals on significantly higher frequencies comparing to the conventional DSM, with minimal signal degradation

Ku-band 4 Output Active Power Divider (APD)

TSMC 55 nm technology — *May 2021 - Apr 2022*

- Design of both one-stage and two-stage APDs and comparison on schematic level
- Simulated as part of transmitter chain's LO distribution for isolation between outputs
- KuKa-band One Input Two Output Balun for LO Mixer Ku and Ka inputs
- Parts of passive layout structures simulated using both EMX and ADS simulators

Active-RC Filter and its Operational Amplifier

TSMC 55 nm technology — *Dec 2020 - May 2021*

- Design of High Unity Gain-Bandwidth Operational Amplifier on schematic level
- Simulating different operational amplifiers in active-RC filter topologies like Rauch and Ackerberg-Mossberg with bandwith of 250 MHz
- Comparison of different topoologies in noise performance and limiting of the finality of uGBW

8 GHz Low Noise Phase Frequency Detector based on Gilbert cell — *Phase Detector*

IHP SiGe 130 nm BiCMOS technology — *Aug 2020 - Sep 2020*

- Simulation of different Gilbert cell based Phase Detectors and different frequency locking techniques on schematic level

57 GHz - 64 GHz Voltage Controlled Oscillator

IBM (GF) SiGe 130 nm BiCMOS technology — *Dec 2019 - Mar 2020*

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

57 GHz - 64 GHz Active Power Divider

IBM (GF) SiGe 130 nm BiCMOS technology — *Apr 2019 - Nov 2019*

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

28 GHz Active Phase Shifter - Vector Modulator

IHP SiGe 130 nm BICMOS technology — *Jan 2019 - Jun 2019*

- Band around 28 GHz (from 26.5 GHz to 29.5 GHz) and controlled by 8-bit ADC simulated on schematic level in Cadence Virtuoso
- Parts of design (all-pass filter, matching networks) EM simulated using ADS Momentum

1 GHz Low Noise Phase-Frequency Detector and Charge Pump

IHP 130 nm BiCMOS technology — *May 2018 - Nov 2018*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

Phase-Frequency detector, CP and Divider as blocks of MDLL

Multiplying Delay Locked Loop

Novelic — *Oct 2018 - Dec 2018*

- Schematic and layout redesign of PFD, CP, divider with surrounding circuits

High Gain Operational Transconductance Amplifier

IHP 130 nm BiCMOS technology — *Mar 2018 - May 2018*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

Small Signal GSM 1800 MHz Amplifier

Wi-Fi Band Amplifier

Microstrip technology — *Dec 2017 - Jan 2018*

- Schematic design using Microwave office
- Layout design using Altium Designer
- Verification using measurement

Custom IC layout for the Configurable IIR Filter

Digital Circuitry

TSMC 180 nm technology — *Mar 2017 - May 2017*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

Work Experience

Novelic

Belgrade, Serbia

Junior Design Engineer — *February 2018 - 2021*

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Nirsen

Belgrade, Serbia

Design Engineer — *2021 - PRESENT*

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