

# Aleksandar N. Vuković

DESIGN ENGINEER · ANALOG RF/MMWAVE IC

Belgrade, Republic of Serbia

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## Education

### School of Electrical Engineering, University of Belgrade

M.Sc. IN COMPUTER SCIENCE AND ENGINEERING

- Master's thesis: All-digital RF Transceiver Based on Parallel and Approximative DSM

Belgrade, Serbia

Oct 2018 - Sep 2021

### School of Electrical Engineering, University of Belgrade

B.Sc. IN COMPUTER SCIENCE AND ENGINEERING

- Bachelor's thesis: 1 GHz Low Noise Phase-Frequency Detector and Charge Pump

Belgrade, Serbia

Oct 2014 - Sep 2018

## Skills

<b>Programming languages/scripting</b>	C/C++, Python, TeX, *nix shell
<b>NI AWR Design Environment</b>	Microwave Office
<b>Cadence Custom IC</b>	Virtuoso Platform, schematic entry, custom layout, physical verification, extraction
<b>Cadence Spectre X</b>	Simulator, RF Option, APS
<b>Cadence EM simulator</b>	EMX Planar 3D Solver
<b>Mentor Graphics</b>	Calibre IC Verification: nmDRC, nmLVS, xRC
<b>Keysight PathWave Design</b>	Momentum
<b>Operating systems</b>	GNU/Linux, Microsoft Windows
<b>Languages</b>	Serbian, English

## Projects

### Flash Analog Digital Converter

TSMC 40 NM LP CMOS TECHNOLOGY

- Redesign of 250 MS/s ADC to have more supply voltage
- Verification of ADC and comparator redesign, Monte Carlo ENOB
- LDO transient simulations, under current load

Ethernet IEEE 802.3

Jun 2023 - Sep 2023

### LC Class C Voltage Controlled Oscillator (6.3 - 13.7 GHz )

TSMC 40 NM CMOS TECHNOLOGY

- Improving phase noise and frequency pushing. Consists of two cores to cover the LO range
- Gate voltage control feedback ensuring oscillation start up and class C operation

LO block VCO

Sep 2022 - Dec 2022

### Ku-band 4 Output Active Power Divider (APD)

TSMC 55 NM TECHNOLOGY

- Design of both one-stage and two-stage APDs and comparison on schematic level
- Simulated as part of transmitter chain's LO distribution for isolation between outputs
- KuKa-band One Input Two Output Balun for LO Mixer Ku and Ka inputs
- Parts of passive layout structures simulated using both EMX and ADS simulators

Ku and Ka band TX - LO distribution

May 2021 - Apr 2022

### All-digital RF Transceiver Based on Parallel and Approximative DSM

PYTHON SCRIPTS

- Behaviour and application of parallel and approximative DSMs is tested using python language
- Parallel and approximative DSMs can generate RF signals on significantly higher frequencies comparing to the conventional DSM, with minimal signal degradation
- All-digital transceivers, delta-sigma modulation (DSM)

All-Digital Delta-Sigma Modulators

Jun 2021 - Oct 2021

### Active-RC Filter and its Operational Amplifier

TSMC 55 NM TECHNOLOGY

- Design of High Unity Gain-Bandwidth Operational Amplifier on schematic level
- Simulating different operational amplifiers in active-RC filter topologies like Rauch and Ackerberg-Mossberg with bandwidth of 250 MHz
- Comparison of different topologies in noise performance and limitations of the finality of uGBW

Ku and Ka band TX - Low Pass Filter

Dec 2020 - May 2021

### 8 GHz Low Noise Phase Frequency Detector based on Gilbert cell

IHP SiGe 130 NM BICMOS TECHNOLOGY

*Phase Detector*

*Aug 2020 - Sep 2020*

- Simulation of different Gilbert cell based Phase Detectors and different frequency locking techniques on schematic level

### 57 GHz - 64 GHz Voltage Controlled Oscillator

IBM (GF) SiGe 130 NM BICMOS TECHNOLOGY

*Radar*

*Dec 2019 - Mar 2020*

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

### 57 GHz - 64 GHz Active Power Divider

IBM (GF) SiGe 130 NM BICMOS TECHNOLOGY

*Radar*

*Apr 2019 - Nov 2019*

- Schematic ported from IHP SiGe 130 nm technology and layout redesigned
- Parts of design (matching networks) EM simulated using ADS Momentum

### 28 GHz Active Phase Shifter - Vector Modulator

IHP SiGe 130 NM BICMOS TECHNOLOGY

*School project*

*Jan 2019 - Jun 2019*

- Band around 28 GHz (from 26.5 GHz to 29.5 GHz) and controlled by 8-bit ADC simulated on schematic level in Cadence Virtuoso
- Parts of design (all-pass filter, matching networks) EM simulated using ADS Momentum

### 1 GHz Low Noise Phase-Frequency Detector and Charge Pump

IHP 130 NM BICMOS TECHNOLOGY

*PLL block*

*May 2018 - Nov 2018*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

### Phase-Frequency detector, CP and Divider as blocks of MDLL

TSMC CMOS I THINK

*Multiplying Delay Locked Loop*

*Oct 2018 - Dec 2018*

- Schematic and layout redesign of PFD, CP, divider with surrounding circuits

### High Gain Operational Transconductance Amplifier

IHP 130 NM BICMOS TECHNOLOGY

*OTA*

*Mar 2018 - May 2018*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

### Small Signal GSM 1800 MHz Amplifier

MICROSTRIP TECHNOLOGY

*Wi-Fi Band Amplifier*

*Dec 2017 - Jan 2018*

- Schematic design using Microwave office
- Layout design using Altium Designer
- Verification via measurement

### Custom IC layout for the Configurable IIR Filter

TSMC 180 NM TECHNOLOGY

*Digital Circuitry*

*Mar 2017 - May 2017*

- Schematic and layout design in Cadence Virtuoso
- Post-Layout verification using ADE L and ADE XL on a QRC extracted model

## Work Experience

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### Novelic

JUNIOR DESIGN ENGINEER

*Belgrade, Serbia*

*February 2018 - 2021*

- First year internship, schematic design, verification, layouting and post-layout verification
- Internal projects, feasibility studies, commercial projects, analog IC design at first, RF/mmwave design later

### Nirsén

DESIGN ENGINEER

*Belgrade, Serbia*

*2021 - PRESENT*

- Mostly commercial projects both analog IC and RF/mmwave design