IO/IO Ring Placement and EMIR Analysis– OBSOLETE Power Amplifier - SiFlower cn

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Introduction - IO/IO ring

IO/IO ring placement with ESD protection and EMIR analysis/ isolation, noise analysis for the whole chip. There is already a good template in place with test benches from our recent testchip.

Questions:

Are IO/IO ring and PAD ring the same thing?

Info:
Pad ring is a ring around the chip that contains all the pads (chip IOs) and ESD protection structures. It's usually one of the things that is handled by part of the layout team - there'll be a lot of interaction between people that are developing the package (making sure that all IOs are routable to where they need to be) as well as making sure that things get internally to the right places with high enough efficiency.

So what's exactly in the pads? Just the ESD protection circuits? Aren't chip IOs pins basically? Shouldn't pins be attached to the actual macro?

Info: Pads will have I/O drivers and ESD protection - additionally, they will have areas where the chip can be touched down on when it is tested in wafer form and (for parts that are wirebonded) areas where the chip can be bonded out.They will be connected to any internal macros also, yes

And what does routability mean?
So you've got a pad ring:

```
[][][][][][][][][][]
[]                  []
[]                  []
[]                  []
[]                  []
[]                  []
[]                  []
[]                  []
[]                  []
[][][][][][][][][][]
```

Info:

And it's got to get mapped to external pins somehow - if it's getting mapped to an XxY ball array it'll either be bonded out to a substrate that will have a few layers to route pads to the destination ball (wirebonded packages) or routed to bumps/pillars that will get attached to the final substrate (flip-chip) or routed to a redistribution layer (RDL) that maps to a ball array directly on the part (WLCSP).

Checking routability is a combination of making sure that you can route things from the origination point on the pad ring to the place where it's actually going to interface to the system - there is a flip side to this which is checking that the ball array has things placed properly so that a system board can be constructed without excessive numbers of blind vias and without requiring too many layers (that signals are able to escape from the ball array).

1 How to design a pad ring?

Need to design a pad ring for my ADC chip, but I knew very little about this (I have some experience in analog IC design though). Is there any resources to begin with?

Info:

Do you have pdk pad and fill cells? Most important thing is planning (of ESD and supply/gnd domains). Depending on technology and packaging you should make sure to select the proper ones (bondwire/probing vs balling/flipchip).

Info:

The main objective of the pad ring is to mate up the cell I/O with the board. The secondary function is to provide ESD protection. Usually answering a few questions will provide you with how to proceed.

Use foundry or company-supplied I/O cells (our company has an I/O compiler that creates a proper library). There are separate I/O cells and methodologies for wire bond, FBGA, and WLBGA-type packaging. Someone should have an idea about the board and thus the package + pinout. There will likely be (at a minimum) ESD clamp/vdd padcells, vss padcells, digital I/O padcells, analog thru padcells, and analog secondary protection padcells.

There are foundry-supplied DRC rules that are specific to pad rings - the padcells should already be designed with these rules in mind. Additional you will need to consider IR drop from a padcell to the nearest ESD clamp and vss connections. You may have to place additional ESD clamp and vss padcells in your pad ring to meet these maximum resistances.

The chip cells should hopefully be floor planned with the pinout/ballout in mind. If you have a wirebond package the the routing from cell to pad ring is straight forward. If you have a type of BGA then there should be at least one (and maybe 2-3) thick RDL top metal layers which are for routing from pad ring to the ball and then likely close to the cell. This is more complicated as there may be another packaging route (FBGA) or board route (WLBGA) to consider.

Unfortunately I am not aware of a good resource that covers everything. If you can narrow down your package type then googling will probably give you some good package vendor documentation.

Info:

Use the IP pads (ARM, Aragio, etc.) for your process if you have access to them. It will reduce tapeout risk but also can be a pain to import into Virtuoso. Use analog IO pads for analog inputs and digital IO pads for the digital I/Os, and VDD and ground pads for power and power clamp. Depending on your design, you may have separate IO and core voltage supplies - don't forget those. The IP pad documentation will have all the information you need on how to use the cells. Don't forget to include the actual physical bond pad as this is not usually in the ESD IO cells in the library. Space and size bond pads according to requirements of your wire bonding vendor. Remember to consider IO pad parasitics in your simulations. If you are at an university, you may want to reach out to the IC design group there to guide you on this so that you get it right the first time.

2 IO/IO ring placement

3 ESD protection

4 EMIR analysis

Cadence Guidelines

EMIR is ex-Voltus

https://community.cadence.com/cadence$_blogs_8/b/cic/posts/using-spectre-aps-for-analysing-emir$

5 Isolation, noise analysis for the whole chip

Introduction - Design Acceptance Criteria

Below is the key specs of the PA for 5G band.

- Technology: TSMC 28nm
- Supply voltage: 3.3V
- Frequency range: from 4.9GHz to 5.9GHz
- output power range: -25dBm to 0dBm with EVM below -38dB.
- OIP3: 35dBm @0dBm

6 Questions

Additional questions regarding design briefly presented:

- input power, gain
- Is the input power range changing in the redesign?
- gain control
- is power efficiency (PAE) of interest?

6.1 Possible Design Considerations

Design considerations that may be important and informative about the current design:

- power combining technique - wilkinson or transformer
- broadband power matching topology
- low output impedance for amplifier compared to 50 Ω

7 Papers to look at

- A 5.8 GHz class-AB power amplifier with 25.4 dBm saturation power and 29.7% PAE
- A 5-5.8 GHz Fully-Integrated CMOS PA for WLAN Applications, Jeng-Han Tsai and Hong-Wun Ou-Yang
- Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off, Gang Liu, Peter Haldi, Tsu-Jae King Liu, Fellow, IEEE, and Ali M. Niknejad, Member, IEEE

Abstract from A 5-5.8 GHz Fully-Integrated CMOS PA for WLAN Applications, Jeng-Han Tsai and Hong-Wun Ou-Yang:

Info: Abstract — A 5-5.8 GHz fully-integrated power amplifier is designed and fabricated in TSMC standard 0.18-μm 1P6M CMOS technology. Utilizing a two-way direct shunt combining technique with an odd mode suppression resistor, the CMOS PA achieves a measured maximum saturation output power (Psat) of 23.1 dBm at 5.2 GHz. The measured output 1-dB compression point (OP1dB) is 18.6 dBm and peak power-added efficiency (PAE) is 19.8 % at 5.2 GHz. By using broadband power matching topology, the output power of the CMOS PA is 22.6 $\pm$ 0.5 dBm from 5 to 5.8 GHz. Index Terms — CMOS technology, radio frequency integrated circuits, power amplifiers, microwave amplifiers.

Abstract from A 5.8 GHz class-AB power amplifier with 25.4 dBm saturation power and 29.7% PAE, Chuan Qin, Lei Zhang*, Li Zhang, Yan Wang, Zhiping Yu

Info: Abstract — In this paper, an effective and succinct radio-frequency (RF) grounding technique for class-AB power amplifier (PA) is presented. The proposed technique employs a grounding path, resonant with a capacitor in series at the center of the fundamental and second-order harmonic frequencies, between the critical ground nodes, to ensure a low impedance path. The power loss due to imperfect grounding is then reduced by 2 dB, and the saturated output power and power added efficiency (PAE) are therefore significantly improved. A fully integrated 5.8-GHz PA with the proposed technique is designed and implemented in a 65-nm CMOS process. Measured result shows a saturated output power of 25.4 dBm and a peak PAE of 29.7%, while with only 2.5 V of supply voltage.

Abstract from Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off, Gang Liu, Peter Haldi, Tsu-Jae King Liu, Fellow, IEEE, and Ali M. Niknejad, Member, IEEE

Info: Abstract — This paper presents a new approach for power amplifier design using deep submicron CMOS technologies. A transformer based voltage combiner is proposed to combine power generated from several low-voltage CMOS amplifiers. Unlike other voltage combining transformers, the architecture presented in this paper provides greater flexibility to access and control the individual amplifiers in a voltage combined amplifier. In this work this voltage combining transformer has been utilized to control output power and improve average efficiency at power back-off. This technique does not degrade instantaneous efficiency at peak power and maintains voltage gain with power back-off. A 1.2 V, 2.4 GHz fully integrated CMOS power amplifier prototype was implemented with thin-oxide transistors in a 0.13 m RF-CMOS process to demonstrate the concept. Neither off-chip components nor bondwires are used for output matching. The power amplifier transmits 24 dBm power with 25% drain efficiency at 1 dB compression point. When driven into saturation, it transmits 27 dBm peak power with 32% drain efficiency. At power back-off, efficiency is greatly improved in the prototype which employs average efficiency enhancement circuitry.

The cascode gate is connected to the supply node when the individual amplifier is on, and it is grounded to turn off the individual amplifier for power back-off (to improve PAE when the output power is backed off).

Abstract from A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90 nm CMOS

Info: Abstract — A fully integrated 5.8 GHz Class AB linear power amplifier (PA) in a standard 90 nm CMOS process using thin oxide transistors utilizes a novel on-chip transformer power combining network. The transformer combines the power of four push-pull stages with low insertion loss over the bandwidth of interest and is compatible with standard CMOS process without any additional analog or RF enhancements. With a 1 V power supply, the PA achieves 24.3 dBm maximum output power at a peak drain efficiency of 27% and 20.5 dBm output power at the 1 dB compression point

8 Conversation about design

You were talking about previous design and also about need to do redesign. What exact parameters you did not match last time, and do you have also starting design and schematic ready, or you would like to ask us to start completely form beginning?

[John]: Compared with current design, we would lower the PA output power from max 16dBm to 0dBm, and reduce the PA area as much as possible. We would like to redesign the existing PA because the current design is silicon proven and we have delivered more than 1 million pcs. And we have a redesign strategy in our mind. We can discuss it in the intake meeting.

I am guessing that we are doing also design and layout due to the fact that it is a RF component?

[John]: yes, that is the plan that you redesign PA and do the layout. We will integrate to the SoC

I am guessing this component will be further integrated in the complex SOC?

[John]: yes, it will be integrated into WiFi SoC.

Do you have power control of PA? If yes do you have other specs?

[John]: yes, we can propose other specs. However, we would purposely only define the most important specs(EVM, OIP3, VDD, Freq, BW, process technology) in our design request because we would give the freedom to the PA designer as much as we can. We can discuss in the intake meeting.

Do you have any special circutry like power detector to measure if antenna is working (connection ok), or the whole power is reflected back. Self performance test.

[John]: No, power detector isn't included in this PA redesign work.

Are those parameters down only one for acceptance criteria?

[John]: They are the key specs. We definitely need more items as acceptance criteria, but we are open to define together with PA design team to give freedom to the PA to make a better trade-off.

You were talking about size? What size you have currently?

[John]: One PA block consists of four identical units. each unit is about 0.13mm2. so for one PA, it is about 0.52mm2.

I am guessing we are using our Cadence tools, and simulators?

[John]: It depends on availability of the CAD tool&PDK version, the cost and the team preference. we can also align in the intake meeting.

9 AI help - collected important info

Technology: TSMC 28nm
Supply voltage: 3.3V
Frequency range: from 4.9GHz to 5.9GHz
output power range: -25dBm to 0dBm with EVM below -38dB.
OIP3: 35dBm @ 0dBm
area: 0.52 mm^2

10 Mail reply and preparation for first meeting

I assume that these 4 identical power amplifiers are connected as power combined amplifiers (connected in parallel or in series when looked from the output balun). If they are, how aggressively do they want to reduce the area, to throw out PA units, how many would be left in the end? How are outputs of these amplifiers connected?

And is there going to be some relaxation for OIP3 from this existing design or does it stay the same?

My additional question is what is the input power for this power amplifier? And does it have any output signal control inside it or does it happen before it?

10.1 How to introduce yourself

Info: The secret is using a simple framework: Present, past, and future.

Present: Start with a present-tense statement to introduce yourself:
Hi, I'm Ashley and I'm a software engineer. My current focus is optimizing customer experience.
Nice to meet you all. My name is Michael and I'm the creative director. I work in the Brooklyn office.
Of course, what you share will depend on the situation and on the audience. If you are not sure what to share, your name and job title is a great place to start. If there's an opportunity to elaborate, you can also share other details such as a current project, your expertise, or your geographical location.

Past: The second part of your introduction is past tense. This is where you can add two or three points that will provide people with relevant details about your background. It is also your opportunity to establish credibility. Consider your education and other credentials, past projects, employers, and accomplishments.
My background is in computer science. Before joining this team, I worked with big data to identify insights for our clients in the health care industry.
I've been at the firm for eight years. Most recently, I worked on the Alpha Financial account, where last year's campaign won us a Webby award.

Future: The third and last part in this framework is future-oriented. This is your opportunity to demonstrate enthusiasm for what's ahead. If you're in a job interview, you could share your eagerness about opportunities at the firm. If you're in a meeting, you could express interest in the meeting topic. If you're kicking off a project with a new team, you could talk about how excited you are, or share your goals for the project.
I'm honored to be here. This project is a significant opportunity for all of us.
I'm excited to work with you all to solve our clients' biggest challenges!

That's it for the self-introduction framework. Present, past, future. Eloquent and effective. By using this approach, you'll not only introduce yourself better, but it also frees you from ruminating on what you'll say when it's your turn to introduce yourself and allows you to listen when others introduce themselves. You will also make it easy for the person who introduces themselves after you, since you'll conclude your self-introduction with positive enthusiasm.
source

11 Reading books and papers on the matter

11.1 Load-pull contours

The load-pull method of RF and microwave power amplifier design, John F. Sevic, Ph.D.

11.2 Shive wave machine

The Shive wave machine, a clever instrument that uses torsion on a wire and suspended weights to propagate a wave that is easy to observe. This machine will help you visualize:

- Transmission lines
- Propagation velocity
- Wavelength
- Impedance
- Matched loads
- Reflections from short and open circuits

- Standing waves
- Standing wave ratio
- Reflection coefficient
- Resonance and tuning
- Quarter-wave matching networks
- Tapered transformers