VCO as part of PLL

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Introduction

working title
This needs to be added to body of document
Complaints and suggestions:

- there is no point in using higher resistances than 20 - 30 kΩ in capacitor bank unit
- test voltage and current for HV_MOSFETs, to test breakdown of mosfets, use software called **Real Expert**
- estimate for drop in phase noise with supply noise and layout and its generous is -120 dBc/Hz
- to further help needs to review design

My problems and work in progress:

- hard-clipped VCO not oscillating at the frequency that is supposed to, drops down to around 1 GHz (example)
- soft-clipped VCO has more frequency modes - CM and DM resonance

1 Technical Novelic evaluation summary

Here are technical Novelic evaluation summary on provided documents (Point 3):

- Overall conclusion is that: the provided report contains almost the same type of the architecture, like provided in Novelic & Nirsen study.
- However, the simulation provided by customer does not include process corners and temp range. We see TT process and nominal temp. It is clear that temperature and process deviation will influence the performance of the power detector, which imposes the design risks.
- Dead zone of PFD which they are claiming that cannot measure is not that critical, more important is blind zone which is in our case on schematic in order of 0.5*Tosc at 8GHz in some corners. This is also a design risk.
- All provided schematics are not including any parasitic estimates which make significant difference as we saw in our simulations. This is a design risk.
- Robustness over supply voltage variation imposes the design risk.
- Further technical explanation is following:
- Reset path of this and all similar PFDs has minimum 5 logic gates in signal path.
- Let's assume propagation through gate is 5ps (schematic, typical, in reality and over PVT is even worse!). Period of signal is 125ps at 8GHz which means we are loosing 20% of period just for propagation. Layout parasitics will degrade this to 40% in typical. For reset delay > 50% of period we cannot make a lock of PLL by design. This presents a design risk.

- In the provided document SiGe solution was not simulated in closed loop scenario - PFD and CP tested separately with optimistic separation between input signals. This presents a design risk.
- Mixer gm PFD is good try but followed by ideal VCO in the provided document. So, we can confirm to get similar PFD values like in initial simulations. But provided simulation does not include any real VCO with imperfections. By this approach PLL will work good if VCO is ideal, with possibly too optimistic phase noise profile. This presents a design risk.
- If the mixer is used in PFD (like possible proposed option) basically we would have PHASE ONLY locking, while if input frequencies of the PFD are significantly apart from each other, so we will not have PLL in LOCK state. This is the most likely scenario since range of input frequencies is 1-8GHz. So most probably this approach can be followed for design.
- In entire document provided by End user, Novelic do not see any VCO design, which is the most critical part besides PFD, so VCO is considered as an ideal VCO.
- Based on Novelic previous experience, and comparison to the state-of-the-art performance in journal/conference publications and/or patents we could not confirm feasibility of making VCO with required phase noise requirements, like in initial specifications.

2 Identified various risks

- VCO phase noise contributors
- PFD topology and “blind spots”
- Discussed design methodology to be finalized in next couple of days
- Obtained PDK and discussed risk mitigation strategies
- Started authoring chip system specification
- Started project plan with internal and external milestones
- Agenda: project progress towards milestones, technical discussion
- Review & signoff of project milestones and plan
- Review system specification draft

2.1 VCO phase noise contributors

Bias
Quality factor of tank
Quality factor of inductor
Localized Backside Etching (LBE)
Core devices contribution

3 PFD topology and blind spots

Reset path delay is needed because of dead zone and that is why blind zone much worse than expected.

4 Discuss design methodology

Probably VCO design methodology

Question 1 *How did we address problems from 2020 feasibility study?*

-

Reference project is LMX 2592 texas instruments
-135 dBc at 1 MHz
8 GHz
IHP 130 nm SiGe
FTR - fine tuning range in percentage

- What is minimum phase noise that can be obtained with perfect supply, typ process, 25 degC, measured at the VCO output with ideal termination and no buffer
- What is the maximum tuning sensitivity that can be used to obtain the above
- What additional techniques need to be explored to improve the above
- Perform noise sensitivity analysis
- Discuss CML buffer concept and LDO topologies

I searched relevant papers for VCO 130 nm BiCMOS or similar technologies and frequency range, and haven't found performance even close to 130 dBc @ 1 Mhz offset.

Question 2 *Based on what was this technology picked for this specification?*

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Question 3 *What is the input reference frequency of PLL? Are there any dividers in PLL?*

-

Question 4 *Is the input from loop filter single ended or differential?*

-

Question 5 *Any estimate for specified VCO output swing?*

-

Question 6 *What additional techniques need to be explored to improve the above?*

-

From what I have seen in papers most promising topology in terms of phase noise is cross-coupled LC VCO class C with potential additional technique of subharmnic injection locking. This is what I plan to try first if no better solutions are provided.

I just realize that BSE should be called LBE (localized backside etch).

a) another question to the customer regarding the overall system. 8 is a great number for a divider, but maybe a bad choice for a multiplier? I don't know how it is currently implemented, but thinking of diodes/BJT with exponential characteristics we get odd harmonics, using MOS we may get even ones, at least a good 2nd. But 8=2*2*2 and 9 is just 3*3 .. one stage less, and in differential design only 9

seems feasible. In that case I tend to say that a non-sinusoidal output would even help to reduce gain in the multipliers (which also adds noise on top of the multiplication itself). Assuming that the mixer needs amplification, each *2 stage should add more than 6dB PN, leading to about 20dB or more degradation. If they want to have options on that multiplication factor, we could more easily do that in the PLL with dividers (which reduce PN). Ideally we reduce the VCO range to just more than an octave in the highest band of interest and divide the rest?

I just want to ensure that we're not rebuilding something 1:1 that would benefit from a different structure (thinking about Bosch's wall scanner .. they asked us to turn their discrete circuit 1:1 into an ASIC ... but the central component was a tunnel diode O:-)).

b) Regarding VCO phase limit tests: Since noise expresses both in amplitude and phase we could use amplitude regulation to generate the tail current (e.g. using a bipolar current mirror). The problem will then be to minimize noise in the current generator. That could be done with the help of a chopper amplifier. Undesired frequency content may be a new issue, but for a differential design I believe it's solvable. For first tests, an ideal amplifier should come close to that. Maybe a bipolar amplifier doesn't even need that.

Make two chips
Testbench to lock PLL, PFD loop filter and VCO.
PFD is CML.
pdk does not support detail inductor modeling.
harmonic filter is not included
loop bandwidth reallistic that can be achieved internally is from 3 MHz to 100 MHz.
up to you if it is 2nd or third order.
spec Review
Prelimiary Design Review PDR and Critical Design Review CDR
70 Mhz below 50 Mhz Kvco?

4.1 List of reference papers

- A Stacked-Complementary 5 GHz Oscillator With Even-Only Differential Harmonic Shaping Achieving -150 dBc/Hz Phase Noise at 10-MHz Offset Using Body-Biased Thin-Oxide 22-nm FDSOI
- A VCO with Implicit Common-Mode Resonance
- A 2.3 - 5-GHz LC-VCO With Source Damping Resistors to Suppress 1/f Noise Up-Conversion
- A 6.7-to-9.2GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO
- A 25!% Tuning Range 7.5- 9.4 GHz Oscillator With 194 FoMT and 400 kHz 1/f3 Corner in 40nm CMOS Technology
- A Filtering Technique to Lower LC Oscillator Phase Noise
- A Low Phase Noise and High FoM Distributed-Swing-Boosting Multi-Core Oscillator Using Harmonic-Impedance-Expanding Technique
- A Low Phase Noise, High Phase Accuracy Quadrature LC-VCO With Dual-Tail Current Biasing to Insert Reconfigurable Phase Delay
- A Low Phase Noise Oscillator Principled on Transformer-Coupled Hard Limiting
- A Noise Circulating Oscillator
- Ultra-Low Phase Noise X-Band BiCMOS VCOs Leveraging the Series Resonance
- An Ultra-Low Phase Noise Class-F2 CMOS Oscillator With 191 dBc/Hz FoM and Long-Term Reliability
- CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise
- Design of LC Resonator for Low Phase Noise Oscillators
- Even-Harmonic Class-E CMOS Oscillator
- Implicit Common-Mode Resonance in LC Oscillators

- Third-Harmonic Injection Technique Applied to a 5.87-to-7.56GHz 65nm CMOS Class-F Oscillator with 192dBc/Hz FOM

4.2 Mail sent after going through papers

And Franceschin paper has the best noise performance by far. It's made in SiGe 55 nm and using bipolars in core, consumes 500 mA and the output swing is clipped by diode connected bipolars which enables this much current without affecting bipolars operation.

Babaie papers are made in CMOS and are more similar to current design. It utilises step up transformers with different common and differential k factors to decouple capacitor bank from the core and control its drain currents to make a clas F2. But I currently don't know how to implement this because I don't have any ideal transformer models with different k factor for differential and common modes.

Ying paper has a similar idea calls it class F23 and also ok results which makes me think this it the most viable idea from all of these papers to try.

4.3 Open points

- Novelic to acquire EVB's for ADF6610, LMX2594
- Packaging, actual implementation
- Testability options within chip
- VCO registers/overriding
- External test requirements/definitions

4.4 Frequency scaling and frequency plan

Formula for scaling phase noise to fundamental (output) frequency:
=AA21-20*LOG10(AC21/7)-20*LOG10(1/AB21)

4.5 Using different models for HBT

BSIM4 and pss (not psp), sometimes pss gives better performance

BSIM4, as the extension of BSIM3 model, addresses the MOSFET physical effects into sub-100nm regime. The continuous scaling of minimum feature size brought challenges to compact modeling in two ways: One is that to push the barriers in making transistors with shorter gate length, advanced process technologies are used such as non-uniform substrate doping. The second is its opportunities to RF applications.

4.6 Regarding VCO design option 2 results

I have simulated pnoise for designs and testbenches Gunther sent me and I don't get the same results.

I beleive simulation using setting multiplenoise that gives phase noise perfrmance that is now being presented is not correct. As for multiple different nets it gives very different values, which makes little sense with the topology. And when I use only one output noise for pnoise simulation I get much worse results (15-20 dBs), but they are consistent.

Sorry to bring other people into this, I thought this is important and I wanted to remove myself from these results presented since I also spent some time simulating this design this past week.

Also for the design Gunther sent me today. The results I got with his testbench:

These are not normalized results so they are 5-6 dBs lower, but still far from what was expected.

rfOutputNoise("dBc/Hz" ?result "pnoise")

4.7 Tasks regarding the VCO option 2

option 2

Review VCO option 2 BJT and CMOS options Review PFD latest results and CP status Review approach going forward and schedule proposals

4.8 30 GHz VCO design

with divider by 4

Parametar	Typical value
Corner	Typical
Temperature	50 °C
Amplitude	550 mVpp
Centre Frequency	30.25 GHz
Tuning Range	0.72 GHz
K_{VCO}	1.45 GHz/V
Tuning range voltage	0.2 V - 0.7 V

Table 1: Specification Requirements

Some key conclusions in terms of phase noise:
Noise at output of VCO is same as at the output of buffer. Main contributors for VCO output noise is output buffer by performing modulation of VCO tank circuit. Second main contributor is noise in references used to generate VCO current bias and noise in power supply.

4.9 Commercial Parts

5 Parts of interest of VCO

List of parts:
VCO core
Differential Varactor (Varactor)
Capacitor bank (unit)

5.1 Differential Varactor

LO block VCO and VCO Buffer

Old project

Introduction

LO block is LC VCO with internal inductor and fully differential output buffer. Its schematic shall ensure differential connection to the mixer LO input and PLL RF input. LO block should have the characteristics given in Table 6. Due to wide frequency range it is necessary to use switchable capacitor banks.

6 Technical Requirements

	LO Requirements	Note	min	typ	max	Units
	VCO Requirements					
1	Full LO range		6300		13700	MHz
2	Phase Noise at 300 kHz				<-101	dBc/Hz
3	Vtune		0.1		1	V
4	Tuning Sensitivity K_{VCO}				100	MHz/V
5	Pushing	TBD			2	MHz/V
6	Output Voltage	TBD	0.8			V_{p-p}
7	Load Impedance				100	fF
	VCO and output Buffer					
8	Output Voltage	TBD	0.8			V
9	Load Impedance	TBD			1000	fF
10	Harmonic suppression (2_{nd}, typ)		-15			dBc
11	Pulling (14 dB Return Loss, Any Phase)	TBD			2	MHz
	General Specifications					
12	Operating Temperature Range		-40		125	°C
13	Supply Voltage		1	1.1	1.2	V
14	Supply Current				20	mA
15	Shutdown Current				10	μA
16	Time to Switch Between Cores			3	5	ms

Table 2: Specification Requirements

Min and max for supply voltage are not defined in the original document, and time for switching between two cores was defined during the meeting.

Currently Full LO range is split between two cores so the requirement should look like this:

	LO range requirements	Note	min	typ	max	Units
1	High Band core LO range		10000		13700	MHz
2	Low Band core LO range		6300		10000	MHz

Table 3: LO Range Two Core Specification Requirements

Question 7 *What's the variation for supply voltage?*

Not defined probably will be the same as the rest of the

Question 8 *K_{VCO} Why is it in the max column?*

Didn't get answer for this. It's probably also typical and a value that is expected by the PLL design.

Process corners can be found at:

`/tech/tsmc/tsmc40/models/spectre/crn40lp_2d5_v2d0_2_shrink0d9_embedded_usage.scs`

7 Scaldio Design Review

Question 9 *How should calibration be implemented to achieve output voltage peak to peak and minimize noise?*

Is it done for whole PLL?

Question 10 *Difference between class-B and class-C vco?*

Scaldio uses class-C, so all parasitic capacitances connected to the tail don't matter. Having trouble with observing the currents of drain so cannot check this and compare them. Scaldio looks something between class C and class B because of V_{gbias} voltage and because adding inductor between tail NMOS and switching pair improves phase noise. This is attributed to class B, while class C only needs tail capacitance.

Lowest bit of digital varactor (L0_PLL_hbVCO_Cdig_SC2B_VCOS_SC2C_PLL) doesn't do anything, isn't even monotonous. Maybe makes more sense when simulating extracted cells. Digital varactor needs to be redesigned, it could lower the Q factor. Main difference between class B and class C can be observed by investigating their drain currents.

7.1 Main testbench

Main testbench covers everything except for frequency pulling and full LO range. The simulation results are obtained at the higher end of the LO range. Phase noise is simulated by pss+pnoise.

Info: With Noise Type=timeaverage and ALL(AM,PM,USB,LSB), you can plot the AM and PM components as well as the total noise. In addition, you can plot phase noise and FM jitter results for oscillators. Plotting is done using the Direct Plot Form. **External link**

Function of phase noise is simulated for PM noise type.
How to choose beat frequency for autonomous system from forum **thread**.

Info: In an autonomous system (e.g. an oscillator), you turn on the "oscillator" checkbox, and the beat frequency is then the estimated frequency, which gives PSS a starting point to solve for the oscillator frequency. It's important when in oscillator mode to select the outputs of the circuit, which include any subharmonics. In other words, if you have an oscillator followed by a divider, point at the divider output, and give the estimated divided frequency as the beat frequency. Again, this is because you need to solve an integer number of cycles of all the frequencies in the circuit. Note, don't use oscillator mode for circuits which aren't oscillators, since you're then trying to get the simulator to solve for an unknown which is not unknown, which may lead to convergence problems.

Most of the I_{bias} tune digital control is not used for the higher band, so by increasing the number of steps to cover even higher frequencies than the original design finer bias control is needed.

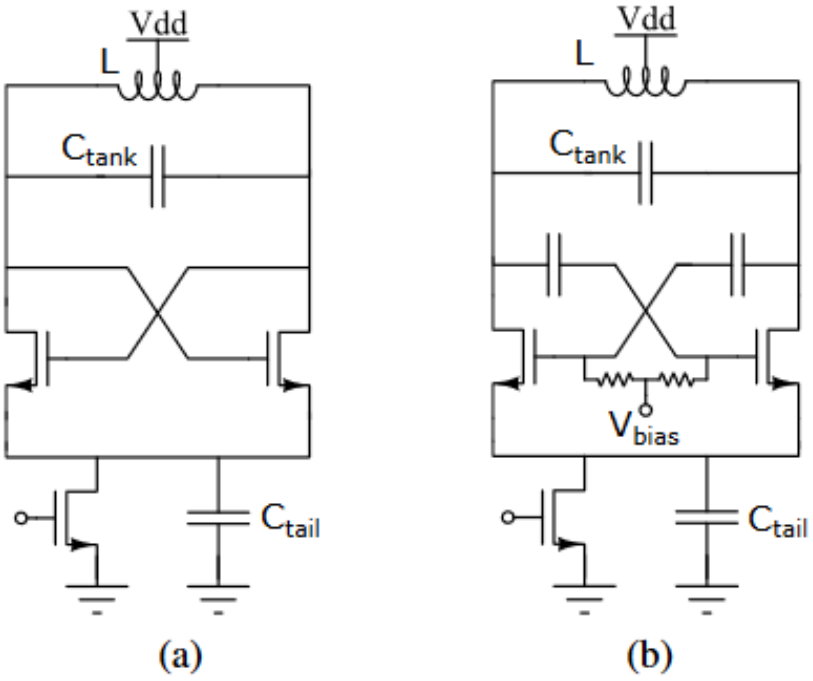

Fig. 1: Oscillator topologies: (a) class-B; (b) class-C.

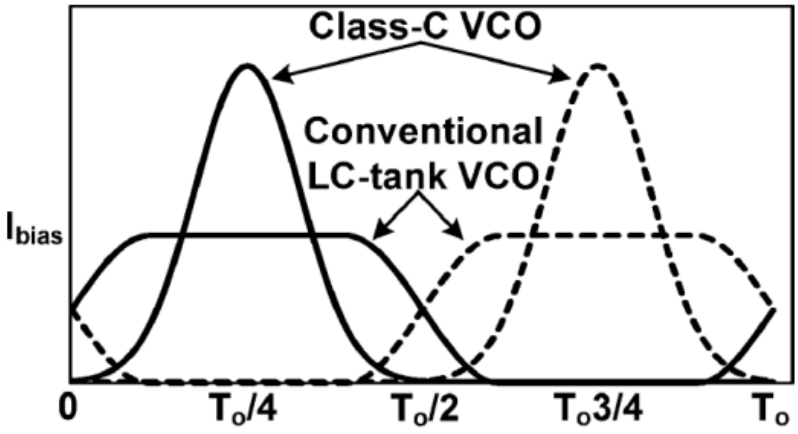

Fig. 2. Drain current of the switch pair FETs for conventional LC-tank VCOs and class-C VCOs.

7.2 Simulation Results for Scaldio design

Simulated only nominal corner with change for V_{DD} only for frequency pushing simulation.

Phase noise changes a lot for different tuning voltages between -90 and -100 dBc/Hz. Phase noise

	LO Requirements	Note	min	typ	max	Sim(Typ)	Units
1	Phase Noise at 300 kHz				<-101	-98	dBc/Hz
2	Tuning Sensitivity K_{VCO}				100	over	MHz/V
3	Pushing	TBD			2	279.7	MHz/V
4	Output Voltage	TBD	800			809.3	mV_{p-p}
5	Harmonic suppression (2_{nd}, typ)		-15			-26.78	dBc
6	Pulling (14 dB Return Loss, Any Phase)	TBD			2	19.51	MHz

Table 4: Scaldio IMEC design Results

is probably not modeled ok because the VCO doesn't have the connection between current bias tail and the switching pair of VCO as transmission line. That inductance and C_{tail} should resonate at $2\omega_O$ (tank oscillating frequency), but only in the case of class B oscillator. Check what type is vco oscillator.

8 Q factor of LC tank

Need testbenches capacitance of tank, varactors and inductor, and for different controls and also corners. Process corners for varactors are the same as MOSFET.

Question 11 *What kind of chip is it?*

What kind of inductance is expected to be connected on V_{DD} and V_{SS} pins. This may or may not change the results. Removed all together right now.

Testbench for differential Q and L of the inductor that is EMX simulated is shown in Figure 1.

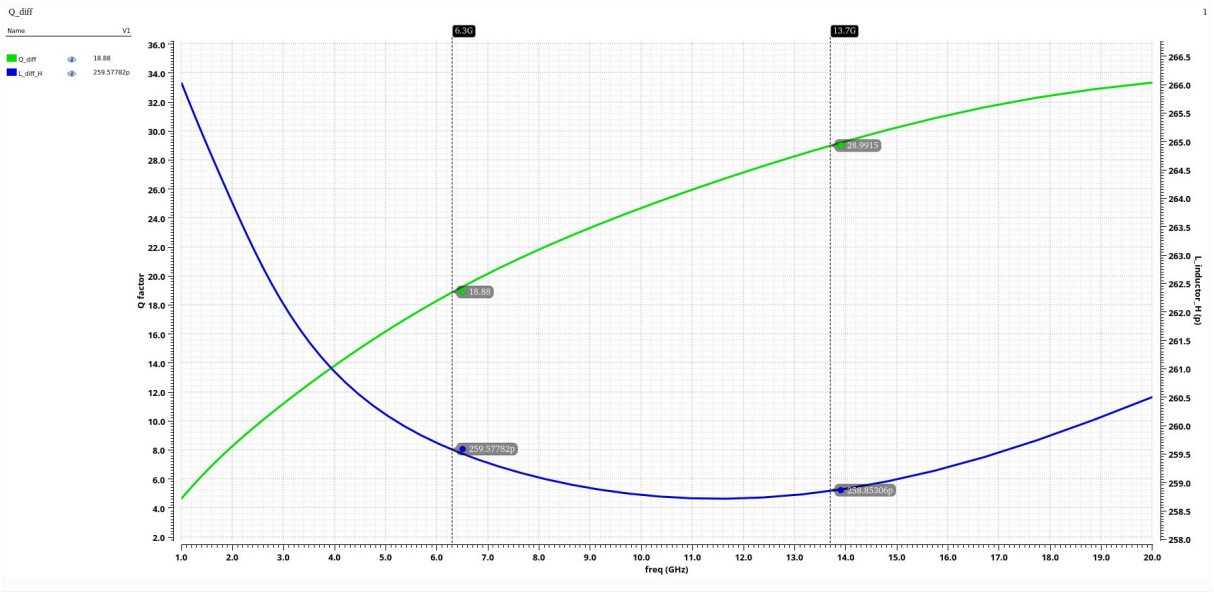

Figure 1: Q factor and inductance of L

Q factor is better at the higher frequency.

Simulated Q factor of both varactors and inductor. Q factor of digital varactor for lower bit controls is not much better than Q of inductor.

Capacitor calculating capacitance and Q factor:

$$Y_{diff}(im) = imag(ypm('sp11)) + imag(ypm('sp22)) - imag(ypm('sp21)) - imag(ypm('sp12)) \quad (1)$$

$$Y_{diff}(re) = real(ypm('sp11)) + real(ypm('sp22)) - real(ypm('sp21)) - real(ypm('sp12)) \quad (2)$$

Capacitance:

$$C_{diff} = \frac{Y_{diff}(im)}{2\pi f} \quad (3)$$

Q factor of capacitor:

$$Q_C = \frac{Y_{diff}(im)}{Y_{diff}(re)} \quad (4)$$

More info can be found in **paper** A Thorough Analysis of the Tank Quality Factor in LC Oscillators with Switched Capacitor Banks.

Found definitions:

$$Q_{LC} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{f_r}{\Delta f} = \frac{\omega_r}{\Delta \omega} = \frac{\tau_d \omega}{2} \quad (5)$$

where τ_d is group delay.

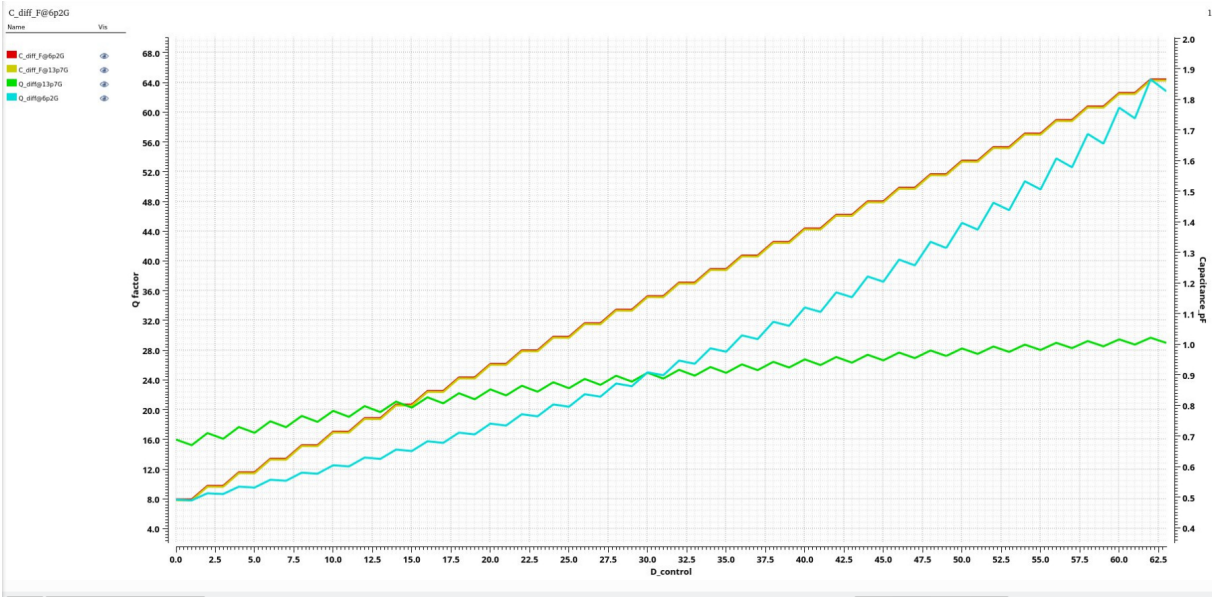

Figure 2: C and Q of digital varactor through controls

Question 12 *How to calculate group delay using sparam analyis?*

?

8.1 Calculating Q factor, LC tank by ringing method

Link to **website** that shows ring down method of calculating Q factor. Not implemented in virtuoso TODO.

9 Figure of Merit different definitions

Info: The theoretical maxima for the FoM of an oscillator is given by $FoM = 174 + 20log_{10}(Q)$ dBc/Hz

How to calculate oscillator FoM? Is Q_L factor dominant enough to just equate it with LC tank Q facor. The widely used FOM is calculated by:

$$FoM = L\{\Delta\omega\}(\Delta f/f_0)^2 PVCO[mW] \tag{6}$$

Where $L\{\Delta\omega\}$ is the phase noise, $\Delta\frac{f}{f_0}$ is the ratio between the offset frequency and the carrier, and P_{VCO} is the power consumption of the VCO-core. There is also FoM^T and FoM_A

$$FoM^T = FoM - 20\log(\frac{FTR}{10}) \tag{7}$$

and

$$FoM_A = FoM + 10\log(A) \tag{8}$$

where A is area [mm^2], and FTR frequency tuning range [%]
Information about digital varactor copied from **External link**

Info: Each bit of MIM varactor contains two MIM capacitors connected differentially with a series switch, two pull-up and two pull-down transistors to effectively turn the varactor between its high and low-capacitance states. Measured intrinsic Q of the MIM capacitor is 80 at 3.6 GHz. When is turned on, i.e., high-capacitance state, the varactor Q drops to 30. When is turned off to be in low-capacitance state, the parasitic capacitance of the MIM capacitor and transistors has an effective of 50. The pull-down transistors set the DC levels for drain and source of at 0 V so that can be efficiently turned into triode region while the weak pull-up transistors set the DC level to VDDOSC to reduce the parasitic capacitance of thus increasing of the parasitic capacitance. The pull-up pMOS can be implemented by either resistors or transistors. The latter was chosen for silicon area efficiency. Compared to MOS varactors, MIM varactors have a much lower . However, since the differential phase-stability inductor is only 10, the impact of lower varactor is tol erable. When the MIM varactor is at its low-capacitance state, the large DCO internal signal swing and the DC level of 1.4-V supply voltage at source/drain of the pull-up transistors force the drain -nwell junction diodes of the pull-up pMOS to momentarily go into forward-bias condition resulting in a latch-up concern. However, since the forward-bias condition occurs only in 50% of a 3–4 GHz period, the latch-up phenomenon with the parasitic BJTs can not be triggered.

10 Lowering frequency pushing and LDO

About Frequency pushing from **this paper**

Info: An LC-tank VCO circuit has been implemented in a standard 0.35 μm CMOS technology. It is based on a two-transistor biasing structure that improves the performance of frequency pushing and frequency tuning range. Final measurement of proposed structure gives 516 MHz tuning range with 2.278 GHz center frequency and about 0.55%/V frequency pushing in the worst case. The achieved FOM is about -180dBc/Hz, which is very close to the simulated value. This structure is proven to be particularly suitable for achieving low FOM in the VCO circuits having low Q factor LC-tank. Both, the proposed structure and the FOM optimization method, can also be applied to the VCO designs for the applications at higher frequencies, such as 5GHz VCOs for Wireless LAN applications.

Question 13 *Can VCO work for lower voltage of 0.9 V?*

This may be needed if LDO is required because of frequency pushing?

Question 14 *Does frequency only happen because of the ripple directly induced by buffers e.g.?*

Or could it happen because of EM crosstalk?

Is frequency pushing testbench good? Look into this paper. Different testbench would be to make a transient change in Vdd and check how much frequency changes.

Results for class C with pmos bias, only dc change of V_{DD}:

Parameter	typical	spec	min	max	ss -40	ss 125	ff -40	ff 125	Units
Frequency Pushing	43.93	< 2	43.93	100.1	100.1	64.36	75.48	64.09	MHz
Frequency	14.6	> 14.2	14.6	15.83	15.54	15.48	15.83	15.59	GHz

This shows some improvement from frequency pushing of 250 - 300 MHz that was observed for the nmos bias of IMEC Scaldio design.

11 Changing topology and lowering phase noise

Decision on why is single sided oscillator chosen instead of double sided oscillator.

Info: However, if non-negligible parasitic capacitances are found at the tank outputs, the phase-noise performance of the DS-VCO may be seriously degraded, while that of the SS-VCO remains unaffected.

More on the $\frac{1}{f^2}$ Phase Noise Performance of CMOS Differential-Pair LC-Tank Oscillators in **paper** by Pietro Andreani.

11.1 Hybrid class C and class B

Info: Further, the proposed VCO solves the issue of the hybrid mixed-signal start-up procedure exposed in [8]. The main drawback of this approach is that, if oscillation stops for some unaccountable reason, the VCO can only be restarted actuating again the whole start-up procedure.

Referenced paper is:

8 J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L.-R. Zheng, "A low power, startup ensured and constant amplitude class-C VCO in $0.18\,\mu\mathrm{m}$ CMOS," IEEE Microw. Wireless Compon. Lett., vol. 21, no. 8, pp. 427–429, 2011. Dec. 2008.

11.2 Enhanced Oscillation Swing

Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing in **this paper.** Phase noise is lowered by lowering V_{gbias}, but it makes oscillations start up harder.

Info: As noted above, the phase noise improves with increasing the oscillation amplitude, which here would mean lowering the gate bias voltage, V_{bias} . Unfortunately, the original class-C oscillator limits the fixed V_{bias} from being set low enough, otherwise the oscillation may not start up. In [11], a high-swing class-C (HSCC) oscillator was introduced, which removed the tail current transistor of the original class-C oscillator [6]. Instead, an automatic amplitude control was introduced to stabilize the oscillation amplitude. In this work, instead of the transformer used in [11], we choose a simple RC bias circuit.

This is from **paper** Dual-Core High-Swing Class-C VCO design, and references

6 A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

11 M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in Proc. ESSCIRC, Sep. 2011, pp. 495–498

11.3 Questions about new double feedback

Amplitude Feedback for Robust start up

11.4 OTA1 - Start up and gate voltage bias control

Referent voltage should be set and controlled around 800 mV. Need tests for OTAs inside for VCO, currently simulated only PM and DC gain, should test different V_{ref} levels.

11.5 OTA2 - Start up and bias control

Referent voltage should be set and controlled around 400 mV. Problem with OTA2 loop is amplifying noise into the tail bias current. So the new problem arises as noise shaping in LOOP2 is needed. If a OTA of low uGBW is used than start up is too slow.

12 Full LO Range and Frequency Recentering

TODO Add corners for **fs sf** and similar. Because the LO range is split on two cores, ideally halved. Results are simulated for process and temperature corners:

Core and Specifictaion	min	max	sim(min)	sim(max)	Units
VCO core split					
High Band Higher limit	13700		15580	16190	MHz
High Band Lower limit		10000	10870	12460	MHz
High Band range	3700		4710	3730	MHz
Low Band Higher limit	10000		13230	14120	MHz
Low Band Lower limit		6300	6724	8028	MHz
Low Band range	3700		6506	6092	MHz

Table 5: LO range specification and simulation for Scaldio LC tank

Expecting the drop for schematic simulated frequency range, covered range should at least be larger than needed when recentered:

$$HBFR = 13700 - 10000 = 3700 < 3730 = 16190 - 12460 \tag{9}$$

For lower band it's similarily calculated

$$HBFR = 10000 - 6300 = 3700 < 6092 = 14120 - 8028 \tag{10}$$

Lower and higher band are assymetrical and they overlap for at least:

$$HBLBoverlap_{high} = 13230 - 10870 = 2360 \tag{11}$$

$$HBLBoverlap_{low} = 14120 - 12460 = 1660 \tag{12}$$

The worst available frequency digital controlled range is $6092 + 3730 - 1660 = 8162$ MHz which is higher than 7400 MHz.

Question 15 *Are the two VCO-s in the same process corner at the same time?*

Yes. If not than the calculations are wrong.

NOTE: Analog varactor 0-Vt-1 change does not work so it wasn't included. Further frequency recentering after extraction will be needed.

13 Pulling testbench and design of VCO buffer

Needs port at and tuning circuit to keep the reflection at -14 dB. Port of reference impedance 10 kΩ and portAdapter from rfExamples. S parameter analysis to show if the reflection really is -14 dB? Load impedance increased from 100 fF to 1000 fF. VCO buffer is also needed because of the frequency pulling. Does each core have a buffer or do they share it? first make a buffer than maybe a question.

By adding two buffers from `LO_FDDQ_v6`, `LO_FDDQ_INHB_v5_JCx_saldio2b` and `LO_FDDQ_BUF_X24` , frequency pulling drops below 1 MHz.

So this specification looks fine, testbench shown:

How does portAdapter work?

Frequency pulling mentions coupling (crosstalk) between different blocks on chip and the VCO.

14 PTAT and CTAT, the temperature independant Vbias for cascode

TODO Simulate and show results of temperature sweep.

15 Effect of too high tail capacitance

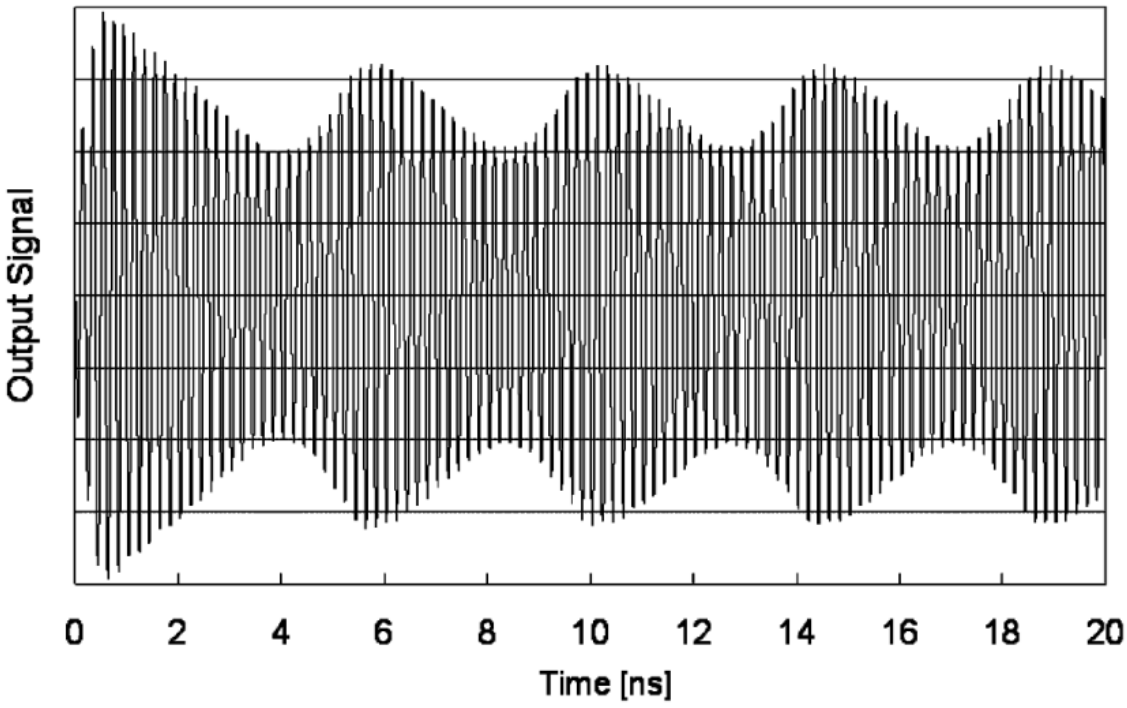

Fig. 10. Effect of too large a tail capacitance: the oscillation suffers from instability, which takes the form of a low-frequency amplitude modulation (squegging).

Figure 3: Squegging

Instability Low frequency amplitude modulation squegging. This was the issue with the original class C with tail current. Is it important for new topology where current bias is PMOS.

16 PLL theory - PLL Lock Detect and calibration

About PLL Lock Detect:

Info: The ability for a PLL to reliably indicate when it is in lock is critical for many applications. An ideal lock detect circuit gives a high indication when the PLL is locked and a low indication when the PLL is unlocked. When VCO calibration finishes it can be indicative if the lock is detected.

PLL VCO calibration usually goes as amplitude frequency and then amplitude calibration, or the other way?

Divide and Conquer algorithm

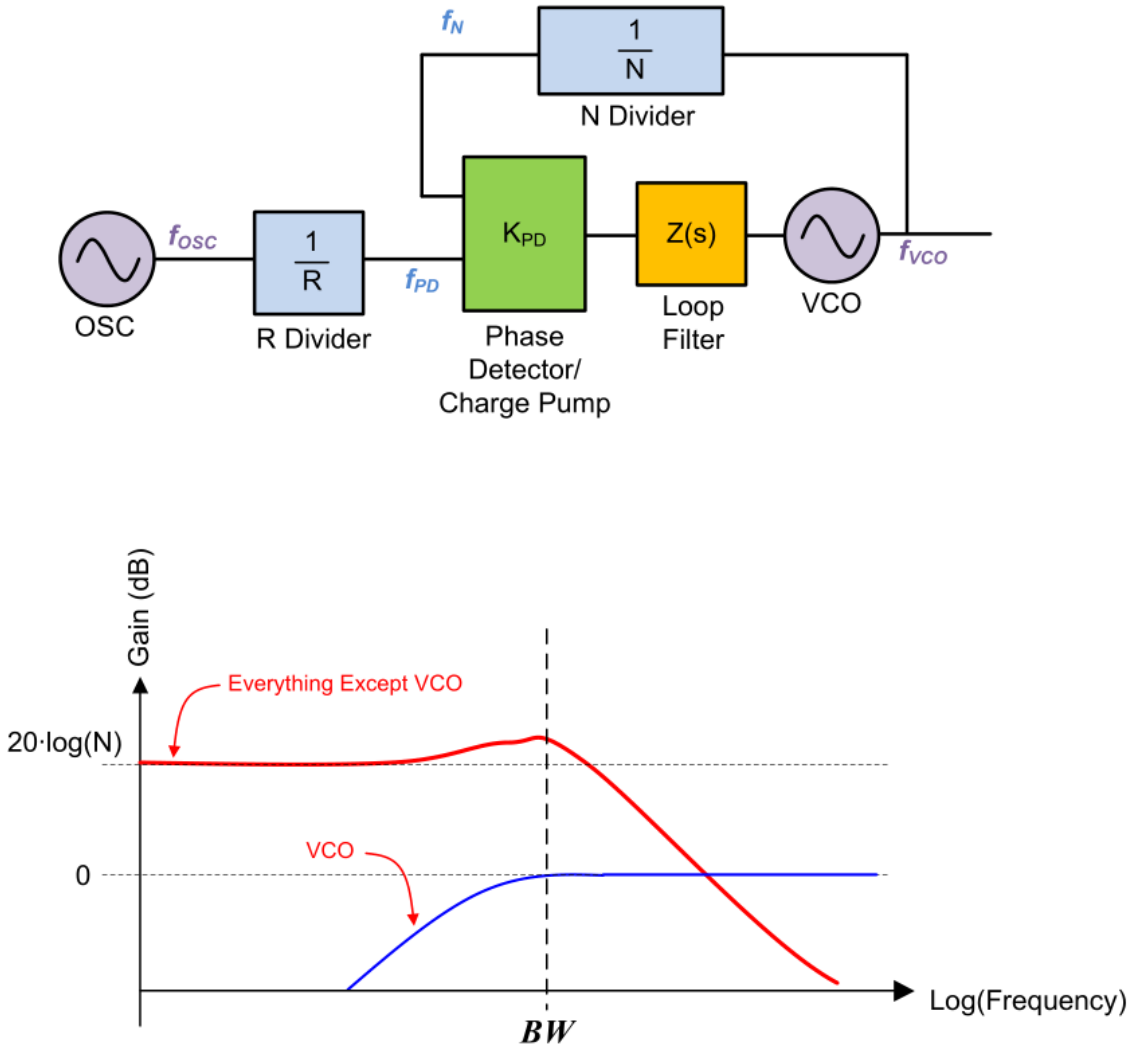

Figure 4: Gain for VCO and other blocks inside of PLL

Info: For the VCO, the noise is suppressed below the loop bandwidth frequency and unshaped above the loop bandwidth.