LO block VCO and VCO Buffer

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Introduction

LO block is LC VCO with internal inductor and fully differential output buffer. Its schematic shall ensure differential connection to the mixer LO input and PLL RF input. LO block should have the characteristics given in Table 1. Due to wide frequency range it is necessary to use switchable capacitor banks.

1 Technical Requirements

	LO Requirements	Note	min	typ	max	Units
	VCO Requirements					
1	Full LO range		6300		13700	MHz
2	Phase Noise at 300 kHz				<-101	dBc/Hz
3	Vtune		0.1		1	V
4	Tuning Sensitivity K_{VCO}				100	MHz/V
5	Pushing	TBD			2	MHz/V
6	Output Voltage	TBD	0.8			V_{p-p}
7	Load Impedance				100	fF
	VCO and output Buffer					
8	Output Voltage	TBD	0.8			V
9	Load Impedance	TBD			1000	fF
10	Harmonic suppression (2_{nd}, typ)		-15			dBc
11	Pulling (14 dB Return Loss, Any Phase)	TBD			2	MHz
	General Specifications					
12	Operating Temperature Range		-40		125	°C
13	Supply Voltage		1	1.1	1.2	V
14	Supply Current				20	mA
15	Shutdown Current				10	μA
16	Time to Switch Between Cores			3	5	ms

Table 1: Specification Requirements

Min and max for supply voltage are not defined in the original document, and time for switching between two cores was defined during the meeting.

Currently Full LO range is split between two cores so the requirement should look like this:

	LO range requirements	Note	min	typ	max	Units
1	High Band core LO range		10000		13700	MHz
2	Low Band core LO range		6300		10000	MHz

Table 2: LO Range Two Core Specification Requirements

Question 1 *What's the variation for supply voltage?*

Not defined probably will be the same as the rest of the

Question 2 K_{VCO} *Why is it in the max column?*

Didn't get answer for this. It's probably also typical and a value that is expected by the PLL design.

Process corners can be found at:

`/tech/tsmc/tsmc40/models/spectre/crn40lp_2d5_v2d0_2_shrink0d9_embedded_usage.scs`

2 Scaldio Design Review

Question 3 *How should calibration be implemented to achieve output voltage peak to peak and minimize noise?*

Is it done for whole PLL?

Question 4 *Difference between class-B and class-C vco?*

Scaldio uses class-C, so all parasitic capacitances connected to the tail don't matter. Having trouble with observing the currents of drain so cannot check this and compare them. Scaldio looks something between class C and class B because of V_{gbias} voltage and because adding inductor between tail NMOS and switching pair improves phase noise. This is attributed to class B, while class C only needs tail capacitance.

Lowest bit of digital varactor (L0_PLL_hbVCO_Cdig_SC2B_VCOS_SC2C_PLL) doesn't do anything, isn't even monotonous. Maybe makes more sense when simulating extracted cells. Digital varactor needs to be redesigned, it could lower the Q factor. Main difference between class B and class C can be observed by investigating their drain currents.

2.1 Main testbench

Main testbench covers everything except for frequency pulling and full LO range. The simulation results are obtained at the higher end of the LO range. Phase noise is simulated by pss+pnoise.

Info: With Noise Type=timeaverage and ALL(AM,PM,USB,LSB), you can plot the AM and PM components as well as the total noise. In addition, you can plot phase noise and FM jitter results for oscillators. Plotting is done using the Direct Plot Form. **External link**

Function of phase noise is simulated for PM noise type.
How to choose beat frequency for autonomous system from forum **thread**.

Info: In an autonomous system (e.g. an oscillator), you turn on the "oscillator" checkbox, and the beat frequency is then the estimated frequency, which gives PSS a starting point to solve for the oscillator frequency. It's important when in oscillator mode to select the outputs of the circuit, which include any subharmonics. In other words, if you have an oscillator followed by a divider, point at the divider output, and give the estimated divided frequency as the beat frequency. Again, this is because you need to solve an integer number of cycles of all the frequencies in the circuit. Note, don't use oscillator mode for circuits which aren't oscillators, since you're then trying to get the simulator to solve for an unknown which is not unknown, which may lead to convergence problems.

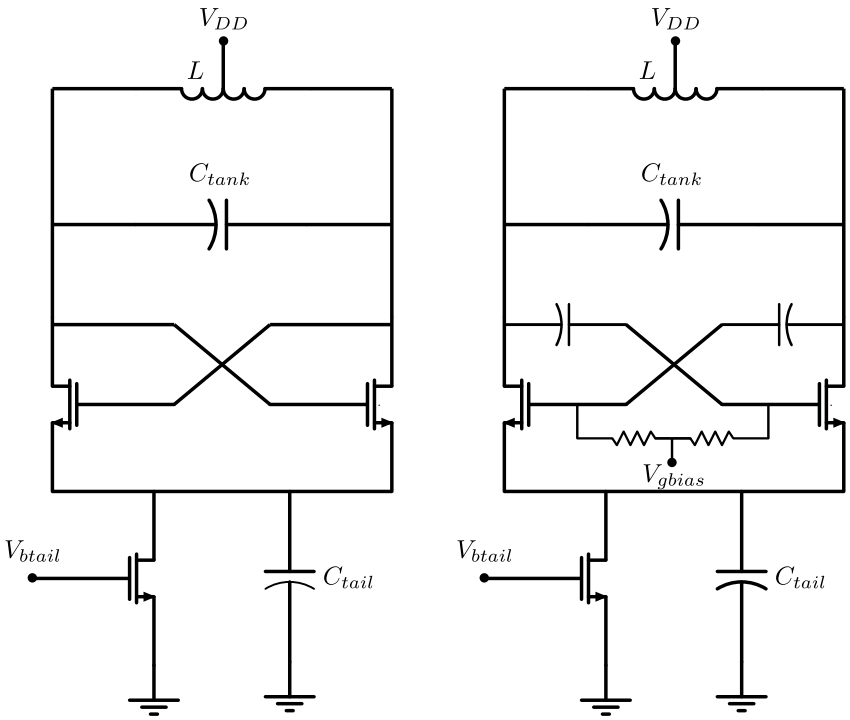

Figure 1: Schematic difference between class C and class B

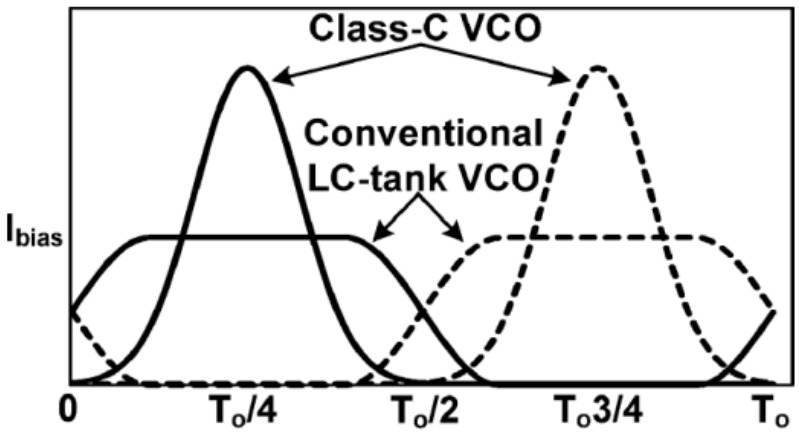

Fig. 2. Drain current of the switch pair FETs for conventional LC-tank VCOs and class-C VCOs.

Most of the I_{bias} tune digital control is not used for the higher band, so by increasing the number of steps to cover even higher frequencies than the original design finer bias control is needed.

2.2 Simulation Results for Scaldio design

Simulated only nominal corner with change for V_{DD} only for frequency pushing simulation.

Phase noise changes a lot for different tuning voltages between -90 and -100 dBc/Hz. Phase noise is probably not modeled ok because the VCO doesn't have the connection between current bias tail and

	LO Requirements	Note	min	typ	max	Sim(Typ)	Units
1	Phase Noise at 300 kHz				<-101	-98	dBc/Hz
2	Tuning Sensitivity K_{VCO}				100	over	MHz/V
3	Pushing	TBD			2	279.7	MHz/V
4	Output Voltage	TBD	800			809.3	mV_{p-p}
5	Harmonic suppression (2_{nd}, typ)		-15			-26.78	dBc
6	Pulling (14 dB Return Loss, Any Phase)	TBD			2	19.51	MHz

Table 3: Scaldio IMEC design Results

the switching pair of VCO as transmission line. That inductance and C_{tail} should resonate at $2\omega_O$ (tank oscillating frequency), but only in the case of class B oscillator. Check what type is vco oscillator.

3 Q factor of LC tank

Need testbenches capacitance of tank, varactors and inductor, and for different controls and also corners. Process corners for varactors are the same as MOSFET.

Question 5 *What kind of chip is it?*

What kind of inductance is expected to be connected on V_{DD} and V_{SS} pins. This may or may not change the results. Removed all together right now.

Testbench for differential Q and L of the inductor that is EMX simulated is shown in Figure 2.

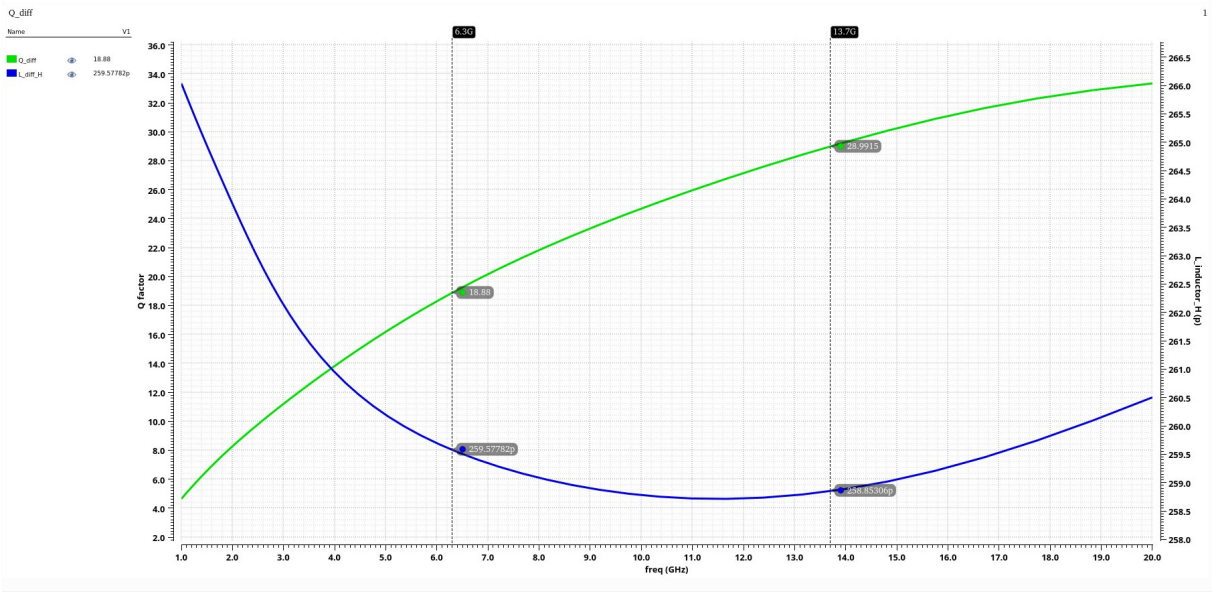

Figure 2: Q factor and inductance of L

Q factor is better at the higher frequency.

Simulated Q factor of both varactors and inductor. Q factor of digital varactor for lower bit controls is not much better than Q of inductor.

Capacitor calculating capacitance and Q factor:

$$Y_{diff}(im) = imag(ypm('sp11)) + imag(ypm('sp22)) - imag(ypm('sp21)) - imag(ypm('sp12)) \quad (1)$$

$$Y_{diff}(re) = real(ypm('sp11)) + real(ypm('sp22)) - real(ypm('sp21)) - real(ypm('sp12)) \quad (2)$$

Capacitance:

$$C_{diff} = \frac{Y_{diff}(im)}{2\pi f} \quad (3)$$

Q factor of capacitor:

$$Q_C = \frac{Y_{diff}(im)}{Y_{diff}(re)} \quad (4)$$

More info can be found in **paper** A Thorough Analysis of the Tank Quality Factor in LC Oscillators with Switched Capacitor Banks.

How to calculate Q factor of tank from the same paper.

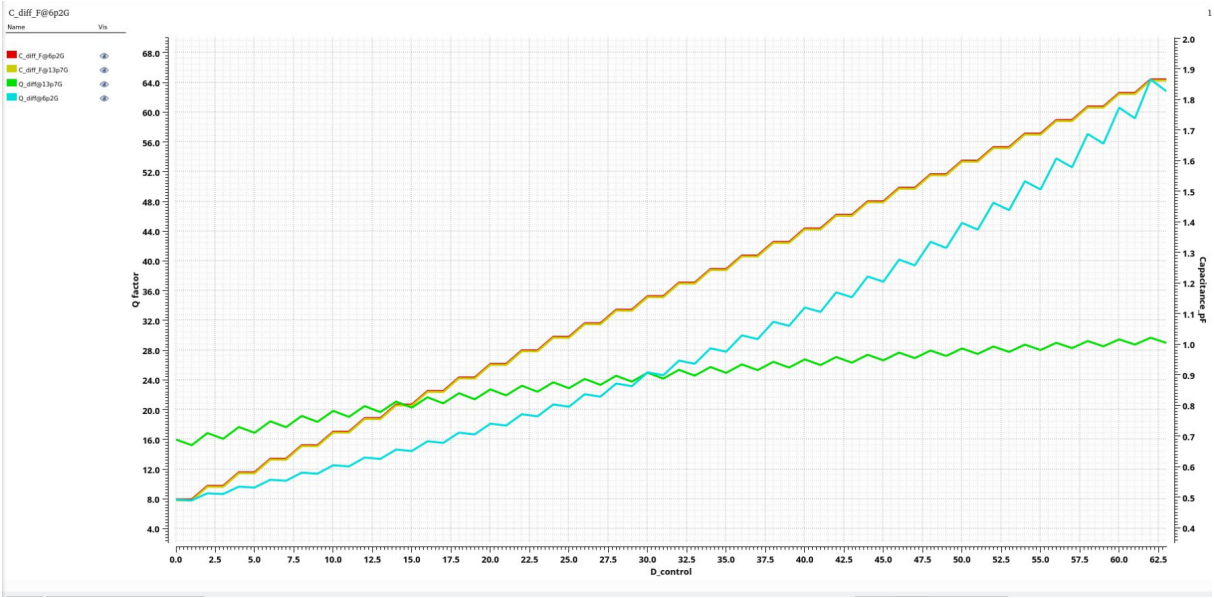

Figure 3: C and Q of digital varactor through controls

Info: It can be proved (and it is a well known result) that the quality factor of the tank is equal to the parallel combination of the quality factor of the inductance, Q_L, and the quality factor of the capacitance, Q_C , that make up the resonant circuit. Once we have the two quality factors Q_L and Q_C is hence very easy to calculate Q_T .

Found definitions:

$$Q_{LC} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{f_r}{\Delta f} = \frac{\omega_r}{\Delta \omega} = \frac{\tau_d \omega}{2} \tag{5}$$

where τ_d is group delay. Also

$$Q_T = Q_{LC} = \omega \frac{ES}{APD} \tag{6}$$

where ES is energy stored and APD is average power dissipation.

Question 6 *How to calculate group delay using sparam analyis?*

?

3.1 Calculating Q factor, LC tank by ringing method

Link to **website** that shows ring down method of calculating Q factor. Not implemented in virtuoso TODO.

4 Figure of Merit different definitions

Info: The theoretical maxima for the FoM of an oscillator is given by $FoM = 174 + 20log_{10}(Q)$ dBc/Hz

How to calculate oscillator FoM? Is Q_L factor dominant enough to just equate it with LC tank Q facor. The widely used FOM is calculated by:

$$FoM = L\{\Delta\omega\}(\Delta f/f_0)^2 PVCO[mW] \tag{7}$$

Where $L\{\Delta\omega\}$ is the phase noise, $\Delta\frac{f}{f_0}$ is the ratio between the offset frequency and the carrier, and P_{VCO} is the power consumption of the VCO-core. There is also FoM^T and FoM_A

$$FoM^T = FoM - 20\log(\frac{FTR}{10}) \tag{8}$$

and

$$FoM_A = FoM + 10\log(A) \tag{9}$$

where A is area [mm^2], and FTR frequency tuning range [$\%$]
Information about digital varactor copied from **External link**

Info: Each bit of MIM varactor contains two MIM capacitors connected differentially with a series switch, two pull-up and two pull-down transistors to effectively turn the varactor between its high and low-capacitance states. Measured intrinsic Q of the MIM capacitor is 80 at 3.6 GHz. When is turned on, i.e., high-capacitance state, the varactor Q drops to 30. When is turned off to be in low-capacitance state, the parasitic capacitance of the MIM capacitor and transistors has an effective of 50. The pull-down transistors set the DC levels for drain and source of at 0 V so that can be efficiently turned into triode region while the weak pull-up transistors set the DC level to VDDOSC to reduce the parasitic capacitance of thus increasing of the parasitic capacitance. The pull-up pMOS can be implemented by either resistors or transistors. The latter was chosen for silicon area efficiency. Compared to MOS varactors, MIM varactors have a much lower . However, since the differential phase-stability inductor is only 10, the impact of lower varactor is tol erable. When the MIM varactor is at its low-capacitance state, the large DCO internal signal swing and the DC level of 1.4-V supply voltage at source/drain of the pull-up transistors force the drain -nwell junction diodes of the pull-up pMOS to momentarily go into forward-bias condition resulting in a latch-up concern. However, since the forward-bias condition occurs only in 50% of a 3–4 GHz period, the latch-up phenomenon with the parasitic BJTs can not be triggered.

5 Lowering frequency pushing and LDO

About Frequency pushing from **this paper**

Info: An LC-tank VCO circuit has been implemented in a standard 0.35 μm CMOS technology. It is based on a two-transistor biasing structure that improves the performance of frequency pushing and frequency tuning range. Final measurement of proposed structure gives 516 MHz tuning range with 2.278 GHz center frequency and about 0.55$\%$/V frequency pushing in the worst case. The achieved FOM is about -180dBc/Hz, which is very close to the simulated value. This structure is proven to be particularly suitable for achieving low FOM in the VCO circuits having low Q factor LC-tank. Both, the proposed structure and the FOM optimization method, can also be applied to the VCO designs for the applications at higher frequencies, such as 5GHz VCOs for Wireless LAN applications.

Question 7 *Can VCO work for lower voltage of 0.9 V?*

This may be needed if LDO is required because of frequency pushing?

Question 8 *Does frequency only happen because of the ripple directly induced by buffers e.g.?*

Or could it happen because of EM crosstalk?

Is frequency pushing testbench good? Look into this paper. Different testbench would be to make a transient change in Vdd and check how much frequency changes.

Results for class C with pmos bias, only dc change of V_{DD}:

Parameter	typical	spec	min	max	ss -40	ss 125	ff -40	ff 125	Units
Frequency Pushing	43.93	< 2	43.93	100.1	100.1	64.36	75.48	64.09	MHz
Frequency	14.6	> 14.2	14.6	15.83	15.54	15.48	15.83	15.59	GHz

This shows some improvement from frequency pushing of 250 - 300 MHz that was observed for the nmos bias of IMEC Scaldio design.

6 Changing topology and lowering phase noise

Decision on why is single sided oscillator chosen instead of double sided oscillator.

Info: However, if non-negligible parasitic capacitances are found at the tank outputs, the phase-noise performance of the DS-VCO may be seriously degraded, while that of the SS-VCO remains unaffected.

More on the $\frac{1}{f^2}$ Phase Noise Performance of CMOS Differential-Pair LC-Tank Oscillators in **paper** by Pietro Andreani.

6.1 Hybrid class C and class B

Info: Further, the proposed VCO solves the issue of the hybrid mixed-signal start-up procedure exposed in [8]. The main drawback of this approach is that, if oscillation stops for some unaccountable reason, the VCO can only be restarted actuating again the whole start-up procedure.

Referenced paper is:

8 J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L.-R. Zheng, "A low power, startup ensured and constant amplitude class-C VCO in $0.18\,\mu\mathrm{m}$ CMOS," IEEE Microw. Wireless Compon. Lett., vol. 21, no. 8, pp. 427–429, 2011. Dec. 2008.

6.2 Enhanced Oscillation Swing

Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing in **this paper.** Phase noise is lowered by lowering V_{gbias}, but it makes oscillations start up harder.

Info: As noted above, the phase noise improves with increasing the oscillation amplitude, which here would mean lowering the gate bias voltage, V_{bias} . Unfortunately, the original class-C oscillator limits the fixed V_{bias} from being set low enough, otherwise the oscillation may not start up. In [11], a high-swing class-C (HSCC) oscillator was introduced, which removed the tail current transistor of the original class-C oscillator [6]. Instead, an automatic amplitude control was introduced to stabilize the oscillation amplitude. In this work, instead of the transformer used in [11], we choose a simple RC bias circuit.

This is from **paper** Dual-Core High-Swing Class-C VCO design, and references

6 A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

11 M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in Proc. ESSCIRC, Sep. 2011, pp. 495–498

6.3 Questions about new double feedback

Amplitude Control Feedback and Voltage bias control for Robust start up.

6.4 OTA1 - Start up and gate voltage bias control

Referent voltage should be set and controlled around 800 mV. Need tests for OTAs inside for VCO, currently simulated only PM and DC gain, should test different V_{ref} levels.

6.5 OTA2 - Start up and bias control

Referent voltage should be set and controlled around 400 mV. Problem with OTA2 loop is amplifying noise into the tail bias current. So the new problem arises as noise shaping in LOOP2 is needed. If a OTA of low uGBW is used than start up is too slow.

7 Full LO Range and Frequency Recentering

TODO Add corners for **fs sf** and similar. Because the LO range is split on two cores, ideally halved. Results are simulated for process and temperature corners:

Core and Specifictaion	min	max	sim(min)	sim(max)	Units
VCO core split					
High Band Higher limit	13700		15580	16190	MHz
High Band Lower limit		10000	10870	12460	MHz
High Band range	3700		4710	3730	MHz
Low Band Higher limit	10000		13230	14120	MHz
Low Band Lower limit		6300	6724	8028	MHz
Low Band range	3700		6506	6092	MHz

Table 4: LO range specification and simulation for Scaldio LC tank

Expecting the drop for schematic simulated frequency range, covered range should at least be larger than needed when recentered:

$$HBFR = 13700 - 10000 = 3700 < 3730 = 16190 - 12460 \tag{10}$$

For lower band it's similarily calculated

$$HBFR = 10000 - 6300 = 3700 < 6092 = 14120 - 8028 \tag{11}$$

Lower and higher band are assymetrical and they overlap for at least:

$$HBLBoverlap_{high} = 13230 - 10870 = 2360 \tag{12}$$

$$HBLBoverlap_{low} = 14120 - 12460 = 1660 \tag{13}$$

The worst available frequency digital controlled range is $6092 + 3730 - 1660 = 8162$ MHz which is higher than 7400 MHz.

Question 9 *Are the two VCO-s in the same process corner at the same time?*

Yes. If not than the calculations are wrong.

NOTE: Analog varactor 0-Vt-1 change does not work so it wasn't included. Further frequency recentering after extraction will be needed.

8 Pulling testbench and design of VCO buffer

Needs port at and tuning circuit to keep the reflection at -14 dB. Port of reference impedance 10 kΩ and portAdapter from rfExamples. S parameter analysis to show if the reflection really is -14 dB? Load impedance increased from 100 fF to 1000 fF. VCO buffer is also needed because of the frequency pulling. Does each core have a buffer or do they share it? first make a buffer than maybe a question.

By adding two buffers from `LO_FDDQ_v6`, `LO_FDDQ_INHB_v5_JCx_saldio2b` and `LO_FDDQ_BUF_X24` , frequency pulling drops below 1 MHz.

So this specification looks fine, testbench shown:

How does portAdapter work?

Frequency pulling mentions coupling (crosstalk) between different blocks on chip and the VCO.

9 PTAT and CTAT, the temperature independant Vbias for cascode

TODO Simulate and show results of temperature sweep.

10 Effect of too high tail capacitance

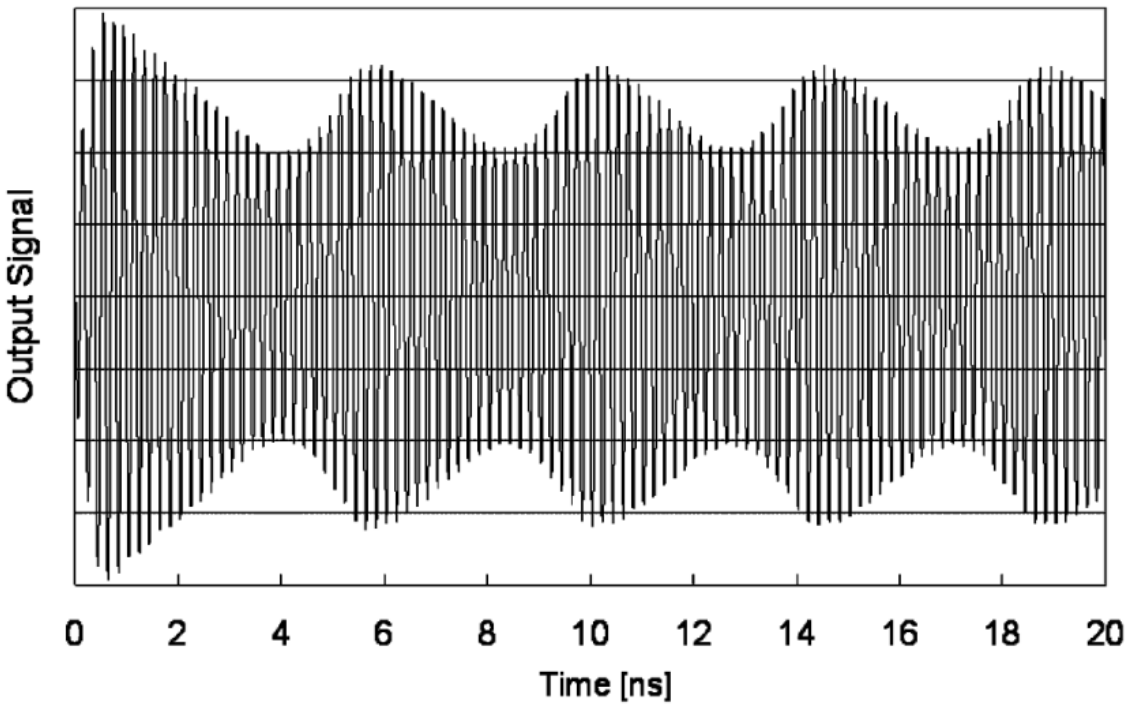

Fig. 10. Effect of too large a tail capacitance: the oscillation suffers from instability, which takes the form of a low-frequency amplitude modulation (squegging).

Figure 4: Squegging

Instability Low frequency amplitude modulation squegging. This was the issue with the original class C with tail current. Is it important for new topology where current bias is PMOS.

TODO simulate for high and for low frequency. How to simulate envelope?

11 PLL theory - PLL Lock Detect and calibration

About PLL Lock Detect:

Info: The ability for a PLL to reliably indicate when it is in lock is critical for many applications. An ideal lock detect circuit gives a high indication when the PLL is locked and a low indication when the PLL is unlocked. When VCO calibration finishes it can be indicative if the lock is detected.

PLL VCO calibration usually goes as amplitude frequency and then amplitude calibration, or the other way?

Divide and Conquer algorithm

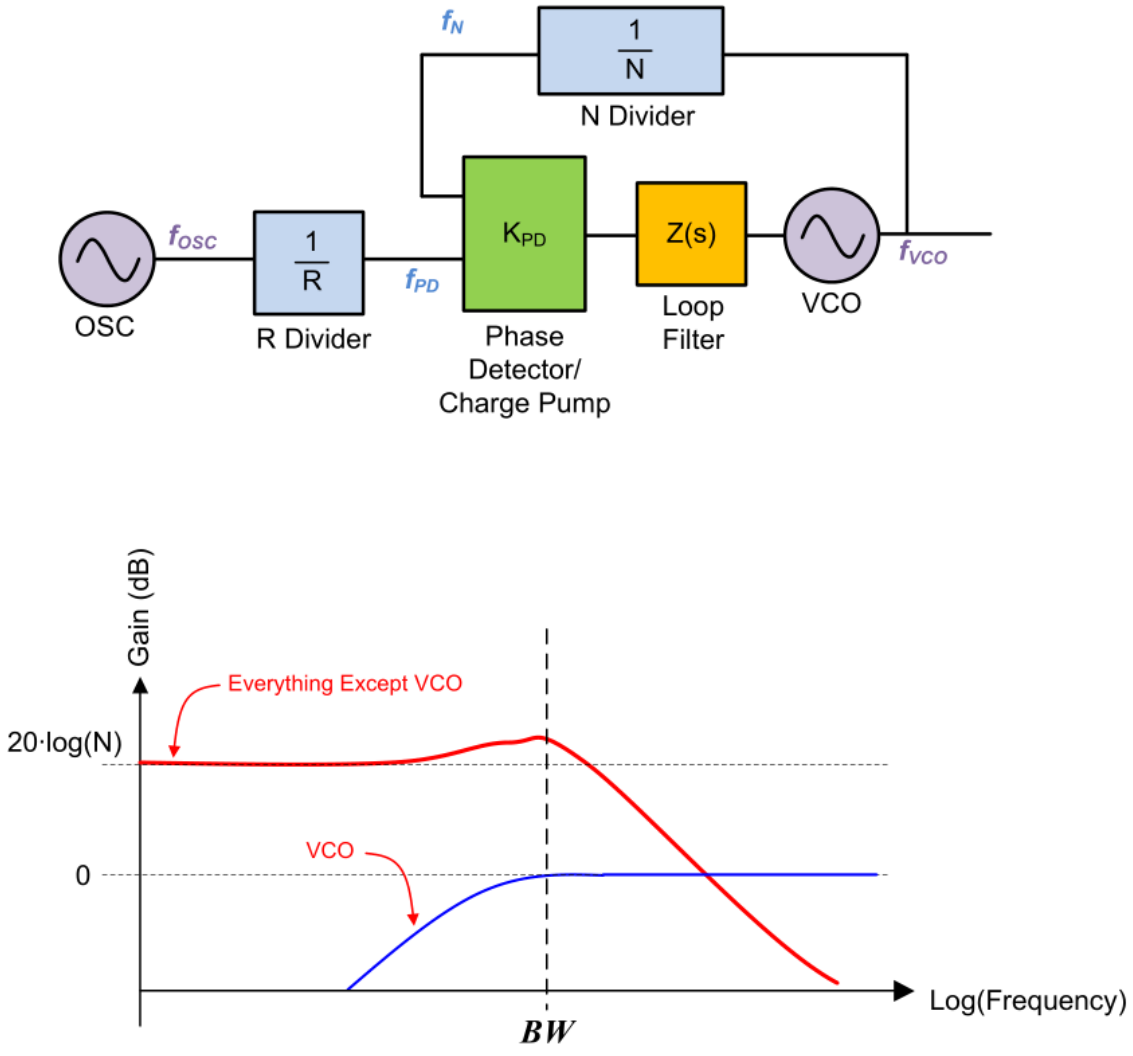

Figure 5: Gain for VCO and other blocks inside of PLL

Info: For the VCO, the noise is suppressed below the loop bandwidth frequency and unshaped above the loop bandwidth.