

Low Noise 6-8 GHz VCO with Differential Tuning as part of PLL

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1 Introduction

Working title needs to be changed VCOs frequency range is changed probably 7-12 GHz and around 4 GHz.

This needs to be added to body of document. The open items from last meeting minutes I recorded are:

- Packaging concerns, risks and schedule
- Die quantity and meaningful sample volume
- test chip content and expectations
- overall schedule for the follow-on tape out in 2025

Planning VCO timeframe per core:

- Design – 10 days
- Layout – 10 days
- Verification – 0 day

2 List of Abbreviations

- CML - Common Mode Logic
- CP - Charge Pump
- CTAT - Complementary to Absolute Temperature - usually misconstrued to represent constant
- DAC - Digital Analog Converter
- ECL - Emitter Coupled Logic
- EDA - Electronic Design Automation
- EM - Electro Magnetic
- EVB - EValuation Board
- FET - Field-Effect Transistor
- FTR - Fine Tuning Range (unit is percentage)
- HCI - Hot Carrier Injection
- LBE - Localized Backsided Etching
- MEMS - MicroElectronical Mechanical Systems
- NBTI - Negative-Bias Temperature Instability
- PBTI - Positive-Bias Temperature Instability
- PCB - Printed Circuit Board
- PFD - Phase Frequency Detector
- PnR - Place and Route
- PSD - Power Spectral Density
- PTAT - Proportional to Absolute Temperature
- Q - Quality (factor usually)
- QFN - Quad Flat No lead
- SIW - Substrate Integrated Waveguide
- TDDB - Time Dependent Dielectric Breakdown
- TOEO - Tuneable Opto-electronic Oscillators
- YIG - Yttrium Iron Garnet
- VCO - Voltage Controlled Oscillator
- PLL - Phase Locked Loop
- RMS - Root Mean Square

3 Quality of Life - software tools

Quality of life regarding LaTex for this document, commercial/proprietary EDA software for this and previous projects and potential open source EDA software for future projects.

3.1 QoL \LaTeX

3.1.1 Colored rows and columns

Coloring inside of table

	x	y	w	z
variable 1	a	b	c	d
variable 2	a	b	c	d

Subfigures examples in comments

3.1.2 Nested tables using tabular

source: You could nest a tabular within another tabular:

One	Two	Three	Four
Een	Twee	Drie	Vier
One	Two	Three	Four

Drie

3.2 Open Source EDA Software

3.2.1 NGSPICE

Regarding open-source PDK for SG13G2, it's work in progress, but I think worth to consider. Even if just the simulator can be replaced with ngspice or xyce, it could boost productivity from not being license-bound. Please check this out:

[ihp sg13g2](#)

Documentation on github is sparse, some more info is here: [openPDK opeentooling and open source design](#)

[open source PDK, research and prototyping](#)

3.2.2 Required libraries - Linux Installation

libxaw7-dev and libreadline6-dev
KiCad plus ngspice

3.2.3 openEMS

openEMS is a free and open source electromagnetic field solver based on the Finite-Difference Time Domain (FDTD) method. Using an improved version of the highly-successful FDTD method (known as Equivalent-Circuit FDTD, or EC-FDTD), openEMS solves Maxwell's equations in discretized space and time to directly simulates the propagation of electromagnetic waves, in a 3D full-wave manner. It has the potential to analyze problems in important applications such as RF/microwave circuit design, antenna, radar, meta-material, and medical research.

3.3 Commercial EDA software

EMX and Momentum

EMX software from Cadence, Momentum from ADS

3.3.1 Change font in Visualisation Cadence

Example:

```
myFont = "Roboto Mono Medium,14,-1,5,75,0,0,0,0,0,0"
envSetVal("viva.horizMarker" "font" 'string myFont)
envSetVal("viva.referenceLineMarker" "font" 'string myFont)
envSetVal("viva.vertMarker" "font" 'string myFont)
envSetVal("viva.pointMarker" "font" 'string myFont)
envSetVal("viva.refPointMarker" "font" 'string myFont)
envSetVal("viva.specMarker" "font" 'string myFont)
envSetVal("viva.interceptMarker" "font" 'string myFont)
envSetVal("viva.circleMarker" "font" 'string myFont)
envSetVal("viva.interceptMarker" "font" 'string myFont)
envSetVal("viva.multiDeltaMarker" "font" 'string myFont)
envSetVal("viva.transEdgeMarker" "font" 'string myFont)

envSetVal("viva.trace" "lineThickness" 'string "thick")
envSetVal("viva.trace" "lineStyle" 'string "solid")
envSetVal("viva.trace" "symbolsOn" 'string "true")
envSetVal("viva.trace" "symbolStyle" 'string "Diamond")
```

3.3.2 VerilogA Decoder Code

Example of 15 bit decoder
<pre>'include "disciplines.vams" module Decoder_15bit_va(L); output [14:0] L; electrical [14:0] L; parameter real tdel = 20.0p, trise = 40p, tfall = 40p, VDD = 1.1; parameter integer select = 0; integer out[14:0], mask, i, j; analog begin @(initial_step) begin for(i=14; i>=0; i=i-1) begin mask=1; for(j=1; j<=i; j=j+1) mask=mask*2; out[i]=(select & mask) >> i; end end</pre>

Example of 15 bit decoder - cont.

```
V(L[0]) <+ transition(VDD * out[0] ,  
    tdel, trise, tfall);  
V(L[1]) <+ transition(VDD * out[1] ,  
    tdel, trise, tfall);  
V(L[2]) <+ transition(VDD * out[2] ,  
    tdel, trise, tfall);  
V(L[3]) <+ transition(VDD * out[3] ,  
    tdel, trise, tfall);  
V(L[4]) <+ transition(VDD * out[4] ,  
    tdel, trise, tfall);  
V(L[5]) <+ transition(VDD * out[5] ,  
    tdel, trise, tfall);  
V(L[6]) <+ transition(VDD * out[6] ,  
    tdel, trise, tfall);  
V(L[7]) <+ transition(VDD * out[7] ,  
    tdel, trise, tfall);  
V(L[8]) <+ transition(VDD * out[8] ,  
    tdel, trise, tfall);  
V(L[9]) <+ transition(VDD * out[9] ,  
    tdel, trise, tfall);  
V(L[10]) <+ transition(VDD * out[10] ,  
    tdel, trise, tfall);  
V(L[11]) <+ transition(VDD * out[11] ,  
    tdel, trise, tfall);  
V(L[12]) <+ transition(VDD * out[12] ,  
    tdel, trise, tfall);  
V(L[13]) <+ transition(VDD * out[13] ,  
    tdel, trise, tfall);  
V(L[14]) <+ transition(VDD * out[14] ,  
    tdel, trise, tfall);  
  
end  
endmodule
```

Saving Histories in ADE explorer

Virtuosity: Exploring Histories

```
envSetVal("maestro.explorer" "onHistoryNameCollision" 'cyclic "Overwrite")
envSetVal("adexl.historyNamePrefix" "showNameHistoryForm" 'boolean t)
envSetVal("maestro.explorer" "onHistoryNameCollision" 'cyclic "IncrementAsNew")
```

PVS Design Flow

PVS has problems with digital circuits using global nets.

- PVS DRC
- PVS LVS - you can setup Quantus from here, generates svdb file, do this after it passes LVS
- Quantus PVS

Curve fitting using Wolfram Alpha

usefull reddit post Wolfram Alpha without programming

Curve fitting for Vtune input range (-1.6 ; 1.6) to calculate polynomial:

```
\{\{-1.6, -2.7\}, \{-1.1, -2.4\}, \{-0.5, -1.8\}, \{0, 0 \}, \{0.5, 1.8\}, \{1.1, 2.4\}, \{1.6, 2.7 \}\}
```

Curve fitting for Vtune input range (0 ; 3.2) to calculate polynomial:

```
\{\{0, -2.7\}, \{0.5, -2.4\}, \{1.1, -1.8\}, \{1.6, 0 \}, \{2.1, 1.8\}, \{2.7, 2.4\}, \{3.2, 2.7 \}\}
```

VerilogA parse code

```
vmsUpdateCellViews(?lib "elta_VCO_aleksandarv" ?cell "vco_va_model" ?view "verilogA")
```

4 Technical specification, Design and Signoff Plan

4.1 Novelic Technical Offer

Document before the start of the project. Here are technical Novelic evaluation summary on provided documents:

- Overall conclusion is that: the provided report contains almost the same type of the architecture, like provided in Novelic & Nirsén study.
- However, the simulation provided by customer does not include process corners and temp range. We see TT process and nominal temp. It is clear that temperature and process deviation will influence the performance of the power detector, which imposes the design risks.
- Dead zone of PFD which they are claiming that cannot measure is not that critical, more important is blind zone which is in our case on schematic in order of $0.5 \times T_{osc}$ at 8GHz in some corners. This is also a design risk.
- All provided schematics are not including any parasitic estimates which make significant difference as we saw in our simulations. This is a design risk.
- Robustness over supply voltage variation imposes the design risk.
- Further technical explanation is following:
 - Reset path of this and all similar PFDs has minimum 5 logic gates in signal path.
 - Let's assume propagation through gate is 5ps (schematic, typical, in reality and over PVT is even worse!). Period of signal is 125ps at 8GHz which means we are losing 20% of period just for propagation. Layout parasitics will degrade this to 40% in typical. For reset delay $> 50\%$ of period we cannot make a lock of PLL by design. This presents a design risk.
 - In the provided document SiGe solution was not simulated in closed loop scenario - PFD and CP tested separately with optimistic separation between input signals. This presents a design risk.
 - Mixer gm PFD is good try but followed by ideal VCO in the provided document. So, we can confirm to get similar PFD values like in initial simulations. But provided simulation does not include any real VCO with imperfections. By this approach PLL will work good if VCO is ideal, with possibly too optimistic phase noise profile. This presents a design risk.
 - If the mixer is used in PFD (like possible proposed option) basically we would have PHASE ONLY locking, while if input frequencies of the PFD are significantly apart from each other, so we will not have PLL in LOCK state. This is the most likely scenario since range of input frequencies is 1-8GHz. So most probably this approach can be followed for design.
 - In entire document provided by End user, Novelic do not see any VCO design, which is the most critical part besides PFD, so VCO is considered as an ideal VCO.
 - Based on Novelic previous experience, and comparison to the state-of-the-art performance in journal/conference publications and/or patents we could not confirm feasibility of making VCO with required phase noise requirements, like in initial specifications.

4.2 Specification and Design Review Plan

Suggestion on how to review and specify chip and comparable options:

- Preliminary Design Review - PDR
- Critical Design Review - CDR
- Sign-off tools - Voltus or Voltera to check currents
- (mentioned once) acquire evaluation boards (EVB) for ADF6610, LMX2594
- Testability options within chip

- VCO registers/overriding
- External test requirements/definitions

Signoff EDA

4.3 References from Novelic feasibility study

Papers that are referenced in the feasibility study concerning Gilbert Cell Mixer Based PD and ECL PFD:

- ng2006 A. W. L. Ng, G. C. T. Leung, Ka-Chun Kwok, L. L. K. Leung and H. C. Luong, "A 1-V 24-GHz 17.5-mW phase-locked loop in a 0.18-/spl mu/m CMOS process," in IEEE Journal of Solid-State Circuits, vol. 41, no. 6, pp. 1236-1244, June 2006, doi: 10.1109/JSSC.2006.874332.
- razavi2002 B. Razavi, "Challenges in the design high-speed clock and data recovery circuits," in IEEE Communications Magazine, vol. 40, no. 8, pp. 94-101, Aug. 2002, doi: 10.1109/MCOM.2002.1024421.
- Pottbacher1992 A. Pottbacher, U. Langmann and H. - Schreiber, "A Si bipolar phase and frequency detector IC for clock extraction up to 8 Gb/s," in IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1747-1751, Dec. 1992, doi: 10.1109/4.173101.
- park2008 Park, Hyun & Kim, Kang & Lim, Sang-Kyu & Ko, Jesoo. (2008). "A 40 Gb/s Clock and Data Recovery Module with Improved Phase-Locked Loop Circuits". Etri Journal - ETRI J. 30. 275-281. 10.4218/etrij.08.1107.0043.
- pantoli2016 L. Pantoli, L. N. Di Muccio, G. Leuzzi, A. Barigelli and F. Vitulli, "Wideband high-linearity low-phase-noise VCO for space communication systems," 2016 11th European Microwave Integrated Circuits Conference (EuMIC), London, 2016, pp. 205-208, doi: 10.1109/EuMIC.2016.7777526.
- florian2017 C. Florian, S. D'Angelo, D. Resca and F. Scappaviva, "A chip set of low phase noise MMIC VCOs at C, X and Ku band in InGaP-GaAs HBT technology for satellite telecommunications," 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI, 2017, pp. 1148-1151, doi: 10.1109/MWSYM.2017.8058802.
- hyvert2015 J. Hyvert, D. Cordeau, J. Paillot, P. Philippe and B. Fahs, "A new class-C very low phase-noise Ku-band VCO in 0.25 μ m SiGe:C BiCMOS technology," 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, 2015, pp. 1-4, doi: 10.1109/MWSYM.2015.7166964.
- hyvert2016 J. Hyvert, D. Cordeau, J. Paillot and P. Philippe, "A very low phase-noise ku-band resistively coupled VCO array in 0.25 μ m SiGe:C BiCMOS," 2016 46th European Microwave Conference (EuMC), London, 2016, pp. 501-504, doi: 10.1109/EuMC.2016.7824389.

5 Packaging Technology Options

- Flip Chip
 - Solder balls on Nickel/Gold finish (time consuming)
 - Heat Spreader (Graphene-based)
 - Underfill materials
 - Redistribution layers(?)
- Copper Pillar (flipped die)
 - 30 µm min diameter, better thermal conductivity
 - More stable (no need for underfill)
 - Heat spreader most likely needed
- Chip on board
 - Glue chip on PCB cavity (non-conductive glue needed if BSE)
 - Only backside cooling available
 - Connect with wirebonds
- Open cavity QFN
 - Similar to chip on board
 - Extra penalty due to higher thermal resistance of package

On packaging from Elad:



Info: I was asked to give my opinion regarding silicone component packaging.

Since the size of the component is (on the major axis) 3.5 and down bonds to the ground are required on both sides, you need to verify the distance of the pads of the component from the edge of the die, the closer you can use a smaller ground surface. Assuming that the pads reach the edge, it will be possible to use a ground surface in a package of 4.1 mm, depending on the planning design rules of the Assembly house.

In light of this, I recommend considering using the RJR air cavity 6 x 6 mm package and its lid. Regarding the glue, since the CTE gap between the component and the packaging is large, I recommend using the glue (I think they thought of this direction) me8456lv, which has a thermal conductivity of around 6W/m

[rjrtechnologies website](#)

QFN stands for Quad Flat No lead.

Number of pins is important for packaging - keep it below 32.

5.1 Flip Chip as a packaging option

Flip chip, also known as controlled collapse chip connection or its abbreviation, C4, is a method for interconnecting dies such as semiconductor devices, IC chips, integrated passive devices and microelectromechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads. This is in contrast to wire bonding, in which the chip is mounted upright and fine wires are welded onto the chip pads and lead frame contacts to interconnect the chip pads to external circuitry.

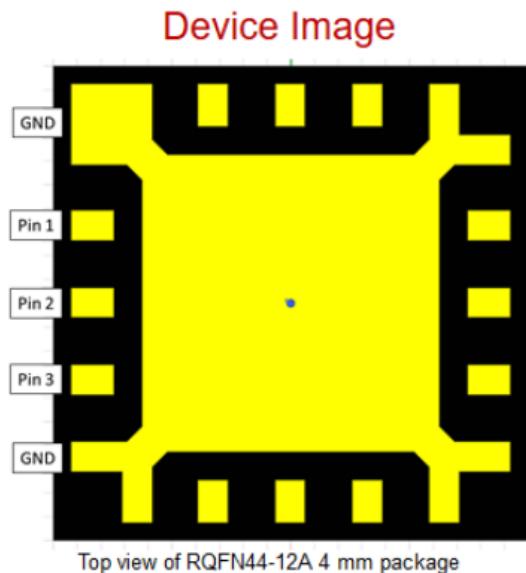


Figure 1: RQFN packaging example

5.2 Packaging house options

Packaging house options are:

- TAI PRO
 - [Website for Production](#)
- PacTech (IHP has collaboration with them)
 - [Website for Wafer Level Packaging Services](#)
- IZM
 - [Website for Fine Pitch Bumping for Pixel Detectors](#)
 - [Website for Single Chip Bumping](#)
- RJR Technologies
 - [Website](#)

5.3 Packaging terms by AMPEON

Packaging is an important element in RF power transistors, influencing both the cost-efficiency and performance of a given device. Since peak powers can vary widely, from as low as 5 W to more than 1 kW, a range of packages is needed to cover every application. The choice of package format (air-cavity or overmolded plastic), often depends on the design requirements, and any **trade-offs to be made between performance and cost**.

[Source for ampleon packaging](#)

Types of packaging:

- Air-Cavity Ceramic (ACC)
- Air-Cavity Plastic (ACP)
- Overmolded Plastic (OMP)

5.4 Definition of terms regarding packaging from RJR technologies

- PRQFN - stands for RJR's thermally enhanced Power aiR-cavity Quad Flat No-leads package
- Substrate - the base material that holds the circuit and components (chips, wires, and caps) of semiconductor devices
- Coupon - a square panel containing a cluster of substrates
- Strip - a rectangular laminate panel containing 4 in-line coupons
- Laminate - a substrate technology composed of several layers that are pressed/laminated together
- Heatslug - a square or rectangular Cu-coin inserted in the middle of the laminate substrate
- Via hole - a hole drilled from top to bottom of the substrate and is used for connecting the terminals on top to the corresponding soldering pads underneath
- ENEPIG - stands for Electroless Nickel Electroless Palladium Immersion Gold; the die bondable and wire bondable plating on top of Cu-traces in a laminate
- Terminal - metal (Cu) traces that serve as connection of the device into the outside world
- Solder resist - a thin layer of polymer that is usually applied on top of Cu-traces of the laminate substrate for protection against oxidation, and around the soldering pads to prevent solder bridges from forming between closely spaced solder pads

5.5 Die layout example

This is an example (estimation) for this PLL project die size and layout:

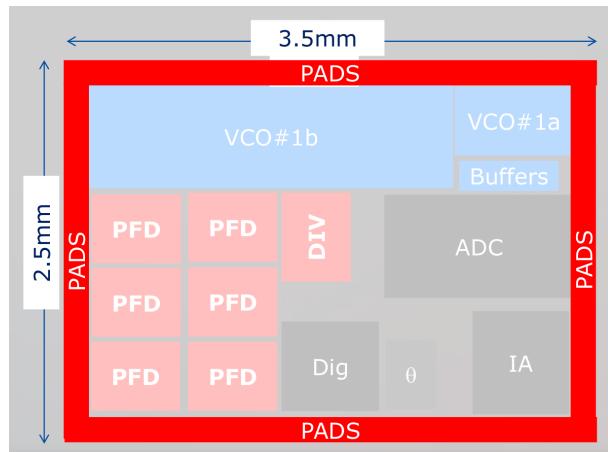


Figure 2: Die layout with pads

Also important is the pin count. Absolute minimum is 8 mm x 8 mm.

Top Level Update

Rough floorplanning will be updated as layout blocks evolve and supply rails are settled (no more 2V5, possible drop of 1V2)
Assuming 6x6mm 0.4mm pitch package, alternatively 7x7 0.5mm

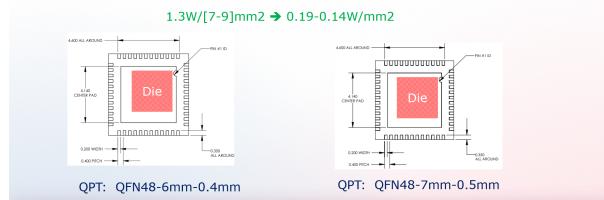


Figure 3: Top layout and packaging choice

6 Test Chip Architecture

Removed CMOS VCO design.

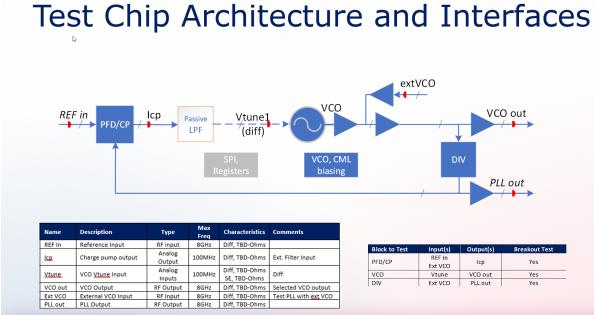


Figure 4: Test Chip Architecture Block Scheme

Identified various risks

- VCO phase noise contributors
- PFD topology and “blind spots”
- Discussed design methodology to be finalized in next couple of days
- Obtained PDK and discussed risk mitigation strategies
- Started authoring chip system specification
- Started project plan with internal and external milestones
- Agenda: project progress towards milestones, technical discussion
- Review & signoff of project milestones and plan
- Review system specification draft
- Packaging option

#	Description	Min	Typ	Max	Units	Conditions
	Input Frequency	1		8	GHz	From Reference generator
	Input Level				mVppd	Accommodating -10..7dBm with external BALUN
	Output Frequency	1		8	GHz	(range)
						(VCO2 range)
	Output Level				mVppd	TBD – prefer differential
	Comparison Frequency	1		8	GHz	
	Loop Bandwidth	1000		3000	kHz	TBD for given configuration
	VCO noise (open loop at 7GHz)		-133		dBc/Hz	At 1MHz
			-153			At 10MHz
						At 100MHz
	REF noise (Test at 7GHz)				dBc/Hz	At 1MHz
						At 10MHz
						At 100MHz
	Frequency Division Ratio		1,2,3,4,6,8		-	
	PLL residual noise (Relative to 1GHz, excluding VCO)				dBc/Hz	At 1kHz
						At 10kHz
						At 100kHz
						At 1MHz
	Settling Time			40	usec	Target
	Spurious Rejection	70			dBc	TBD

6.1 PLL overall performance table

PLL overall performance table:

7 VCO Theory and Design

VCO design methodology and specification is split into theory and design.

7.1 VCO Theory

Phase noise characterization

Phase noise represents the short term stability of the oscillator. VCO phase noise contributors listed:

- Biasing - voltage and current
- Quality factor of tank
 - Quality factor of inductor
 - Quality factor of capacitor bank / capacitor bank unit
 - Quality factor of varactor / varactor bank - Differential Tuning vs Single-Ended Tuning
- Core devices contribution
 - The noise sources in a MOS transistor are: thermal noise in the channel, 1/f noise, Noise in the resistive poly gate, noise due to the distributed substrate resistance, shot noise associated with the leakage current of the drain source reverse.
 - Noise in HBT !?
- Supply Noise - since LDO is external, used a plot from LDO documentation
- Amplitude Regulation circuit connection
- Peak Detector - negligible simulated
- ISF - Impulse Sensitivity Function - introduces proposed solutions of having non sinewave on tank / or parts of tank (noise sensitivity analysis)

Noise in HBTs

Next paragraph(s) are from [Physics and Modeling of Noise in SiGe HBT Devices and Circuits](#)

The ability to simultaneously achieve high cutoff frequency (f_T), low base resistance (r_b), and high current gain (β) using Si processing underlies the low levels of low frequency 1/f noise, RF noise and phase noise of SiGe HBTs. We will show that the phase noise corner frequency in SiGe HBT oscillators is typically much smaller than the 1/f corner frequency measured under dc biasing.

Origin of Shot Noise - The conventional wisdom is that the power spectral density (PSD) of the base and collector current noises are 2qI or “shot” like. The standard derivation of the magic 2qI shot noise assumes a Poisson stream of an elementary charge q. These charges need to overcome a potential barrier, and thus flow in a completely uncorrelated manner.

The primary RF noise sources in a SiGe HBT are the noises associated with the dc base and collector currents and the thermal noise of the base resistance. We first discuss physics and models of these noise sources.

Lmin is used for HBTs in these low noise applications.

Leeson equation

According to Leeson's Formula, the phase noise in the $\frac{1}{f^2}$ region at an offset frequency $\Delta\omega$ from an oscillation frequency of ω_{OSC} , is given in equation:

$$PNw(\Delta\omega) = kTR \frac{F}{V_o^2} \left(\frac{\omega_{OSC}}{Q\Delta\omega} \right)^2 \quad (1)$$

where k, T, R, V_0 , Q and F are the Boltzmann's constant, the absolute temperature, the equivalent tank parallel resistance, the peak oscillation amplitude, the tank quality factor, and the noise factor, respectively.

Phase noise of VCO according to Leeson's formula behaves like:

$$PN = 10 * \log(K * F^2) \quad (2)$$

with change of VCO frequency.

Question 1 How are these two equations the same?

Time Dependent Dielectric Breakdown

Concerns on reliability of design, SOA - safe operating area.

Test bench for Frequency Pushing and Frequency Pulling

Frequency pulling is more straightforward than frequency pushing.



Info: Frequency pushing is caused by the VCO's sensitivity to supply voltages. Pushing is a measure of the sensitivity of the VCO output frequency to supply voltage and is expressed in MHZ/volt. The setup shown in Figure 1 can also be used for this measurement. The supply voltage is set at its nominal setting and the VCO frequency is recorded for different tune voltages. Next, the supply voltage is increased by 1 volt and the VCO frequency is measured for different tune voltages as before. Lastly, the supply voltage is decreased by 1 volt from the nominal, and the frequency is measured for different tune voltages once more. At a given tuning voltage, the frequency change due to 1 volt supply voltage change gives the pushing. It may be different at different tuning voltages. A simple program can also automate these measurements

Frequency scaling and frequency plan

Formula for normalizing (scaling) phase noise to fundamental (output) frequency:

$$PN_{norm} = PN_{meas} - 20 * \log_{10}\left(\frac{freq_{meas}}{freq_{norm}}\right) - 20 * \log_{10}\left(\frac{1}{PN_{offset}} [MHz]\right)$$

Scaling for phase noise in DIV+PFD+CP is different its 10 times log.

Suppressed Up-converted Flicker Noise

From CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise - Aly Ismail, Asad A. Abidi



Info: Flicker noise can upconvert around the carrier frequency in many ways, but in practical oscillators two are most important. We illustrate them at work in the conventional differential LC oscillator.

- 1 In the current-limited regime, the tail current governs the steady-state oscillation amplitude. Therefore, 1/f fluctuations in the tail current source (M3) produce low frequency random AM. The random AM envelope modulates the effective capacitance of the tuning varactor, converting AM into FM. The FM sidebands appear as close-in phase noise.
- 2 Flicker noise in the differential pair (M1, M2), modelled by an equivalent noise voltage associated with one transistor in the pair, is injected into the LC resonator as current noise at baseband and at the 2nd harmonic. This cannot account for close-in phase noise. However, the flicker noise also modulates the 2nd harmonic voltage waveform at the tail every half period, inducing a noisy current in CTAIL. After commutation through M1, M2, this current mixes down to the oscillation frequency and presents a fluctuating capacitance across the LC resonator. The resulting random FM upconverts 1/f noise into close-in phase noise.

OBSOLETE

Explored theoretical solutions that are now abandoned:

Localized Backside Etching

Local backside etching (LBE) is a post operation on chip to improve quality (Q) factor of inductor. Affect around 1 kHz offset is 3-4 dB, and around 0.6 - 1 dB at 1 MHz.

Subharmonic Injection Locking

From what I have seen in papers most promising topology in terms of phase noise is cross-coupled LC VCO class C with potential additional technique of subharmonic injection locking. This is what I plan to try first if no better solutions are provided. Subharmonic injection locking might be too narrowband.

Tunnel Diode



Info: The resonant tunnelling diode (RTD) has been investigated in many high frequency applications, including 712 GHz oscillators [1], voltage controlled oscillators (VCOs) with low power consumption [2], high output power oscillators [3], and also analog-to-digital converters [4].

A tunnel diode is a special type characterized by its ability to exhibit negative resistance. Unlike conventional diodes, which show positive resistance, tunnel diodes can conduct in the reverse bias region under certain conditions. This property makes them invaluable in various electronic applications, especially high-frequency circuits.

- 1 Mats Ärlelid, Mikael Nilsson, Gvidas Astromskas, Erik Lind, and Lars-Erik Wernersson, “[High Tuning-Range VCO Using a Gated Tunnel Diode](#),” Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007,-798-G-5-4pp. 798-799

Emitter and Source Degeneration

Source capacitive degeneration (CTAIL) is used to improve phase noise performance.

[Analysis of Emitter Degenerated LC Oscillators Using Bipolar Technologies](#) - J. H. C. Zhan, K. Maurice, J. S. Duster, K. T. Kornegay

VCO Phase Noise Theoretical Limit

Regarding VCO phase limit tests: Since noise expresses both in amplitude and phase we could use amplitude regulation to generate the tail current (e.g. using a bipolar current mirror). The problem will then be to minimize noise in the current generator. That could be done with the help of a chopper amplifier. Undesired frequency content may be a new issue, but for a differential design I believe it's solvable. For first tests, an ideal amplifier should come close to that. Maybe a bipolar amplifier doesn't even need that.

Trade-off and FoM for VCO Phase Noise and Power Consumption

Power consumption is not a priority for this project.

Substrate integrated waveguide resonators

Substrate integrated waveguide (SIW) resonators are characterized by high quality (Q) factor, easy integration with planer circuits, and lower conductive loss.

Oscillators made in SIW :Samundra K. Thapa, Baichuan Chen, Adel Barakat, Kuniaki Yoshitomi, Ramesh K. Pokharel Miniaturized Slot-Loaded SIW Resonator and Its Application to C-band Low Phase Noise Oscillator

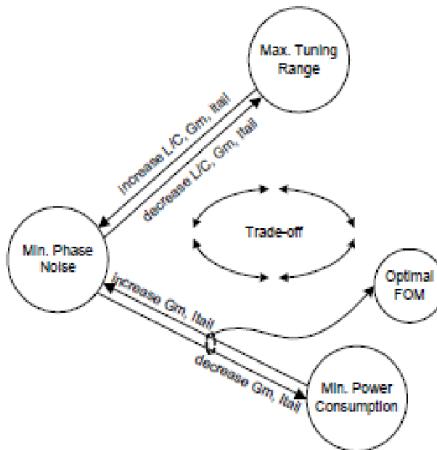


Fig.2. FOM Optimization Guideline

The widely used FOM is calculated by

$$\text{FOM} = L\{\Delta\omega\}(\Delta f/f_0)^2 \text{PVCO}/\text{mW} \quad (1)$$

Figure 5: VCO FoM Optimization and Definition

Z. Chen, W. Hong, J. Chen and J. Zhou, "Design of High-Q Tunable SIW Resonator and Its Application to Low Phase Noise VCO," in IEEE Microwave and Wireless Components Letters, vol. 23, no. 1, pp. 43-45, Jan. 2013.

More papers:

- 6 F. F. He, K. Wu, W. Hong, L. Han and X. Chen, "A Low Phase-Noise VCO Using an Electronically Tunable Substrate Integrated Waveguide Resonator," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 12, pp. 3452-3458, Dec. 2010.
- 7 Z. Yang, B. Luo, J. Dong, T. Yang and H. Jin, "Low phase noise oscillator based on quarter mode substrate integrated technique," IEICE Electronics Express, vol. 12, no. 6, pp. 1-6, 2015.
- 8 C. M. Wu, T. Itoh, A. K. Poddar and U. L. Rohde, "A C-band tunable oscillator based on complementary coupled resonator using substrate integrated waveguide cavity," 2014 44th European Microwave Conference, Rome, 2014, pp. 715-718.

A Noise Circulating Oscillator

Oscillator phase noise is a fundamental metric that governs a wide variety of design aspects in modern communication and sensing systems [1], [2]

1. B. Razavi, RF Microelectronics, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2011.
2. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 2004.

List of SiGe papers

This is a list of papers regarding the CMOS technology similar to 130 nm collected by Anthony.

1. A Stacked-Complementary 5 GHz Oscillator With Even-Only Differential Harmonic Shaping Achieving -150 dBc/Hz Phase Noise at 10-MHz Offset Using Body-Biased Thin-Oxide 22-nm FDSOI
2. A VCO with Implicit Common-Mode Resonance

3. A 2.3 - 5-GHz LC-VCO With Source Damping Resistors to Suppress 1/f Noise Up-Conversion
4. A 6.7-to-9.2GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO
5. A 25% Tuning Range 7.5- 9.4 GHz Oscillator With 194 FoMT and 400 kHz 1/f3 Corner in 40nm CMOS Technology
6. A Filtering Technique to Lower LC Oscillator Phase Noise
7. A Low Phase Noise and High FoM Distributed-Swing-Boosting Multi-Core Oscillator Using Harmonic-Impedance-Expanding Technique
8. A Low Phase Noise, High Phase Accuracy Quadrature LC-VCO With Dual-Tail Current Biasing to Insert Reconfigurable Phase Delay
9. A Low Phase Noise Oscillator Principled on Transformer-Coupled Hard Limiting
10. A Noise Circulating Oscillator
11. Ultra-Low Phase Noise X-Band BiCMOS VCOs Leveraging the Series Resonance
12. An Ultra-Low Phase Noise Class-F2 CMOS Oscillator With 191 dBc/Hz FoM and Long-Term Reliability
13. CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise - Aly Ismail, Asad A. Abidi
14. Design of LC Resonator for Low Phase Noise Oscillators
15. Even-Harmonic Class-E CMOS Oscillator
16. Implicit Common-Mode Resonance in LC Oscillators
17. Third-Harmonic Injection Technique Applied to a 5.87-to-7.56 GHz 65nm CMOS Class-F Oscillator with 192dBc/Hz FOM

List of CMOS papers

Franceschin paper has the best noise performance by far. It's made in SiGe 55 nm and using bipolar transistors in core, consumes 500 mA and the output swing is clipped by diode connected bipolars which enables this much current without affecting bipolars operation.

Babaie papers are made in CMOS and are more similar to current design. It utilises step up transformers with different common and differential k factors to decouple capacitor bank from the core and control its drain currents to make a class F2. But I currently don't know how to implement this because I don't have any ideal transformer models with different k factor for differential and common modes.

Ying paper has a similar idea calls it class F23 and also ok results which makes me think this is the most viable idea from all of these papers to try.

Paper on YIG VCO

A Low-Noise Transmission-Type Yttrium Iron Garnet Tuned Oscillator Based on a SiGe MMIC and Bond-Coupling Operating up to 48 GHz Marcel van Delden , Student Member, IEEE, Nils Pohl , Senior Member, IEEE, Klaus Aufinger , Member, IEEE, Christoph Baer , Member, IEEE, and Thomas Musch, Member, IEEE

i

Info: Second, tuneable opto-electronic oscillators (TOEO) use sophisticated optical resonators to tune the output frequency in the microwave range. They offer a high bandwidth of up to more than one octave and low phase noise at the same time [19], [20]. However, TOEOs require at least a laser, an optical resonator, an electrooptic phase or amplitude modulator, a fast photodiode, a delay line as well as a filter, and an amplifier for microwave frequencies. High-performance TOEOs like [19], [20] require even more and sophisticated components. Thus, TOEOs are expensive and complex.

VCO test methods

Mini Circuits VCO test methods explains how to measure and set up tests for:

- output power and frequency
- tuning sensitivity and linearity
- harmonics and spurious level
- frequency pushing
- frequency pulling
- modulation bandwidth
- modern method using a powerful VCO/PLL test system HP4352S
- phase noise

About modern method: HP has recently introduced a powerful VCO/PLL test system, the HP4352S which is pictured in Figure 4(a). It has built-in low noise power supplies and is available for VCO testing. It measures VCO characteristics such as frequency, tuning linearity, output power, and harmonics as a function of tuning voltage. It can also be used to measure pushing, output power vs. Vcc, phase noise at a given offset vs. VtUne or Vcc, etc. The instrument is user friendly and does not need calibration. A set up using this instrument is illustrated in Figure 4(b). FIGURES NOT SHOWN

7.2 Technical requirements for VCO

#	LO Requirements	Note	Lmin	typ	max	Units
VCO Requirements						
1	Full LO range		7000		12000	MHz
1a	Number of cores			8	16	/
2	Phase Noise at 1 MHz				<-135	dBc/Hz
3	differential Vtune		1.92		3.6	V
4	Tuning Sensitivity K_{VCO}		?<30		?< 50	MHz/V
4a	Type of Tuning			diff		/
5	Pushing	TBD			2	MHz/V
6	Output Voltage p-p	TBD	0.8			V_{p-p}
6	Output CM range	TBD			V_{DD}	
7	Load Impedance				100	fF
VCO and output Buffer						
8	Output Voltage	TBD	?0.8			V_{p-p}
9	Load Impedance	TBD			?1000	fF
10	Harmonic suppression (2_{nd} , typ)		-15			dBc
11	Pulling (14 dB Return Loss, Any Phase)	TBD			2	MHz
General Specifications						
12	Operating Temperature Range		-40		105	°C
13	Supply Voltage VCO ($\pm 5\%$)		4.75	5	5.25	V
	Supply Voltage VCO ($\pm 10\%$)		4.5	5	5.5	V
13a	Supply Voltage ANA ($\pm 5\%$)		3.42	3.6	3.78	V
	Supply Voltage ANA ($\pm 10\%$)		3.24	3.6	3.96	V
13b	Supply Voltage DIG ($\pm 5\%$)		1.14	1.2	1.26	V
	Supply Voltage DIG ($\pm 10\%$)		1.08	1.2	1.32	V
14	Supply Current				?20	mA
15	Shutdown Current				?10	μA
16	Time to Switch Between Cores			?3	?5	ms

Table 1: Specification Requirements

7.3 VCO Design

- What is minimum phase noise that can be obtained with perfect supply, typ process, 25 degC, measured at the VCO output with ideal termination and no buffer
- What is the maximum tuning sensitivity that can be used to obtain the above
- What additional techniques need to be explored to improve the above
- Perform noise sensitivity analysis like ISF
- Discuss CML buffer concept and LDO topologies

Previous open points on VCO:

- the effects of BSE on phase noise (i.e. is it really needed)
- there is no point in using higher resistances than 20 - 30 k Ω in capacitor bank unit
- test voltage and current for HV_MOSFETs, to test breakdown of mosfets, use software called **Real Expert**
- estimate for drop in phase noise with supply noise and layout and its generous is -120 dBc/Hz
- to further help needs to review design

A another question to the customer regarding the overall system. 8 is a great number for a divider, but maybe a bad choice for a multiplier? I don't know how it is currently implemented, but thinking of diodes/BJT with exponential characteristics we get odd harmonics, using MOS we may get even ones, at least a good 2nd. But $8=2^2*2^2$ and 9 is just 3^3 .. one stage less, and in differential design only 9 seems feasible. In that case I tend to say that a non-sinusoidal output would even help to reduce gain in the multipliers (which also adds noise on top of the multiplication itself). Assuming that the mixer needs amplification, each *2 stage should add more than 6dB PN, leading to about 20dB or more degradation. If they want to have options on that multiplication factor, we could more easily do that in the PLL with dividers (which reduce PN). Ideally we reduce the VCO range to just more than an octave in the highest band of interest and divide the rest?

7.4 Using different models for HBT

BSIM4 and psp* (not pss), sometimes psp* gives better performance

BSIM4, as the extension of BSIM3 model, addresses the MOSFET physical effects into sub-100nm regime. The continuous scaling of minimum feature size brought challenges to compact modeling in two ways: One is that to push the barriers in making transistors with shorter gate length, advanced process technologies are used such as non-uniform substrate doping. The second is its opportunities to RF applications.

7.5 Problem with discontinuity of RF model

When simulating design with nmosHVRF models this error appears:

```
WARNING (SPECTRE-16780): LTE tolerance was temporarily relaxed to step over a
discontinuity in the signal: i_VCO.i_VCO_core.N3:int_INT3. Check the design
or use '+diagnose' to get more information.
```

Further occurrences of this warning will be suppressed

I changed the model parameter:

```
+ swnqs      = 0.0 * rfmode * 5.0
In section of sg13g2_moshv_psp_parm.scs/
sg13g2_hv_nmos / model sg13g2_hv_nmos_psp pspnqs103.
```

7.6 30 GHz VCO design

by Stefan Jović

Performance summary:

Parameter	Typical value
Corner	Typical
Temperature	50 °C
Amplitude	550 mVpp
Centre Frequency	30.25 GHz
Tuning Range	0.72 GHz
K_{VCO}	1.45 GHz/V
Tuning range voltage	0.2 V - 0.7 V

Table 2: Specification Requirements

Some key conclusions in terms of phase noise:

Noise at output of VCO is same as at the output of buffer. Main contributors for VCO output noise is output buffer by performing modulation of VCO tank circuit. Second main contributor is noise in references used to generate VCO current bias and noise in power supply.

Note that current tail bias mirror is using PTAT current.

Question 2 Why is PTAT used?

VCO output swing or VCO output freq or sth else?

7.7 VCO sub blocks and relevant blocks

List of sub blocks:

- VCO core (# is 8 for BiCMOS)
- Differential tuning circuit - varactor (bank)
- Capacitor bank
- Current or Voltage Bias
- Bandgap Reference
- Output Buffer

7.8 Design of VCO Tank

7.8.1 Differential Varactor

2 papers

Option 1 is referencing [paper](#) A 44 GHz Differentially Tuned VCO with 4GHz Tuning Range in 0.12 μ m SOI CMOS

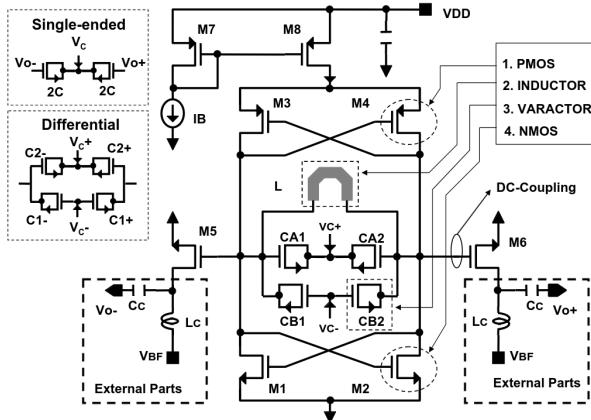


Figure 22.4.1: Differentially tuned 44GHz VCO schematic.

Option 2 is referencing [paper](#) A 23-mW 60-GHz Differential Sub-Sampling PLL with an NMOS-Only Differential-Inductively-Tuned VCO

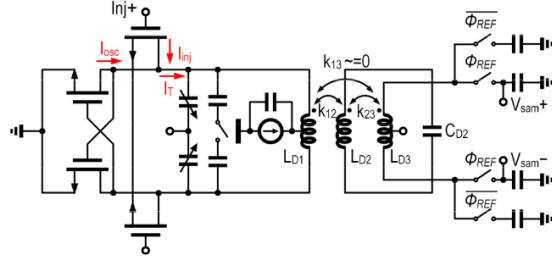
low Q part of Varactor tuning range:

Testbench for comparing differential and single-ended tuning:

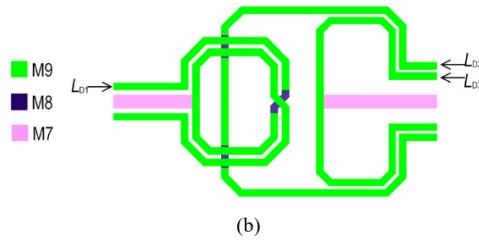
Results of comparative analysis.

Regarding linearity of differential tuning (I assume you are talking about this), I could not figure this out, and opted for single-ended tuning. The problem is that differential tuning has less capacitance change and inherently loads tank with more capacitance, resulting in lower VCO frequency which results in lower phase noise when normalized to 7 GHz, and also lower tuning range.

Red and yellow are differential "varactors" and green C56 is single-ended. On the left is sweep of tuning voltage to see change in capacitance, on the right derivative of this - indicates KVCO and "linearity".



(a)



(b)

Fig. 3. (a) Proposed differential co-design of ILFD and PD and
(b) design of the coupled coils for the co-design.

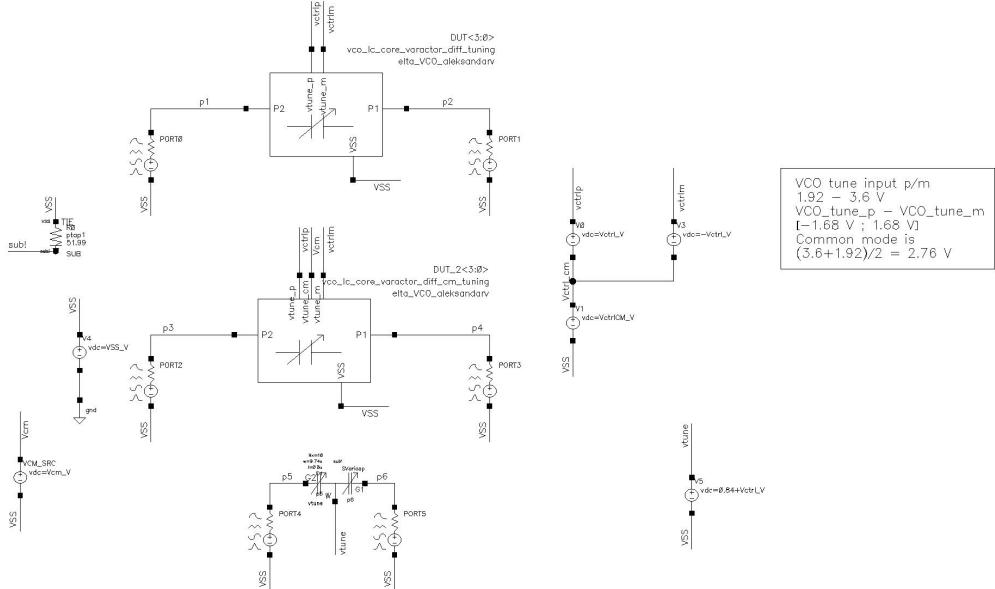


Figure 6: Testbench for capacitive varactors

Yellow is more "linear" than red and it uses "common mode voltage" $V_{tunecm} = VDD$, while red one is the simple one.

This is the schematic for the yellow C_{34} one v_{tunecm} is connected to supply.
Red plot represents this differential "varactor" without cm voltage $C12$.
 Q factor is worse for differential tuning vs single-ended tuning.

7.8.2 Design of Capacitor Bank and CB Unit

2 Single-ended banks vs Differential capacitor banks

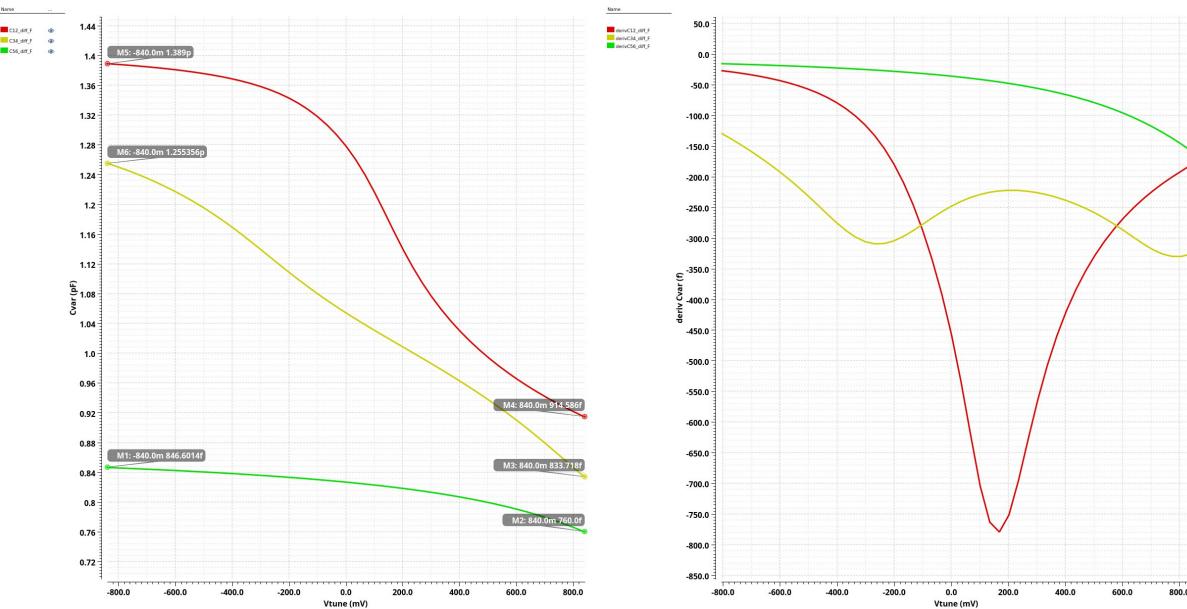


Figure 7: Simulation Results Cvar and deriv(Cvar) over Vtune

7.8.3 Design of Inductor

Electro-magnetic simulator is needed. Technology Parameters if calculations are to be done. Look up the metal stack and info

Parameter	Value	Unit
Substrate resistivity	X	$\Omega\text{-cm}$
Substrate thickness	?	um
Silicon dielectric constant	?	no unit
Oxide thickness (M3-Sub)	?	um
Oxide thickness (M3-M2)	?	um
SiO_2 dielectric constant	?	no unit
Metal resistivity	?	$\Omega\text{-um}$
Top Metal (M?) thickness	?	um
Other metal thickness	?	um

Table 3: Technology Parameters

Inductor can be also switchable, if we need to improve the crude tuning range.

7.8.4 Comments and Problems July Design vco10

I ran simulations on vco10 schematic level and with ideal bias (for base of hbt cascode in vco core)
LSB of fine capacitor bank is 16 fF.

8 Non VCO parts of PLL

- Bandgap PTAT (CTAT?)
- Digital: State Machines, fuses are not available
- Digital: Register Bank for VCO bands, cores
- DAC, not necessary, could use external
- PFD + CP
- Passive Differential Loop Filter
- Balun is off chip. Multiplexer is high frequency up to 80 GHz - differential amplifier structure.
- PLL lock circuit

8.1 Divider

- division ratios needed : 1/2/3/4/12
- using ecl logic same as PFD

8.2 PFD

PFD topology and blind zone

Reset path delay is needed because of dead zone and that is why blind zone was much worse than expected.

8.3 Loop Filter

Two options are:

option 1	option 2
active	passive
External OpAmp	Diff Charge Pump
Single-ended Tuning	Differential Tuning

Passive loop filter is chosen because of better phase noise performance.

Active Loop Filter Operational Amplifier

OA Characteristic	Impact/Considerations
Supply Voltage	The op amp needs to allow the supply range needed for rail-to-rail i/o operation. No obligation to use negative supply rail.
I/O Common mode range	Output common mode range should allow the VCO to cover the entire tuning range and the input also needs to be rail to rail.*
Noise Voltage (nV/\sqrt{Hz})	The voltage noise causes phase noise degradation, especially near the loop bandwidth. Smaller is better.
Minimum Stable Gain	Unity gain stable is preferred.
Input Bias Currents	This parameter will affect phase detector spurs. Smaller is better.
Gain Bandwidth Product	As a rough rule of thumb, one would want the gain bandwidth product to be at least 50 times the loop bandwidth.

* This is important even in fixed bias topologies as the input voltage connected to the PLL charge pump output will start at the lower rail on power-up.

Some commercial part examples to look into:

- OP184
- AD820
- AD8661

8.4 OTA

Example of specification:

Parameter	Value			Unit
	Min	Nom	Max	
Supply Voltage V_{DD}		3.3		V
Supply Ground V_{SS}		0		V
Supply Variation	-5		5	%
Temperature range	-40		+125	°C
Common Mode Input Range	0.1		3.2	V
Common Mode Output Range	1		2.3	V
Gain Bandwidth	30			MHz
Common-mode rejection ratio @BW	40			dB
Power supply rejection ratio @BW	40			dB
Variation of transconductance	-10		+10	%
Slew Rate	20			$V \mu S^{-1}$
Input Voltage Offset	-100		100	μV
Phase Margin	65			dB
DC Gain	50			dB
Current Dissipation			1	mA
Area			0.05	mm
Capacitive load		1		pF

8.5 Level Shifters

Level shifters are digital circuits that change the high level of signal. In this case from 3.3 V to 1.2 V and other way around.

Example paper for level shifters [\[pdf\]](#) [High2low Level Shifter](#)

9 Supply Regulation

Needed to reduce the number of supplies.

9.1 LDO - Low Drop Out Regulators

Is external filter (capacitor) needed?

9.2 Bandgap

Are bandgaps always cvt? PTAT

9.3 Ready Bit

Needs a comparator to check 1.2V supply voltage is higher than some level

		Schematic			Extracted			
Delay times	#	bcs	nom	wcs	bcs	nom	wcs	Unit
lvlsh 3p3V to 1p2V	tq_1p2_fall_s	144.5p	211p	301.8p	147.1p	214.7p	307p	s
	tq_1p2_rise_s	322.8p	504.4p	815.2p	328.3p	512.8p	828p	s
	tqc_1p2_fall_s	285.2p	432.6p	672.9p	290.2p	439.9p	683p	s
	tqc_1p2_rise_s	94.38p	140.7p	201.6p	96.26p	143.5p	205.5p	s
lvlsh 1p2V to 3p3V	tq_3p3_fall_s	298.3p	530.2p	1.544n	355.1p	642.2p	1.867n	s
	tq_3p3_rise_s	176.9p	357.1p	1.382n	196.9p	413.8p	1.688n	s
	tqc_3p3_fall_s	272.7p	472.4p	1.455n	315.7p	563.3p	1.786n	s
	tqc_3p3_rise_s	202p	417.1p	1.476n	238.8p	501.6p	1.781n	s
Current consumption for 100 MHz clock	I_lsh12_33_rms_A	69.55u	89.78u	121.7u	75.13u	96.94u	130.7u	A
	I_lsh33_12_rms_A	22.01u	27.65u	36.54u	22.35u	28.09u	37.12u	A
80 ps 90%-10% input								

9.4 Serial Peripheral Interface

by Rustam and Nikola

Looking at SPI slave digital core I see that it will be impossible to redesign it manually to 3.3V. First of all, it will be mess for our layout engineers, because there are too many unstructured cells in this design. PnR is going to be a very exhausting job.

As for the register bank, I suppose that we can do it manually due to repetitive structure it will be copy/paste as Guenter mentioned before. I prepared a block diagram with my design suggestions. In this example I'm using byte addressing according to existing memory allocation.

Here I'm assuming IO cells with 3.3V coreside. So, we should put level shifters from 3.3V to 1.2V on SPI ports. If we will have IO cells with 1.2V coreside we could drop out this level shifters group.

Then we have digital core SPI slave on core logic 1.2V that we will design using standard digital flow using genus/innovus and so on. Then we should put other level shifters from 1.2V to 3.3V on register bank control signals. There won't be many of them, only 21 units. Then we have 3.3V supplied register bank.

For register bank we must get some clock to store data. I see 3 options where we can get clock:

1. we can use existing clock SCLK from SPI port, this way is not ideal, but if we have few free pads, we can go this way.
2. we can use external clock from pad, it is preferable option.
3. we can use internal generated clock from RC generator, but we should design it at first

Talking about core supply rails I see two options: external Vdd pad or internal regulator which, as I understand it, we don't have now either. First option with external pad is preferable, but again we will need one more pad.

We should decide which way we choose depending on our possibilities and go on.

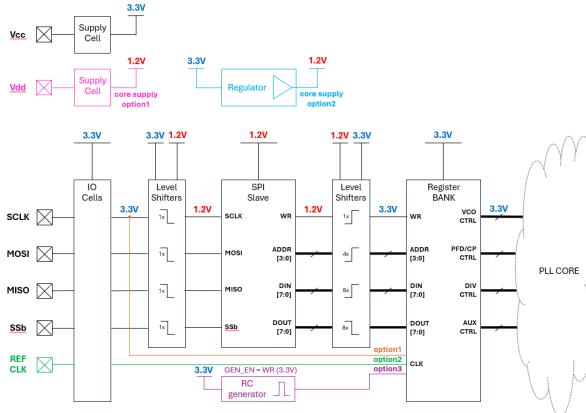


Figure 8: SPI block scheme suggestion

There may be some inconsistency in your proposed requirements. I would like to investigate this to make things clearer. Your memory allocation assumes byte addressing and has 13 bytes of data. If we are talking about byte addressing, then we need 4 address bits. But your SPI format proposes 12-bit word addressing and only 3 address bits, plus 1-bit used for R/W annotation.

Test Chip Draft Memory Allocation

Basic Format: Total wordlength: 16bit, ADDR, R/W: upper 4bits, Data: lower 12b for data Options: Adding a test loop for the SPI to verify writes by reading register content back 8 or 12b readback

Then I see two options for resolving the issue:

Option 1: We can use byte addressing according to existing memory allocation. So, we will use 4 address bits to allocate up to 16 bytes. In this case we should change the command format to: 3 MSB bits - don't care; ADDR - 4 bits; R/W - LSB bit of first byte; DATA - second byte

Option 2: We can use addressing according to your proposed command format. So, we will use 3 address bits to allocate up to 8 words with 12-bit word length. In this case we should change existing memory allocation table. This is the example:

Block	Function	R/W	Type	Bits	Memory Bytes
VCO	VCO Enable	W	EN	1	1
VCO	Test Input (Bypass)	W	EN	1	1
VCO	Test Output	W	EN	1	1
VCO	Band Select	W	sel	8	1
VCO	Varactor Select	W	sel	16	2
VCO	Bias Select	W	sel	8	1
PFD/CP	PFD/CP Enable	W	EN	4	1
PFD/CP	CP Bank Select	W	sel	4	1
PFD/CP	Icp Select	W	sel	8	1
DIV	DIV Enable	W	EN	1	1
DIV	Output Select	W	EN	4	1
DIV	Modulus Control	W	sel	8	1
AUX	Test Data (various)	R	?	12	2
AUX	Test MUX Select	W	sel	4	1
AUX	Test MUX Read	R	sel	2	
				Total Bytes=>	13
				Total Bits=>	104

Figure 9: Test Chip SPI Draft Memory Allocation

CMD format	CMD Byte 1								CMD Byte 2
	7	6	5	4	3	2	1	0	7
option 1	x	x	x	A3	A2	A1	A0	RW	D7
option 2	A2	A1	A0	RW	D11	D10	D9	D8	D7

Block	Function	R/W	Type	Bits	#Bit	#Word			CMD Byte 2
VCO	VCO Enable	W	EN	1	0	0	1	0	7
VCO	Test Input (Bypass)	W	EN	1	1		A0	RW	D7
VCO	Test Output	W	EN	1	2		D9	D8	D7
VCO	Band Select	W	sel	8	3:10				
	Dummy			11					
VCO	Varactor Select part 1	W	sel	12	0:11	1			
VCO	Varactor Select part 2	W	sel	4	0:3	2			
VCO	Bias Select	W	sel	8	4:11				
PFD/CP	PFD/CP Enable	W	EN	4	0:3	3			
PFD/CP	CP Bank Select	W	sel	4	4:7				
PFD/CP	Icp Select part 1	W	sel	4	8:11				
PFD/CP	Icp Select part 2	W	sel	4	0:3	4			
DIV	DIV Enable	W	EN	1	4				
DIV	CP Bank Select	W	EN	4	5:8				
DIV	Modulus Control	W	sel	3	9:11				
DIV	Modulus Control	W	sel	5	0:4	5			
AUX	Test MUX Select	W	sel	4	5:8				
AUX	Test MUX Read	R	sel	2	9:10				
	Dummy	R	-	1	11				

Regarding the clock: I would prefer not to have an external dedicated clock and also I am a bit worried about an internal clock that may not be fully synchronous to the SPI clock. This leaves the option of using the SPI clock as my preferred solution.

Regarding the register bank: I do like your option 1, i.e. using 4 addressing bits.

Regarding the 1.2 V supply, yes we do not have an internal LDO so we have to rely only to external

supplies. Given the very low power consumption at 1.2V I am wondering if we can try any low effort/low cost regulation techniques

9.4.1 Synchronizer Design

Synchronization Hierarchy: [source](#)

- Mesochronous Synchronizers
 - delay-line synchronizer
 - two-register synchronizer
 - FIFO synchronizer
- Plesiochronous Synchronizers
 - phase slip and flow control
- Periodic Synchronizers
 - clock prediction - looking
- into the future

10 Commercial Parts

Commercial parts used as alternative or to augment the design.

LMX2592

LMX2592 High Performance, Wideband PLLatinuTM RF Synthesizer With Integrated VCO

- VCO Phase Noise: -134.5 dBc/Hz at 1-MHz
- Offset for 6-GHz Output
- Industry Leading Phase Noise Performance
- VCO Phase Noise: -134.5 dBc/Hz at 1-MHz Offset for 6-GHz Output
- Normalized PLL Noise Floor: -231 dBc/Hz
- Normalized PLL Flicker Noise: -126 dBc/Hz - 49-fs RMS Jitter (12 kHz to 20 MHz) for 6 GHz Output

Applications:

- Test and Measurement Equipment
- Defence and RADAR
- Microwave Backhaul
- High-Performance Clock Source for High-Speed
- Data Converters
- Satellite Communications

TPS7A8300

Texas Instruments: TPS7A8300 2-A,6- μ V RMS,RF,LDOVoltage Regulator

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $(1.1 \text{ V} \leq V_{IN} < 1.4 \text{ V}$ and $3.0 \text{ V} \leq V_{IN} \leq 6.5 \text{ V}$) or $(V_{IN} \geq 1.4 \text{ V}$ and V_{BIAS} open) ⁽¹⁾), $V_{IN} \geq V_{OUT(TARGET)} + 0.3 \text{ V}$, $V_{OUT(TARGET)} = 0.8 \text{ V}$, OUT connected to 50 Ω to GND, $V_{EN} = 1.1 \text{ V}$, $C_{OUT} = 22 \mu\text{F}$, $C_{NRSS} = 0 \text{ nF}$, $C_{PF} = 10 \text{ nF}$, and PG pin pulled up to V_{IN} with 100 k Ω , unless otherwise noted.

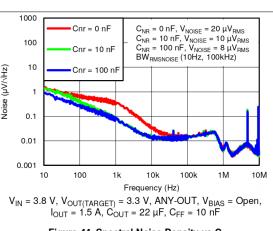
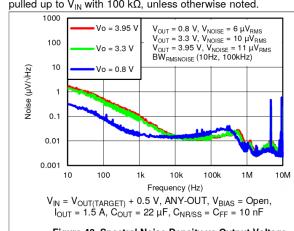


Figure 43. Spectral Noise Density vs Output Voltage

HP4352S

powerful VCO/PLL test system, the HP4352S

10.1 I/O Baluns

Presented commercial parts that could be used:

- Minicircuits TCM1-83X
- Marki Microwave BALH-0012SSG

11 Old Project

Old project LO block VCO and VCO Buffer for topcon late 2022.

11.1 Introduction

LO block is LC VCO with internal inductor and fully differential output buffer. Its schematic shall ensure differential connection to the mixer LO input and PLL RF input.

11.2 Technical Requirements

#	LO Requirements	Note	min	typ	max	Units
VCO Requirements						
1	Full LO range		6300		13700	MHz
2	Phase Noise at 300 kHz				<-101	dBc/Hz
3	Vtune		0.1		1	V
4	Tuning Sensitivity K_{VCO}				100	MHz/V
5	Pushing	TBD			2	MHz/V
6	Output Voltage	TBD	0.8			V_{p-p}
7	Load Impedance				100	fF
VCO and output Buffer						
8	Output Voltage	TBD	0.8			V
9	Load Impedance	TBD			1000	fF
10	Harmonic suppression (2_{nd} , typ)		-15			dBc
11	Pulling (14 dB Return Loss, Any Phase)	TBD			2	MHz
General Specifications						
12	Operating Temperature Range		-40		125	°C
13	Supply Voltage		1	1.1	1.2	V
14	Supply Current				20	mA
15	Shutdown Current				10	μA
16	Time to Switch Between Cores			3	5	ms

Table 4: Specification Requirements

LO block should have the characteristics given in Table ???. Due to wide frequency range it is necessary to use switchable capacitor banks. Min and max for supply voltage are not defined in the original document, and time for switching between two cores was defined during the meeting. Currently Full LO range is split between two cores so the requirement should look like this:

	LO range requirements	Note	min	typ	max	Units
1	High Band core LO range		10000		13700	MHz
2	Low Band core LO range		6300		10000	MHz

Table 5: LO Range Two Core Specification Requirements

Question 3 What's the variation for supply voltage?

Not defined probably will be the same as the rest of the

Question 4 K_{VCO} Why is it in the max column?

Didn't get answer for this. It's probably also typical and a value that is expected by the PLL design.

Process corners can be found at:

```
/tech/tsmc/tsmc40/models/spectre/crn40lp_2d5_v2d0_2_shrink0d9_embedded_usage.scs
```

11.3 Scaldio Design Review

Question 5 How should calibration be implemented to achieve output voltage peak to peak and minimize noise?

Is it done for whole PLL?

Question 6 Difference between class-B and class-C vco?

Scaldio uses class-C, so all parasitic capacitances connected to the tail don't matter. Having trouble with observing the currents of drain so cannot check this and compare them. Scaldio looks something between class C and class B because of V_{gbias} voltage and because adding inductor between tail NMOS and switching pair improves phase noise. This is attributed to class B, while class C only needs tail capacitance.

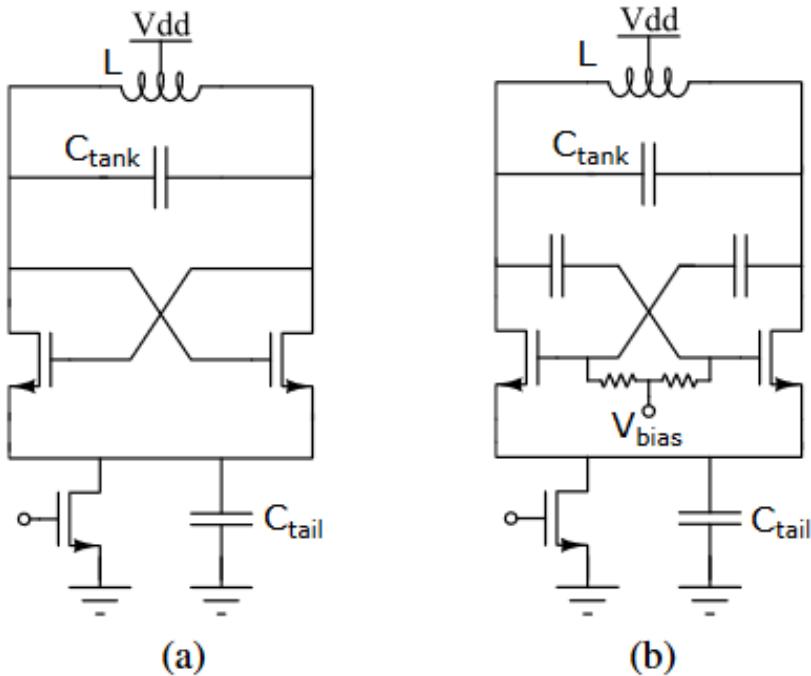


Fig. 1: Oscillator topologies: (a) class-B; (b) class-C.

Lowest bit of digital varactor (L0_PLL_hbVCO_Cdig_SC2B_VCOS_SC2C_PLL) doesn't do anything, isn't even monotonous. Maybe makes more sense when simulating extracted cells. Digital varactor needs to be redesigned, it could lower the Q factor. Main difference between class B and class C can be observed by investigating their drain currents.

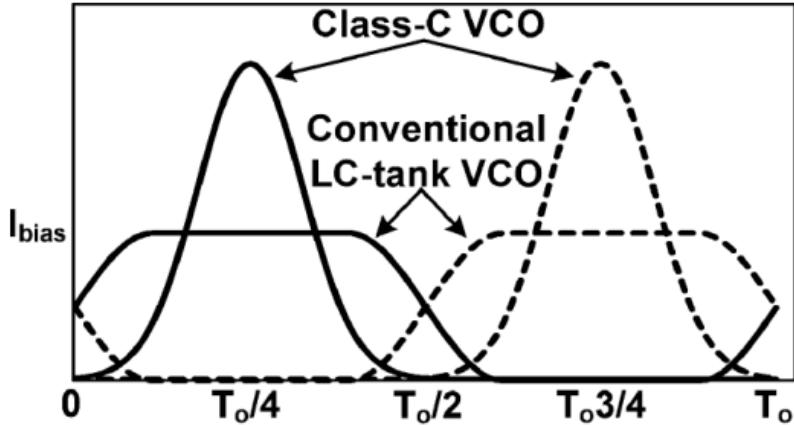


Fig. 2. Drain current of the switch pair FETs for conventional LC-tank VCOs and class-C VCOs.

11.4 Main testbench

Main testbench covers everything except for frequency pulling and full LO range. The simulation results are obtained at the higher end of the LO range. Phase noise is simulated by pss+pnoise.



Info: With Noise Type=timeaverage and ALL(AM,PM,USB,LSB), you can plot the AM and PM components as well as the total noise. In addition, you can plot phase noise and FM jitter results for oscillators. Plotting is done using the Direct Plot Form. [External link](#)

Function of phase noise is simulated for PM noise type.

How to choose beat frequency for autonomous system from forum [thread](#).



Info: In an autonomous system (e.g. an oscillator), you turn on the "oscillator" checkbox, and the beat frequency is then the estimated frequency, which gives PSS a starting point to solve for the oscillator frequency. It's important when in oscillator mode to select the outputs of the circuit, which include any subharmonics. In other words, if you have an oscillator followed by a divider, point at the divider output, and give the estimated divided frequency as the beat frequency. Again, this is because you need to solve an integer number of cycles of all the frequencies in the circuit. Note, don't use oscillator mode for circuits which aren't oscillators, since you're then trying to get the simulator to solve for an unknown which is not unknown, which may lead to convergence problems.

Most of the I_{bias} tune digital control is not used for the higher band, so by increasing the number of steps to cover even higher frequencies than the original design finer bias control is needed.

11.5 Simulation Results for Scaldio design

Simulated only nominal corner with change for V_{DD} only for frequency pushing simulation.

Phase noise changes a lot for different tuning voltages between -90 and -100 dBc/Hz. Phase noise is probably not modeled ok because the VCO doesn't have the connection between current bias tail and the switching pair of VCO as transmission line. That inductance and C_{tail} should resonate at $2\omega_O$ (tank oscillating frequency), but only in the case of class B oscillator. Check what type is vco oscillator.

	LO Requirements	Note	min	typ	max	Sim(Typ)	Units
1	Phase Noise at 300 kHz				<-101	-98	dBc/Hz
2	Tuning Sensitivity K_{VCO}				100	over	MHz/V
3	Pushing	TBD			2	279.7	MHz/V
4	Output Voltage	TBD	800			809.3	mV_{p-p}
5	Harmonic suppression (2_{nd} , typ)		-15			-26.78	dBc
6	Pulling (14 dB Return Loss, Any Phase)	TBD			2	19.51	MHz

Table 6: Scaldio IMEC design Results

11.6 Q factor of LC tank

Need testbenches capacitance of tank, varactors and inductor, and for different controls and also corners. Process corners for varactors are the same as MOSFET.

Question 7 *What kind of chip is it?*

What kind of inductance is expected to be connected on V_{DD} and V_{SS} pins. This may or may not change the results. Removed all together right now.

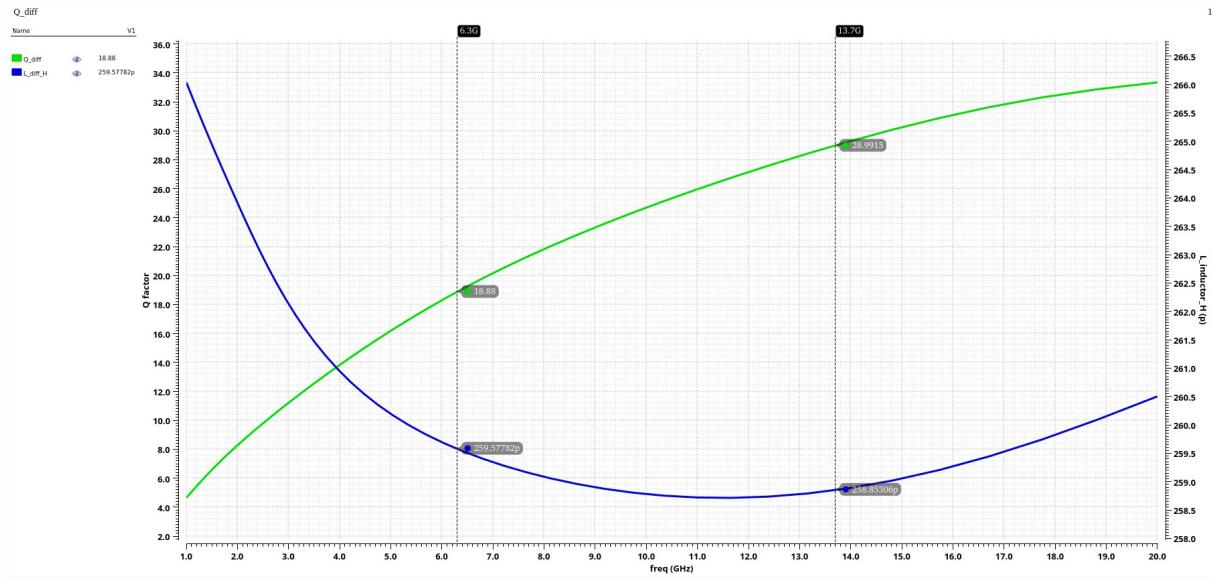


Figure 10: Q factor and inductance of L

Testbench for differential Q and L of the inductor that is EMX simulated is shown in Figure 10. Q factor is better at the higher frequency.

Simulated Q factor of both varactors and inductor. Q factor of digital varactor for lower bit controls is not much better than Q of inductor.

Capacitor calculating capacitance and Q factor:

$$Y_{diff}(im) = \text{imag}(ypm('sp11)) + \text{imag}(ypm('sp22)) - \text{imag}(ypm('sp21)) - \text{imag}(ypm('sp12)) \quad (3)$$

$$Y_{diff}(re) = \text{real}(ypm('sp11)) + \text{real}(ypm('sp22)) - \text{real}(ypm('sp21)) - \text{real}(ypm('sp12)) \quad (4)$$

Capacitance:

$$C_{diff} = \frac{Y_{diff}(im)}{2\pi f} \quad (5)$$

Q factor of capacitor:

$$Q_C = \frac{Y_{diff}(im)}{Y_{diff}(re)} \quad (6)$$

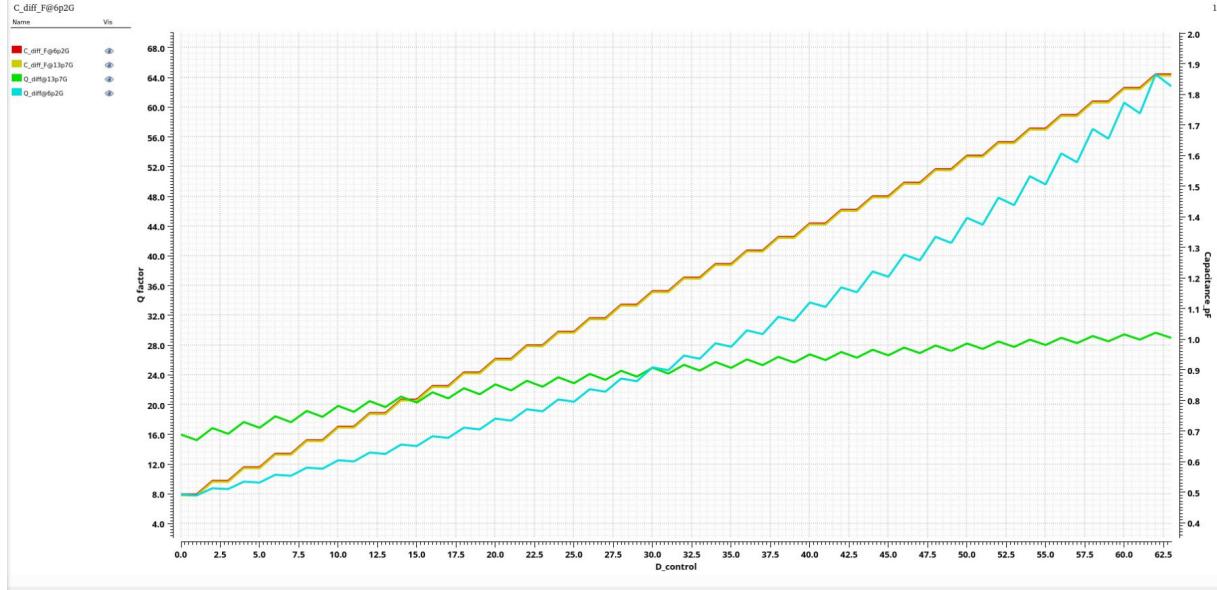


Figure 11: C and Q of digital varactor through controls

More info can be found in [paper](#) A Thorough Analysis of the Tank Quality Factor in LC Oscillators with Switched Capacitor Banks.

Found definitions:

$$Q_{LC} = \frac{1}{R} \sqrt{\frac{L}{C}} = \frac{f_r}{\Delta f} = \frac{\omega_r}{\Delta\omega} = \frac{\tau_d \omega}{2} \quad (7)$$

where τ_d is group delay.

Question 8 How to calculate group delay using sparam analysis?

?

11.7 Calculating Q factor, LC tank by ringing method

Link to [website](#) that shows ring down method of calculating Q factor. Not implemented in virtuoso TODO.

11.7.1 Figure of Merit different definitions



Info: The theoretical maxima for the FoM of an oscillator is given by $FoM = 174 + 20 \log_{10}(Q) \text{ dBc/Hz}$

How to calculate oscillator FoM? Is Q_L factor dominant enough to just equate it with LC tank Q factor. The widely used FOM is calculated by:

$$FoM = L\{\Delta\omega\}(\Delta f/f_0)^2 P_{VCO}[mW] \quad (8)$$

Where $L\{\Delta\omega\}$ is the phase noise, $\Delta f/f_0$ is the ratio between the offset frequency and the carrier, and P_{VCO} is the power consumption of the VCO-core. There is also FoM^T and FoM_A

$$FoM^T = FoM - 20 \log\left(\frac{FTR}{10}\right) \quad (9)$$

and

$$FoMA = FoM + 10 \log(A) \quad (10)$$

where A is area [mm^2], and FTR frequency tuning range [%]

Information about digital varactor copied from [External link](#)



Info: Each bit of MIM varactor contains two MIM capacitors connected differentially with a series switch, two pull-up and two pull-down transistors to effectively turn the varactor between its high and low-capacitance states. Measured intrinsic Q of the MIM capacitor is 80 at 3.6 GHz. When is turned on, i.e., high-capacitance state, the varactor Q drops to 30. When is turned off to be in low-capacitance state, the parasitic capacitance of the MIM capacitor and transistors has an effective of 50. The pull-down transistors set the DC levels for drain and source of at 0 V so that can be efficiently turned into triode region while the weak pull-up transistors set the DC level to VDDOSC to reduce the parasitic capacitance of thus increasing of the parasitic capacitance. The pull-up pMOS can be implemented by either resistors or transistors. The latter was chosen for silicon area efficiency. Compared to MOS varactors, MIM varactors have a much lower . However, since the differential phase-stability inductor is only 10, the impact of lower varactor is tolerable. When the MIM varactor is at its low-capacitance state, the large DCO internal signal swing and the DC level of 1.4-V supply voltage at source/drain of the pull-up transistors force the drain -nwell junction diodes of the pull-up pMOS to momentarily go into forward-bias condition resulting in a latch-up concern. However, since the forward-bias condition occurs only in 50% of a 3–4 GHz period, the latch-up phenomenon with the parasitic BJTs can not be triggered.

11.8 Lowering frequency pushing and LDO

About Frequency pushing from [this paper](#)



Info: An LC-tank VCO circuit has been implemented in a standard $0.35 \mu m$ CMOS technology. It is based on a two-transistor biasing structure that improves the performance of frequency pushing and frequency tuning range. Final measurement of proposed structure gives 516 MHz tuning range with 2.278 GHz center frequency and about 0.55%/V frequency pushing in the worst case. The achieved FOM is about -180dBc/Hz, which is very close to the simulated value. This structure is proven to be particularly suitable for achieving low FOM in the VCO circuits having low Q factor LC-tank. Both, the proposed structure and the FOM optimization method, can also be applied to the VCO designs for the applications at higher frequencies, such as 5GHz VCOs for Wireless LAN applications.

Question 9 Can VCO work for lower voltage of 0.9 V?

This may be needed if LDO is required because of frequency pushing?

Question 10 Does frequency only happen because of the ripple directly induced by buffers e.g.?

Or could it happen because of EM crosstalk?

Is frequency pushing testbench good? Look into this paper. Different testbench would be to make a transient change in Vdd and check how much frequency changes.

Results for class C with pmos bias, only dc change of V_{DD} :

Parameter	typical	spec	min	max	ss -40	ss 125	ff -40	ff 125	Units
Frequency Pushing	43.93	< 2	43.93	100.1	100.1	64.36	75.48	64.09	MHz
Frequency	14.6	> 14.2	14.6	15.83	15.54	15.48	15.83	15.59	GHz

This shows some improvement from frequency pushing of 250 - 300 MHz that was observed for the nmos bias of IMEC Scaldio design.

11.9 Changing topology and lowering phase noise

Decision on why is single sided oscillator chosen instead of double sided oscillator.



Info: However, if non-negligible parasitic capacitances are found at the tank outputs, the phase-noise performance of the DS-VCO may be seriously degraded, while that of the SS-VCO remains unaffected.

More on the $\frac{1}{f^2}$ Phase Noise Performance of CMOS Differential-Pair LC-Tank Oscillators in [paper](#) by Pietro Andreani.

11.10 Hybrid class C and class B



Info: Further, the proposed VCO solves the issue of the hybrid mixed-signal start-up procedure exposed in [8]. The main drawback of this approach is that, if oscillation stops for some unaccountable reason, the VCO can only be restarted actuating again the whole start-up procedure.

Referenced paper is:

- 8 J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L.-R. Zheng, “A low power, startup ensured and constant amplitude class-C VCO in 0.18 μm CMOS,” IEEE Microw. Wireless Compon. Lett., vol. 21, no. 8, pp. 427–429, 2011. Dec. 2008.

11.11 Enhanced Oscillation Swing

Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing in [this paper](#). Phase noise is lowered by lowering V_{gbias} , but it makes oscillations start up harder.



Info: As noted above, the phase noise improves with increasing the oscillation amplitude, which here would mean lowering the gate bias voltage, V_{bias} . Unfortunately, the original class-C oscillator limits the fixed V_{bias} from being set low enough, otherwise the oscillation may not start up. In [11], a high-swing class-C (HSCC) oscillator was introduced, which removed the tail current transistor of the original class-C oscillator [6]. Instead, an automatic amplitude control was introduced to stabilize the oscillation amplitude. In this work, instead of the transformer used in [11], we choose a simple RC bias circuit.

This is from [paper](#) Dual-Core High-Swing Class-C VCO design, and references

- 6 A. Mazzanti and P. Andreani, “Class-C harmonic CMOS VCOs, with a general result on phase noise,” IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
- 11 M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, “High-swing class-C VCO,” in Proc. ESSCIRC, Sep. 2011, pp. 495–498

11.12 Questions about new double feedback

Amplitude Feedback for Robust start up

11.13 OTA1 - Start up and gate voltage bias control

Referent voltage should be set and controlled around 800 mV. Need tests for OTAs inside for VCO, currently simulated only PM and DC gain, should test different V_{ref} levels.

11.14 OTA2 - Start up and bias control

Referent voltage should be set and controlled around 400 mV. Problem with OTA2 loop is amplifying noise into the tail bias current. So the new problem arises as noise shaping in LOOP2 is needed. If a OTA of low uGBW is used than start up is too slow.

11.15 Full LO Range and Frequency Recentering

TODO Add corners for fs sf and similar. Because the LO range is split on two cores, ideally halved. Results are simulated for process and temperature corners:

Core and Specifictaion	min	max	sim(min)	sim(max)	Units
VCO core split					
High Band Higher limit	13700		15580	16190	MHz
High Band Lower limit		10000	10870	12460	MHz
High Band range	3700		4710	3730	MHz
Low Band Higher limit	10000		13230	14120	MHz
Low Band Lower limit		6300	6724	8028	MHz
Low Band range	3700		6506	6092	MHz

Table 7: LO range specification and simulation for Scaldio LC tank

Expecting the drop for schematic simulated frequency range, covered range should at least be larger than needed when recentered:

$$HBFR = 13700 - 10000 = 3700 < 3730 = 16190 - 12460 \quad (11)$$

For lower band it's similarly calculated

$$HBFR = 10000 - 6300 = 3700 < 6092 = 14120 - 8028 \quad (12)$$

Lower and higher band are assymetrical and they overlap for at least:

$$HBLBoverlap_{high} = 13230 - 10870 = 2360 \quad (13)$$

$$HBLBoverlap_{low} = 14120 - 12460 = 1660 \quad (14)$$

The worst available frequency digital controlled range is $6092 + 3730 - 1660 = 8162$ MHz which is higher than 7400 MHz.

Question 11 Are the two VCO-s in the same process corner at the same time?

Yes. If not than the calculations are wrong.

NOTE: Analog varactor 0-Vt-1 change does not work so it wasn't included. Further frequency recentering after extraction will be needed.

11.16 Pulling testbench and design of VCO buffer

Needs port at and tuning circuit to keep the reflection at -14 dB. Port of reference impedance 10 kΩ and portAdapter from rfExamples. S parameter analysis to show if the reflection really is -14 dB? Load impedance increased from 100 fF to 1000 fF. VCO buffer is also needed because of the frequency pulling. Does each core have a buffer or do they share it? first make a buffer than maybe a question.

By adding two buffers from LO_FDDQ_v6, LO_FDDQ_INHB_v5_JCx_saldo2b and LO_FDDQ_Buf_X24 , frequency pulling drops below 1 MHz.

So this specification looks fine, testbench shown:

How does portAdapter work?

Frequency pulling mentions coupling (crosstalk) between different blocks on chip and the VCO.

11.17 PTAT and CTAT, the temperature independant Vbias for cascode

TODO Simulate and show results of temperature sweep.

11.18 Effect of too high tail capacitance

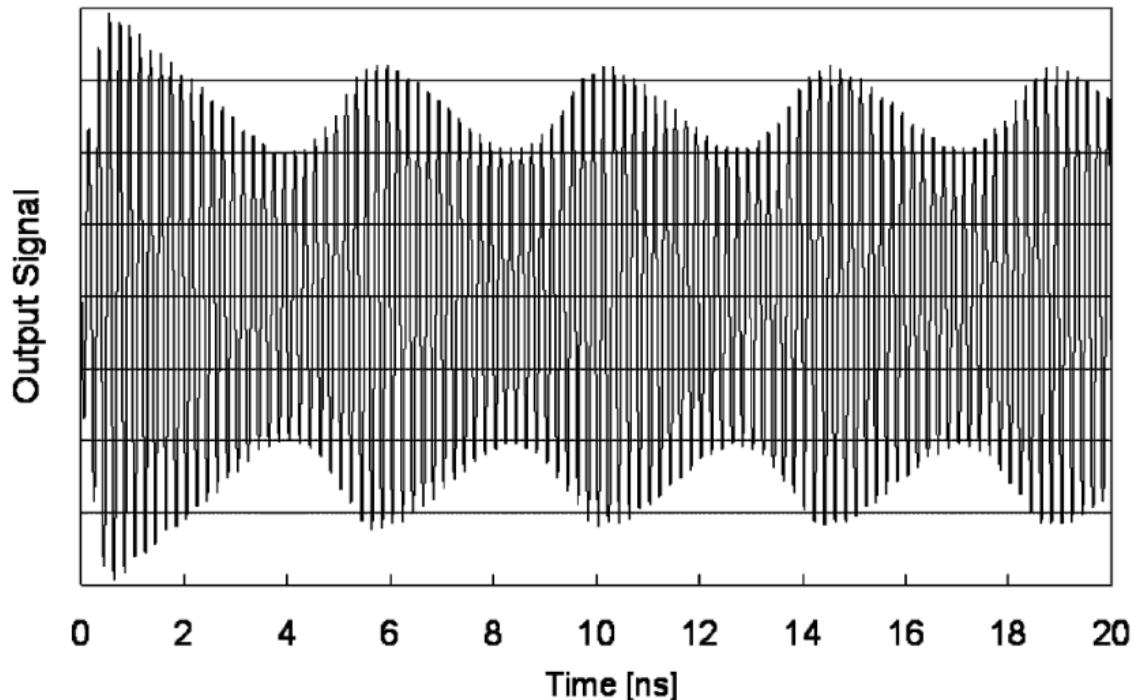


Fig. 10. Effect of too large a tail capacitance: the oscillation suffers from instability, which takes the form of a low-frequency amplitude modulation (squeegging).

Figure 12: Squeegging

Instability Low frequency amplitude modulation squeegging. This was the issue with the original class C with tail current. Is it important for new topology where current bias is PMOS.

11.19 PLL theory - PLL Lock Detect and calibration

About PLL Lock Detect:

i

Info: The ability for a PLL to reliably indicate when it is in lock is critical for many applications. An ideal lock detect circuit gives a high indication when the PLL is locked and a low indication when the PLL is unlocked. When VCO calibration finishes it can be indicative if the lock is detected.

PLL VCO calibration usually goes as amplitude frequency and then amplitude calibration, or the other way?

Divide and Conquer algorithm

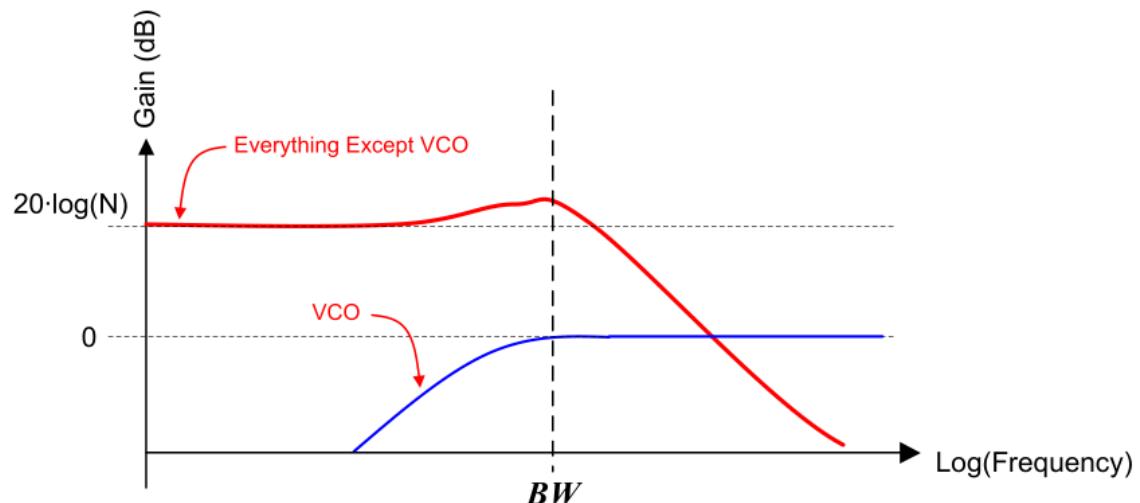
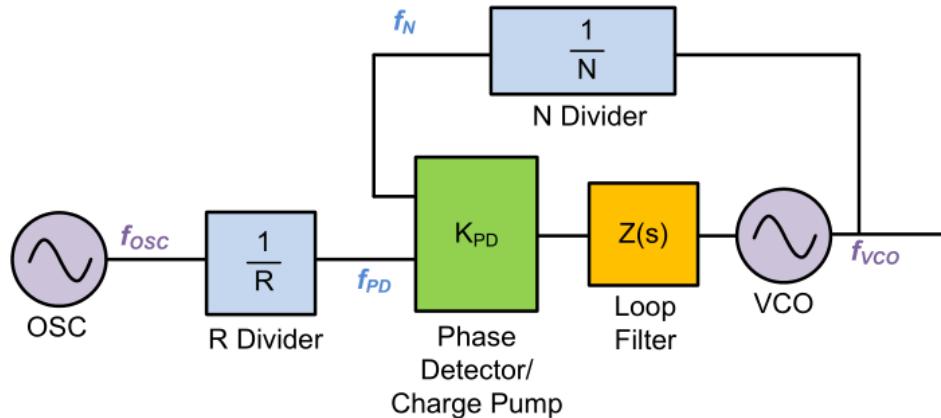


Figure 13: Gain for VCO and other blocks inside of PLL

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Info: For the VCO, the noise is suppressed below the loop bandwidth frequency and unshaped above the loop bandwidth.