Low Noise 6-8 GHz VCO with Differential Tuning as part of PLL

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Introduction

working title
This needs to be added to body of document
The open items I recorded are:

- the effects of BSE on phase noise (i.e. is it really needed)
- Packaging concerns, risks and schedule
- Die quantity and meaningful sample volume
- test chip content and expectations
- overall schedule for the follow-on tapeout in 2025

Complaints and suggestions regarding VCO

- there is no point in using higher resistances than 20 - 30 kΩ in capacitor bank unit
- test voltage and current for HV_MOSFETs, to test breakdown of mosfets, use software called **Real Expert**
- estimate for drop in phase noise with supply noise and layout and its generous is -120 dBc/Hz
- to further help needs to review design

My current problems and work in progress

- (OBSOLETE) hard-clipped VCO not oscillating at the frequency that is supposed to, drops down to around 1 GHz (example)
- (OBSOLETE) soft-clipped VCO has more frequency modes - CM and DM resonance
- Reliablity of design, breakdown voltages. TDDB is Time Dependent Dielectric Breakdown.
- making a differential varactor instead of the single-ended one
- What is the name of metal stack process to be used in EM simulations?

Planning to do at some point

- design a 400 to 500 pH inductor (search for a paper that has decent Q factor around 4-8 GHz range)
- design a PTAT bandgap voltage reference to swich the gate from cascaded NMOS to reference
- make a testbench for frequency pushing and frequency pulling (look at the old VCO project)
- (DOWNTHELINE) Peak Detector

1 NGSPICE

Regarding open-source PDK for SG13G2, it's work in progress, but I think worth to consider. Even if just the simulator can be replaced with ngspice or xyce, it could boost productivity from not being license-bound. Please check this out: **ihp sg13g2**

Documentation on github is sparse, some more info is here: **openPDK opeentooling and open source design**

open source PDK, research and prototyping

1.1 Required libraries - Linux Installation

libxaw7-dev and libreadline6-dev
KiCad plus ngspice

1.2 openEMS

openEMS is a free and open source electromagnetic field solver based on the Finite-Difference Time Domain (FDTD) method. Using an improved version of the highly-successful FDTD method (known as Equivalent-Circuit FDTD, or EC-FDTD), openEMS solves Maxwell's equations in discretized space and time to directly simulates the propagation of electromagnetic waves, in a 3D full-wave manner. It has the potential to analyze problems in important applications such as RF/microwave circuit design, antenna, radar, meta-material, and medical research.

2 Evaluation Summary

2.1 Novelic Technical Offer

Here are technical Novelic evaluation summary on provided documents:

- Overall conclusion is that: the provided report contains almost the same type of the architecture, like provided in Novelic & Nirsen study.
- However, the simulation provided by customer does not include process corners and temp range. We see TT process and nominal temp. It is clear that temperature and process deviation will influence the performance of the power detector, which imposes the design risks.
- Dead zone of PFD which they are claiming that cannot measure is not that critical, more important is blind zone which is in our case on schematic in order of 0.5*Tosc at 8GHz in some corners. This is also a design risk.
- All provided schematics are not including any parasitic estimates which make significant difference as we saw in our simulations. This is a design risk.
- Robustness over supply voltage variation imposes the design risk.
- Further technical explanation is following:
- Reset path of this and all similar PFDs has minimum 5 logic gates in signal path.
- Let's assume propagation through gate is 5ps (schematic, typical, in reality and over PVT is even worse!). Period of signal is 125ps at 8GHz which means we are loosing 20% of period just for propagation. Layout parasitics will degrade this to 40% in typical. For reset delay > 50% of period we cannot make a lock of PLL by design. This presents a design risk.
- In the provided document SiGe solution was not simulated in closed loop scenario - PFD and CP tested separately with optimistic separation between input signals. This presents a design risk.
- Mixer gm PFD is good try but followed by ideal VCO in the provided document. So, we can confirm to get similar PFD values like in initial simulations. But provided simulation does not include any real VCO with imperfections. By this approach PLL will work good if VCO is ideal, with possibly too optimistic phase noise profile. This presents a design risk.
- If the mixer is used in PFD (like possible proposed option) basically we would have PHASE ONLY locking, while if input frequencies of the PFD are significantly apart from each other, so we will not have PLL in LOCK state. This is the most likely scenario since range of input frequencies is 1-8GHz. So most probably this approach can be followed for design.
- In entire document provided by End user, Novelic do not see any VCO design, which is the most critical part besides PFD, so VCO is considered as an ideal VCO.
- Based on Novelic previous experience, and comparison to the state-of-the-art performance in journal/conference publications and/or patents we could not confirm feasibility of making VCO with required phase noise requirements, like in initial specifications.

2.2 Specification and Design Review Plan

- Prelimiary Design Review - PDR
- Critical Design Review - CDR

Voltus or Voltera to check currents

2.3 Open points

- Novelic to acquire EVB's for ADF6610, LMX2594
- Testability options within chip
- VCO registers/overriding
- External test requirements/definitions

2.4 List of reference papers

This is a list of papers regarding the CMOS technology similar to 130 nm collected by Anthony.

1. A Stacked-Complementary 5 GHz Oscillator With Even-Only Differential Harmonic Shaping Achieving -150 dBc/Hz Phase Noise at 10-MHz Offset Using Body-Biased Thin-Oxide 22-nm FDSOI
2. A VCO with Implicit Common-Mode Resonance
3. A 2.3 - 5-GHz LC-VCO With Source Damping Resistors to Suppress 1/f Noise Up-Conversion
4. A 6.7-to-9.2GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO
5. A 25% Tuning Range 7.5- 9.4 GHz Oscillator With 194 FoMT and 400 kHz 1/f3 Corner in 40nm CMOS Technology
6. A Filtering Technique to Lower LC Oscillator Phase Noise
7. A Low Phase Noise and High FoM Distributed-Swing-Boosting Multi-Core Oscillator Using Harmonic-Impedance-Expanding Technique
8. A Low Phase Noise, High Phase Accuracy Quadrature LC-VCO With Dual-Tail Current Biasing to Insert Reconfigurable Phase Delay
9. A Low Phase Noise Oscillator Principled on Transformer-Coupled Hard Limiting
10. A Noise Circulating Oscillator
11. Ultra-Low Phase Noise X-Band BiCMOS VCOs Leveraging the Series Resonance
12. An Ultra-Low Phase Noise Class-F2 CMOS Oscillator With 191 dBc/Hz FoM and Long-Term Reliability
13. CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise - Aly Ismail, Asad A. Abidi
14. Design of LC Resonator for Low Phase Noise Oscillators
15. Even-Harmonic Class-E CMOS Oscillator
16. Implicit Common-Mode Resonance in LC Oscillators
17. Third-Harmonic Injection Technique Applied to a 5.87-to-7.56 GHz 65nm CMOS Class-F Oscillator with 192dBc/Hz FOM

2.5 A Noise Circulating Oscillator

Oscillator phase noise is a fundamental metric that governs a wide variety of design aspects in modern communication and sensing systems [1], [2]

1. B. Razavi, RF Microelectronics, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2011.
2. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 2004.

2.6 Mail sent after going through CMOS papers

Franceschin paper has the best noise performance by far. It's made in SiGe 55 nm and using bipolars in core, consumes 500 mA and the output swing is clipped by diode connected bipolars which enables this much current without affecting bipolars operation.

Babaie papers are made in CMOS and are more similar to current design. It utilises step up transformers with different common and differential k factors to decouple capacitor bank from the core and control its drain currents to make a clas F2. But I currently don't know how to implement this because I don't have any ideal transformer models with different k factor for differential and common modes.

Ying paper has a similar idea calls it class F23 and also ok results which makes me think this it the most viable idea from all of these papers to try.

3 Packaging Technology Options

- Flip Chip
  - Solder balls on Nickel/Gold finish (time consuming)
  - Heat Spreader (Graphene-based)
  - Underfill materials
  - Redistribution layers(?)
- Copper Pillar (flipped die)
  - 30um min diameter, better thermal conductivity
  - More stable (no need for underfill)
  - Heat spreader most likely needed
- Chip on board
  - Glue chip on PCB cavity (non-conductive glue needed if BSE)
  - Only backside cooling available
  - Connect with wirebonds
- Open cavity QFN
  - Similar to chip on board
  - Extra penalty due to higher thermal resistance of package

On packaging from Elad:

Info: I was asked to give my opinion regarding silicone component packaging.
Since the size of the component is (on the major axis) 3.5 and down bonds to the ground are required on both sides, you need to verify the distance of the pads of the component from the edge of the die, the closer you can use a smaller ground surface. Assuming that the pads reach the edge, it will be possible to use a ground surface in a package of 4.1 mm, depending on the planning design rules of the Assembly house.
In light of this, I recommend considering using the RJR air cavity 6 x 6 mm package and its lid.
Regarding the glue, since the CTE gap between the component and the packaging is large, I recommend using the glue (I think they thought of this direction) me8456lv, which has a thermal conductivity of around 6W/m
rjrtechnologies website

QFN stands for **Q**uad **F**lat **N**o lead.
Number of pins is important for packaging - keep it below 32.

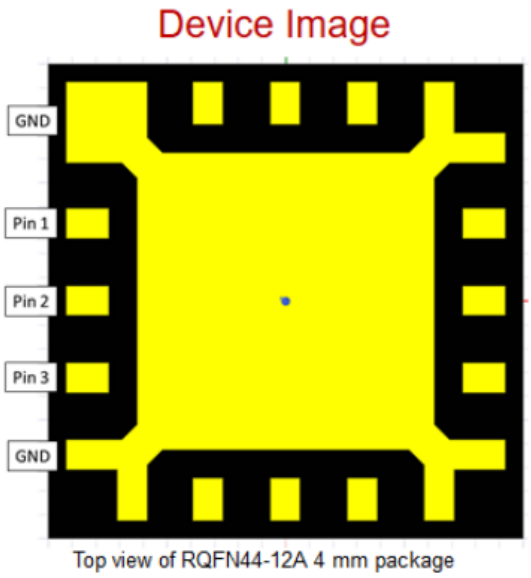

Figure 1: RQFN packaging example

3.1 Flip Chip as a packaging option

Flip chip, also known as controlled collapse chip connection or its abbreviation, C4, is a method for interconnecting dies such as semiconductor devices, IC chips, integrated passive devices and microelectromechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads. This is in contrast to wire bonding, in which the chip is mounted upright and fine wires are welded onto the chip pads and lead frame contacts to interconnect the chip pads to external circuitry.

3.2 Packaging house options

Packaging house options are:

- TAI PRO
  - **Website for Production**
- PacTech (IHP has collaboration with them)
  - **Website for Wafer Level Packaging Services**

- IZM
  - **Website for Fine Pitch Bumping for Pixel Detectors**
  - **Website for Single Chip Bumping**
- RJR Technologies
  - **Website**

3.3 Packaging terms by ampleon

Packaging is an important element in RF power transistors, influencing both the cost-efficiency and performance of a given device. Since peak powers can vary widely, from as low as 5 W to more than 1 kW, a range of packages is needed to cover every application. The choice of package format (air-cavity or overmolded plastic), often depends on the design requirements, and any **trade-offs to be made between performance and cost.**

Source for ampleon packaging
Types of packaging:

- Air-Cavity Ceramic (ACC)
- Air-Cavity Plastic (ACP)
- Overmolded Plastic (OMP)

3.4 Definition of terms regarding packaging from RJR technologies

- PRQFN - stands for RJR's thermally enhanced **P**ower ai**R**-cavity **Q**uad **F**lat **N**o-leads package
- Substrate - the base material that holds the circuit and components (chips, wires, and caps) of semiconductor devices
- Coupon - a square panel containing a cluster of substrates
- Strip - a rectangular laminate panel containing 4 in-line coupons
- Laminate - a substrate technology composed of several layers that are pressed/laminated together
- Heatslug - a square or rectangular Cu-coin inserted in the middle of the laminate substrate
- Via hole - a hole drilled from top to bottom of the substrate and is used for connecting the terminals on top to the corresponding soldering pads underneath
- ENEPIG - stands for Electroless Nickel Electroless Palladium Immersion Gold; the die bondable and wire bondable plating on top of Cu-traces in a laminate
- Terminal - metal (Cu) traces that serves as connection of the device into the outside world
- Solder resist - a thin layer of polymer that is usually applied on top of Cu-traces of the laminate substrate for protection against oxidation, and around the soldering pads to prevent solder bridges from forming between closely spaced solder pads

3.5 Die layout example

This is an example (estimation) for this PLL project die size and layout:
Also important is the pin count. Absolute minimum is 8 mm x 8 mm.

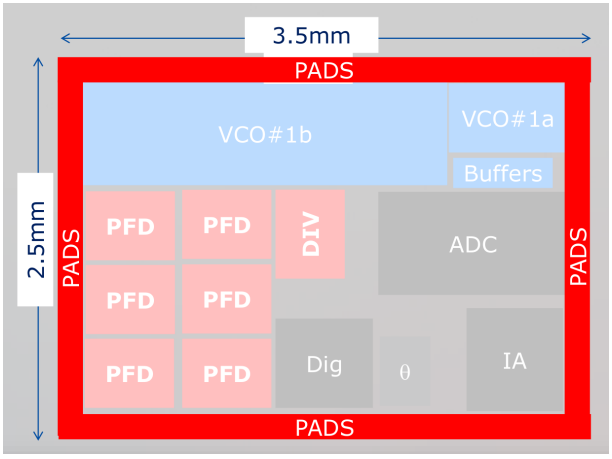

Figure 2: Die layout with pads

4 Identified various risks

- VCO phase noise contributors
- PFD topology and “blind spots”
- Discussed design methodology to be finalized in next couple of days
- Obtained PDK and discussed risk mitigation strategies
- Started authoring chip system specification
- Started project plan with internal and external milestones
- Agenda: project progress towards milestones, technical discussion
- Review & signoff of project milestones and plan
- Review system specification draft
- Packaging option

4.1 VCO phase noise contributors

Bias, current mirror vs resistor plus voltage reference
Quality factor of tank
Quality factor of inductor
Localized Backside Etching (LBE)
Core devices contribution - The noise sources in a MOS transistor are: thermal noise in the channel, 1/f noise, Noise in the resistive poly gate, noise due to the distributed substrate resistance, shot noise associated with the leakage current of the drain source reverse.

PFD is CML. Has prebuffers, charge pump.

Phase noise characterisatiom

Should it be characterized near DC like current noise or at higher frequency (att 8 GHz)

Leeson equation

According to Leeson’s Formula, the phase noise in the $\frac{1}{f^2}$ region at an offset frequency $\Delta\omega$ from an oscillation frequency of ω_{OSC}, is given in equation:

$$PNw(\Delta\omega) = kTR\frac{F}{{V_o}^2}(\frac{\omega_{OSC}}{Q\Delta\omega})^2 \quad (1)$$

where k, T, R, V_0, Q and F are the Boltzmann's constant, the absolute temperature, the equivalent tank parallel resistance, the peak oscillation amplitude, the tank quality factor, and the noise factor, respectively.

5 Blocks needed

- Bandgap PTAT (CTAT?)
- Digital: State Machines, fuses are not available
- Digital: Register Bank for VCO bands, cores

6 VCO Design methodology

Only VCO design inquiries

Technical requirements

	LO Requirements	Note	min	typ	max	Units
	VCO Requirements					
1	Full LO range		4000		8000	MHz
1a	Number of cores			2	4	/
2	Phase Noise at 1 MHz				<-135	dBc/Hz
3	differential Vtune		0.1		Vdd-x	V
4	Tuning Sensitivity K_{VCO}		?<30		?< 50	MHz/V
5	Pushing	TBD			2	MHz/V
6	Output Voltage p-p	TBD	0.8			V_{p-p}
7	Load Impedance				100	fF
	VCO and output Buffer					
8	Output Voltage	TBD	?0.8			V_{p-p}
9	Load Impedance	TBD			?1000	fF
10	Harmonic suppression (2_{nd}, typ)		-15			dBc
11	Pulling (14 dB Return Loss, Any Phase)	TBD			2	MHz
	General Specifications					
12	Operating Temperature Range		-40		105	°C
13	Supply Voltage ($\pm 5\%$)		2.375	2.5	2.625	V
14	Supply Current				?20	mA
15	Shutdown Current				?10	μA
16	Time to Switch Between Cores			?3	?5	ms

Table 1: Specification Requirements

- What is minimum phase noise that can be obtained with perfect supply, typ process, 25 degC, measured at the VCO output with ideal termination and no buffer
- What is the maximum tuning sensitivity that can be used to obtain the above
- What additional techniques need to be explored to improve the above
- Perform noise sensitivity analysis like ISF
- Discuss CML buffer concept and LDO topologies

Question 1 *Based on what was this technology picked for this specification?*

Based on previous feasibility study.

Question 2 *What is the input reference frequency of PLL? Are there any dividers in PLL?*

Input reference frequency is from 1 GHz to 8 GHz. There are for sure even if the VCO is (4-8 GHz), 2 and 3 dividers are needed.

Question 3 *Is the input from loop filter single ended or differential?*

It's differential. It also makes more sense for phase noise performance ?!

Question 4 *How will the PLL lock be detected?*

-

Question 5 *What additional techniques need to be explored to improve the above?*

Local backside etching (LBE) to improve quality (Q) factor of inductor. Affect around 1 kHz offset is 3-4 dBs, and around 0.6 - 1 dB at 1 MHz .

Info: From what I have seen in papers most promising topology in terms of phase noise is cross-coupled LC VCO class C with potential additional technique of subharmnic injection locking. This is what I plan to try first if no better solutions are provided.
Subharmonic injection lockign might be too narrowband.

A another question to the customer regarding the overall system. 8 is a great number for a divider, but maybe a bad choice for a multiplier? I don't know how it is currently implemented, but thinking of diodes/BJT with exponential characteristics we get odd harmonics, using MOS we may get even ones, at least a good 2nd. But 8=2*2*2 and 9 is just 3*3 .. one stage less, and in differential design only 9 seems feasible. In that case I tend to say that a non-sinusoidal output would even help to reduce gain in the multipliers (which also adds noise on top of the multiplication itself). Assuming that the mixer needs amplification, each *2 stage should add more than 6dB PN, leading to about 20dB or more degradation. If they want to have options on that multiplication factor, we could more easily do that in the PLL with dividers (which reduce PN). Ideally we reduce the VCO range to just more than an octave in the highest band of interest and divide the rest?

B I just want to ensure that we're not rebuilding something 1:1 that would benefit from a different structure (thinking about Bosch's wall scanner .. they asked us to turn their discrete circuit 1:1 into an ASIC ... but the central component was a tunnel diode).

Info: The resonant tunneling diode (RTD) has been investigated in many high frequency applications, including 712 GHz oscillators [1], voltage controlled oscillators (VCOs) with low power consumption [2], high output power oscillators [3], and also analog-to-digital converters [4].

A tunnel diode is a special type characterized by its ability to exhibit negative resistance. Unlike conventional diodes, which show positive resistance, tunnel diodes can conduct in the reverse bias region under certain conditions. This property makes them invaluable in various electronic applications, especially high-frequency circuits.

- Mats Ärlelid, Mikael Nilsson, Gvidas Astromskas, Erik Lind, and Lars-Erik Wernersson, "High Tuning-Range VCO Using a Gated Tunnel Diode," Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007,-798-G-5-4pp. 798-799

C Regarding VCO phase limit tests: Since noise expresses both in amplitude and phase we could use amplitude regulation to generate the tail current (e.g. using a bipolar current mirror). The problem will then be to minimize noise in the current generator. That could be done with the help of a chopper amplifier. Undesired frequency content may be a new issue, but for a differential design I believe it's solvable. For first tests, an ideal amplifier should come close to that. Maybe a bipolar amplifier doesn't even need that.

Make two chips (probably for different options for VCO)
Testbench to lock PLL, PFD loop filter and VCO.

pdk does not support detail inductor modeling.

harmonic filter is not included

loop bandwidth reallistic that can be achieved internally is from 3 MHz to 100 MHz.

up to you if it is 2nd or third order.

From CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise - Aly Ismail, Asad A. Abidi

Info: Flicker noise can upconvert around the carrier frequency in many ways, but in practical oscillators two are most important. We illustrate them at work in the conventional differential LC oscillator.

Info: 1. In the current-limited regime, the tail current governs the steady-state oscillation amplitude. Therefore, 1/f fluctuations in the tail current source (M3) produce low frequency random AM. The random AM envelope modulates the effective capacitance of the tuning varactor, converting AM into FM. The FM sidebands appear as close-in phase noise.

Info: 2. Flicker noise in the differential pair (M1, M2), modeled by an equivalent noise voltage associated with one transistor in the pair, is injected into the LC resonator as current noise at baseband and at the 2nd harmonic. This cannot account for close-in phase noise. However, the flicker noise also modulates the 2nd harmonic voltage waveform at the tail every half period, inducing a noisy current in Ctail. After commutation through M1, M2, this current mixes down to the oscillation frequency and presents a fluctuating capacitance across the LC resonator. The resulting random FM upconverts 1/f noise into close-in phase noise.

6.1 Frequency scaling and frequency plan

Formula for normalizing (scaling) phase noise to fundamental (output) frequency:

$$PN_{norm} = PN_{meas} - 20 * log_{10}(\frac{freq_{meas}}{freq_{norm}}) - 20 * log_{10}(\frac{1}{PNoffset}[MHz])$$

Scaling for phase noise in DIV+PFD+CP is different its 10 times log.

6.2 Using different models for HBT

BSIM4 and psp* (not pss), sometimes psp* gives better performance

BSIM4, as the extension of BSIM3 model, addresses the MOSFET physical effects into sub-100nm regime. The continuous scaling of minimum feature size brought challenges to compact modeling in two ways: One is that to push the barriers in making transistors with shorter gate length, advanced process technologies are used such as non-uniform substrate doping. The second is its opportunities to RF applications.

6.3 Regarding VCO design option 2 results

I believe simulation using setting multiplenoise that gives phase noise perfrmance that is now being presented is not correct. As for multiple different nets it gives very different values, which makes little sense with the topology. And when I use only one output noise for pnoise simulation I get much worse results (15-20 dBs), but they are consistent.

Sorry to bring other people into this, I thought this is important and I wanted to remove myself from these results presented since I also spent some time simulating this design this past week.

6.4 Tasks regarding the VCO option 2 and 1

option 2
Review VCO option 2 BJT and CMOS options
Review PFD latest results and CP status
Review approach going forward and schedule proposals

Guenter/Aleksandar/Anthime, can we have for each of the blocks (VCO1a, VCO1b, PFD/CP) a status page showing:
performance summary (if different than the VCO comparison table)
any special needs (supply, BSE etc)
projected area
risks so far

6.5 Problem with discontinuity of RF model

When simulating design with nmosHVRF models this error appears:

```
WARNING (SPECTRE-16780): LTE tolerance was temporarily relaxed to step over a
discontinuity in the signal: i_VCO.i_VCO_core.N3:int_INT3. Check the design
or use '+diagnose' to get more information.
        Further occurrences of this warning will be suppressed
```

I changed the model parameter:

```
+ swnqs         =  0.0 * rfmode * 5.0
In section of sg13g2_moshv_psp_parm.scs/
sg13g2_hv_nmos / model sg13g2_hv_nmos_psp pspnqs103.
```

6.6 30 GHz VCO design

Performance summary:

Parametar	Typical value
Corner	Typical
Temperature	50 °C
Amplitude	550 mVpp
Centre Frequency	30.25 GHz
Tuning Range	0.72 GHz
K_{VCO}	1.45 GHz/V
Tuning range voltage	0.2 V - 0.7 V

Table 2: Specification Requirements

Some key conclusions in terms of phase noise:
Noise at output of VCO is same as at the output of buffer. Main contributors for VCO output noise is output buffer by performing modulation of VCO tank circuit. Second main contributor is noise in references used to generate VCO current bias and noise in power supply.
Note that current tail bias mirror is using PTAT current.

Question 6 *Why is PTAT used?*

VCO output swing or VCO output freq or sth else?

6.7 Parts of interest of VCO

List of parts:
VCO core
Differential Varactor (Varactor)
Capacitor bank (unit)
Current and voltage bias - emmiter and source degeneration
Bandgap reference generation for v gate col bias control

6.7.1 Balun is external

Balun is off chip Multiplexer is high frequency up to 80 GHz - differntial amplifier structure.

6.8 Emmiter vs Source degneration

source capacitive degeneration

6.8.1 Paper on YIG VCO

A Low-Noise Transmission-Type Yttrium Iron Garnet Tuned Oscillator Based on a SiGe MMIC and Bond-Coupling Operating up to 48 GHz Marcel van Delden , Student Member, IEEE, Nils Pohl , Senior Member, IEEE, Klaus Aufinger , Member, IEEE, Christoph Baer , Member, IEEE, and Thomas Musch, Member, IEEE

Info: Second, tunable opto-electronic oscillators (TOEO) use sophisticated optical resonators to tune the output frequency in the microwave range. They offer a high bandwidth of up to more than one octave and low phase noise at the same time [19], [20]. However, TOEOs require at least a laser, an optical resonator, an electrooptic phase or amplitude modulator, a fast photodiode, a delay line as well as a filter, and an amplifier for microwave frequencies. High-performance TOEOs like [19], [20] require even more and sophisticated components. Thus, TOEOs are expensive and complex.

7 Design of VCO Tank

7.1 Differential Varactor

2 papers

Option 1 is referencing **paper** A 44 GHz Differentially Tuned VCO with 4GHz Tuning Range in 0.12 um SOI CMOS

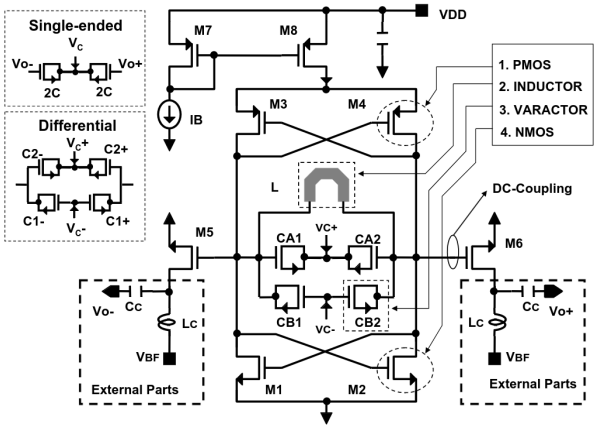

Figure 22.4.1: Differentially tuned 44GHz VCO schematic.

Option 2 is referencing **paper** A 23-mW 60-GHz Differential Sub-Sampling PLL with an NMOS-Only Differential-Inductively-Tuned VCO

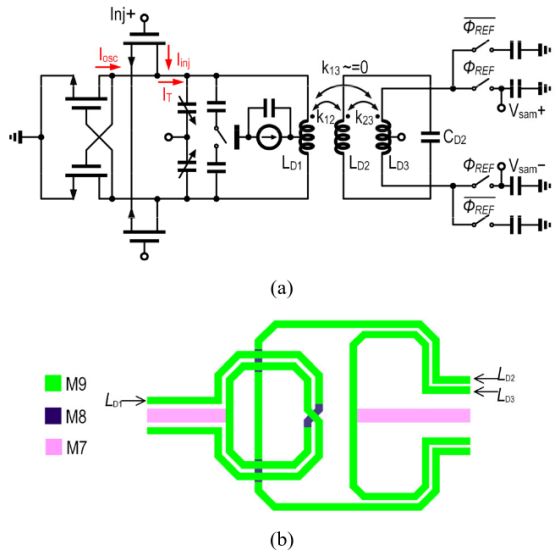

Fig. 3. (a) Proposed differential co-design of ILFD and PD and (b) design of the coupled coils for the co-design.

low Q part of Varactor tuning range:

Info:

Q factor is worse for differential tuning vs single-edned tuning.

7.2 Design of Capacitor Bank

2 Single-ended banks vs Differential capacitor banks

7.3 Design of Inductor

Electro-Magnetic simulator is needed. Technology Parameters if calculations are to be done. Look up the metal stack and info

Parameter	Value	Unit
Substrate resistivity	X	Ω-cm
Substrate thickness	?	um
Silicon dielectric constant	?	no unit
Oxide thickness (M3-Sub)	?	um
Oxide thickness (M3-M2)	?	um
SiO_2 dielectric constant	?	no unit
Metal resistivity	?	Ω-um
Top Metal (M?) thickness	?	um
Other metal thickness	?	um

Table 3: Technology Parameters

Inductor can be also switchable,

8 Non VCO parts of PLL

8.1 PFD topology and blind zone

Reset path delay is needed because of dead zone and that is why blind zone was much worse than expected.

8.2 Loop Filter

differential

9 Commercial Parts

Commercial parts used as alternative or to augment the design.

LMX2592

LMX2592 High Performance, Wideband PLLatinuTM RF Synthesizer With Integrated VCO
VCO Phase Noise: –134.5 dBc/Hz at 1-MHz
Offset for 6-GHz Output
Industry Leading Phase Noise Performance
VCO Phase Noise: –134.5 dBc/Hz at 1-MHz Offset for 6-GHz Output
Normalized PLL Noise Floor: –231 dBc/Hz
Normalized PLL Flicker Noise: –126 dBc/Hz – 49-fs RMS Jitter (12 kHz to 20 MHz) for 6 GHz Output
Applications:

- Test and Measurement Equipment
- Defense and RADAR
- Microwave Backhaul
- High-Performance Clock Source for High-Speed
- Data Converters
- Satellite Communications

TPS7A8300

Texas Instruments: TPS7A8300 2-A,6-µV RMS,RF,LDOVoltage Regulator

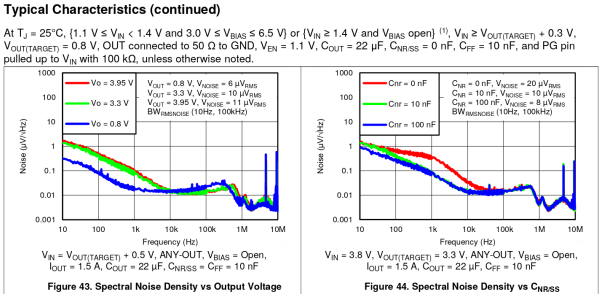

Figure 43. Spectral Noise Density vs Output Voltage

Figure 44. Spectral Noise Density vs $C_{NR/SS}$

10 LO block VCO and VCO Buffer - old project

Old project for topcon INSERTDATE

10.1 Introduction

LO block is LC VCO with internal inductor and fully differential output buffer. Its schematic shall ensure differential connection to the mixer LO input and PLL RF input. LO block should have the characteristics given in Table 10.2. Due to wide frequency range it is necessary to use switchable capacitor banks.

10.2 Technical Requirements

	LO Requirements	Note	min	typ	max	Units
	VCO Requirements					
1	Full LO range		6300		13700	MHz
2	Phase Noise at 300 kHz				<-101	dBc/Hz
3	Vtune		0.1		1	V
4	Tuning Sensitivity K_{VCO}				100	MHz/V
5	Pushing	TBD			2	MHz/V
6	Output Voltage	TBD	0.8			V_{p-p}
7	Load Impedance				100	fF
	VCO and output Buffer					
8	Output Voltage	TBD	0.8			V
9	Load Impedance	TBD			1000	fF
10	Harmonic suppression (2_{nd}, typ)		-15			dBc
11	Pulling (14 dB Return Loss, Any Phase)	TBD			2	MHz
	General Specifications					
12	Operating Temperature Range		-40		125	°C
13	Supply Voltage		1	1.1	1.2	V
14	Supply Current				20	mA
15	Shutdown Current				10	μA
16	Time to Switch Between Cores			3	5	ms

Table 4: Specification Requirements

Min and max for supply voltage are not defined in the original document, and time for switching between two cores was defined during the meeting.

Currently Full LO range is split between two cores so the requirement should look like this:

	LO range requirements	Note	min	typ	max	Units
1	High Band core LO range		10000		13700	MHz
2	Low Band core LO range		6300		10000	MHz

Table 5: LO Range Two Core Specification Requirements

Question 7 *What's the variation for supply voltage?*

Not defined probably will be the same as the rest of the

Question 8 K_{VCO} *Why is it in the max column?*

Didn't get answer for this. It's probably also typical and a value that is expected by the PLL design.

Process corners can be found at:

`/tech/tsmc/tsmc40/models/spectre/crn40lp_2d5_v2d0_2_shrink0d9_embedded_usage.scs`

10.3 Scaldio Design Review

Question 9 *How should calibration be implemented to achieve output voltage peak to peak and minimize noise?*

Is it done for whole PLL?

Question 10 *Difference between class-B and class-C vco?*

Scaldio uses class-C, so all parasitic capacitances connected to the tail don't matter. Having trouble with observing the currents of drain so cannot check this and compare them. Scaldio looks something between class C and class B because of V_{gbias} voltage and because adding inductor between tail NMOS and switching pair improves phase noise. This is attributed to class B, while class C only needs tail capacitance.

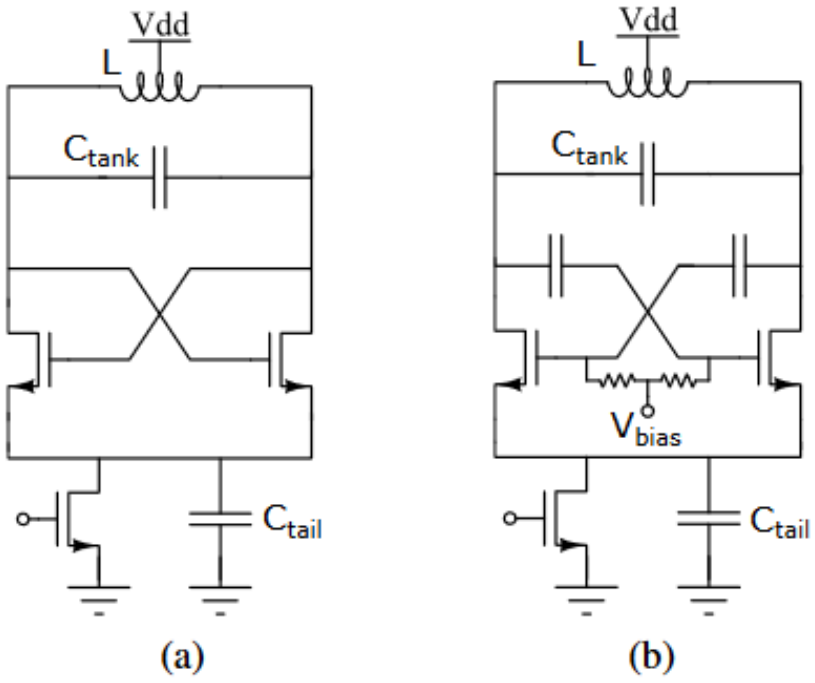

Fig. 1: Oscillator topologies: (a) class-B; (b) class-C.

Lowest bit of digital varactor (L0_PLL_hbVCO_Cdig_SC2B_VCOS_SC2C_PLL) doesn't do anything, isn't even monotonous. Maybe makes more sense when simulating extracted cells. Digital varactor needs to be redesigned, it could lower the Q factor. Main difference between class B and class C can be observed by investigating their drain currents.

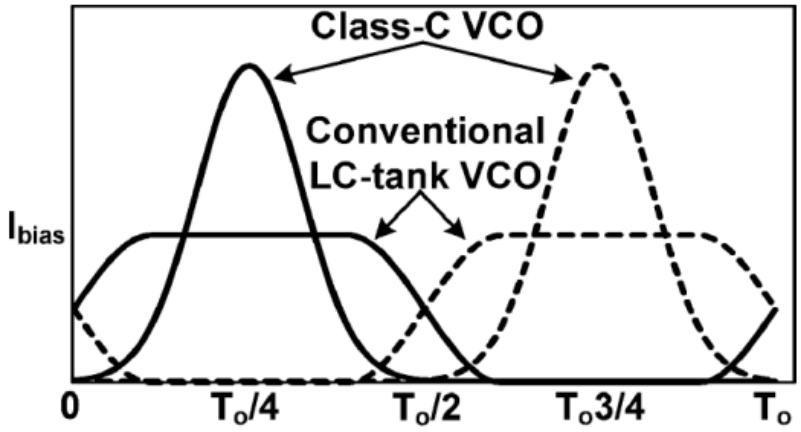

Fig. 2. Drain current of the switch pair FETs for conventional LC-tank VCOs and class-C VCOs.

10.4 Main testbench

Main testbench covers everything except for frequency pulling and full LO range. The simulation results are obtained at the higher end of the LO range. Phase noise is simulated by pss+pnoise.

Info: With Noise Type=timeaverage and ALL(AM,PM,USB,LSB), you can plot the AM and PM components as well as the total noise. In addition, you can plot phase noise and FM jitter results for oscillators. Plotting is done using the Direct Plot Form. **External link**

Function of phase noise is simulated for PM noise type.
How to choose beat frequency for autonomous system from forum **thread**.

Info: In an autonomous system (e.g. an oscillator), you turn on the "oscillator" checkbox, and the beat frequency is then the estimated frequency, which gives PSS a starting point to solve for the oscillator frequency. It's important when in oscillator mode to select the outputs of the circuit, which include any subharmonics. In other words, if you have an oscillator followed by a divider, point at the divider output, and give the estimated divided frequency as the beat frequency. Again, this is because you need to solve an integer number of cycles of all the frequencies in the circuit. Note, don't use oscillator mode for circuits which aren't oscillators, since you're then trying to get the simulator to solve for an unknown which is not unknown, which may lead to convergence problems.

Most of the I_{bias} tune digital control is not used for the higher band, so by increasing the number of steps to cover even higher frequencies than the original design finer bias control is needed.

10.5 Simulation Results for Scaldio design

Simulated only nominal corner with change for V_{DD} only for frequency pushing simulation.

Phase noise changes a lot for different tuning voltages between -90 and -100 dBc/Hz. Phase noise is probably not modeled ok because the VCO doesn't have the connection between current bias tail and the switching pair of VCO as transmission line. That inductance and C_{tail} should resonate at $2\omega_O$ (tank oscillating frequency), but only in the case of class B oscillator. Check what type is vco oscillator.

	LO Requirements	Note	min	typ	max	Sim(Typ)	Units
1	Phase Noise at 300 kHz				<-101	-98	dBc/Hz
2	Tuning Sensitivity K_{VCO}				100	over	MHz/V
3	Pushing	TBD			2	279.7	MHz/V
4	Output Voltage	TBD	800			809.3	mV_{p-p}
5	Harmonic suppression (2_{nd}, typ)		-15			-26.78	dBc
6	Pulling (14 dB Return Loss, Any Phase)	TBD			2	19.51	MHz

Table 6: Scaldio IMEC design Results

10.6 Q factor of LC tank

Need testbenches capacitance of tank, varactors and inductor, and for different controls and also corners. Process corners for varactors are the same as MOSFET.

Question 11 *What kind of chip is it?*

What kind of inductance is expected to be connected on V_{DD} and V_{SS} pins. This may or may not change the results. Removed all together right now.

Testbench for differential Q and L of the inductor that is EMX simulated is shown in Figure 3.

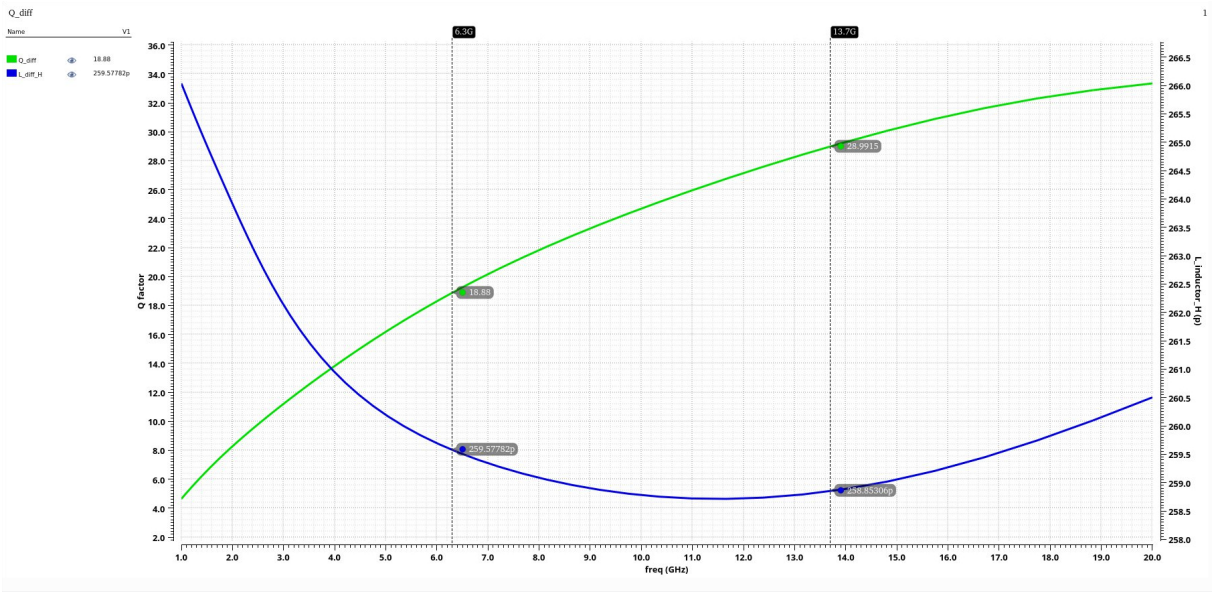

Figure 3: Q factor and inductance of L

Q factor is better at the higher frequency.

Simulated Q factor of both varactors and inductor. Q factor of digital varactor for lower bit controls is not much better than Q of inductor.

Capacitor calculating capacitance and Q factor:

$$Y_{diff}(im) = imag(ypm('sp11)) + imag(ypm('sp22)) - imag(ypm('sp21)) - imag(ypm('sp12)) \quad (2)$$

$$Y_{diff}(re) = real(ypm('sp11)) + real(ypm('sp22)) - real(ypm('sp21)) - real(ypm('sp12)) \quad (3)$$

Capacitance:

$$C_{diff} = \frac{Y_{diff}(im)}{2\pi f} \quad (4)$$

Q factor of capacitor:

$$Q_C = \frac{Y_{diff}(im)}{Y_{diff}(re)} \tag{5}$$

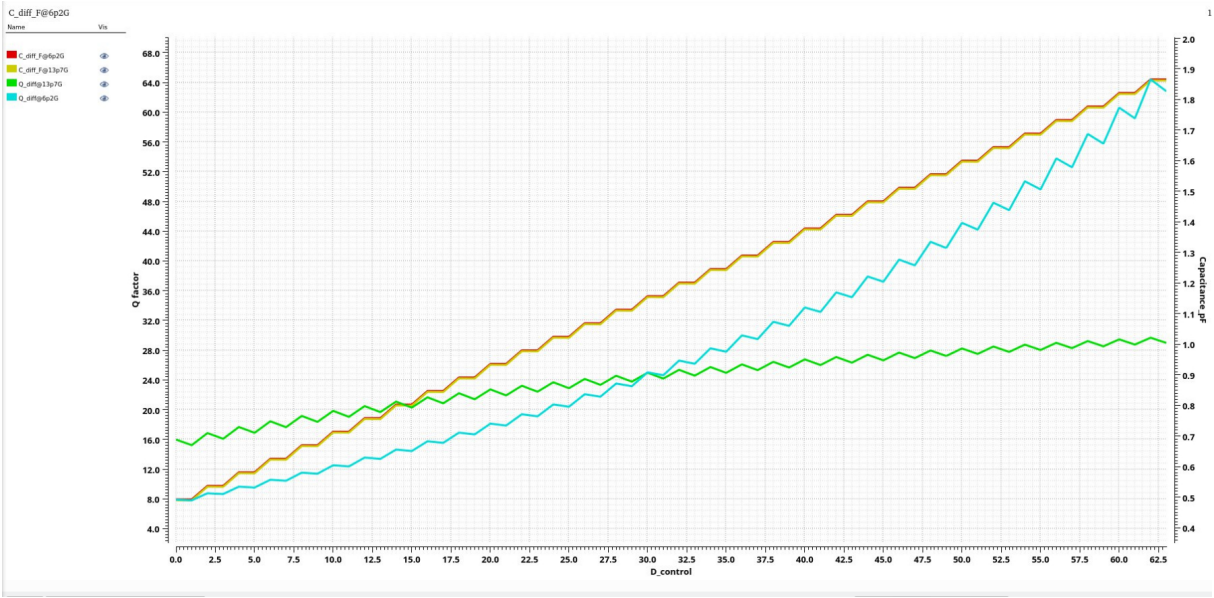

Figure 4: C and Q of digital varactor through controls

More info can be found in **paper** A Thorough Analysis of the Tank Quality Factor in LC Oscillators with Switched Capacitor Banks.

Found definitions:

$$Q_{LC} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{f_r}{\Delta f} = \frac{\omega_r}{\Delta \omega} = \frac{\tau_d \omega}{2} \tag{6}$$

where τ_d is group delay.

Question 12 *How to calculate group delay using sparam analyis?*

?

10.7 Calculating Q factor, LC tank by ringing method

Link to **website** that shows ring down method of calculating Q factor. Not implemented in virtuoso TODO.

10.7.1 Figure of Merit different definitions

Info: The theoretical maxima for the FoM of an oscillator is given by $FoM = 174 + 20log_{10}(Q)$ dBc/Hz

How to calculate oscillator FoM? Is Q_L factor dominant enough to just equate it with LC tank Q facor. The widely used FOM is calculated by:

$$FoM = L\{\Delta\omega\}(\Delta f/f_0)^2 PVCO[mW] \tag{7}$$

Where $L\{\Delta\omega\}$ is the phase noise, $\Delta\frac{f}{f_0}$ is the ratio between the offset frequency and the carrier, and P_{VCO} is the power consumption of the VCO-core. There is also FoM^T and FoM_A

$$FoM^T = FoM - 20\log(\frac{FTR}{10}) \tag{8}$$

and

$$FoM_A = FoM + 10\log(A) \tag{9}$$

where A is area [mm^2], and FTR frequency tuning range [$\%$]
Information about digital varactor copied from **External link**

Info: Each bit of MIM varactor contains two MIM capacitors connected differentially with a series switch, two pull-up and two pull-down transistors to effectively turn the varactor between its high and low-capacitance states. Measured intrinsic Q of the MIM capacitor is 80 at 3.6 GHz. When is turned on, i.e., high-capacitance state, the varactor Q drops to 30. When is turned off to be in low-capacitance state, the parasitic capacitance of the MIM capacitor and transistors has an effective of 50. The pull-down transistors set the DC levels for drain and source of at 0 V so that can be efficiently turned into triode region while the weak pull-up transistors set the DC level to VDDOSC to reduce the parasitic capacitance of thus increasing of the parasitic capacitance. The pull-up pMOS can be implemented by either resistors or transistors. The latter was chosen for silicon area efficiency. Compared to MOS varactors, MIM varactors have a much lower . However, since the differential phase-stability inductor is only 10, the impact of lower varactor is tol erable. When the MIM varactor is at its low-capacitance state, the large DCO internal signal swing and the DC level of 1.4-V supply voltage at source/drain of the pull-up transistors force the drain -nwell junction diodes of the pull-up pMOS to momentarily go into forward-bias condition resulting in a latch-up concern. However, since the forward-bias condition occurs only in 50% of a 3–4 GHz period, the latch-up phenomenon with the parasitic BJTs can not be triggered.

10.8 Lowering frequency pushing and LDO

About Frequency pushing from **this paper**

Info: An LC-tank VCO circuit has been implemented in a standard 0.35 μm CMOS technology. It is based on a two-transistor biasing structure that improves the performance of frequency pushing and frequency tuning range. Final measurement of proposed structure gives 516 MHz tuning range with 2.278 GHz center frequency and about 0.55$\%$/V frequency pushing in the worst case. The achieved FOM is about -180dBc/Hz, which is very close to the simulated value. This structure is proven to be particularly suitable for achieving low FOM in the VCO circuits having low Q factor LC-tank. Both, the proposed structure and the FOM optimization method, can also be applied to the VCO designs for the applications at higher frequencies, such as 5GHz VCOs for Wireless LAN applications.

Question 13 *Can VCO work for lower voltage of 0.9 V?*

This may be needed if LDO is required because of frequency pushing?

Question 14 *Does frequency only happen because of the ripple directly induced by buffers e.g.?*

Or could it happen because of EM crosstalk?

Is frequency pushing testbench good? Look into this paper. Different testbench would be to make a transient change in Vdd and check how much frequency changes.

Results for class C with pmos bias, only dc change of V_{DD}:

Parameter	typical	spec	min	max	ss -40	ss 125	ff -40	ff 125	Units
Frequency Pushing	43.93	< 2	43.93	100.1	100.1	64.36	75.48	64.09	MHz
Frequency	14.6	> 14.2	14.6	15.83	15.54	15.48	15.83	15.59	GHz

This shows some improvement from frequency pushing of 250 - 300 MHz that was observed for the nmos bias of IMEC Scaldio design.

10.9 Changing topology and lowering phase noise

Decision on why is single sided oscillator chosen instead of double sided oscillator.

Info: However, if non-negligible parasitic capacitances are found at the tank outputs, the phase-noise performance of the DS-VCO may be seriously degraded, while that of the SS-VCO remains unaffected.

More on the $\frac{1}{f^2}$ Phase Noise Performance of CMOS Differential-Pair LC-Tank Oscillators in **paper** by Pietro Andreani.

10.10 Hybrid class C and class B

Info: Further, the proposed VCO solves the issue of the hybrid mixed-signal start-up procedure exposed in [8]. The main drawback of this approach is that, if oscillation stops for some unaccountable reason, the VCO can only be restarted actuating again the whole start-up procedure.

Referenced paper is:

8 J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L.-R. Zheng, "A low power, startup ensured and constant amplitude class-C VCO in $0.18\,\mu\mathrm{m}$ CMOS," IEEE Microw. Wireless Compon. Lett., vol. 21, no. 8, pp. 427–429, 2011. Dec. 2008.

10.11 Enhanced Oscillation Swing

Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing in **this paper.** Phase noise is lowered by lowering V_{gbias}, but it makes oscillations start up harder.

Info: As noted above, the phase noise improves with increasing the oscillation amplitude, which here would mean lowering the gate bias voltage, V_{bias} . Unfortunately, the original class-C oscillator limits the fixed V_{bias} from being set low enough, otherwise the oscillation may not start up. In [11], a high-swing class-C (HSCC) oscillator was introduced, which removed the tail current transistor of the original class-C oscillator [6]. Instead, an automatic amplitude control was introduced to stabilize the oscillation amplitude. In this work, instead of the transformer used in [11], we choose a simple RC bias circuit.

This is from **paper** Dual-Core High-Swing Class-C VCO design, and references

6 A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

11 M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in Proc. ESSCIRC, Sep. 2011, pp. 495–498

10.12 Questions about new double feedback

Amplitude Feedback for Robust start up

10.13 OTA1 - Start up and gate voltage bias control

Referent voltage should be set and controlled around 800 mV. Need tests for OTAs inside for VCO, currently simulated only PM and DC gain, should test different V_{ref} levels.

10.14 OTA2 - Start up and bias control

Referent voltage should be set and controlled around 400 mV. Problem with OTA2 loop is amplifying noise into the tail bias current. So the new problem arises as noise shaping in LOOP2 is needed. If a OTA of low uGBW is used than start up is too slow.

10.15 Full LO Range and Frequency Recentering

TODO Add corners for **fs sf** and similar. Because the LO range is split on two cores, ideally halved. Results are simulated for process and temperature corners:

Core and Specifictaion	min	max	sim(min)	sim(max)	Units
VCO core split					
High Band Higher limit	13700		15580	16190	MHz
High Band Lower limit		10000	10870	12460	MHz
High Band range	3700		4710	3730	MHz
Low Band Higher limit	10000		13230	14120	MHz
Low Band Lower limit		6300	6724	8028	MHz
Low Band range	3700		6506	6092	MHz

Table 7: LO range specification and simulation for Scaldio LC tank

Expecting the drop for schematic simulated frequency range, covered range should at least be larger than needed when recentered:

$$HBFR = 13700 - 10000 = 3700 < 3730 = 16190 - 12460 \tag{10}$$

For lower band it's similarily calculated

$$HBFR = 10000 - 6300 = 3700 < 6092 = 14120 - 8028 \tag{11}$$

Lower and higher band are assymetrical and they overlap for at least:

$$HBLBoverlap_{high} = 13230 - 10870 = 2360 \tag{12}$$

$$HBLBoverlap_{low} = 14120 - 12460 = 1660 \tag{13}$$

The worst available frequency digital controlled range is $6092 + 3730 - 1660 = 8162$ MHz which is higher than 7400 MHz.

Question 15 *Are the two VCO-s in the same process corner at the same time?*

Yes. If not than the calculations are wrong.

NOTE: Analog varactor 0-Vt-1 change does not work so it wasn't included. Further frequency recentering after extraction will be needed.

10.16 Pulling testbench and design of VCO buffer

Needs port at and tuning circuit to keep the reflection at -14 dB. Port of reference impedance 10 kΩ and portAdapter from rfExamples. S parameter analysis to show if the reflection really is -14 dB? Load impedance increased from 100 fF to 1000 fF. VCO buffer is also needed because of the frequency pulling. Does each core have a buffer or do they share it? first make a buffer than maybe a question.

By adding two buffers from `LO_FDDQ_v6`, `LO_FDDQ_INHB_v5_JCx_saldio2b` and `LO_FDDQ_BUF_X24` , frequency pulling drops below 1 MHz.

So this specification looks fine, testbench shown:

How does portAdapter work?

Frequency pulling mentions coupling (crosstalk) between different blocks on chip and the VCO.

10.17 PTAT and CTAT, the temperature independant Vbias for cascode

TODO Simulate and show results of temperature sweep.

10.18 Effect of too high tail capacitance

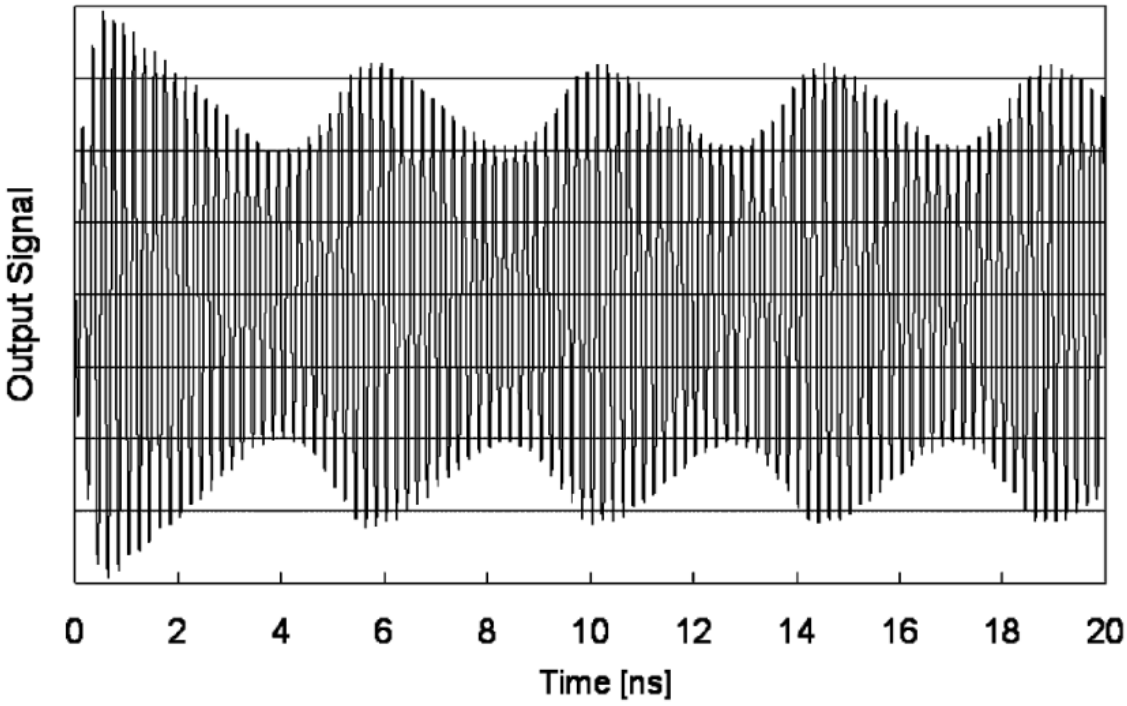

Fig. 10. Effect of too large a tail capacitance: the oscillation suffers from instability, which takes the form of a low-frequency amplitude modulation (squegging).

Figure 5: Squegging

Instability Low frequency amplitude modulation squegging. This was the issue with the original class C with tail current. Is it important for new topology where current bias is PMOS.

10.19 PLL theory - PLL Lock Detect and calibration

About PLL Lock Detect:

Info: The ability for a PLL to reliably indicate when it is in lock is critical for many applications. An ideal lock detect circuit gives a high indication when the PLL is locked and a low indication when the PLL is unlocked. When VCO calibration finishes it can be indicative if the lock is detected.

PLL VCO calibration usually goes as amplitude frequency and then amplitude calibration, or the other way?

Divide and Conquer algorithm

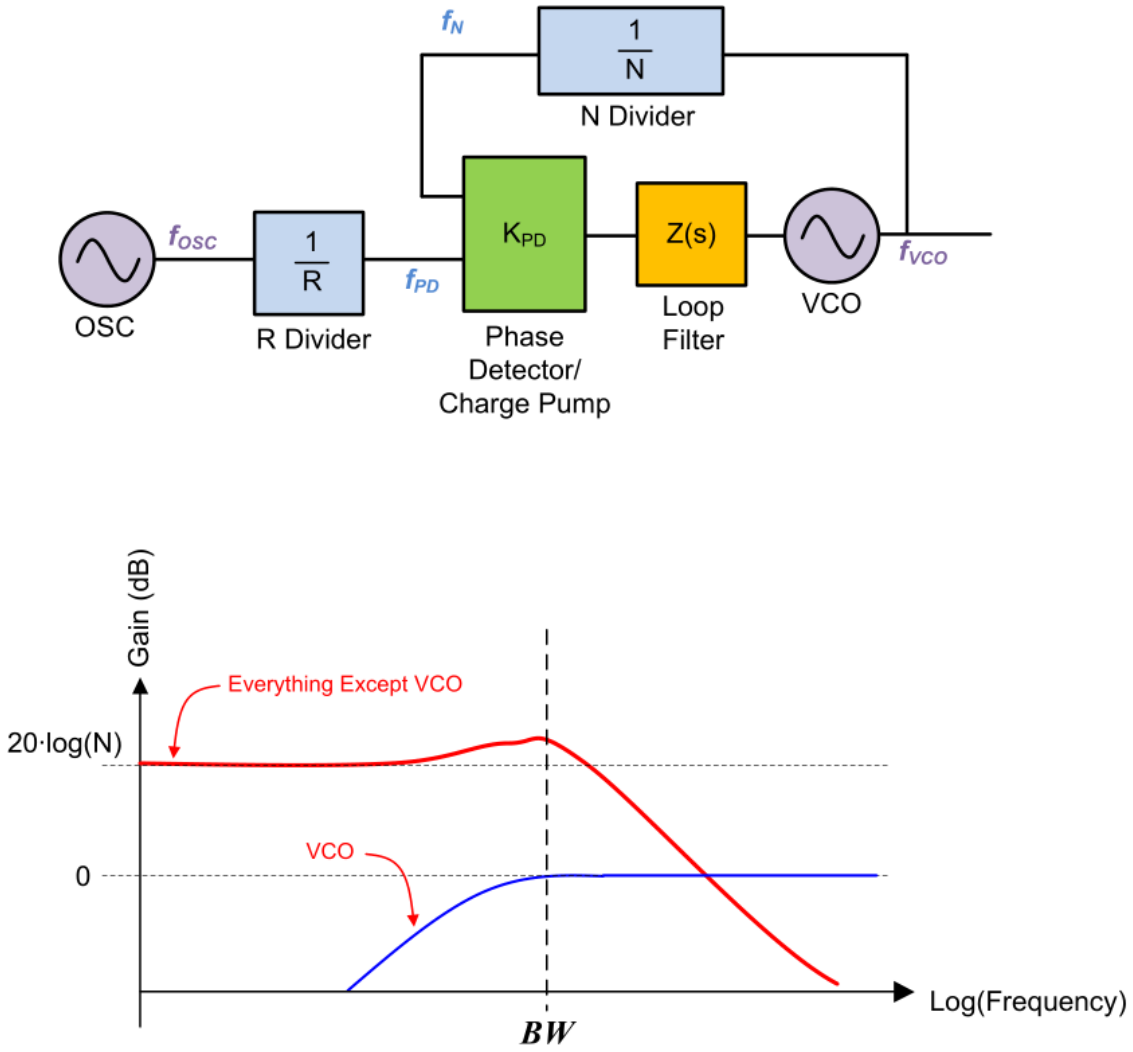

Figure 6: Gain for VCO and other blocks inside of PLL

Info: For the VCO, the noise is suppressed below the loop bandwidth frequency and unshaped above the loop bandwidth.