

## 2022-2023 Logic Circuits Final Exam

A combinational circuit that takes 2-bit signed 2's complement form A number ( $A_1A_0$ ) and B number ( $B_1B_0$ ) as input is requested to perform  $C=A+B$  operation in signed 2's complement form at its output.

A	B	C
00	00	00
00	01	01
00	10	10
00	11	11
01	00	01
01	01	10
01	10	11
01	11	00
10	00	11
10	01	00
10	10	01
10	11	10
11	00	01
11	01	10
11	10	11
11	11	00

Q1: How many bits are required for output?  
a) 2 b) 3 c) 4 d) 5

Q2: What is the logical expression of the least significant output?  
a)  $A_0 \oplus B_0$  b)  $A_0 \oplus B_0$  c)  $A_0 + B_0$  d)  $A_0 \cdot B_0$

Q3: How many 2-input NAND gates can we achieve the least significant output with? (NOT including Gates will be)  
a) 2 b) 3 c) 4 d) 5

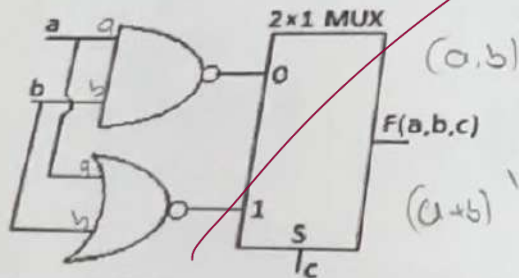
Q4: We want to design a circuit with a minimum number of AND, OR, and NOT gates that will allow a 4-bit A number ( $A_3A_2A_1A_0$ ) to output 1 if it is greater than 10 (10 in decimal system). What would be the logical expression of the output?  
a)  $A_3 + A_1$  b)  $(A_3 + A_1) \cdot A_0$  c)  $A_3A_2 + A_3A_1A_0$  d)  $A_3A_2 + A_1 \cdot A_0$

$A_3$	$A_2$	$A_1$	$A_0$	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Q5: X is a 3-bit number in 2's complement form. Our combinational circuit is required to perform  $Z=X^2+2X+1$ . How many bits must the Z output in 2's complement form be?  
a) 4 b) 5 c) 6 d) 7

$$x = \begin{matrix} 2 & 1 & 0 \\ 0 & 1 & 1 \end{matrix} \quad x^2 + 2x + 1 = 8 + 3 + 1 = 13$$

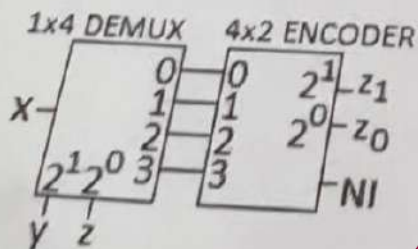
Q6: The minterms of the F output of the circuit below. What is the expression in terms of?  
a)  $\Sigma(2,4,6,7)$  b)  $\Sigma(4,5,6,7)$  c)  $\Sigma(1,3,5,6,7)$  d)  $\Sigma(0,1,2,4)$



$$-16 \quad -13 = 10011$$

2's
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

Answer 3 questions according to the circuit below.  
NOT: NI output 1 if no information comes to the inputs of the encoder and in this case the outputs  $z_1$  and  $z_0$  are unimportant.



Q7: What is the expression for the  $z_1$  output?  
a) x b) y c) z d)  $x'$

Q8: What is the expression for the  $z_0$  output?  
a) x b) y c) z d)  $x'$

Q9: What is the expression for the NI output?  
a) x b) y c) z d)  $x'$

Q10: A decoder circuit will be designed for the 7-segment display with common anode. Depending on the inputs ( $S_1$  and  $S_0$ ) of the decoder circuit, it is desired to display the numbers between 0 and 3. Based on this information, what would be the logical expression of the a segment output?

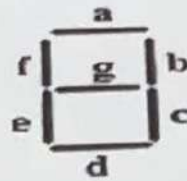
$S_1S_0 = 00$  ise ☐

$S_1S_0 = 01$  ise ☐

$S_1S_0 = 10$  ise ☐

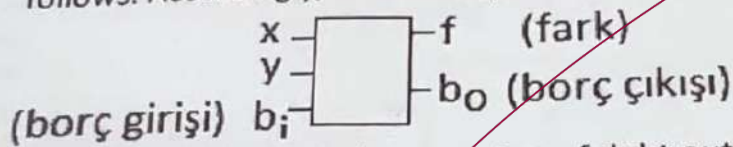
$S_1S_0 = 11$  ise ☐

$S_1$	$S_0$	a
0	0	1
0	1	0
1	0	1
1	1	1



- a)  $S_1'.S_0$  b)  $S_1'+S_0$  c)  $S_1+S_0$  d)  $S_1.S_0$

The block representation of the full extractor is as follows. Accordingly, answer 2 questions.



Q11: What is the logical expression of debt output?

- a)  $x'.b_i + x'y + y.b_i$  b)  $x'y + b_i$  c)  $(x - y)b_i$  d)  $xyb_i$

Q12: Complete extractor with decoder and OR gates we want to realize. How should we choose?

- a) 1 tane 2x4 decoder, 2 OR gate  
b) 1 tane 3x8 decoder, 2 OR gate  
c) 1 tane 2x4 decoder, 1 OR gate  
d) 2 tane 3x8 decoder, 1 OR gate

Q13:  $f(a,b,c,d)$  prime implicants;

$c'd'$ ,  $ac'$ ,  $a'bd'$ ,  $a'bc$  and then

Which of the following is not a essential prime implicants?

- a)  $c'd'$  b)  $ac'$  c)  $a'bd'$  d)  $a'bc$

Q14: What would be the f output of the circuit below?

- a)  $xy' + z$  b)  $x' + y$  c)  $x'yz$  d)  $x' + y' + z'$

