

2022-2023 Logic Circuits Final Exam

A combinational circuit that takes 2-bit signed 2's complement form A number (A_1A_0) and B number (B_1B_0) as input is requested to perform $C=A+B$ operation in signed 2's complement form at its output.

Q1: How many bits are required for output?
a) 2 b) 3 c) 4 d) 5

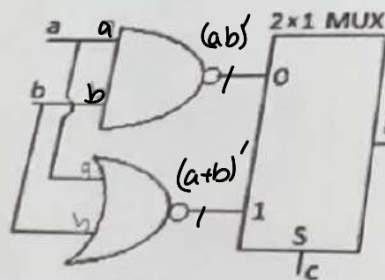
Q2: What is the logical expression of the least significant output?
a) $A_0 \oplus B_0$ b) $A_0 \oplus B_0$ c) $A_0 + B_0$ d) $A_0 \cdot B_0$

Q3: How many 2-input NAND gates can we achieve the least significant output with? (NOT including Gates will be)
a) 2 b) 3 c) 4 d) 5

Q4: We want to design a circuit with a minimum number of AND, OR, and NOT gates that will allow a 4-bit A number ($A_3A_2A_1A_0$) to output 1 if it is greater than 10 (10 in decimal system). What would be the logical expression of the output?
a) $A_3 + A_1$ b) $A_3 + A_1 \cdot A_0$ c) $A_3A_2 + A_3A_1A_0$ d) $A_3A_2 + A_1 \cdot A_0$

Q5: X is a 3-bit number in 2's complement form. Our combinational circuit is required to perform $Z=X^2+2X+1$. How many bits must the Z output in 2's complement form be?
a) 4 b) 5 c) 6 d) 7

Q6: The minterms of the F output of the circuit below. What is the expression in terms of?
a) $\Sigma(2,4,6,7)$ b) $\Sigma(4,5,6,7)$ c) $\Sigma(1,3,5,6,7)$ d) $\Sigma(0,1,2,4)$



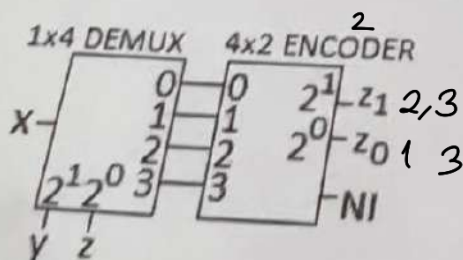
$$F(a,b,c) \rightarrow (ab)'c' + (a+b)'c$$

$$(a+b)'a'c' + b'c' + a'b'c$$

$$0-0 \quad -00 \quad 001$$

Answer 3 questions according to the circuit below.

NOT: NI output 1 if no information comes to the inputs of the encoder and in this case the outputs z_1 and z_0 are unimportant.



D_0	D_1	D_2	D_3	z_0	z_1
0	0	0	0	x	x
1	0	0	0		
	1				

$xy'z'$
 $xy'z$

Q7: What is the expression for the z_1 output?

a) x b) y c) z d) x' $xy'z' + xy'z \Rightarrow xy$

Q8: What is the expression for the z_0 output?

a) x b) y c) z d) x' $xy'z + xy'z' \Rightarrow xz$

Q9: What is the expression for the NI output?

a) x b) y c) z d) x'

$z'z'$

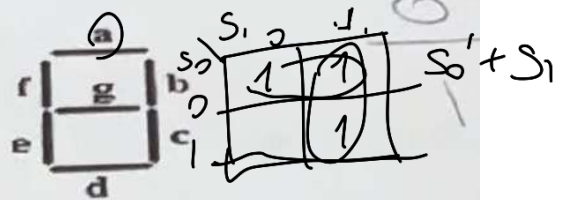
Q10: A decoder circuit will be designed for the 7-segment display with common anode. Depending on the inputs (S_1 and S_0) of the decoder circuit, it is desired to display the numbers between 0 and 3. Based on this information, what would be the logical expression of the a segment output?

$S_1S_0 = 00$ ise ☐

$S_1S_0 = 01$ ise ☐

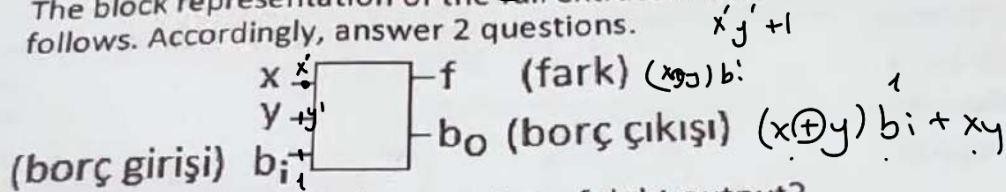
$S_1S_0 = 10$ ise ☐

$S_1S_0 = 11$ ise ☐



a) $S_1'.S_0$ b) $S_1'+S_0$ c) S_1+S_0 d) S_1+S_0

The block representation of the full extractor is as follows. Accordingly, answer 2 questions.



Q11: What is the logical expression of debt output?

a) $x'.bi + x'y + y.bi$ b) $x'y + bi$ c) $(x \oplus y)bi$ d) $xybi$

Q12: Complete extractor with decoder and OR gates we want to realize. How should we choose?

- a) 1 tane 2x4 decoder, 2 OR gate
- b) 1 tane 3x8 decoder, 2 OR gate
- c) 1 tane 2x4 decoder, 1 OR gate
- d) 2 tane 3x8 decoder, 1 OR gate

Q13: $f(a,b,c,d)$ prime implicants ;

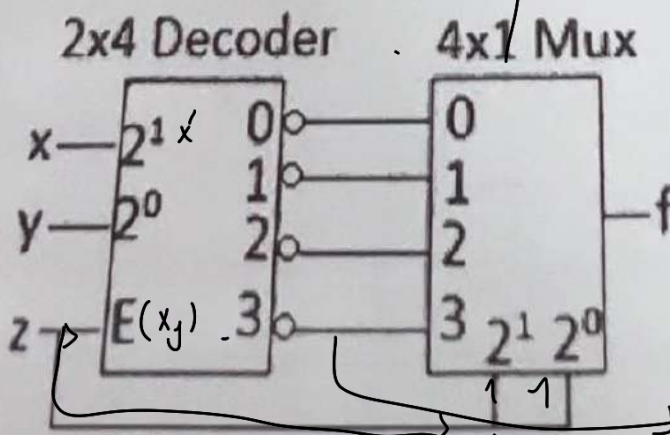
$c'd'$, ac' , $a'bd'$, $a'bc$ and then

Which of the following is not a essential prime implicants?

a) $c'd'$ b) ac' c) $a'bd'$ d) $a'bc$

Q14: What would be the f output of the circuit below?

a) $xy' + z$ b) $x' + y$ c) $x'y$ d) $x' + y' + z'$



$$z = 1$$

$$x' + y' + z'$$

$$x'y$$