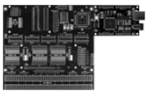
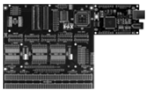


EEL 3744

Menu

- System Clock on XMEGA

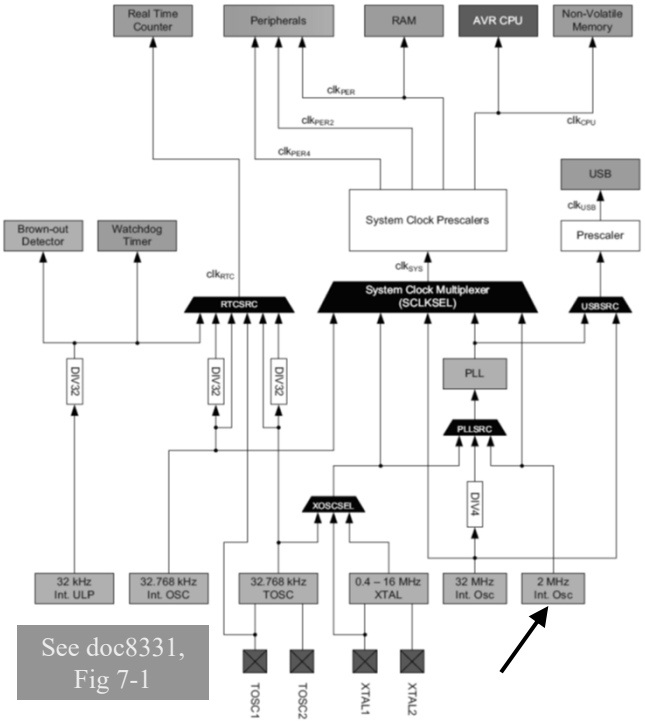
See examples on web-site:
doc8331 (section 7), ATxmega128a1udef.inc, lab3_s18_clock_timers_ebi.pdf



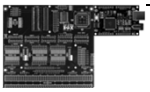
EEL 3

XMEGA Clock System

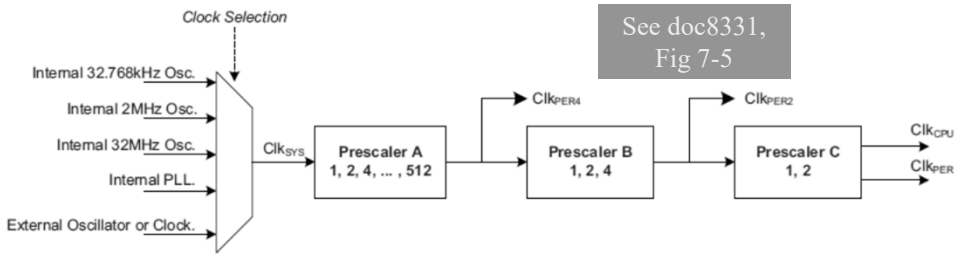
- Read doc8331, section 7



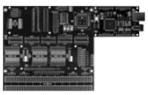
See doc8331, Fig 7-1



EEL 3744 System Clock Selection/Prescalers



- Internal **2 MHz** is the default on the XMEGA
- If want something else, usually set internal Osc to **32 MHz** and then use **Prescaler A**
  - >For 32 MHz, use the following values and registers
    - – OSC_RC32MEN_bm, OSC_CTRL, OSC_Status, OSC_RC32MRDY_bp, CCP_IOREG_gc, CPU_CCP, CLK_SCLKSEL_RC32M_gc, CLK_CTRL



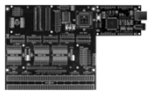
EEL 3744 Interrupts and Changing the System Clock

- You can not allow interrupts while changing the system clock source
  - >The Configuration Change Protection Register, CPU_CCP (see doc 8331, section 3.14.1), and the CCP_IOREG disable interrupts for a few clock cycles to give time to change the clock source

```
ldi  r16, CCP_IOREG_gc
sts CPU_CCP, r16
```

ATxmega128a1udef.inc

  - – `CCP_IOREG_gc` is an example of a group configuration value
    - ☞ You can find this (and similar) in the ATxmega128a1udef.inc file



EEL 3744

Changing the System Clock

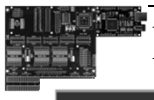
- Once the clock is set to 32 MHz, you can change the system clock by using CLK_PSCTRL along with CLK_PSADIV_x_gc, CLK_PSBCDIV_y_gc, where x is a power of 2 between 1 and 512 and y corresponds to a Prescaler B value B and Prescaler C value
  - >Both Prescaler B value B and Prescaler C are usually 1:

```
.equ CLK_PSBCDIV_1_1_gc = (0x00<<0)
       ; Divide B by 1 and C by 1
```

  - >For a Prescaler A value of 4 ATxmega128a1udef.inc

```
.equ CLK_PSADIV_4_gc = (0x03<<2) ; Divide by 4
```

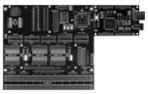
    - See doc8331, Table 7-2 (on next page)



EEL 3744 System Clock Prescaler A

PSADIV[4:0]	Group configuration	Description
00000	1	No division
00001	2	Divide by 2
00011	4	Divide by 4
00101	8	Divide by 8
00111	16	Divide by 16
01001	32	Divide by 32
01011	64	Divide by 64
01101	128	Divide by 128
01111	256	Divide by 256
10001	512	Divide by 512
10101		Reserved
10111		Reserved

See doc8331, Table 7-2



EEL 3744
Oscillator Control Register

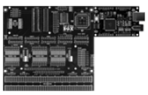
- **PLLEN**: PLL Enable
- **XOSCEN**: External Oscillator Enable
- **RC32KEN**: 32.768 kHz Internal Osc Enable
- **RC32MEN**: 32 MHz Internal Oscillator Enable
- **RC2MEN**: 2 MHz Internal Oscillator Enable
  >By default, the 2 MHz internal oscillator is enabled

See doc8331, Section 7.10.1

Normally use one of these

OSC_CTRL

7	6	5	4	3	2	1	0
–	–	–	PLLEN	XOSCEN	RC32KEN	RC32MEN	RC2MEN
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1



EEL 3744
Oscillator Status Register

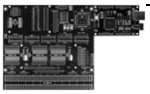
- Must assure that the OSC clock is ready before making changes
- **PLLRDY**: PLL Ready
- **XOSCRDY**: External Clock Source Ready
- **RC32KRDY**: 32.768 kHz Internal Osc Ready
- **RC32MEN**: 32 MHz Internal Oscillator Ready
- **RC2MEN**: 2 MHz Internal Oscillator Ready

See doc8331, Section 7.10.2

Normally use one of these

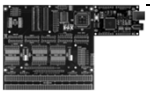
OSC_STATUS

7	6	5	4	3	2	1	0
–	–	–	PLLRDY	XOSCRDY	RC32KRDY	RC32MRDY	RC2MRDY
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0



EEL 3744 Steps in Setting the XMEGA Clock Source

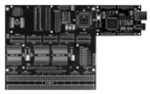
1. Enable the 32 MHz oscillator using OSC_CTRL register
2. Create a loop that waits until the 32 MHz osc. is ready:
   a) Read the OSC_STATUS register
   b) Poll the RC32MRDY flag until it is set (which signals that the 32 MHz oscillator is stable and ready)
3. Write the IOREG signature to the CPU_CCP register
   > This allows you to make changes to the CLK_CTRL register within the next 4 clock cycles
4. Immediately after writing to the CPU_CCP register, select the 32 MHz oscillator via the CLK_CTRL register
   > Now the board is running at 32 MHz



EEL 3744 Steps in Setting the XMEGA Clock Source

5. Next there is the option to divide the clock to lower frequencies. Use the CLK_PSCTRL register
   > See tables 7-2 and 7-3 in doc 8331
   > This register is protected by the CCP just like CLK_CTRL, so you must write the IOREG signature to the CPU_CCP register, and **THEN** write to the CLK_PSCTRL register with your desired clock division configuration

- **<u>Summarizing:</u>**
  1. Enable 32 MHz oscillator
  2. Wait for the oscillator to stabilize
  3. Select the 32 MHz oscillator as the new clock source
  4. Divide the clock, if needed


EEL 3744

The End!