Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Analog Comparator A	**Registers**			
	ACA_AC0CTRL	896	0x380	Analog Comparator 0 Control
	ACA_AC1CTRL	897	0x381	Analog Comparator 1 Control
	ACA_AC0MUXCTRL	898	0x382	Analog Comparator 0 MUX Control
	ACA_AC1MUXCTRL	899	0x383	Analog Comparator 1 MUX Control
	ACA_CTRLA	900	0x384	Control Register A
	ACA_CTRLB	901	0x385	Control Register B
	ACA_WINCTRL	902	0x386	Window Mode Control
	ACA_STATUS	903	0x387	Status
	Interrupt Vectors			
	ACA_AC0_vect	136	0x88	AC0 Interrupt
	ACA_AC1_vect	138	0x8A	AC1 Interrupt
	ACA_ACW_vect	140	0x8C	ACW Window Mode Interrupt
Analog Comparator B	**Registers**			
	ACB_AC0CTRL	912	0x390	Analog Comparator 0 Control
	ACB_AC1CTRL	913	0x391	Analog Comparator 1 Control
	ACB_AC0MUXCTRL	914	0x392	Analog Comparator 0 MUX Control
	ACB_AC1MUXCTRL	915	0x393	Analog Comparator 1 MUX Control
	ACB_CTRLA	916	0x394	Control Register A
	ACB_CTRLB	917	0x395	Control Register B
	ACB_WINCTRL	918	0x396	Window Mode Control
	ACB_STATUS	919	0x397	Status
	Interrupt Vectors			
	ACB_AC0_vect	72	0x48	AC0 Interrupt
	ACB_AC1_vect	74	0x4A	AC1 Interrupt
	ACB_ACW_vect	76	0x4C	ACW Window Mode Interrupt
	Registers			
	ADCA_CTRLA	512	0x200	Control Register A
	ADCA_CTRLB	513	0x201	Control Register B
	ADCA_REFCTRL	514	0x202	Reference Control
	ADCA_EVCTRL	515	0x203	Event Control
	ADCA_PRESCALER	516	0x204	Clock Prescaler
	ADCA_INTFLAGS	518	0x206	Interrupt Flags
	ADCA_TEMP	519	0x207	Temporary Register
	ADCA_CAL	524	0x20C	Calibration Value
	ADCA_CH0RES	528	0x210	Channel 0 Result
	ADCA_CH1RES	530	0x212	Channel 1 Result
	ADCA_CH2RES	532	0x214	Channel 2 Result
	ADCA_CH3RES	534	0x216	Channel 3 Result
	ADCA_CMP	536	0x218	Compare Value
	ADCA_CH0_CTRL	544	0x220	Control Register
	ADCA_CH0_MUXCTRL	545	0x221	MUX Control
	ADCA_CH0_INTCTRL	546	0x222	Channel Interrupt Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Analog to Digital Converter A	ADCA_CH0_INTFLAGS	547	0x223	Interrupt Flags
	ADCA_CH0_RES	548	0x224	Channel Result
	ADCA_CH0_SCAN	550	0x226	Input Channel Scan
	ADCA_CH1_CTRL	552	0x228	Control Register
	ADCA_CH1_MUXCTRL	553	0x229	MUX Control
	ADCA_CH1_INTCTRL	554	0x22A	Channel Interrupt Control Register
	ADCA_CH1_INTFLAGS	555	0x22B	Interrupt Flags
	ADCA_CH1_RES	556	0x22C	Channel Result
	ADCA_CH1_SCAN	558	0x22E	Input Channel Scan
	ADCA_CH2_CTRL	560	0x230	Control Register
	ADCA_CH2_MUXCTRL	561	0x231	MUX Control
	ADCA_CH2_INTCTRL	562	0x232	Channel Interrupt Control Register
	ADCA_CH2_INTFLAGS	563	0x233	Interrupt Flags
	ADCA_CH2_RES	564	0x234	Channel Result
	ADCA_CH2_SCAN	566	0x236	Input Channel Scan
	ADCA_CH3_CTRL	568	0x238	Control Register
	ADCA_CH3_MUXCTRL	569	0x239	MUX Control
	ADCA_CH3_INTCTRL	570	0x23A	Channel Interrupt Control Register
	ADCA_CH3_INTFLAGS	571	0x23B	Interrupt Flags
	ADCA_CH3_RES	572	0x23C	Channel Result
	ADCA_CH3_SCAN	574	0x23E	Input Channel Scan
	Interrupt Vectors			
	ADCA_CH0_vect	142	0x8E	Interrupt 0
	ADCA_CH1_vect	144	0x90	Interrupt 1
	ADCA_CH2_vect	146	0x92	Interrupt 2
	ADCA_CH3_vect	148	0x94	Interrupt 3
	Registers			
	ADCB_CTRLA	576	0x240	Control Register A
	ADCB_CTRLB	577	0x241	Control Register B
	ADCB_REFCTRL	578	0x242	Reference Control
	ADCB_EVCTRL	579	0x243	Event Control
	ADCB_PRESCALER	580	0x244	Clock Prescaler
	ADCB_INTFLAGS	582	0x246	Interrupt Flags
	ADCB_TEMP	583	0x247	Temporary Register
	ADCB_CAL	588	0x24C	Calibration Value
	ADCB_CH0RES	592	0x250	Channel 0 Result
	ADCB_CH1RES	594	0x252	Channel 1 Result
	ADCB_CH2RES	596	0x254	Channel 2 Result
	ADCB_CH3RES	598	0x256	Channel 3 Result
	ADCB_CMP	600	0x258	Compare Value
	ADCB_CH0_CTRL	608	0x260	Control Register
	ADCB_CH0_MUXCTRL	609	0x261	MUX Control
	ADCB_CH0_INTCTRL	610	0x262	Channel Interrupt Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Analog to Digital Converter B	ADCB_CH0_INTFLAGS	611	0x263	Interrupt Flags
	ADCB_CH0_RES	612	0x264	Channel Result
	ADCB_CH0_SCAN	614	0x266	Input Channel Scan
	ADCB_CH1_CTRL	616	0x268	Control Register
	ADCB_CH1_MUXCTRL	617	0x269	MUX Control
	ADCB_CH1_INTCTRL	618	0x26A	Channel Interrupt Control Register
	ADCB_CH1_INTFLAGS	619	0x26B	Interrupt Flags
	ADCB_CH1_RES	620	0x26C	Channel Result
	ADCB_CH1_SCAN	622	0x26E	Input Channel Scan
	ADCB_CH2_CTRL	624	0x270	Control Register
	ADCB_CH2_MUXCTRL	625	0x271	MUX Control
	ADCB_CH2_INTCTRL	626	0x272	Channel Interrupt Control Register
	ADCB_CH2_INTFLAGS	627	0x273	Interrupt Flags
	ADCB_CH2_RES	628	0x274	Channel Result
	ADCB_CH2_SCAN	630	0x276	Input Channel Scan
	ADCB_CH3_CTRL	632	0x278	Control Register
	ADCB_CH3_MUXCTRL	633	0x279	MUX Control
	ADCB_CH3_INTCTRL	634	0x27A	Channel Interrupt Control Register
	ADCB_CH3_INTFLAGS	635	0x27B	Interrupt Flags
	ADCB_CH3_RES	636	0x27C	Channel Result
	ADCB_CH3_SCAN	638	0x27E	Input Channel Scan
	Interrupt Vectors			
	ADCB_CH0_vect	78	0x4E	Interrupt 0
	ADCB_CH1_vect	80	0x50	Interrupt 1
	ADCB_CH2_vect	82	0x52	Interrupt 2
	ADCB_CH3_vect	84	0x54	Interrupt 3
Advanced Waveform Extension on Port C	**Registers**			
	AWEXC_CTRL	2176	0x880	Control Register
	AWEXC_FDEMASK	2178	0x882	Fault Detection Event Mask
	AWEXC_FDCTRL	2179	0x883	Fault Detection Control Register
	AWEXC_STATUS	2180	0x884	Status Register
	AWEXC_STATUSSET	2181	0x885	Status Set Register
	AWEXC_DTBOTH	2182	0x886	Dead Time Both Sides
	AWEXC_DTBOTHBUF	2183	0x887	Dead Time Both Sides Buffer
	AWEXC_DTLS	2184	0x888	Dead Time Low Side
	AWEXC_DTHS	2185	0x889	Dead Time High Side
	AWEXC_DTLSBUF	2186	0x88A	Dead Time Low Side Buffer
	AWEXC_DTHSBUF	2187	0x88B	Dead Time High Side Buffer
	AWEXC_OUTOVEN	2188	0x88C	Output Override Enable
n on Port E	**Registers**			
	AWEXE_CTRL	2688	0xA80	Control Register
	AWEXE_FDEMASK	2690	0xA82	Fault Detection Event Mask
	AWEXE_FDCTRL	2691	0xA83	Fault Detection Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Advanced Waveform Extensio	AWEXE_STATUS	2692	0xA84	Status Register
	AWEXE_STATUSSET	2693	0xA85	Status Set Register
	AWEXE_DTBOTH	2694	0xA86	Dead Time Both Sides
	AWEXE_DTBOTHBUF	2695	0xA87	Dead Time Both Sides Buffer
	AWEXE_DTLS	2696	0xA88	Dead Time Low Side
	AWEXE_DTHS	2697	0xA89	Dead Time High Side
	AWEXE_DTLSBUF	2698	0xA8A	Dead Time Low Side Buffer
	AWEXE_DTHSBUF	2699	0xA8B	Dead Time High Side Buffer
	AWEXE_OUTOVEN	2700	0xA8C	Output Override Enable
Cyclic Redundancy Check Generator	CRC_CTRL	208	0xD0	Control Register
	CRC_STATUS	209	0xD1	Status Register
	CRC_DATAIN	211	0xD3	Data Input
	CRC_CHECKSUM0	212	0xD4	Checksum byte 0
	CRC_CHECKSUM1	213	0xD5	Checksum byte 1
	CRC_CHECKSUM2	214	0xD6	Checksum byte 2
	CRC_CHECKSUM3	215	0xD7	Checksum byte 3
Clock System	**Registers**			
	CLK_CTRL	64	0x40	Control Register
	CLK_PSCTRL	65	0x41	Prescaler Control Register
	CLK_LOCK	66	0x42	Lock register
	CLK_RTCCTRL	67	0x43	RTC Control Register
	CLK_USBCTRL	68	0x44	USB Control Register
Digital Frequency Locked Loop (2MHz)	**Registers**			
	DFLLRC2M_CTRL	104	0x68	Control Register
	DFLLRC2M_CALA	106	0x6A	Calibration Register A
	DFLLRC2M_CALB	107	0x6B	Calibration Register B
	DFLLRC2M_COMP0	108	0x6C	Oscillator Compare Register 0
	DFLLRC2M_COMP1	109	0x6D	Oscillator Compare Register 1
	DFLLRC2M_COMP2	110	0x6E	Oscillator Compare Register 2
Digital Frequency Locked Loop (32MHz)	**Registers**			
	DFLLRC32M_CTRL	96	0x60	Control Register
	DFLLRC32M_CALA	98	0x62	Calibration Register A
	DFLLRC32M_CALB	99	0x63	Calibration Register B
	DFLLRC32M_COMP0	100	0x64	Oscillator Compare Register 0
	DFLLRC32M_COMP1	101	0x65	Oscillator Compare Register 1
	DFLLRC32M_COMP2	102	0x66	Oscillator Compare Register 2
CPU Registers	**Registers**			
	CPU_CCP	52	0x34	Configuration Change Protection
	CPU_RAMPD	56	0x38	Ramp D
	CPU_RAMPX	57	0x39	Ramp X
	CPU_RAMPY	58	0x3A	Ramp Y
	CPU_RAMPZ	59	0x3B	Ramp Z
	CPU_EIND	60	0x3C	Extended Indirect Jump

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	CPU_SPL	61	0x3D	Stack Pointer Low
	CPU_SPH	62	0x3E	Stack Pointer High
	CPU_SREG	63	0x3F	Status Register
Digital to Analog Converter A	**Registers**			
	DACA_CTRLA	768	0x300	Control Register A
	DACA_CTRLB	769	0x301	Control Register B
	DACA_CTRLC	770	0x302	Control Register C
	DACA_EVCTRL	771	0x303	Event Input Control
	DACA_TIMCTRL	772	0x304	Timing Control
	DACA_STATUS	773	0x305	Status
	DACA_CH0GAINCAL	776	0x308	Gain Calibration
	DACA_CH0OFFSETCAL	777	0x309	Offset Calibration
	DACA_CH1GAINCAL	778	0x30A	Gain Calibration
	DACA_CH1OFFSETCAL	779	0x30B	Offset Calibration
	DACA_CH0DATA	792	0x318	Channel 0 Data
	DACA_CH1DATA	794	0x31A	Channel 1 Data
Digital to Analog Converter B	**Registers**			
	DACB_CTRLA	800	0x320	Control Register A
	DACB_CTRLB	801	0x321	Control Register B
	DACB_CTRLC	802	0x322	Control Register C
	DACB_EVCTRL	803	0x323	Event Input Control
	DACB_TIMCTRL	804	0x324	Timing Control
	DACB_STATUS	805	0x325	Status
	DACB_CH0GAINCAL	808	0x328	Gain Calibration
	DACB_CH0OFFSETCAL	809	0x329	Offset Calibration
	DACB_CH1GAINCAL	810	0x32A	Gain Calibration
	DACB_CH1OFFSETCAL	811	0x32B	Offset Calibration
	DACB_CH0DATA	824	0x338	Channel 0 Data
	DACB_CH1DATA	826	0x33A	Channel 1 Data
	Registers			
	DMA_CTRL	256	0x100	Control
	DMA_INTFLAGS	259	0x103	Transfer Interrupt Status
	DMA_STATUS	260	0x104	Status
	DMA_TEMP	262	0x106	Temporary Register For 1624-bit Access
	DMA_CH0_CTRLA	272	0x110	Channel Control
	DMA_CH0_CTRLB	273	0x111	Channel Control
	DMA_CH0_ADDRCTRL	274	0x112	Address Control
	DMA_CH0_TRIGSRC	275	0x113	Channel Trigger Source
	DMA_CH0_TRFCNT	276	0x114	Channel Block Transfer Count
	DMA_CH0_REPCNT	278	0x116	Channel Repeat Count
	DMA_CH0_SRCADDR0	280	0x118	Channel Source Address 0
	DMA_CH0_SRCADDR1	281	0x119	Channel Source Address 1
	DMA_CH0_SRCADDR2	282	0x11A	Channel Source Address 2

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
DMA Controller	DMA_CH0_DESTADDR0	284	0x11C	Channel Destination Address 0
	DMA_CH0_DESTADDR1	285	0x11D	Channel Destination Address 1
	DMA_CH0_DESTADDR2	286	0x11E	Channel Destination Address 2
	DMA_CH1_CTRLA	288	0x120	Channel Control
	DMA_CH1_CTRLB	289	0x121	Channel Control
	DMA_CH1_ADDRCTRL	290	0x122	Address Control
	DMA_CH1_TRIGSRC	291	0x123	Channel Trigger Source
	DMA_CH1_TRFCNT	292	0x124	Channel Block Transfer Count
	DMA_CH1_REPCNT	294	0x126	Channel Repeat Count
	DMA_CH1_SRCADDR0	296	0x128	Channel Source Address 0
	DMA_CH1_SRCADDR1	297	0x129	Channel Source Address 1
	DMA_CH1_SRCADDR2	298	0x12A	Channel Source Address 2
	DMA_CH1_DESTADDR0	300	0x12C	Channel Destination Address 0
	DMA_CH1_DESTADDR1	301	0x12D	Channel Destination Address 1
	DMA_CH1_DESTADDR2	302	0x12E	Channel Destination Address 2
	DMA_CH2_CTRLA	304	0x130	Channel Control
	DMA_CH2_CTRLB	305	0x131	Channel Control
	DMA_CH2_ADDRCTRL	306	0x132	Address Control
	DMA_CH2_TRIGSRC	307	0x133	Channel Trigger Source
	DMA_CH2_TRFCNT	308	0x134	Channel Block Transfer Count
	DMA_CH2_REPCNT	310	0x136	Channel Repeat Count
	DMA_CH2_SRCADDR0	312	0x138	Channel Source Address 0
	DMA_CH2_SRCADDR1	313	0x139	Channel Source Address 1
	DMA_CH2_SRCADDR2	314	0x13A	Channel Source Address 2
	DMA_CH2_DESTADDR0	316	0x13C	Channel Destination Address 0
	DMA_CH2_DESTADDR1	317	0x13D	Channel Destination Address 1
	DMA_CH2_DESTADDR2	318	0x13E	Channel Destination Address 2
	DMA_CH3_CTRLA	320	0x140	Channel Control
	DMA_CH3_CTRLB	321	0x141	Channel Control
	DMA_CH3_ADDRCTRL	322	0x142	Address Control
	DMA_CH3_TRIGSRC	323	0x143	Channel Trigger Source
	DMA_CH3_TRFCNT	324	0x144	Channel Block Transfer Count
	DMA_CH3_REPCNT	326	0x146	Channel Repeat Count
	DMA_CH3_SRCADDR0	328	0x148	Channel Source Address 0
	DMA_CH3_SRCADDR1	329	0x149	Channel Source Address 1
	DMA_CH3_SRCADDR2	330	0x14A	Channel Source Address 2
	DMA_CH3_DESTADDR0	332	0x14C	Channel Destination Address 0
	DMA_CH3_DESTADDR1	333	0x14D	Channel Destination Address 1
	DMA_CH3_DESTADDR2	334	0x14E	Channel Destination Address 2
	Interrupt Vectors			
	DMA_CH0_vect	12	0xC	Channel 0 Interrupt
	DMA_CH1_vect	14	0xE	Channel 1 Interrupt
	DMA_CH2_vect	16	0x10	Channel 2 Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	DMA_CH3_vect	18	0x12	Channel 3 Interrupt
Event System	**Registers**			
	EVSYS_CH0MUX	384	0x180	Event Channel 0 Multiplexer
	EVSYS_CH1MUX	385	0x181	Event Channel 1 Multiplexer
	EVSYS_CH2MUX	386	0x182	Event Channel 2 Multiplexer
	EVSYS_CH3MUX	387	0x183	Event Channel 3 Multiplexer
	EVSYS_CH4MUX	388	0x184	Event Channel 4 Multiplexer
	EVSYS_CH5MUX	389	0x185	Event Channel 5 Multiplexer
	EVSYS_CH6MUX	390	0x186	Event Channel 6 Multiplexer
	EVSYS_CH7MUX	391	0x187	Event Channel 7 Multiplexer
	EVSYS_CH0CTRL	392	0x188	Channel 0 Control Register
	EVSYS_CH1CTRL	393	0x189	Channel 1 Control Register
	EVSYS_CH2CTRL	394	0x18A	Channel 2 Control Register
	EVSYS_CH3CTRL	395	0x18B	Channel 3 Control Register
	EVSYS_CH4CTRL	396	0x18C	Channel 4 Control Register
	EVSYS_CH5CTRL	397	0x18D	Channel 5 Control Register
	EVSYS_CH6CTRL	398	0x18E	Channel 6 Control Register
	EVSYS_CH7CTRL	399	0x18F	Channel 7 Control Register
	EVSYS_STROBE	400	0x190	Event Strobe
	EVSYS_DATA	401	0x191	Event Data
External Bus Interface (EBI)	**Registers**			
	EBI_CTRL	1088	0x440	Control
	EBI_SDRAMCTRLA	1089	0x441	SDRAM Control Register A
	EBI_REFRESH	1092	0x444	SDRAM Refresh Period
	EBI_INITDLY	1094	0x446	SDRAM Initialization Delay
	EBI_SDRAMCTRLB	1096	0x448	SDRAM Control Register B
	EBI_SDRAMCTRLC	1097	0x449	SDRAM Control Register C
	EBI_CS0_CTRLA	1104	0x450	Chip Select Control Register A
	EBI_CS0_CTRLB	1105	0x451	Chip Select Control Register B
	EBI_CS0_BASEADDR	1106	0x452	Chip Select Base Address
	EBI_CS1_CTRLA	1108	0x454	Chip Select Control Register A
	EBI_CS1_CTRLB	1109	0x455	Chip Select Control Register B
	EBI_CS1_BASEADDR	1110	0x456	Chip Select Base Address
	EBI_CS2_CTRLA	1112	0x458	Chip Select Control Register A
	EBI_CS2_CTRLB	1113	0x459	Chip Select Control Register B
	EBI_CS2_BASEADDR	1114	0x45A	Chip Select Base Address
	EBI_CS3_CTRLA	1116	0x45C	Chip Select Control Register A
	EBI_CS3_CTRLB	1117	0x45D	Chip Select Control Register B
	EBI_CS3_BASEADDR	1118	0x45E	Chip Select Base Address
gh Resolution Extension	**Registers**			
	HIRESC_CTRLA	2192	0x890	Control Register
	HIRESD_CTRLA	2448	0x990	Control Register
	HIRESE_CTRLA	2704	0xA90	Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Hi	HIRESF_CTRLA	2960	0xB90	Control Register
IR Com. Module	**Registers**			
	IRCOM_CTRL	2296	0x8F8	Control Register
	IRCOM_TXPLCTRL	2297	0x8F9	IrDA Transmitter Pulse Length Control Register
	IRCOM_RXPLCTRL	2298	0x8FA	IrDA Receiver Pulse Length Control Register
MCU Control	**Registers**			
	MCU_DEVID0	144	0x90	Device ID byte 0
	MCU_DEVID1	145	0x91	Device ID byte 1
	MCU_DEVID2	146	0x92	Device ID byte 2
	MCU_REVID	147	0x93	Revision ID
	MCU_JTAGUID	148	0x94	JTAG User ID
	MCU_MCUCR	150	0x96	MCU Control
	MCU_ANAINIT	151	0x97	Analog Startup Delay
	MCU_EVSYSLOCK	152	0x98	Event System Lock
	MCU_AWEXLOCK	153	0x99	AWEX Lock
Non-Volatile Memory	**Registers**			
	NVM_ADDR0	448	0x1C0	Address Register 0
	NVM_ADDR1	449	0x1C1	Address Register 1
	NVM_ADDR2	450	0x1C2	Address Register 2
	NVM_DATA0	452	0x1C4	Data Register 0
	NVM_DATA1	453	0x1C5	Data Register 1
	NVM_DATA2	454	0x1C6	Data Register 2
	NVM_CMD	458	0x1CA	Command
	NVM_CTRLA	459	0x1CB	Control Register A
	NVM_CTRLB	460	0x1CC	Control Register B
	NVM_INTCTRL	461	0x1CD	Interrupt Control
	NVM_STATUS	463	0x1CF	Status
	NVM_LOCKBITS	464	0x1D0	Lock Bits
	Interrupt Vectors			
	NVM_EE_vect	64	0x40	EE Interrupt
	NVM_SPM_vect	66	0x42	SPM Interrupt
Oscillator Control	**Registers**			
	OSC_CTRL	80	0x50	Control Register
	OSC_STATUS	81	0x51	Status Register
	OSC_XOSCCTRL	82	0x52	External Oscillator Control Register
	OSC_XOSCFAIL	83	0x53	Oscillator Failure Detection Register
	OSC_RC32KCAL	84	0x54	32.768 kHz Internal Oscillator Calibration Register
	OSC_PLLCTRL	85	0x55	PLL Control Register
	OSC_DFLLCTRL	86	0x56	DFLL Control Register
	Interrupt Vectors			
	OSC_OSCF_vect	2	0x2	Oscillator Failure Interrupt (NMI)
on	**Registers**			

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Port Configuratio	PORTCFG_MPCMASK	176	0xB0	Multi-pin Configuration Mask
	PORTCFG_VPCTRLA	178	0xB2	Virtual Port Control Register A
	PORTCFG_VPCTRLB	179	0xB3	Virtual Port Control Register B
	PORTCFG_CLKEVOUT	180	0xB4	Clock and Event Out Register
	PORTCFG_EVOUTSEL	182	0xB6	Event Output Select
PORT A	**Registers**			
	PORTA_DIR	1536	0x600	IO Port Data Direction
	PORTA_DIRSET	1537	0x601	IO Port Data Direction Set
	PORTA_DIRCLR	1538	0x602	IO Port Data Direction Clear
	PORTA_DIRTGL	1539	0x603	IO Port Data Direction Toggle
	PORTA_OUT	1540	0x604	IO Port Output
	PORTA_OUTSET	1541	0x605	IO Port Output Set
	PORTA_OUTCLR	1542	0x606	IO Port Output Clear
	PORTA_OUTTGL	1543	0x607	IO Port Output Toggle
	PORTA_IN	1544	0x608	IO port Input
	PORTA_INTCTRL	1545	0x609	Interrupt Control Register
	PORTA_INT0MASK	1546	0x60A	Port Interrupt 0 Mask
	PORTA_INT1MASK	1547	0x60B	Port Interrupt 1 Mask
	PORTA_INTFLAGS	1548	0x60C	Interrupt Flag Register
	PORTA_REMAP	1550	0x60E	IO Port Pin Remap Register
	PORTA_PIN0CTRL	1552	0x610	Pin 0 Control Register
	PORTA_PIN1CTRL	1553	0x611	Pin 1 Control Register
	PORTA_PIN2CTRL	1554	0x612	Pin 2 Control Register
	PORTA_PIN3CTRL	1555	0x613	Pin 3 Control Register
	PORTA_PIN4CTRL	1556	0x614	Pin 4 Control Register
	PORTA_PIN5CTRL	1557	0x615	Pin 5 Control Register
	PORTA_PIN6CTRL	1558	0x616	Pin 6 Control Register
	PORTA_PIN7CTRL	1559	0x617	Pin 7 Control Register
	Interrupt Vectors			
	PORTA_INT0_vect	132	0x84	External Interrupt 0
	PORTA_INT1_vect	134	0x86	External Interrupt 1
	Registers			
	PORTB_DIR	1568	0x620	IO Port Data Direction
	PORTB_DIRSET	1569	0x621	IO Port Data Direction Set
	PORTB_DIRCLR	1570	0x622	IO Port Data Direction Clear
	PORTB_DIRTGL	1571	0x623	IO Port Data Direction Toggle
	PORTB_OUT	1572	0x624	IO Port Output
	PORTB_OUTSET	1573	0x625	IO Port Output Set
	PORTB_OUTCLR	1574	0x626	IO Port Output Clear
	PORTB_OUTTGL	1575	0x627	IO Port Output Toggle
	PORTB_IN	1576	0x628	IO port Input
	PORTB_INTCTRL	1577	0x629	Interrupt Control Register
	PORTB_INT0MASK	1578	0x62A	Port Interrupt 0 Mask

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
PORT B	PORTB_INT1MASK	1579	0x62B	Port Interrupt 1 Mask
	PORTB_INTFLAGS	1580	0x62C	Interrupt Flag Register
	PORTB_REMAP	1582	0x62E	IO Port Pin Remap Register
	PORTB_PIN0CTRL	1584	0x630	Pin 0 Control Register
	PORTB_PIN1CTRL	1585	0x631	Pin 1 Control Register
	PORTB_PIN2CTRL	1586	0x632	Pin 2 Control Register
	PORTB_PIN3CTRL	1587	0x633	Pin 3 Control Register
	PORTB_PIN4CTRL	1588	0x634	Pin 4 Control Register
	PORTB_PIN5CTRL	1589	0x635	Pin 5 Control Register
	PORTB_PIN6CTRL	1590	0x636	Pin 6 Control Register
	PORTB_PIN7CTRL	1591	0x637	Pin 7 Control Register
	Interrupt Vectors			
	PORTB_INT0_vect	68	0x44	External Interrupt 0
	PORTB_INT1_vect	70	0x46	External Interrupt 1
PORT C	**Registers**			
	PORTC_DIR	1600	0x640	IO Port Data Direction
	PORTC_DIRSET	1601	0x641	IO Port Data Direction Set
	PORTC_DIRCLR	1602	0x642	IO Port Data Direction Clear
	PORTC_DIRTGL	1603	0x643	IO Port Data Direction Toggle
	PORTC_OUT	1604	0x644	IO Port Output
	PORTC_OUTSET	1605	0x645	IO Port Output Set
	PORTC_OUTCLR	1606	0x646	IO Port Output Clear
	PORTC_OUTTGL	1607	0x647	IO Port Output Toggle
	PORTC_IN	1608	0x648	IO port Input
	PORTC_INTCTRL	1609	0x649	Interrupt Control Register
	PORTC_INT0MASK	1610	0x64A	Port Interrupt 0 Mask
	PORTC_INT1MASK	1611	0x64B	Port Interrupt 1 Mask
	PORTC_INTFLAGS	1612	0x64C	Interrupt Flag Register
	PORTC_REMAP	1614	0x64E	IO Port Pin Remap Register
	PORTC_PIN0CTRL	1616	0x650	Pin 0 Control Register
	PORTC_PIN1CTRL	1617	0x651	Pin 1 Control Register
	PORTC_PIN2CTRL	1618	0x652	Pin 2 Control Register
	PORTC_PIN3CTRL	1619	0x653	Pin 3 Control Register
	PORTC_PIN4CTRL	1620	0x654	Pin 4 Control Register
	PORTC_PIN5CTRL	1621	0x655	Pin 5 Control Register
	PORTC_PIN6CTRL	1622	0x656	Pin 6 Control Register
	PORTC_PIN7CTRL	1623	0x657	Pin 7 Control Register
	Interrupt Vectors			
	PORTC_INT0_vect	4	0x4	External Interrupt 0
	PORTC_INT1_vect	6	0x6	External Interrupt 1
	Registers			
	PORTD_DIR	1632	0x660	IO Port Data Direction
	PORTD_DIRSET	1633	0x661	IO Port Data Direction Set

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
PORT D	PORTD_DIRCLR	1634	0x662	IO Port Data Direction Clear
	PORTD_DIRTGL	1635	0x663	IO Port Data Direction Toggle
	PORTD_OUT	1636	0x664	IO Port Output
	PORTD_OUTSET	1637	0x665	IO Port Output Set
	PORTD_OUTCLR	1638	0x666	IO Port Output Clear
	PORTD_OUTTGL	1639	0x667	IO Port Output Toggle
	PORTD_IN	1640	0x668	IO port Input
	PORTD_INTCTRL	1641	0x669	Interrupt Control Register
	PORTD_INT0MASK	1642	0x66A	Port Interrupt 0 Mask
	PORTD_INT1MASK	1643	0x66B	Port Interrupt 1 Mask
	PORTD_INTFLAGS	1644	0x66C	Interrupt Flag Register
	PORTD_REMAP	1646	0x66E	IO Port Pin Remap Register
	PORTD_PIN0CTRL	1648	0x670	Pin 0 Control Register
	PORTD_PIN1CTRL	1649	0x671	Pin 1 Control Register
	PORTD_PIN2CTRL	1650	0x672	Pin 2 Control Register
	PORTD_PIN3CTRL	1651	0x673	Pin 3 Control Register
	PORTD_PIN4CTRL	1652	0x674	Pin 4 Control Register
	PORTD_PIN5CTRL	1653	0x675	Pin 5 Control Register
	PORTD_PIN6CTRL	1654	0x676	Pin 6 Control Register
	PORTD_PIN7CTRL	1655	0x677	Pin 7 Control Register
	Interrupt Vectors			
	PORTD_INT0_vect	128	0x80	External Interrupt 0
	PORTD_INT1_vect	130	0x82	External Interrupt 1
PORT E	**Registers**			
	PORTE_DIR	1664	0x680	IO Port Data Direction
	PORTE_DIRSET	1665	0x681	IO Port Data Direction Set
	PORTE_DIRCLR	1666	0x682	IO Port Data Direction Clear
	PORTE_DIRTGL	1667	0x683	IO Port Data Direction Toggle
	PORTE_OUT	1668	0x684	IO Port Output
	PORTE_OUTSET	1669	0x685	IO Port Output Set
	PORTE_OUTCLR	1670	0x686	IO Port Output Clear
	PORTE_OUTTGL	1671	0x687	IO Port Output Toggle
	PORTE_IN	1672	0x688	IO port Input
	PORTE_INTCTRL	1673	0x689	Interrupt Control Register
	PORTE_INT0MASK	1674	0x68A	Port Interrupt 0 Mask
	PORTE_INT1MASK	1675	0x68B	Port Interrupt 1 Mask
	PORTE_INTFLAGS	1676	0x68C	Interrupt Flag Register
	PORTE_REMAP	1678	0x68E	IO Port Pin Remap Register
	PORTE_PIN0CTRL	1680	0x690	Pin 0 Control Register
	PORTE_PIN1CTRL	1681	0x691	Pin 1 Control Register
	PORTE_PIN2CTRL	1682	0x692	Pin 2 Control Register
	PORTE_PIN3CTRL	1683	0x693	Pin 3 Control Register
	PORTE_PIN4CTRL	1684	0x694	Pin 4 Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	PORTE_PIN5CTRL	1685	0x695	Pin 5 Control Register
	PORTE_PIN6CTRL	1686	0x696	Pin 6 Control Register
	PORTE_PIN7CTRL	1687	0x697	Pin 7 Control Register
	Interrupt Vectors			
	PORTE_INT0_vect	86	0x56	External Interrupt 0
	PORTE_INT1_vect	88	0x58	External Interrupt 1
PORT F	**Registers**			
	PORTF_DIR	1696	0x6A0	IO Port Data Direction
	PORTF_DIRSET	1697	0x6A1	IO Port Data Direction Set
	PORTF_DIRCLR	1698	0x6A2	IO Port Data Direction Clear
	PORTF_DIRTGL	1699	0x6A3	IO Port Data Direction Toggle
	PORTF_OUT	1700	0x6A4	IO Port Output
	PORTF_OUTSET	1701	0x6A5	IO Port Output Set
	PORTF_OUTCLR	1702	0x6A6	IO Port Output Clear
	PORTF_OUTTGL	1703	0x6A7	IO Port Output Toggle
	PORTF_IN	1704	0x6A8	IO port Input
	PORTF_INTCTRL	1705	0x6A9	Interrupt Control Register
	PORTF_INT0MASK	1706	0x6AA	Port Interrupt 0 Mask
	PORTF_INT1MASK	1707	0x6AB	Port Interrupt 1 Mask
	PORTF_INTFLAGS	1708	0x6AC	Interrupt Flag Register
	PORTF_REMAP	1710	0x6AE	IO Port Pin Remap Register
	PORTF_PIN0CTRL	1712	0x6B0	Pin 0 Control Register
	PORTF_PIN1CTRL	1713	0x6B1	Pin 1 Control Register
	PORTF_PIN2CTRL	1714	0x6B2	Pin 2 Control Register
	PORTF_PIN3CTRL	1715	0x6B3	Pin 3 Control Register
	PORTF_PIN4CTRL	1716	0x6B4	Pin 4 Control Register
	PORTF_PIN5CTRL	1717	0x6B5	Pin 5 Control Register
	PORTF_PIN6CTRL	1718	0x6B6	Pin 6 Control Register
	PORTF_PIN7CTRL	1719	0x6B7	Pin 7 Control Register
	Interrupt Vectors			
	PORTF_INT0_vect	208	0xD0	External Interrupt 0
	PORTF_INT1_vect	210	0xD2	External Interrupt 1
	Registers			
	PORTH_DIR	1760	0x6E0	IO Port Data Direction
	PORTH_DIRSET	1761	0x6E1	IO Port Data Direction Set
	PORTH_DIRCLR	1762	0x6E2	IO Port Data Direction Clear
	PORTH_DIRTGL	1763	0x6E3	IO Port Data Direction Toggle
	PORTH_OUT	1764	0x6E4	IO Port Output
	PORTH_OUTSET	1765	0x6E5	IO Port Output Set
	PORTH_OUTCLR	1766	0x6E6	IO Port Output Clear
	PORTH_OUTTGL	1767	0x6E7	IO Port Output Toggle
	PORTH_IN	1768	0x6E8	IO port Input
	PORTH_INTCTRL	1769	0x6E9	Interrupt Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
PORT H	PORTH_INT0MASK	1770	0x6EA	Port Interrupt 0 Mask
	PORTH_INT1MASK	1771	0x6EB	Port Interrupt 1 Mask
	PORTH_INTFLAGS	1772	0x6EC	Interrupt Flag Register
	PORTH_REMAP	1774	0x6EE	IO Port Pin Remap Register
	PORTH_PIN0CTRL	1776	0x6F0	Pin 0 Control Register
	PORTH_PIN1CTRL	1777	0x6F1	Pin 1 Control Register
	PORTH_PIN2CTRL	1778	0x6F2	Pin 2 Control Register
	PORTH_PIN3CTRL	1779	0x6F3	Pin 3 Control Register
	PORTH_PIN4CTRL	1780	0x6F4	Pin 4 Control Register
	PORTH_PIN5CTRL	1781	0x6F5	Pin 5 Control Register
	PORTH_PIN6CTRL	1782	0x6F6	Pin 6 Control Register
	PORTH_PIN7CTRL	1783	0x6F7	Pin 7 Control Register
	Interrupt Vectors			
	PORTH_INT0_vect	192	0xC0	External Interrupt 0
	PORTH_INT1_vect	194	0xC2	External Interrupt 1
PORT J	**Registers**			
	PORTJ_DIR	1792	0x700	IO Port Data Direction
	PORTJ_DIRSET	1793	0x701	IO Port Data Direction Set
	PORTJ_DIRCLR	1794	0x702	IO Port Data Direction Clear
	PORTJ_DIRTGL	1795	0x703	IO Port Data Direction Toggle
	PORTJ_OUT	1796	0x704	IO Port Output
	PORTJ_OUTSET	1797	0x705	IO Port Output Set
	PORTJ_OUTCLR	1798	0x706	IO Port Output Clear
	PORTJ_OUTTGL	1799	0x707	IO Port Output Toggle
	PORTJ_IN	1800	0x708	IO port Input
	PORTJ_INTCTRL	1801	0x709	Interrupt Control Register
	PORTJ_INT0MASK	1802	0x70A	Port Interrupt 0 Mask
	PORTJ_INT1MASK	1803	0x70B	Port Interrupt 1 Mask
	PORTJ_INTFLAGS	1804	0x70C	Interrupt Flag Register
	PORTJ_REMAP	1806	0x70E	IO Port Pin Remap Register
	PORTJ_PIN0CTRL	1808	0x710	Pin 0 Control Register
	PORTJ_PIN1CTRL	1809	0x711	Pin 1 Control Register
	PORTJ_PIN2CTRL	1810	0x712	Pin 2 Control Register
	PORTJ_PIN3CTRL	1811	0x713	Pin 3 Control Register
	PORTJ_PIN4CTRL	1812	0x714	Pin 4 Control Register
	PORTJ_PIN5CTRL	1813	0x715	Pin 5 Control Register
	PORTJ_PIN6CTRL	1814	0x716	Pin 6 Control Register
	PORTJ_PIN7CTRL	1815	0x717	Pin 7 Control Register
	Interrupt Vectors			
	PORTJ_INT0_vect	196	0xC4	External Interrupt 0
	PORTJ_INT1_vect	198	0xC6	External Interrupt 1
	Registers			
	PORTK_DIR	1824	0x720	IO Port Data Direction

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
PORT K	PORTK_DIRSET	1825	0x721	IO Port Data Direction Set
	PORTK_DIRCLR	1826	0x722	IO Port Data Direction Clear
	PORTK_DIRTGL	1827	0x723	IO Port Data Direction Toggle
	PORTK_OUT	1828	0x724	IO Port Output
	PORTK_OUTSET	1829	0x725	IO Port Output Set
	PORTK_OUTCLR	1830	0x726	IO Port Output Clear
	PORTK_OUTTGL	1831	0x727	IO Port Output Toggle
	PORTK_IN	1832	0x728	IO port Input
	PORTK_INTCTRL	1833	0x729	Interrupt Control Register
	PORTK_INT0MASK	1834	0x72A	Port Interrupt 0 Mask
	PORTK_INT1MASK	1835	0x72B	Port Interrupt 1 Mask
	PORTK_INTFLAGS	1836	0x72C	Interrupt Flag Register
	PORTK_REMAP	1838	0x72E	IO Port Pin Remap Register
	PORTK_PIN0CTRL	1840	0x730	Pin 0 Control Register
	PORTK_PIN1CTRL	1841	0x731	Pin 1 Control Register
	PORTK_PIN2CTRL	1842	0x732	Pin 2 Control Register
	PORTK_PIN3CTRL	1843	0x733	Pin 3 Control Register
	PORTK_PIN4CTRL	1844	0x734	Pin 4 Control Register
	PORTK_PIN5CTRL	1845	0x735	Pin 5 Control Register
	PORTK_PIN6CTRL	1846	0x736	Pin 6 Control Register
	PORTK_PIN7CTRL	1847	0x737	Pin 7 Control Register
	Interrupt Vectors			
	PORTK_INT0_vect	200	0xC8	External Interrupt 0
	PORTK_INT1_vect	202	0xCA	External Interrupt 1
PORT Q	**Registers**			
	PORTQ_DIR	1984	0x7C0	IO Port Data Direction
	PORTQ_DIRSET	1985	0x7C1	IO Port Data Direction Set
	PORTQ_DIRCLR	1986	0x7C2	IO Port Data Direction Clear
	PORTQ_DIRTGL	1987	0x7C3	IO Port Data Direction Toggle
	PORTQ_OUT	1988	0x7C4	IO Port Output
	PORTQ_OUTSET	1989	0x7C5	IO Port Output Set
	PORTQ_OUTCLR	1990	0x7C6	IO Port Output Clear
	PORTQ_OUTTGL	1991	0x7C7	IO Port Output Toggle
	PORTQ_IN	1992	0x7C8	IO port Input
	PORTQ_INTCTRL	1993	0x7C9	Interrupt Control Register
	PORTQ_INT0MASK	1994	0x7CA	Port Interrupt 0 Mask
	PORTQ_INT1MASK	1995	0x7CB	Port Interrupt 1 Mask
	PORTQ_INTFLAGS	1996	0x7CC	Interrupt Flag Register
	PORTQ_REMAP	1998	0x7CE	IO Port Pin Remap Register
	PORTQ_PIN0CTRL	2000	0x7D0	Pin 0 Control Register
	PORTQ_PIN1CTRL	2001	0x7D1	Pin 1 Control Register
	PORTQ_PIN2CTRL	2002	0x7D2	Pin 2 Control Register
	PORTQ_PIN3CTRL	2003	0x7D3	Pin 3 Control Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	PORTQ_PIN4CTRL	2004	0x7D4	Pin 4 Control Register
	PORTQ_PIN5CTRL	2005	0x7D5	Pin 5 Control Register
	PORTQ_PIN6CTRL	2006	0x7D6	Pin 6 Control Register
	PORTQ_PIN7CTRL	2007	0x7D7	Pin 7 Control Register
	Interrupt Vectors			
	PORTQ_INT0_vect	188	0xBC	External Interrupt 0
	PORTQ_INT1_vect	190	0xBE	External Interrupt 1
PORT R	**Registers**			
	PORTR_DIR	2016	0x7E0	IO Port Data Direction
	PORTR_DIRSET	2017	0x7E1	IO Port Data Direction Set
	PORTR_DIRCLR	2018	0x7E2	IO Port Data Direction Clear
	PORTR_DIRTGL	2019	0x7E3	IO Port Data Direction Toggle
	PORTR_OUT	2020	0x7E4	IO Port Output
	PORTR_OUTSET	2021	0x7E5	IO Port Output Set
	PORTR_OUTCLR	2022	0x7E6	IO Port Output Clear
	PORTR_OUTTGL	2023	0x7E7	IO Port Output Toggle
	PORTR_IN	2024	0x7E8	IO port Input
	PORTR_INTCTRL	2025	0x7E9	Interrupt Control Register
	PORTR_INT0MASK	2026	0x7EA	Port Interrupt 0 Mask
	PORTR_INT1MASK	2027	0x7EB	Port Interrupt 1 Mask
	PORTR_INTFLAGS	2028	0x7EC	Interrupt Flag Register
	PORTR_REMAP	2030	0x7EE	IO Port Pin Remap Register
	PORTR_PIN0CTRL	2032	0x7F0	Pin 0 Control Register
	PORTR_PIN1CTRL	2033	0x7F1	Pin 1 Control Register
	PORTR_PIN2CTRL	2034	0x7F2	Pin 2 Control Register
	PORTR_PIN3CTRL	2035	0x7F3	Pin 3 Control Register
	PORTR_PIN4CTRL	2036	0x7F4	Pin 4 Control Register
	PORTR_PIN5CTRL	2037	0x7F5	Pin 5 Control Register
	PORTR_PIN6CTRL	2038	0x7F6	Pin 6 Control Register
	PORTR_PIN7CTRL	2039	0x7F7	Pin 7 Control Register
	Interrupt Vectors			
	PORTR_INT0_vect	8	0x8	External Interrupt 0
	PORTR_INT1_vect	10	0xA	External Interrupt 1
PMIC	**Registers**			
	PMIC_STATUS	160	0xA0	Status Register
	PMIC_INTPRI	161	0xA1	Interrupt Priority
	PMIC_CTRL	162	0xA2	Control Register
Power Reduction	**Registers**			
	PR_PRGEN	112	0x70	General Power Reduction
	PR_PRPA	113	0x71	Power Reduction Port A
	PR_PRPB	114	0x72	Power Reduction Port B
	PR_PRPC	115	0x73	Power Reduction Port C
	PR_PRPD	116	0x74	Power Reduction Port D

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
F	PR_PRPE	117	0x75	Power Reduction Port E
	PR_PRPF	118	0x76	Power Reduction Port F
Reset Cont.				**Registers**
	RST_STATUS	120	0x78	Status Register
	RST_CTRL	121	0x79	Control Register
Real Time Clock				**Registers**
	RTC_CTRL	1024	0x400	Control Register
	RTC_STATUS	1025	0x401	Status Register
	RTC_INTCTRL	1026	0x402	Interrupt Control Register
	RTC_INTFLAGS	1027	0x403	Interrupt Flags
	RTC_TEMP	1028	0x404	Temporary register
	RTC_CNT	1032	0x408	Count Register
	RTC_PER	1034	0x40A	Period Register
	RTC_COMP	1036	0x40C	Compare Register
				Interrupt Vectors
	RTC_COMP_vect	22	0x16	Compare Interrupt
	RTC_OVF_vect	20	0x14	Overflow Interrupt
Serial Peripheral Interface C				**Registers**
	SPIC_CTRL	2240	0x8C0	Control Register
	SPIC_INTCTRL	2241	0x8C1	Interrupt Control Register
	SPIC_STATUS	2242	0x8C2	Status Register
	SPIC_DATA	2243	0x8C3	Data Register
				Interrupt Vectors
	SPIC_INT_vect	48	0x30	SPI Interrupt
Serial Peripheral Interface D				**Registers**
	SPID_CTRL	2496	0x9C0	Control Register
	SPID_INTCTRL	2497	0x9C1	Interrupt Control Register
	SPID_STATUS	2498	0x9C2	Status Register
	SPID_DATA	2499	0x9C3	Data Register
				Interrupt Vectors
	SPID_INT_vect	174	0xAE	SPI Interrupt
Serial Peripheral Interface E				**Registers**
	SPIE_CTRL	2752	0xAC0	Control Register
	SPIE_INTCTRL	2753	0xAC1	Interrupt Control Register
	SPIE_STATUS	2754	0xAC2	Status Register
	SPIE_DATA	2755	0xAC3	Data Register
				Interrupt Vectors
	SPIE_INT_vect	114	0x72	SPI Interrupt
rial Peripheral Interface F				**Registers**
	SPIF_CTRL	3008		Control Register
	SPIF_INTCTRL	3009		Interrupt Control Register
	SPIF_STATUS	3010		Status Register
	SPIF_DATA	3011		Data Register

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Sel	**Interrupt Vectors**			
	SPIF_INT_vect	236	0xEC	SPI Interrupt
Slp Cntr.	**Registers**			
	SLEEP_CTRL	72		Control Register
Timer/Counter 0 on Port C	**Registers**			
	TCC0_CTRLA	2048	0x800	Control Register A
	TCC0_CTRLB	2049	0x801	Control Register B
	TCC0_CTRLC	2050	0x802	Control register C
	TCC0_CTRLD	2051	0x803	Control Register D
	TCC0_CTRLE	2052	0x804	Control Register E
	TCC0_INTCTRLA	2054	0x806	Interrupt Control Register A
	TCC0_INTCTRLB	2055	0x807	Interrupt Control Register B
	TCC0_CTRLFCLR	2056	0x808	Control Register F Clear
	TCC0_CTRLFSET	2057	0x809	Control Register F Set
	TCC0_CTRLGCLR	2058	0x80A	Control Register G Clear
	TCC0_CTRLGSET	2059	0x80B	Control Register G Set
	TCC0_INTFLAGS	2060	0x80C	Interrupt Flag Register
	TCC0_TEMP	2063	0x80F	Temporary Register For 16-bit Access
	TCC0_CNT	2080	0x820	Count
	TCC0_PER	2086	0x826	Period
	TCC0_CCA	2088	0x828	Compare or Capture A
	TCC0_CCB	2090	0x82A	Compare or Capture B
	TCC0_CCC	2092	0x82C	Compare or Capture C
	TCC0_CCD	2094	0x82E	Compare or Capture D
	TCC0_PERBUF	2102	0x836	Period Buffer
	TCC0_CCABUF	2104	0x838	Compare Or Capture A Buffer
	TCC0_CCBBUF	2106	0x83A	Compare Or Capture B Buffer
	TCC0_CCCBUF	2108	0x83C	Compare Or Capture C Buffer
	TCC0_CCDBUF	2110	0x83E	Compare Or Capture D Buffer
	Interrupt Vectors			
	TCC0_CCA_vect	32	0x20	Compare or Capture A Interrupt
	TCC0_CCB_vect	34	0x22	Compare or Capture B Interrupt
	TCC0_CCC_vect	36	0x24	Compare or Capture C Interrupt
	TCC0_CCD_vect	38	0x26	Compare or Capture D Interrupt
	TCC0_ERR_vect	30	0x1E	Error Interrupt
	TCC0_OVF_vect	28	0x1C	Overflow Interrupt
	Registers			
	TCC1_CTRLA	2112	0x840	Control Register A
	TCC1_CTRLB	2113	0x841	Control Register B
	TCC1_CTRLC	2114	0x842	Control register C
	TCC1_CTRLD	2115	0x843	Control Register D
	TCC1_CTRLE	2116	0x844	Control Register E
	TCC1_INTCTRLA	2118	0x846	Interrupt Control Register A

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Timer/Counter 1 on Port C	TCC1_INTCTRLB	2119	0x847	Interrupt Control Register B
	TCC1_CTRLFCLR	2120	0x848	Control Register F Clear
	TCC1_CTRLFSET	2121	0x849	Control Register F Set
	TCC1_CTRLGCLR	2122	0x84A	Control Register G Clear
	TCC1_CTRLGSET	2123	0x84B	Control Register G Set
	TCC1_INTFLAGS	2124	0x84C	Interrupt Flag Register
	TCC1_TEMP	2127	0x84F	Temporary Register For 16-bit Access
	TCC1_CNT	2144	0x860	Count
	TCC1_PER	2150	0x866	Period
	TCC1_CCA	2152	0x868	Compare or Capture A
	TCC1_CCB	2154	0x86A	Compare or Capture B
	TCC1_PERBUF	2166	0x876	Period Buffer
	TCC1_CCABUF	2168	0x878	Compare Or Capture A Buffer
	TCC1_CCBBUF	2170	0x87A	Compare Or Capture B Buffer
	Interrupt Vectors			
	TCC1_CCA_vect	44	0x2C	Compare or Capture A Interrupt
	TCC1_CCB_vect	46	0x2E	Compare or Capture B Interrupt
	TCC1_ERR_vect	42	0x2A	Error Interrupt
	TCC1_OVF_vect	40	0x28	Overflow Interrupt
Timer/Counter 2 on Port C	**Registers**			
	TCC2_CTRLA	2048	0x800	Control Register A
	TCC2_CTRLB	2049	0x801	Control Register B
	TCC2_CTRLC	2050	0x802	Control register C
	TCC2_CTRLE	2052	0x804	Control Register E
	TCC2_INTCTRLA	2054	0x806	Interrupt Control Register A
	TCC2_INTCTRLB	2055	0x807	Interrupt Control Register B
	TCC2_CTRLF	2057	0x809	Control Register F
	TCC2_INTFLAGS	2060	0x80C	Interrupt Flag Register
	TCC2_LCNT	2080	0x820	Low Byte Count
	TCC2_HCNT	2081	0x821	High Byte Count
	TCC2_LPER	2086	0x826	Low Byte Period
	TCC2_HPER	2087	0x827	High Byte Period
	TCC2_LCMPA	2088	0x828	Low Byte Compare A
	TCC2_HCMPA	2089	0x829	High Byte Compare A
	TCC2_LCMPB	2090	0x82A	Low Byte Compare B
	TCC2_HCMPB	2091	0x82B	High Byte Compare B
	TCC2_LCMPC	2092	0x82C	Low Byte Compare C
	TCC2_HCMPC	2093	0x82D	High Byte Compare C
	TCC2_LCMPD	2094	0x82E	Low Byte Compare D
	TCC2_HCMPD	2095	0x82F	High Byte Compare D
	Interrupt Vectors			
	TCC2_HUNF_vect	30	0x1E	High Byte Underflow Interrupt
	TCC2_LCMPA_vect	32	0x20	Low Byte Compare A Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	TCC2_LCMPB_vect	34	0x22	Low Byte Compare B Interrupt
	TCC2_LCMPC_vect	36	0x24	Low Byte Compare C Interrupt
	TCC2_LCMPD_vect	38	0x26	Low Byte Compare D Interrupt
	TCC2_LUNF_vect	28	0x1C	Low Byte Underflow Interrupt
Timer/Counter 0 on Port D	**Registers**			
	TCD0_CTRLA	2304	0x900	Control Register A
	TCD0_CTRLB	2305	0x901	Control Register B
	TCD0_CTRLC	2306	0x902	Control register C
	TCD0_CTRLD	2307	0x903	Control Register D
	TCD0_CTRLE	2308	0x904	Control Register E
	TCD0_INTCTRLA	2310	0x906	Interrupt Control Register A
	TCD0_INTCTRLB	2311	0x907	Interrupt Control Register B
	TCD0_CTRLFCLR	2312	0x908	Control Register F Clear
	TCD0_CTRLFSET	2313	0x909	Control Register F Set
	TCD0_CTRLGCLR	2314	0x90A	Control Register G Clear
	TCD0_CTRLGSET	2315	0x90B	Control Register G Set
	TCD0_INTFLAGS	2316	0x90C	Interrupt Flag Register
	TCD0_TEMP	2319	0x90F	Temporary Register For 16-bit Access
	TCD0_CNT	2336	0x920	Count
	TCD0_PER	2342	0x926	Period
	TCD0_CCA	2344	0x928	Compare or Capture A
	TCD0_CCB	2346	0x92A	Compare or Capture B
	TCD0_CCC	2348	0x92C	Compare or Capture C
	TCD0_CCD	2350	0x92E	Compare or Capture D
	TCD0_PERBUF	2358	0x936	Period Buffer
	TCD0_CCABUF	2360	0x938	Compare Or Capture A Buffer
	TCD0_CCBBUF	2362	0x93A	Compare Or Capture B Buffer
	TCD0_CCCBUF	2364	0x93C	Compare Or Capture C Buffer
	TCD0_CCDBUF	2366	0x93E	Compare Or Capture D Buffer
	Interrupt Vectors			
	TCD0_CCA_vect	158	0x9E	Compare or Capture A Interrupt
	TCD0_CCB_vect	160	0xA0	Compare or Capture B Interrupt
	TCD0_CCC_vect	162	0xA2	Compare or Capture C Interrupt
	TCD0_CCD_vect	164	0xA4	Compare or Capture D Interrupt
	TCD0_ERR_vect	156	0x9C	Error Interrupt
	TCD0_OVF_vect	154	0x9A	Overflow Interrupt
	Registers			
	TCD1_CTRLA	2368	0x940	Control Register A
	TCD1_CTRLB	2369	0x941	Control Register B
	TCD1_CTRLC	2370	0x942	Control register C
	TCD1_CTRLD	2371	0x943	Control Register D
	TCD1_CTRLE	2372	0x944	Control Register E
	TCD1_INTCTRLA	2374	0x946	Interrupt Control Register A

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Timer/Counter 1 on Port D	TCD1_INTCTRLB	2375	0x947	Interrupt Control Register B
	TCD1_CTRLFCLR	2376	0x948	Control Register F Clear
	TCD1_CTRLFSET	2377	0x949	Control Register F Set
	TCD1_CTRLGCLR	2378	0x94A	Control Register G Clear
	TCD1_CTRLGSET	2379	0x94B	Control Register G Set
	TCD1_INTFLAGS	2380	0x94C	Interrupt Flag Register
	TCD1_TEMP	2383	0x94F	Temporary Register For 16-bit Access
	TCD1_CNT	2400	0x960	Count
	TCD1_PER	2406	0x966	Period
	TCD1_CCA	2408	0x968	Compare or Capture A
	TCD1_CCB	2410	0x96A	Compare or Capture B
	TCD1_PERBUF	2422	0x976	Period Buffer
	TCD1_CCABUF	2424	0x978	Compare Or Capture A Buffer
	TCD1_CCBBUF	2426	0x97A	Compare Or Capture B Buffer
	Interrupt Vectors			
	TCD1_CCA_vect	170	0xAA	Compare or Capture A Interrupt
	TCD1_CCB_vect	172	0xAC	Compare or Capture B Interrupt
	TCD1_ERR_vect	168	0xA8	Error Interrupt
	TCD1_OVF_vect	166	0xA6	Overflow Interrupt
Timer/Counter 2 on Port D	**Registers**			
	TCD2_CTRLA	2304	0x900	Control Register A
	TCD2_CTRLB	2305	0x901	Control Register B
	TCD2_CTRLC	2306	0x902	Control register C
	TCD2_CTRLE	2308	0x904	Control Register E
	TCD2_INTCTRLA	2310	0x906	Interrupt Control Register A
	TCD2_INTCTRLB	2311	0x907	Interrupt Control Register B
	TCD2_CTRLF	2313	0x909	Control Register F
	TCD2_INTFLAGS	2316	0x90C	Interrupt Flag Register
	TCD2_LCNT	2336	0x920	Low Byte Count
	TCD2_HCNT	2337	0x921	High Byte Count
	TCD2_LPER	2342	0x926	Low Byte Period
	TCD2_HPER	2343	0x927	High Byte Period
	TCD2_LCMPA	2344	0x928	Low Byte Compare A
	TCD2_HCMPA	2345	0x929	High Byte Compare A
	TCD2_LCMPB	2346	0x92A	Low Byte Compare B
	TCD2_HCMPB	2347	0x92B	High Byte Compare B
	TCD2_LCMPC	2348	0x92C	Low Byte Compare C
	TCD2_HCMPC	2349	0x92D	High Byte Compare C
	TCD2_LCMPD	2350	0x92E	Low Byte Compare D
	TCD2_HCMPD	2351	0x92F	High Byte Compare D
	Interrupt Vectors			
	TCD2_HUNF_vect	156	0x9C	High Byte Underflow Interrupt
	TCD2_LCMPA_vect	158	0x9E	Low Byte Compare A Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	TCD2_LCMPB_vect	160	0xA0	Low Byte Compare B Interrupt
	TCD2_LCMPC_vect	162	0xA2	Low Byte Compare C Interrupt
	TCD2_LCMPD_vect	164	0xA4	Low Byte Compare D Interrupt
	TCD2_LUNF_vect	154	0x9A	Low Byte Underflow Interrupt
Timer/Counter 0 on Port E	**Registers**			
	TCE0_CTRLA	2560	0xA00	Control Register A
	TCE0_CTRLB	2561	0xA01	Control Register B
	TCE0_CTRLC	2562	0xA02	Control register C
	TCE0_CTRLD	2563	0xA03	Control Register D
	TCE0_CTRLE	2564	0xA04	Control Register E
	TCE0_INTCTRLA	2566	0xA06	Interrupt Control Register A
	TCE0_INTCTRLB	2567	0xA07	Interrupt Control Register B
	TCE0_CTRLFCLR	2568	0xA08	Control Register F Clear
	TCE0_CTRLFSET	2569	0xA09	Control Register F Set
	TCE0_CTRLGCLR	2570	0xA0A	Control Register G Clear
	TCE0_CTRLGSET	2571	0xA0B	Control Register G Set
	TCE0_INTFLAGS	2572	0xA0C	Interrupt Flag Register
	TCE0_TEMP	2575	0xA0F	Temporary Register For 16-bit Access
	TCE0_CNT	2592	0xA20	Count
	TCE0_PER	2598	0xA26	Period
	TCE0_CCA	2600	0xA28	Compare or Capture A
	TCE0_CCB	2602	0xA2A	Compare or Capture B
	TCE0_CCC	2604	0xA2C	Compare or Capture C
	TCE0_CCD	2606	0xA2E	Compare or Capture D
	TCE0_PERBUF	2614	0xA36	Period Buffer
	TCE0_CCABUF	2616	0xA38	Compare Or Capture A Buffer
	TCE0_CCBBUF	2618	0xA3A	Compare Or Capture B Buffer
	TCE0_CCCBUF	2620	0xA3C	Compare Or Capture C Buffer
	TCE0_CCDBUF	2622	0xA3E	Compare Or Capture D Buffer
	Interrupt Vectors			
	TCE0_CCA_vect	98	0x62	Compare or Capture A Interrupt
	TCE0_CCB_vect	100	0x64	Compare or Capture B Interrupt
	TCE0_CCC_vect	102	0x66	Compare or Capture C Interrupt
	TCE0_CCD_vect	104	0x68	Compare or Capture D Interrupt
	TCE0_ERR_vect	96	0x60	Error Interrupt
	TCE0_OVF_vect	94	0x5E	Overflow Interrupt
	Registers			
	TCE1_CTRLA	2624	0xA40	Control Register A
	TCE1_CTRLB	2625	0xA41	Control Register B
	TCE1_CTRLC	2626	0xA42	Control register C
	TCE1_CTRLD	2627	0xA43	Control Register D
	TCE1_CTRLE	2628	0xA44	Control Register E
	TCE1_INTCTRLA	2630	0xA46	Interrupt Control Register A

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Timer/Counter 1 on Port E	TCE1_INTCTRLB	2631	0xA47	Interrupt Control Register B
	TCE1_CTRLFCLR	2632	0xA48	Control Register F Clear
	TCE1_CTRLFSET	2633	0xA49	Control Register F Set
	TCE1_CTRLGCLR	2634	0xA4A	Control Register G Clear
	TCE1_CTRLGSET	2635	0xA4B	Control Register G Set
	TCE1_INTFLAGS	2636	0xA4C	Interrupt Flag Register
	TCE1_TEMP	2639	0xA4F	Temporary Register For 16-bit Access
	TCE1_CNT	2656	0xA60	Count
	TCE1_PER	2662	0xA66	Period
	TCE1_CCA	2664	0xA68	Compare or Capture A
	TCE1_CCB	2666	0xA6A	Compare or Capture B
	TCE1_PERBUF	2678	0xA76	Period Buffer
	TCE1_CCABUF	2680	0xA78	Compare Or Capture A Buffer
	TCE1_CCBBUF	2682	0xA7A	Compare Or Capture B Buffer
	Interrupt Vectors			
	TCE1_CCA_vect	110	0x6E	Compare or Capture A Interrupt
	TCE1_CCB_vect	112	0x70	Compare or Capture B Interrupt
	TCE1_ERR_vect	108	0x6C	Error Interrupt
	TCE1_OVF_vect	106	0x6A	Overflow Interrupt
Timer/Counter 2 on Port E	**Registers**			
	TCE2_CTRLA	2560	0xA00	Control Register A
	TCE2_CTRLB	2561	0xA01	Control Register B
	TCE2_CTRLC	2562	0xA02	Control register C
	TCE2_CTRLE	2564	0xA04	Control Register E
	TCE2_INTCTRLA	2566	0xA06	Interrupt Control Register A
	TCE2_INTCTRLB	2567	0xA07	Interrupt Control Register B
	TCE2_CTRLF	2569	0xA09	Control Register F
	TCE2_INTFLAGS	2572	0xA0C	Interrupt Flag Register
	TCE2_LCNT	2592	0xA20	Low Byte Count
	TCE2_HCNT	2593	0xA21	High Byte Count
	TCE2_LPER	2598	0xA26	Low Byte Period
	TCE2_HPER	2599	0xA27	High Byte Period
	TCE2_LCMPA	2600	0xA28	Low Byte Compare A
	TCE2_HCMPA	2601	0xA29	High Byte Compare A
	TCE2_LCMPB	2602	0xA2A	Low Byte Compare B
	TCE2_HCMPB	2603	0xA2B	High Byte Compare B
	TCE2_LCMPC	2604	0xA2C	Low Byte Compare C
	TCE2_HCMPC	2605	0xA2D	High Byte Compare C
	TCE2_LCMPD	2606	0xA2E	Low Byte Compare D
	TCE2_HCMPD	2607	0xA2F	High Byte Compare D
	Interrupt Vectors			
	TCE2_HUNF_vect	96	0x60	High Byte Underflow Interrupt
	TCE2_LCMPA_vect	98	0x62	Low Byte Compare A Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	TCE2_LCMPB_vect	100	0x64	Low Byte Compare B Interrupt
	TCE2_LCMPC_vect	102	0x66	Low Byte Compare C Interrupt
	TCE2_LCMPD_vect	104	0x68	Low Byte Compare D Interrupt
	TCE2_LUNF_vect	94	0x5E	Low Byte Underflow Interrupt
Timer/Counter 0 on Port F	**Registers**			
	TCF0_CTRLA	2816	0xB00	Control Register A
	TCF0_CTRLB	2817	0xB01	Control Register B
	TCF0_CTRLC	2818	0xB02	Control register C
	TCF0_CTRLD	2819	0xB03	Control Register D
	TCF0_CTRLE	2820	0xB04	Control Register E
	TCF0_INTCTRLA	2822	0xB06	Interrupt Control Register A
	TCF0_INTCTRLB	2823	0xB07	Interrupt Control Register B
	TCF0_CTRLFCLR	2824	0xB08	Control Register F Clear
	TCF0_CTRLFSET	2825	0xB09	Control Register F Set
	TCF0_CTRLGCLR	2826	0xB0A	Control Register G Clear
	TCF0_CTRLGSET	2827	0xB0B	Control Register G Set
	TCF0_INTFLAGS	2828	0xB0C	Interrupt Flag Register
	TCF0_TEMP	2831	0xB0F	Temporary Register For 16-bit Access
	TCF0_CNT	2848	0xB20	Count
	TCF0_PER	2854	0xB26	Period
	TCF0_CCA	2856	0xB28	Compare or Capture A
	TCF0_CCB	2858	0xB2A	Compare or Capture B
	TCF0_CCC	2860	0xB2C	Compare or Capture C
	TCF0_CCD	2862	0xB2E	Compare or Capture D
	TCF0_PERBUF	2870	0xB36	Period Buffer
	TCF0_CCABUF	2872	0xB38	Compare Or Capture A Buffer
	TCF0_CCBBUF	2874	0xB3A	Compare Or Capture B Buffer
	TCF0_CCCBUF	2876	0xB3C	Compare Or Capture C Buffer
	TCF0_CCDBUF	2878	0xB3E	Compare Or Capture D Buffer
	Interrupt Vectors			
	TCF0_CCA_vect	220	0xDC	Compare or Capture A Interrupt
	TCF0_CCB_vect	222	0xDE	Compare or Capture B Interrupt
	TCF0_CCC_vect	224	0xE0	Compare or Capture C Interrupt
	TCF0_CCD_vect	226	0xE2	Compare or Capture D Interrupt
	TCF0_ERR_vect	218	0xDA	Error Interrupt
	TCF0_OVF_vect	216	0xD8	Overflow Interrupt
	Registers			
	TCF1_CTRLA	2880	0xB40	Control Register A
	TCF1_CTRLB	2881	0xB41	Control Register B
	TCF1_CTRLC	2882	0xB42	Control register C
	TCF1_CTRLD	2883	0xB43	Control Register D
	TCF1_CTRLE	2884	0xB44	Control Register E
	TCF1_INTCTRLA	2886	0xB46	Interrupt Control Register A

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Timer/Counter 1 on Port F	TCF1_INTCTRLB	2887	0xB47	Interrupt Control Register B
	TCF1_CTRLFCLR	2888	0xB48	Control Register F Clear
	TCF1_CTRLFSET	2889	0xB49	Control Register F Set
	TCF1_CTRLGCLR	2890	0xB4A	Control Register G Clear
	TCF1_CTRLGSET	2891	0xB4B	Control Register G Set
	TCF1_INTFLAGS	2892	0xB4C	Interrupt Flag Register
	TCF1_TEMP	2895	0xB4F	Temporary Register For 16-bit Access
	TCF1_CNT	2912	0xB60	Count
	TCF1_PER	2918	0xB66	Period
	TCF1_CCA	2920	0xB68	Compare or Capture A
	TCF1_CCB	2922	0xB6A	Compare or Capture B
	TCF1_PERBUF	2934	0xB76	Period Buffer
	TCF1_CCABUF	2936	0xB78	Compare Or Capture A Buffer
	TCF1_CCBBUF	2938	0xB7A	Compare Or Capture B Buffer
	Interrupt Vectors			
	TCF1_CCA_vect	232	0xE8	Compare or Capture A Interrupt
	TCF1_CCB_vect	234	0xEA	Compare or Capture B Interrupt
	TCF1_ERR_vect	230	0xE6	Error Interrupt
	TCF1_OVF_vect	228	0xE4	Overflow Interrupt
Timer/Counter 2 on Port F	**Registers**			
	TCF2_CTRLA	2816	0xB00	Control Register A
	TCF2_CTRLB	2817	0xB01	Control Register B
	TCF2_CTRLC	2818	0xB02	Control register C
	TCF2_CTRLE	2820	0xB04	Control Register E
	TCF2_INTCTRLA	2822	0xB06	Interrupt Control Register A
	TCF2_INTCTRLB	2823	0xB07	Interrupt Control Register B
	TCF2_CTRLF	2825	0xB09	Control Register F
	TCF2_INTFLAGS	2828	0xB0C	Interrupt Flag Register
	TCF2_LCNT	2848	0xB20	Low Byte Count
	TCF2_HCNT	2849	0xB21	High Byte Count
	TCF2_LPER	2854	0xB26	Low Byte Period
	TCF2_HPER	2855	0xB27	High Byte Period
	TCF2_LCMPA	2856	0xB28	Low Byte Compare A
	TCF2_HCMPA	2857	0xB29	High Byte Compare A
	TCF2_LCMPB	2858	0xB2A	Low Byte Compare B
	TCF2_HCMPB	2859	0xB2B	High Byte Compare B
	TCF2_LCMPC	2860	0xB2C	Low Byte Compare C
	TCF2_HCMPC	2861	0xB2D	High Byte Compare C
	TCF2_LCMPD	2862	0xB2E	Low Byte Compare D
	TCF2_HCMPD	2863	0xB2F	High Byte Compare D
	Interrupt Vectors			
	TCF2_HUNF_vect	218	0xDA	High Byte Underflow Interrupt
	TCF2_LCMPA_vect	220	0xDC	Low Byte Compare A Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	TCF2_LCMPB_vect	222	0xDE	Low Byte Compare B Interrupt
	TCF2_LCMPC_vect	224	0xE0	Low Byte Compare C Interrupt
	TCF2_LCMPD_vect	226	0xE2	Low Byte Compare D Interrupt
	TCF2_LUNF_vect	216	0xD8	Low Byte Underflow Interrupt
Two Wire Interfaceon Port C	**Registers**			
	TWIC_CTRL	1152	0x480	TWI Common Control Register
	TWIC_MASTER_CTRLA	1153	0x481	Control Register A
	TWIC_MASTER_CTRLB	1154	0x482	Control Register B
	TWIC_MASTER_CTRLC	1155	0x483	Control Register C
	TWIC_MASTER_STATUS	1156	0x484	Status Register
	TWIC_MASTER_BAUD	1157	0x485	Baurd Rate Control Register
	TWIC_MASTER_ADDR	1158	0x486	Address Register
	TWIC_MASTER_DATA	1159	0x487	Data Register
	TWIC_SLAVE_CTRLA	1160	0x488	Control Register A
	TWIC_SLAVE_CTRLB	1161	0x489	Control Register B
	TWIC_SLAVE_STATUS	1162	0x48A	Status Register
	TWIC_SLAVE_ADDR	1163	0x48B	Address Register
	TWIC_SLAVE_DATA	1164	0x48C	Data Register
	TWIC_SLAVE_ADDRMASK	1165	0x48D	Address Mask Register
	Interrupt Vectors			
	TWIC_TWIM_vect	26	0x1A	TWI Master Interrupt
	TWIC_TWIS_vect	24	0x18	TWI Slave Interrupt
Two Wire Interfaceon Port D	**Registers**			
	TWID_CTRL	1168	0x490	TWI Common Control Register
	TWID_MASTER_CTRLA	1169	0x491	Control Register A
	TWID_MASTER_CTRLB	1170	0x492	Control Register B
	TWID_MASTER_CTRLC	1171	0x493	Control Register C
	TWID_MASTER_STATUS	1172	0x494	Status Register
	TWID_MASTER_BAUD	1173	0x495	Baurd Rate Control Register
	TWID_MASTER_ADDR	1174	0x496	Address Register
	TWID_MASTER_DATA	1175	0x497	Data Register
	TWID_SLAVE_CTRLA	1176	0x498	Control Register A
	TWID_SLAVE_CTRLB	1177	0x499	Control Register B
	TWID_SLAVE_STATUS	1178	0x49A	Status Register
	TWID_SLAVE_ADDR	1179	0x49B	Address Register
	TWID_SLAVE_DATA	1180	0x49C	Data Register
	TWID_SLAVE_ADDRMASK	1181	0x49D	Address Mask Register
	Interrupt Vectors			
	TWID_TWIM_vect	152	0x98	TWI Master Interrupt
	TWID_TWIS_vect	150	0x96	TWI Slave Interrupt
	Registers			
	TWIE_CTRL	1184	0x4A0	TWI Common Control Register
	TWIE_MASTER_CTRLA	1185	0x4A1	Control Register A

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
Two Wire Interfaceon Port E	TWIE_MASTER_CTRLB	1186	0x4A2	Control Register B
	TWIE_MASTER_CTRLC	1187	0x4A3	Control Register C
	TWIE_MASTER_STATUS	1188	0x4A4	Status Register
	TWIE_MASTER_BAUD	1189	0x4A5	Baurd Rate Control Register
	TWIE_MASTER_ADDR	1190	0x4A6	Address Register
	TWIE_MASTER_DATA	1191	0x4A7	Data Register
	TWIE_SLAVE_CTRLA	1192	0x4A8	Control Register A
	TWIE_SLAVE_CTRLB	1193	0x4A9	Control Register B
	TWIE_SLAVE_STATUS	1194	0x4AA	Status Register
	TWIE_SLAVE_ADDR	1195	0x4AB	Address Register
	TWIE_SLAVE_DATA	1196	0x4AC	Data Register
	TWIE_SLAVE_ADDRMASK	1197	0x4AD	Address Mask Register
	Interrupt Vectors			
	TWIE_TWIM_vect	92	0x5C	TWI Master Interrupt
	TWIE_TWIS_vect	90	0x5A	TWI Slave Interrupt
Two Wire Interfaceon Port F	**Registers**			
	TWIF_CTRL	1200	0x4B0	TWI Common Control Register
	TWIF_MASTER_CTRLA	1201	0x4B1	Control Register A
	TWIF_MASTER_CTRLB	1202	0x4B2	Control Register B
	TWIF_MASTER_CTRLC	1203	0x4B3	Control Register C
	TWIF_MASTER_STATUS	1204	0x4B4	Status Register
	TWIF_MASTER_BAUD	1205	0x4B5	Baurd Rate Control Register
	TWIF_MASTER_ADDR	1206	0x4B6	Address Register
	TWIF_MASTER_DATA	1207	0x4B7	Data Register
	TWIF_SLAVE_CTRLA	1208	0x4B8	Control Register A
	TWIF_SLAVE_CTRLB	1209	0x4B9	Control Register B
	TWIF_SLAVE_STATUS	1210	0x4BA	Status Register
	TWIF_SLAVE_ADDR	1211	0x4BB	Address Register
	TWIF_SLAVE_DATA	1212	0x4BC	Data Register
	TWIF_SLAVE_ADDRMASK	1213	0x4BD	Address Mask Register
	Interrupt Vectors			
	TWIF_TWIM_vect	214	0xD6	TWI Master Interrupt
	TWIF_TWIS_vect	212	0xD4	TWI Slave Interrupt
USART0 on Port C	**Registers**			
	USARTC0_DATA	2208	0x8A0	Data Register
	USARTC0_STATUS	2209	0x8A1	Status Register
	USARTC0_CTRLA	2211	0x8A3	Control Register A
	USARTC0_CTRLB	2212	0x8A4	Control Register B
	USARTC0_CTRLC	2213	0x8A5	Control Register C
	USARTC0_BAUDCTRLA	2214	0x8A6	Baud Rate Control Register A
	USARTC0_BAUDCTRLB	2215	0x8A7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTC0_DRE_vect	52	0x34	Data Register Empty Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	USARTC0_RXC_vect	50	0x32	Reception Complete Interrupt
	USARTC0_TXC_vect	54	0x36	Transmission Complete Interrupt
USART1 on Port C	**Registers**			
	USARTC1_DATA	2224	0x8B0	Data Register
	USARTC1_STATUS	2225	0x8B1	Status Register
	USARTC1_CTRLA	2227	0x8B3	Control Register A
	USARTC1_CTRLB	2228	0x8B4	Control Register B
	USARTC1_CTRLC	2229	0x8B5	Control Register C
	USARTC1_BAUDCTRLA	2230	0x8B6	Baud Rate Control Register A
	USARTC1_BAUDCTRLB	2231	0x8B7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTC1_DRE_vect	58	0x3A	Data Register Empty Interrupt
	USARTC1_RXC_vect	56	0x38	Reception Complete Interrupt
	USARTC1_TXC_vect	60	0x3C	Transmission Complete Interrupt
USART0 on Port D	**Registers**			
	USARTD0_DATA	2464	0x9A0	Data Register
	USARTD0_STATUS	2465	0x9A1	Status Register
	USARTD0_CTRLA	2467	0x9A3	Control Register A
	USARTD0_CTRLB	2468	0x9A4	Control Register B
	USARTD0_CTRLC	2469	0x9A5	Control Register C
	USARTD0_BAUDCTRLA	2470	0x9A6	Baud Rate Control Register A
	USARTD0_BAUDCTRLB	2471	0x9A7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTD0_DRE_vect	178	0xB2	Data Register Empty Interrupt
	USARTD0_RXC_vect	176	0xB0	Reception Complete Interrupt
	USARTD0_TXC_vect	180	0xB4	Transmission Complete Interrupt
USART1 on Port D	**Registers**			
	USARTD1_DATA	2480	0x9B0	Data Register
	USARTD1_STATUS	2481	0x9B1	Status Register
	USARTD1_CTRLA	2483	0x9B3	Control Register A
	USARTD1_CTRLB	2484	0x9B4	Control Register B
	USARTD1_CTRLC	2485	0x9B5	Control Register C
	USARTD1_BAUDCTRLA	2486	0x9B6	Baud Rate Control Register A
	USARTD1_BAUDCTRLB	2487	0x9B7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTD1_DRE_vect	184	0xB8	Data Register Empty Interrupt
	USARTD1_RXC_vect	182	0xB6	Reception Complete Interrupt
	USARTD1_TXC_vect	186	0xBA	Transmission Complete Interrupt
E	**Registers**			
	USARTE0_DATA	2720	0xAA0	Data Register
	USARTE0_STATUS	2721	0xAA1	Status Register
	USARTE0_CTRLA	2723	0xAA3	Control Register A

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
USART0 on Port	USARTE0_CTRLB	2724	0xAA4	Control Register B
	USARTE0_CTRLC	2725	0xAA5	Control Register C
	USARTE0_BAUDCTRLA	2726	0xAA6	Baud Rate Control Register A
	USARTE0_BAUDCTRLB	2727	0xAA7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTE0_DRE_vect	118	0x76	Data Register Empty Interrupt
	USARTE0_RXC_vect	116	0x74	Reception Complete Interrupt
	USARTE0_TXC_vect	120	0x78	Transmission Complete Interrupt
USART1 on Port E	**Registers**			
	USARTE1_DATA	2736	0xAB0	Data Register
	USARTE1_STATUS	2737	0xAB1	Status Register
	USARTE1_CTRLA	2739	0xAB3	Control Register A
	USARTE1_CTRLB	2740	0xAB4	Control Register B
	USARTE1_CTRLC	2741	0xAB5	Control Register C
	USARTE1_BAUDCTRLA	2742	0xAB6	Baud Rate Control Register A
	USARTE1_BAUDCTRLB	2743	0xAB7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTE1_DRE_vect	124	0x7C	Data Register Empty Interrupt
	USARTE1_RXC_vect	122	0x7A	Reception Complete Interrupt
	USARTE1_TXC_vect	126	0x7E	Transmission Complete Interrupt
USART0 on Port F	**Registers**			
	USARTF0_DATA	2976	0xBA0	Data Register
	USARTF0_STATUS	2977	0xBA1	Status Register
	USARTF0_CTRLA	2979	0xBA3	Control Register A
	USARTF0_CTRLB	2980	0xBA4	Control Register B
	USARTF0_CTRLC	2981	0xBA5	Control Register C
	USARTF0_BAUDCTRLA	2982	0xBA6	Baud Rate Control Register A
	USARTF0_BAUDCTRLB	2983	0xBA7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTF0_DRE_vect	240	0xF0	Data Register Empty Interrupt
	USARTF0_RXC_vect	238	0xEE	Reception Complete Interrupt
	USARTF0_TXC_vect	242	0xF2	Transmission Complete Interrupt
USART1 on Port F	**Registers**			
	USARTF1_DATA	2992	0xBB0	Data Register
	USARTF1_STATUS	2993	0xBB1	Status Register
	USARTF1_CTRLA	2995	0xBB3	Control Register A
	USARTF1_CTRLB	2996	0xBB4	Control Register B
	USARTF1_CTRLC	2997	0xBB5	Control Register C
	USARTF1_BAUDCTRLA	2998	0xBB6	Baud Rate Control Register A
	USARTF1_BAUDCTRLB	2999	0xBB7	Baud Rate Control Register B
	Interrupt Vectors			
	USARTF1_DRE_vect	246	0xF6	Data Register Empty Interrupt
	USARTF1_RXC_vect	244	0xF4	Reception Complete Interrupt

Device	Name	$Addr_{10}$	$Addr_{16}$	Description
	USARTF1_TXC_vect	248	0xF8	Transmission Complete Interrupt
Universal Serial Bus (USB)	**Registers**			
	USB_CTRLA	1216	0x4C0	Control Register A
	USB_CTRLB	1217	0x4C1	Control Register B
	USB_STATUS	1218	0x4C2	Status Register
	USB_ADDR	1219	0x4C3	Address Register
	USB_FIFOWP	1220	0x4C4	FIFO Write Pointer Register
	USB_FIFORP	1221	0x4C5	FIFO Read Pointer Register
	USB_EPPTR	1222	0x4C6	Endpoint Configuration Table Pointer
	USB_INTCTRLA	1224	0x4C8	Interrupt Control Register A
	USB_INTCTRLB	1225	0x4C9	Interrupt Control Register B
	USB_INTFLAGSACLR	1226	0x4CA	Clear Interrupt Flag Register A
	USB_INTFLAGSASET	1227	0x4CB	Set Interrupt Flag Register A
	USB_INTFLAGSBCLR	1228	0x4CC	Clear Interrupt Flag Register B
	USB_INTFLAGSBSET	1229	0x4CD	Set Interrupt Flag Register B
	USB_CAL0	1274	0x4FA	Calibration Byte 0
	USB_CAL1	1275	0x4FB	Calibration Byte 1
	Interrupt Vectors			
	USB_BUSEVENT_vect	250	0xFA	SOF
	USB_TRNCOMPL_vect	252	0xFC	Transaction complete interrupt
Watchdog Timer	**Registers**			
	WDT_CTRL	128	0x80	Control
	WDT_WINCTRL	129	0x81	Windowed Mode Control
	WDT_STATUS	130	0x82	Status