Education

Boston University, Boston, MA	Computer Engineering	Ph. D., 2016
Boston University, Boston, MA	Electrical Engineering	B. S., 2010

Employment History

SiFive *Senior Staff Engineer*	San Mateo, CA (remote)	09/2020–present
IBM *Research Staff Member*	Yorktown Heights, NY	02/2019–09/2020
IBM *Postdoctoral Researcher*	Yorktown Heights, NY	08/2016–02/2019
NASA *Space Technology Research Fellow*	Pasadena, CA	05/2015–07/2015 06/2014–08/2014 06/2013–08/2013
Intel Corporation *Graduate Technical Intern*	Hudson, MA	05/2011–09/2011 07/2010–08/2010
Boston University *Undergraduate Teaching Assistant*	Boston, MA	01/2010–05/2010 01/2009–05/2009

Honors, Awards, and Fellowships

NASA Space Technology Research Fellowship	08/2012–08/2016
CELEST/CompNet Award	04/2012
Boston University Dean's Fellowship	09/2010–09/2011
P. T. Hsu Memorial Award for Outstanding Senior Design Project	05/2010
Boston University Engineering Scholar Award	09/2006–05/2010

Grants

DARPA	DSSoC	HR001118C0122	Staff	08/2018–09/2020
DARPA	PERFECT	HR001113C0022	Staff	08/2016–08/2018

Program Committees and Reviews

IEEE Transactions on Computers	Article Reviewer	2022
Chisel Community Conference China (CCCC)	Program Committee	2021
Future of Computing Architectures (FOCA) Workshop	Selection Committee	2020
Chisel Community Conference (CCC)	Program Committee	2018
IEEE Micro	Article Reviewer	2018
IEEE Micro	Article Reviewer	2016

Open Source Activities (GitHub)

Maintainer

`llvm/circt`	C++, MLIR	Circuit IR Compilers and Tools [W1, C1, C2]	410 commits 33541++ 13593--
`chipsalliance/firrtl`	Scala	Circuit Intermediate Representation and Compiler [C7, C10]	200 commits 17461++ 9444--
`chipsalliance/chisel3`	Scala	Scala-embedded hardware DSL [W1, W2, W4, W5]	158 commits 8001++ 3421--
`chipsalliance/firrtl-spec`	Markdown	Specification for the FIRRTL language	25 commits 1177++ 1375--

Contributor

`chipsalliance/rocket-chip`	Scala	Rocket Chip Generator	34 commits 766++ 257--
`riscv/riscv-fesvr`	C	RISC-V Frontend Server	9 commits 298++ 148--
`riscv/riscv-tools`	Shell	RISC-V Tools (GNU Toolchain, ISA Simulator, Tests)	3 commits 3++ 3--

Author

`seldridge/verilog`	Verilog	Repository for basic (and not so basic) Verilog blocks with high re-use potential	390 Stars
`bu-icsg/dana`	Scala	Dynamically Allocated Neural Network Accelerator for the RISC-V Rocket Microprocessor in Chisel [Th1, W8, W9, W10, C17]	178 Stars
`seldridge/rocket-rocc-examples`	C	Tests for example Rocket Custom Coprocessors	57 Stars
`IBM/hdl-tools`	Tcl	Facilitates building open source tools for working with hardware description languages (HDLs)	51 Stars
`IBM/rocc-software`	C	C/Assembly macros for talking with Rocket Custom Coprocessors (RoCCs)	48 Stars
`sifive/chisel-circt`	Scala	Library to compile Chisel circuits using CIRCT [C2]	42 Stars
`IBM/chiffre`	Scala	A fault-injection framework using Chisel and FIRRTL [C9, C11, D1]	25 Stars
`IBM/esp-chisel-accelerators`	Scala	Embedded Scalable Platform accelerator socket [C6]	17 Stars
`IBM/firrtl-mode`	Emacs Lisp	Major mode for editing FIRRTL files in Emacs	3 Stars
`seldridge/make-markdown`	Shell	Collecting personal knowledge in Markdown	
`seldridge/cv-simple`	LaTeX	Simple LaTeX CV (this document)	

Publications

Peer Reviewed Conference Publications

[C1] Schuyler Eldridge, Prithayan Barua, Aliaksei Chapyzhenka, Adam Izraelevitz, Jack Koenig, Chris Lattner, Andrew Lenharth, George Leontiev, Fabian Schuiki, Ram Sunder, Andrew Young, and Richard Xia. "MLIR as Hardware Compiler Infrastructure". In: *Workshop on Open-Source EDA Technology (WOSET)*. 2021. URL: https://woset-workshop.github.io/PDFs/2021/a06-slides.pdf.

[C2] Schuyler Eldridge, Andrew Lenharth, Andrew Young, Prithayan Barua, Fabian Schuiki, Hanchen Ye, Aliaksei Chapyzhenka, Jack Koenig, Adam Izraelevitz, George Leontiev, Ram Sunder, and Chris Lattner. "The Next Generation FIRRTL Compiler". In: *2nd Chisel Community Conference China (CCCC)*. 2021.

[C3] Leila Delshadtehrani, Sadullah Canakci, Boyou Zhou, Schuyler Eldridge, Ajay Joshi, and Manuel Egele. "A Chisel-based Programmable Hardware Monitor". In: *3rd Chisel Community Conference (CCC)*. 2020. URL: https://drive.google.com/file/d/1xUmuLmaHRQZMAQBOUd95enD4LLeD8n2I/view.

[C4] Leila Delshadtehrani, Sadullah Canakci, Boyou Zhou, Schuyler Eldridge, Ajay Joshi, and Manuel Egele. "A Programmable Hardware Monitor for Security of RISC-V Processors". In: *Boston Area Architecture Conference (BARC)*. Jan. 2020.

[C5] Leila Delshadtehrani, Sadullah Canakci, Boyou Zhou, Schuyler Eldridge, Ajay Joshi, and Manuel Egele. "PHMon: A Programmable Hardware Monitor and its Security Applications". In: *USENIX Security Symposium 2020*. 2020. URL: https://www.usenix.org/system/files/sec20-delshadtehrani.pdf.

[C6] Schuyler Eldridge. "Building Loosely-coupled RISC-V Accelerators". In: *FOSDEM 2020*. 2020. URL: https://fosdem.org/2020/schedule/event/riscv_chisel/.

[C7] Schuyler Eldridge. "Improving Chisel/FIRRTL Verilog Generation". In: *3rd Chisel Community Conference (CCC)*. 2020. URL: https://drive.google.com/file/d/1d-aGKsKII2J7G1OO_rmcgMzb3ijvmtQo/view.

[C8] N. Chandramoorthy, K. Swaminathan, M. Cochet, A. Paidimarri, S. Eldridge, R. Joshi, M. Ziegler, A. Buyuktosunoglu, and P. Bose. "Resilient Low Voltage Accelerators for High Energy Efficiency". In: *2019 IEEE International Symposium on High Performance Computer Architecture (HPCA)*. Feb. 2019, pp. 147–158. DOI: 10.1109/HPCA.2019.00034. URL: https://ieeexplore.ieee.org/abstract/document/8675205.

[C9] Schuyler Eldridge, Alper Buyuktosunoglu, and Pradip Bose. "Chiffre: A Configurable Hardware Fault Injection Framework for RISC-V Systems". In: *2nd Workshop on Computer Architecture Research with RISC-V (CARRV '18)*. 2018. URL: https://carrv.github.io/2018/papers/CARRV_2018_paper_2.pdf.

[C10] Schuyler Eldridge and Adam Izraelevitz. "Annotations and Hardware Construction Languages". In: *1st Chisel Community Conference (CCC)*. 2018. URL: https://www.youtube.com/watch?v=4YGIdjMNI6Q.

[C11] Schuyler Eldridge, Vaibhav Verma, Xinfei Guo, Alec Roelke, Karthik Swaminathan, Nandhini Chandramoorthy, Martin Cochet, Alper Buyuktosunoglu, Christos Vezyrtzis, Rajiv Joshi, Matt Ziegler, Mircea Stan, and Pradip Bose. "VELOUR: Very Low Voltage Operation Under Resilience Constraints". In: *50th GOMACTech Conference*. 2018.

[C12] Mateja Putic, Swagath Venkataramani, Schuyler Eldridge, Alper Buyuktosunoglu, Pradip Bose, and Mircea Stan. "DyHard-DNN: Even More DNN Acceleration with Dynamic Hardware Reconfiguration". In: *55th Annual Design Automation Conference (DAC)*. 2018.

[C13] Ramon Bertran, Pradip Bose, David M. Brooks, Jeff Burns, Alper Buyuktosunoglu, Nandhini Chandramoorthy, Eric Cheng, Martin Cochet, Schuyler Eldridge, Daniel Friedman, Hans M. Jacobson, Rajiv V. Joshi, Subhasish Mitra, Robert K. Montoye, Arun Paidimarri, Pritish Parida, Kevin Skadron, Mircea Stan, Karthik Swaminathan, Augusto Vega, Swagath Venkataramani, Christos Vezyrtzis, Gu-Yeon Wei, John-David Wellman, and Matthew M. Ziegler. "Very Low Voltage (VLV) Design". In: *2017 IEEE International Conference on Computer Design, ICCD 2017, Boston, MA, USA, November 5-8, 2017*. 2017, pp. 601–604. URL: https://doi.org/10.1109/ICCD.2017.105.

[C14] Leila Delshadtehrani, Jonathan Appavoo, Manuel Egele, Ajay Joshi, and Schuyler Eldridge. "Varanus: An Infrastructure for Programmable Hardware Monitoring Units". In: *Boston Area Architecture Conference (BARC)*. Jan. 2017. URL: https://megele.io/barc2017.pdf.

[C15] Schuyler Eldridge, Karthik Swaminathan, Nandhini Chandramoorthy, Alper Buyuktosunoglu, Alec Roelke, Vaibhav Verma, Rajiv Joshi, Mircea Stan, and Pradip Bose. "A Low Voltage RISC-V Heterogeneous System". In: *1st Workshop on Computer Architecture Research with RISC-V (CARRV '17)*. 2017. URL: https://carrv.github.io/2017/papers/eldridge-velour-carrv2017.pdf.

[C16] Schuyler Eldridge and Ajay Joshi. "Exploiting Hidden Layer Modular Redundancy for Fault-Tolerance in Neural Network Accelerators". In: *Boston Area Architecture Conference (BARC)*. Jan. 2015. URL: http://people.bu.edu/joshi/files/Eldridge_BARC_2015.pdf.

[C17] Schuyler Eldridge, Amos Waterland, Margo Seltzer, Jonathan Appavoo, and Ajay Joshi. "Towards General-Purpose Neural Network Computing". In: *2015 International Conference on Parallel Architecture and Compilation, PACT 2015, San Francisco, CA, USA, October 18-21, 2015*. IEEE Computer Society, Oct. 2015, pp. 99–112. ISBN: 978-1-4673-9524-3. URL: https://dash.harvard.edu/bitstream/handle/1/30779603/82681851.pdf?sequence=1.

[C18] Jonathan Appavoo, Amos Waterland, Schuyler Eldridge, Katherine Zhao, Ajay Joshi, Steve Homer, and Margo Seltzer. "Programmable Smart Machines: A Hybrid Neuromorphic Approach to General Purpose Computation". In: *NeuroArch Workshop*. 2014. URL: http://people.bu.edu/joshi/files/appavoo-neuroarch-2014.pdf.

[C19] Schuyler Eldridge, Florian Raudies, David Zou, and Ajay Joshi. "Neural network-based accelerators for transcendental function approximation". In: *Great Lakes Symposium on VLSI 2014, GLSVLSI '14, Houston, TX, USA - May 21 - 23, 2014*. 2014, pp. 169–174. URL: http://people.bu.edu/joshi/files/glsvlsi2014-eldridge.pdf.

[C20] Schuyler Eldridge, Florian Raudies, and Ajay Joshi. "Approximate Computation using a Neuralized Floating Point Unit". In: *Brain Inspired Computing Workshop*. 2013. URL: http://people.bu.edu/joshi/files/approx-fpu-bic2013.pdf.

Peer Reviewed Journal Articles

[J1] Leila Delshadtehrani, Schuyler Eldridge, Sadullah Canakci, Manuel Egele, and Ajay Joshi. "Nile: A Programmable Monitoring Coprocessor". In: *Computer Architecture Letters* 17.1 (2018), pp. 92–95. URL: https://doi.org/10.1109/LCA.2017.2784416.

[J2] F. Raudies, S. Eldridge, A. Joshi, and M. Versace. "Learning to Navigate in a Virtual World using Optic Flow and Stereo Disparity Signals". In: *Artificial Life and Robotics* 19.2 (2014), pp. 157–169. URL: https://link.springer.com/article/10.1007/s10015-014-0153-1.

Patents and Patent Applications

[P1] Swagath Venkataramani, Schuyler Eldridge, Karthik V. Swaminathan, Alper Buyuktosunoglu, and Pradip Bose and. "Low-overhead Error Prediction and Preemption in Deep Neural Network Using Apriori Network Statistics". US Patent 11,016,840. International Business Machines Corp. 2020.

[P2] Pradip Bose, Alper Buyuktosunoglu, Schuyler Eldridge, Karthik V. Swaminathan, Augusto Vega, and Swagath Venkataramani. "Reducing the Cost of N Modular Redundancy for Neural Networks". US Patent App. 15/806,393. International Business Machines Corp. 2019.

[P3] Pradip Bose, Alper Buyuktosunoglu, Schuyler Eldridge, Karthik V. Swaminathan, and Swagath Venkataramani. "System and Method for Consensus-based Representation and Error Checking for Neural Networks". US Patent App. 15/825,660. International Business Machines Corp. 2019.

[P4] Pradip Bose, Alper Buyuktosunoglu, Schuyler Eldridge, Karthik V. Swaminathan, and Yazhou Zu. "Determination and Correction of Physical Circuit Event Related Errors of a Hardware Design". US Patent 10,690,723. International Business Machines Corp. 2019.

[P5] Alper Buyuktosunoglu, Swagath Venkataramani, Rajiv Joshi, Karthik V. Swaminathan, Schuyler Eldridge, and Pradip Bose. "Self-evaluating array of memory". US Patent 10,607,715. International Business Machines Corp. 2018.

[P6] Vinodh Gopal, James D. Guilford, Schuyler Eldridge Gilbert M. Wolrich, Erdinc Ozturk, and Wajdi K. Feghali. "Digest Generation". US Patent 9,292,548. Intel Corporation. 2016.

Demonstrations

[D1] Alec Roelke, Schuyler Eldridge, and Mircea Stan. "VELOUR: Very Low Voltage Operation Under Resilience Constraints". In: *3rd Workshop on Cognitive Architectures*. 2018.

Technical Reports

[TR1] F. Raudies, S. Eldridge, A. Joshi, and M. Versace. *Reinforcement Learning of Visual Navigation Using Distances Extracted from Stereo Disparity or Optic Flow*. BU/ECE-2013-1. 2013. URL: `http://people.bu.edu/joshi/files/TechReportNo-ECE-2013-1-LearningVisualNavigation.pdf`.

Theses

[Th1] Schuyler Eldridge. "Neural network computing using on-chip accelerators". PhD thesis. Boston University, 2016. URL: `https://open.bu.edu/handle/2144/19511`.

Workshop Talks and Posters

[W1] Schuyler Eldridge. "What's New in Established HDLs?" In: *Recent Developments in Hardware Description Languages Tutorial at Field-Programmable Custom Computing Machines (FCCM)*. 2022.

[W2] Schuyler Eldridge. "I Wanna Be a Chisel/FIRRTL Developer". In: *3rd Chisel Community Conference (CCC)*. 2020. URL: `https://drive.google.com/file/d/1z79UbAquTBbtCvS_Eefu_ZVuFAqkdpIz/view`.

[W3] Jonathan Bachrach, Schuyler Eldridge, Richard Lin, Jack Koenig, and Adam Izraelevitz. "CCC 2018 Keynote". In: *1st Chisel Community Conference (CCC)*. 2018. URL: `https://www.youtube.com/watch?v=MvmchgayCq4`.

[W4] Schuyler Eldridge. "Chisel Libraries Breakdown". In: *1st Chisel Community Conference (CCC)*. 2018. URL: `https://www.youtube.com/watch?v=uLDGh0Hq1Ik`.

[W5] Schuyler Eldridge and Pradip Bose. "Agile System Development using Open Source Hardware Components". In: *Workshop on Modeling and Simulation of Systems and Applications (ModSim)*. 2018.

[W6] Schuyler Eldridge and Pradip Bose. "System Architectural Support for AI at the Edge". In: *2nd Workshop on Advances in IoT Architecture and Systems (AIoTAS)*. 2018.

[W7] Schuyler Eldridge, Ramon Bertran, Alper Buyuktosunoglu, and Pradip Bose. "MicroProbe: An Open Source Microbenchmark Generator Ported to the RISC-V ISA". In: *7th RISC-V Workshop*. 2017. URL: `https://content.riscv.org/wp-content/uploads/2017/12/Tue1424-riscv-microprobe-presentation.pdf`.

[W8] Schuyler Eldridge, Han Dong, Thomas Unger, Marcia Sahaya Louis, Leila Delshad Tehrani, Jonathan Appavoo, and Ajay Joshi. "X-FILES/DANA: RISC-V Hardware/Software for Neural Networks". In: *4th RISC-V Workshop*. 2016. URL: `http://people.bu.edu/schuye/files/riscv2016-eldridge-poster.pdf`.

[W9] Schuyler Eldridge, Marcia Sahaya Louis, Thomas Unger, Jonathan Appavoo, and Ajay Joshi. "Learning-on-chip using Fixed Point Arithmetic for Neural Network Accelerators". In: *53rd Annual Design Automation Conference (DAC)*. 2016. URL: `http://people.bu.edu/schuye/files/dac2016-eldridge-poster.pdf`.

[W10] Schuyler Eldridge, Thomas Unger, Marcia Sahaya Louis, Margo Seltzer, Jonathan Appavoo, and Ajay Joshi. "Neural Networks as Function Primitives: Software/Hardware Support with X-FILES/DANA". In: *Boston Area Architecture Conference (BARC)*. 2016. URL: `http://people.bu.edu/joshi/files/eldridge_barc2016.pdf`.

Panel Participation

Panelist: "Building Efficient and Resilient AI Systems"	03/2018
3rd Workshop on Cognitive Architectures	Williamsburg, VA
Panelist: "Open Discussion – Current State of RISC-V Research"	10/2017
1st Workshop on Computer Architecture Research with RISC-V (CARRV)	Boston, MA

Thesis Committees

4^{th} Reader	Ph. D.	University of Virginia	Alec Roelke, "Improving Reliability and Security with Aging and Pre-RTL Modeling"	2018

Doctoral Advisor

Ajay Joshi (Boston University)