## Education

| | | |
|---|---|---|
| Boston University, Boston, MA | Computer Engineering | Ph. D., 2016 |
| Boston University, Boston, MA | Electrical Engineering | B. S., 2010 |

## Employment History

| | | |
|---|---|---|
| Postdoctoral Researcher | Reliability and Power Aware Microarchitectures<br>IBM T. J. Watson Research Center, NY | 08/16–present |
| Space Technology Research Fellow | Robotic Systems Estimation, Decision, and Control<br>NASA Jet Propulsion Lab, Pasadena, CA | 05/15–07/15<br>06/14–08/14<br>06/13–08/13 |
| Graduate Technical Intern | Server Memory Controller Validation<br>Intel Corporation, Hudson, MA | 05/11–09/11 |
| Graduate Technical Intern | Data Center and Connected Systems<br>Intel Corporation, Hudson, MA | 07/10–08/10 |
| Undergraduate Teaching Assistant | Undergraduate Logic Design<br>Boston University | 01/10–05/10<br>01/09–05/09 |

## Honors, Awards, and Fellowships

| | |
|---|---|
| NASA Space Technology Research Fellowship | 08/12–08/16 |
| CELEST/CompNet Award | 2012/04/23 |
| Boston University Dean's Fellowship | 09/10–09/11 |
| P. T. Hsu Memorial Award for Outstanding Senior Design Project | 2010/05/03 |
| Boston University Engineering Scholar Award | 09/06–05/10 |

## Grants

| | | | |
|---|---|---|---|
| PERFECT: Efficient Resilience in Embedded Computing | DARPA | Staff | 2016/08/27–2018/08/31 |
| DSSoC: Domain Specific System on Chip | DARPA | Staff | 2018/08/01–present |

## Program Committees and Reviews

| | | |
|---|---|---|
| Chisel Community Conference (CCC) | Program Committee | 2018 |
| IEEE Micro | Article Reviewer | 2018 |
| IEEE Micro | Article Reviewer | 2016 |

## Open Source Activities (GitHub)

### Maintainer

| | | | |
|---|---|---|---|
| seldridge/verilog | Verilog | Repository for basic (and not so basic) Verilog blocks with high re-use potential | 126 Stars |
| bu-icsg/dana | Scala | Dynamically Allocated Neural Network Accelerator for the RISC-V Rocket Microprocessor in Chisel | 70 Stars |
| seldridge/rocket-rocc-examples | C | Tests for example Rocket Custom Coprocessors | 16 Stars |
| IBM/hdl-tools | Tcl | Facilitates building open source tools for working with hardware description languages (HDLs) | 16 Stars |
| IBM/rocc-software | C | C/Assembly macros for talking with Rocket Custom Coprocessors (RoCCs) | 11 Stars |
| IBM/perfect-chisel | Scala | Chisel artifacts developed under IBM's involvement with the DARPA PERFECT program | 8 Stars |
| IBM/firrtl-mode | Emacs Lisp | Major mode for editing FIRRTL files in Emacs | 1 Stars |
| IBM/chiffre | Scala | A fault-injection framework using Chisel and FIRRTL | 1 Stars |

### Contributor

| | | | |
|---|---|---|---|
| freechipsproject/rocket-chip | Scala | Rocket Chip Generator | 25 commits 411++ 198-- |
| freechipsproject/firrtl | Scala | Flexible Intermediate Representation for RTL | 17 commits 1582++ 622-- |
| riscv/riscv-fesvr | C | RISC-V Frontend Server | 9 commits 298++ 148-- |
| freechipsproject/chisel3 | Scala | Constructing Hardware in a Scala Embedded Language version 3 | 6 commits 469++ 7-- |
| riscv/riscv-tools | Shell | RISC-V Tools (GNU Toolchain, ISA Simulator, Tests) | 3 commits 3++ 3-- |
| ucb-bar/chisel | Scala | Constructing Hardware in a Scala Embedded Language version 2 | 2 commits 17++ 3-- |
| ucb-bar/generator-bootcamp | Scala | Generator Bootcamp Material: Learn Chisel the Right Way | 1 commit 4++ 4-- |
| ccelio/riscv-boom-doc | LaTeX | Documentation for the BOOM processor | 1 commit 1++ 1-- |
| melpa/melpa | Emacs Lisp | Recipes and build machinery for the biggest Emacs package repo | 1 commit 3++ 0-- |

## Publications

### Peer Reviewed Conference Publications


[1] Schuyler Eldridge, Alper Buyuktosunoglu, and Pradip Bose. "Chiffre: A Configurable Hardware Fault Injection Framework for RISC-V Systems". In: *2nd Workshop on Computer Architecture Research with RISC-V (CARRV '18)*. 2018. URL: https://carrv.github.io/2018/papers/CARRV_2018_paper_2.pdf.

[2] Schuyler Eldridge, Vaibhav Verma, Xinfei Guo, Alec Roelke, Karthik Swaminathan, Nandhini Chandramoorthy, Martin Cochet, Alper Buyuktosunoglu, Christos Vezyrtzis, Rajiv Joshi, Matt Ziegler, Mircea Stan, and Pradip Bose. "VELOUR: Very Low Voltage Operation Under Resilience Constraints". In: *50th GOMACTech Conference*. 2018.

[3] Mateja Putic, Swagath Venkataramani, Schuyler Eldridge, Alper Buyuktosunoglu, Pradip Bose, and Mircea Stan. "DyHard-DNN: Even More DNN Acceleration with Dynamic Hardware Reconfiguration". In: *55th Annual Design Automation Conference (DAC)*. 2018.

[4] Ramon Bertran, Pradip Bose, David M. Brooks, Jeff Burns, Alper Buyuktosunoglu, Nandhini Chandramoorthy, Eric Cheng, Martin Cochet, Schuyler Eldridge, Daniel Friedman, Hans M. Jacobson, Rajiv V. Joshi, Subhasish Mitra, Robert K. Montoye, Arun Paidimarri, Pritish Parida, Kevin Skadron, Mircea Stan, Karthik Swaminathan, Augusto Vega, Swagath Venkataramani, Christos Vezyrtzis, Gu-Yeon Wei, John-David Wellman, and Matthew M. Ziegler. "Very Low Voltage (VLV) Design". In: *2017 IEEE International Conference on Computer Design, ICCD 2017, Boston, MA, USA, November 5-8, 2017*. 2017, pp. 601–604. URL: https://doi.org/10.1109/ICCD.2017.105.

[5] Leila Delshadtehrani, Jonathan Appavoo, Manuel Egele, Ajay Joshi, and Schuyler Eldridge. "Varanus: An Infrastructure for Programmable Hardware Monitoring Units". In: *Boston Area Architecture Conference (BARC)*. Jan. 2017. URL: https://megele.io/barc2017.pdf.

[6] Schuyler Eldridge, Karthik Swaminathan, Nandhini Chandramoorthy, Alper Buyuktosunoglu, Alec Roelke, Vaibhav Verma, Rajiv Joshi, Mircea Stan, and Pradip Bose. "A Low Voltage RISC-V Heterogeneous System". In: *1st Workshop on Computer Architecture Research with RISC-V (CARRV '17)*. 2017. URL: https://carrv.github.io/2017/papers/eldridge-velour-carrv2017.pdf.

[7] Schuyler Eldridge and Ajay Joshi. "Exploiting Hidden Layer Modular Redundancy for Fault-Tolerance in Neural Network Accelerators". In: *Boston Area Architecture Conference (BARC)*. Jan. 2015. URL: http://people.bu.edu/joshi/files/Eldridge_BARC_2015.pdf.

[8] Schuyler Eldridge, Amos Waterland, Margo Seltzer, Jonathan Appavoo, and Ajay Joshi. "Towards General-Purpose Neural Network Computing". In: *2015 International Conference on Parallel Architecture and Compilation, PACT 2015, San Francisco, CA, USA, October 18-21, 2015*. IEEE Computer Society, Oct. 2015, pp. 99–112. ISBN: 978-1-4673-9524-3. URL: https://dash.harvard.edu/bitstream/handle/1/30779603/82681851.pdf?sequence=1.

[9] Jonathan Appavoo, Amos Waterland, Schuyler Eldridge, Katherine Zhao, Ajay Joshi, Steve Homer, and Margo Seltzer. "Programmable Smart Machines: A Hybrid Neuromorphic Approach to General Purpose Computation". In: *NeuroArch Workshop*. 2014. URL: http://people.bu.edu/joshi/files/appavoo-neuroarch-2014.pdf.

[10] Schuyler Eldridge, Florian Raudies, David Zou, and Ajay Joshi. "Neural network-based accelerators for transcendental function approximation". In: *Great Lakes Symposium on VLSI 2014, GLSVLSI '14, Houston, TX, USA - May 21 - 23, 2014*. 2014, pp. 169–174. URL: http://people.bu.edu/joshi/files/glsvlsi2014-eldridge.pdf.

[11] Schuyler Eldridge, Florian Raudies, and Ajay Joshi. "Approximate Computation using a Neuralized Floating Point Unit". In: *Brain Inspired Computing Workshop*. 2013. URL: http://people.bu.edu/joshi/files/approx-fpu-bic2013.pdf.

### Peer Reviewed Journal Articles

[1] Leila Delshadtehrani, Schuyler Eldridge, Sadullah Canakci, Manuel Egele, and Ajay Joshi. "Nile: A Programmable Monitoring Coprocessor". In: *Computer Architecture Letters* 17.1 (2018), pp. 92–95. URL: https://doi.org/10.1109/LCA.2017.2784416.

[2] F. Raudies, S. Eldridge, A. Joshi, and M. Versace. "Learning to Navigate in a Virtual World using Optic Flow and Stereo Disparity Signals". In: *Artificial Life and Robotics* 19.2 (2014), pp. 157–169. URL: https://link.springer.com/article/10.1007/s10015-014-0153-1.

### Patents

[1] Vinodh Gopal, James D. Guilford, Schuyler Eldridge Gilbert M. Wolrich, Erdinc Ozturk, and Wasdi K. Feghali. "Digest Generation". US9292548B2. Intel Corporation. 2016.

### Demonstrations

[1] Alec Roelke, Schuyler Eldridge, and Mircea Stan. "VELOUR: Very Low Voltage Operation Under Resilience Constraints". In: *3rd Workshop on Cognitive Architectures*. 2018.

### Technical Reports

[1] F. Raudies, S. Eldridge, A. Joshi, and M. Versace. *Reinforcement Learning of Visual Navigation Using Distances Extracted from Stereo Disparity or Optic Flow*. BU/ECE-2013-1. 2013. URL: http://people.bu.edu/joshi/files/TechReportNo-ECE-2013-1-LearningVisualNavigation.pdf.

### Theses

[1] "Neural network computing using on-chip accelerators". PhD thesis. Boston University, 2016. URL: https://open.bu.edu/handle/2144/19511.

## Workshop Talks and Posters

[1] Schuyler Eldridge and Pradip Bose. "Agile System Development using Open Source Hardware Components". In: *Workshop on Modeling and Simulation of Systems and Applications (ModSim)*. 2018.

[2] Schuyler Eldridge and Pradip Bose. "System Architectural Support for AI at the Edge". In: *2nd Workshop on Advances in IoT Architecture and Systems (AIoTAS)*. 2018.

[3] Schuyler Eldridge, Ramon Bertran, Alper Buyuktosunoglu, and Pradip Bose. "MicroProbe: An Open Source Microbenchmark Generator Ported to the RISC-V ISA". In: *7th RISC-V Workshop*. 2017. URL: https://content.riscv.org/wp-content/uploads/2017/12/Tue1424-riscv-microprobe-presentation.pdf.

[4] Schuyler Eldridge, Han Dong, Thomas Unger, Marcia Sahaya Louis, Leila Delshad Tehrani, Jonathan Appavoo, and Ajay Joshi. "X-FILES/DANA: RISC-V Hardware/Software for Neural Networks". In: *4th RISC-V Workshop*. 2016. URL: http://people.bu.edu/schuye/files/riscv2016-eldridge-poster.pdf.

[5] Schuyler Eldridge, Marcia Sahaya Louis, Thomas Unger, Jonathan Appavoo, and Ajay Joshi. "Learning-on-chip using Fixed Point Arithmetic for Neural Network Accelerators". In: *53rd Annual Design Automation Conference (DAC)*. 2016. URL: http://people.bu.edu/schuye/files/dac2016-eldridge-poster.pdf.

[6] Schuyler Eldridge, Thomas Unger, Marcia Sahaya Louis, Margo Seltzer, Jonathan Appavoo, and Ajay Joshi. "Neural Networks as Function Primitives: Software/Hardware Support with X-FILES/DANA". In: *Boston Area Architecture Conference (BARC)*. 2016. URL: http://people.bu.edu/joshi/files/eldridge_barc2016.pdf.

## Panel Participation

| | |
|---|---|
| Panelist: "Open Discussion – Current State of RISC-V Research"<br>1st Workshop on Computer Architecture Research with RISC-V (CARRV) | 2017/10/14<br>Boston, MA |
| Panelist: "Building Efficient and Resilient AI Systems"<br>3rd Workshop on Cognitive Architectures | 2018/03/24<br>Williamsburg, VA |

## Thesis Committees

| | | | | |
|---|---|---|---|---|
| $4^{\text{th}}$ Reader | Ph. D. | University of Virginia | Alec Roelke, "Improving Reliability and Security with Aging and Pre-RTL Modeling" | 2018 |

## Doctoral Advisor

Ajay Joshi (Boston University)