Jade Bird Display

JBD013VGA Datasheet

Revision: v2.24

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JADE BIRD DISPLAY (SHANGHAI) LIMITED

JBD013VGA

640x480 uLED display with SPI/Quad-SPI interface

Features

- **Pixel:**
  - Resolution: 640x480
  - Total number of pixels: 660x504
  - Color: monochrome (Red/Blue/Green)
  - Pixel pitch: 4μm
  - Active area: 2.64mm x 2.02mm (0.13-inch Diagonal)
  - Luminance: Max Brightness driving at 50A/cm2
    - 450nm is 500K Cd/m2
    - 525nm is 4000K Cd/m2
    - 625nm is 200K Cd/m2
  - Gray levels: 16 (4bit)
  - ULED panels can self-refresh internally and refresh rate is from 30Hz to 480Hz.
- **Memories**
  - 1.2M bits of SRAM memory
- **Reset and power management**
  - I/Os supply: V_{DD} = 1.62V to 3.6V
    - (Typical:1.8v)
  - Core supply: V_{DDCORE} = 1.08V to 1.32V
    - (Typical:1.2v)
  - Cathode supply: V_{COM}= -1.3V to -3.0V
    - (Typical:-2v)
  - Low power modes: Screen off, Deep power down
- **Clock management**
  - External crystal resonator
  - External clock input
  - Internal OSC compatible
- **Control**
  - Luminance control: Register configuration
  - Control & data transfer interface: Quad-SPI/SPI
  - Adjustable Center of image(640x480) in range of pixel area (660x504)
- **Display Control**
  - Display enable/disable
  - Image mirror (up down / left right)
  - Self-test
- **Communication interfaces**
  - Up to two SPI interfaces
    - Standard Mode supports normal SPI protocol, maximum data rate 32 Mbit/s.
    - Quad Mode supports Quad-SPI protocol, maximum data rate 128 Mbps.
- **IC Power consumption**
  - Typically, 30mW, variable depending on image content and global brightness.
  - Deep power down current < 50uA.
- **Temperature range**
  - Operating temperature range: -20°C to 85°C
  - Storage temperature: -40°C to 90°C

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1 Description

The JBD013VGA uLED panel is an active-matrix micro display intended for near-to-eye applications that demand high brightness, compact size and low power consumption. The active array is composed of 640*480 circular pixels with 4um pitch. JBD013VGA is a micro LED display chip with SPI/QSPI interface.

Table 1. JBD013VGA device features

Key Features	JBD013VGA
Format Resolution	640 * 480
Total Pixels	660 * 504
Pixel dimension	4um * 4 um
Active Area	2.64mm * 2.02mm
Die Size	3.64 mm* 4.28mm
Package Size	4.12 mm* 5.82mm
Gray scale	16 (4 bits)
Panel Refresh Rate	30~480 Hz
Interface	Quad-SPI/SPI
Integrated memory	1.2Mb
Cable	FPC/FFC
uLED Voltage	3.2V
IC backplane power consumption	30mW
DPD Mode power consumption	<50uA
Operating temperature	-20°C to 85°C
Storage temperature	-40°C to 90°C

Note: DPD → Deep Power Down

The top-level block diagram for JBD013VGA IC is shown in *Figure 2*. The IC mainly contains register & control circuit, buffer circuit, pixel array, and SPI/QSPI interface. Pixel buffer receives external pixel data and transfers them into pixel array line by line. Pixel buffer can store one full frame data. After the Pixel buffer receives the correct frame data, Sync command needs to be sent to transfer buffer data to pixel driver array. High frequency data and control signals are transferred through SPI/Quad-SPI interface. The corresponding register needs to be configured with SPI/Quad-SPI command before pixel data can be transferred. The pixel data can also be directly transferring into the pixel driver array with bypassing the pixel buffer to obtain a lower display latency. However, this mode can only support frame data with 1-bit gray level.

2 Pin Description

Figure 1. Pin Diagram (Die view)

Table 2. JBD013VGA pin definition

Name	Function	Input type	Output type	Description
SCLK	SCLK	ST	-	Serial clock input
CSB	CSB	ST	-	Chip select input
SI/IO0	SI	ST	-	SPI data input
	IO0	ST	CMOS	Quad SPI data input output 0
SO/IO1	SO	ST	CMOS	SPI data output
	IO1	ST	CMOS	Quad SPI data input output 1
IO2	IO2	ST	CMOS	Quad SPI data input output 2
IO3	IO3	ST	CMOS	Quad SPI Data input output 3
XIN/CLKIN	XIN	XTAL	XTAL	Crystal in
	CLKIN	ST	-	External clock input
XOUT	XOUT	XTAL	XTAL	Crystal output
RSTN	RSTN	RST	-	Reset input
VDDIO	VDDIO	Power	-	IO Power Supply
VDD12IO	VDDIO	Power	-	1.2V IO Core Power Supply
VDD12	VDD CORE	Power	-	1.2V Internal Power Supply
VDD12P	VDD Panel	Power	-	1.2v Power for panel
VCOM	VCOM	Power	-	-1.3V~-3.0V Cathode Voltage
GND	GND	Power	-	Ground reference

Legend: CMOS= CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

XTAL = Crystal levels

RST=Reset pin with embedded weak pull-up resistor

3 Block Diagram

Figure 2. Panel IC Diagram

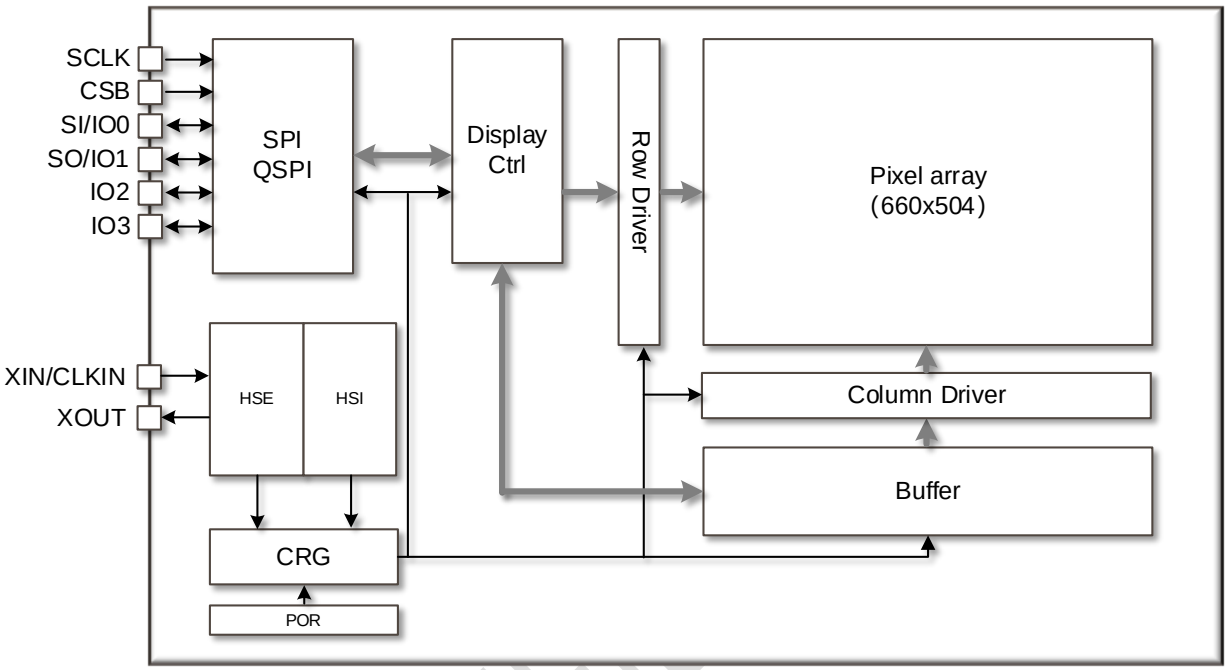
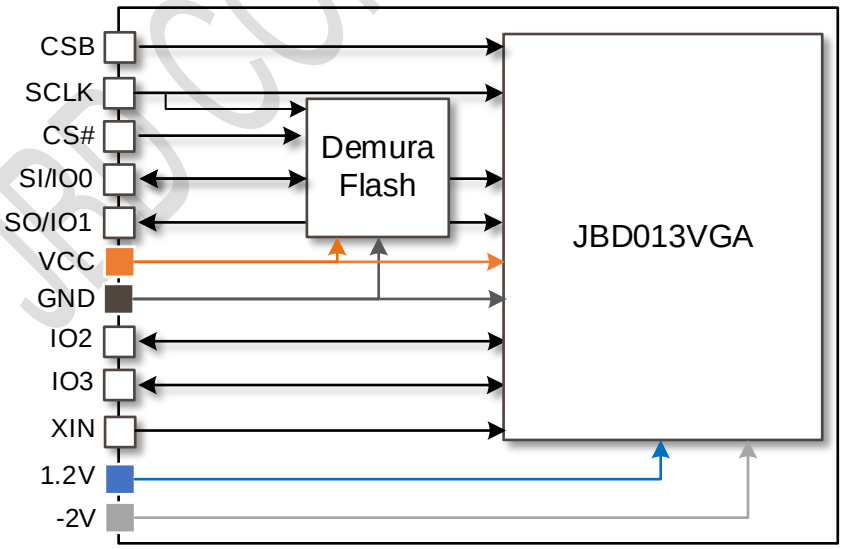


Figure 3. Package Diagram



4 Functional Description

4.1 Display operation

4.1.1 Display Control

The Panel refresh rate can be set to 30Hz~480Hz through register configurations.

Display disable: All uLED pixels scan signals are turned off.

Display enable: All uLED pixels scan signals are ready to turn on.

Image mirror: Mirror panel image through corresponding command, Up/Down or Left/Right. Ref *Figure 4*.

Self-test: The panel can show internal test patterns through self-test commands, which can be used to check the quality of panel. Ref *Figure 5*.

Figure 4 Mirror Operation Diagram

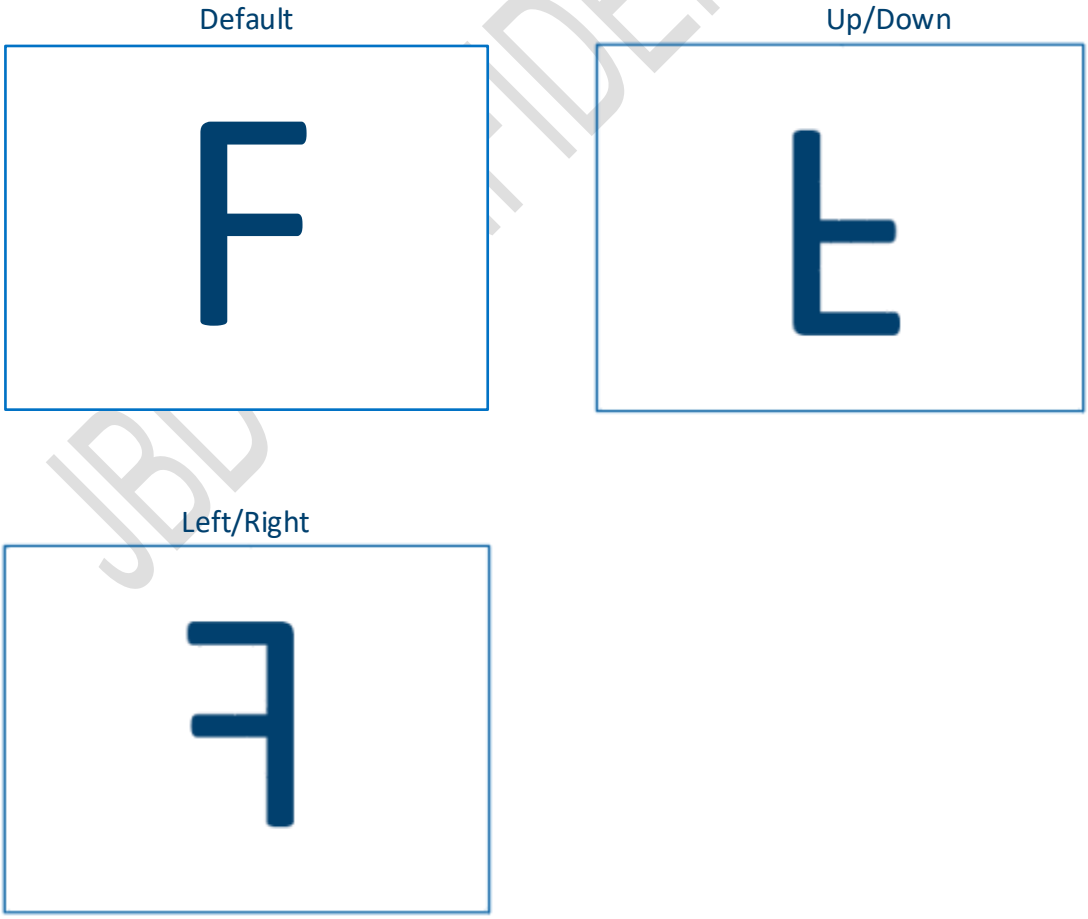
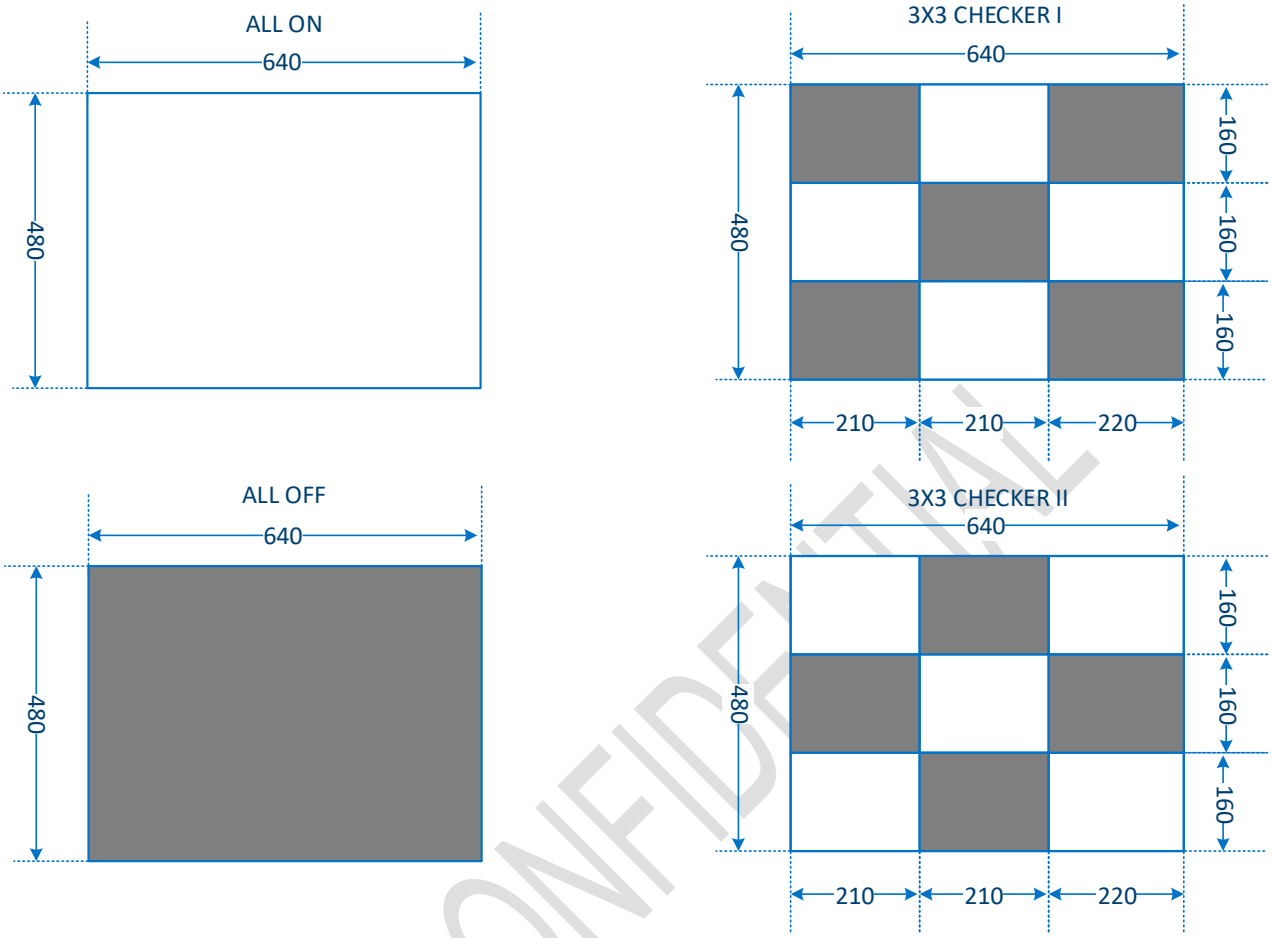


Figure 5 Self-test Image Diagram



4.1.2 Display Solution

Resolution: 640x480

Total number of pixels: 660x504, extra 20 columns and 24 rows pixels for optical alignment purpose.

Color: monochrome (Red/Blue/Green)

4.1.3 Brightness Control

Brightness control: There are above 5000 adjustment levels for global brightness adjusted by register configurations.

4.1.4 Display Process Flow

Before displaying an image or video on the panel, the value of configuration registers need to be set at first. Then the Display Enable command is needed to send.

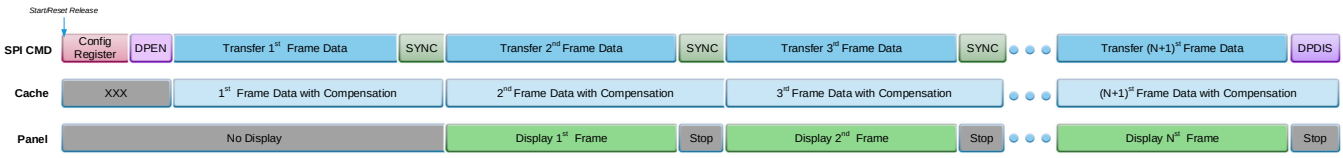
This is followed by transferring the frame data to buffer space. Next, a SYNC command is sent to update the buffer data to panel.

The screen is turned OFF during SYNC period (about 1ms). The screen turns ON and the panel displays the image after SYNC is finished. The panel display scan frequency can be adjusted by configuration register.

Master device can transfer subsequent frame data during the period of panel display, another SYNC command will update the panel image.

If nothing needs to be displayed, the Display disable command is used. See the diagram below:

Figure 6 Display Process Flow Diagram



4.2 Data Operation

4.2.1 Internal Buffer Control

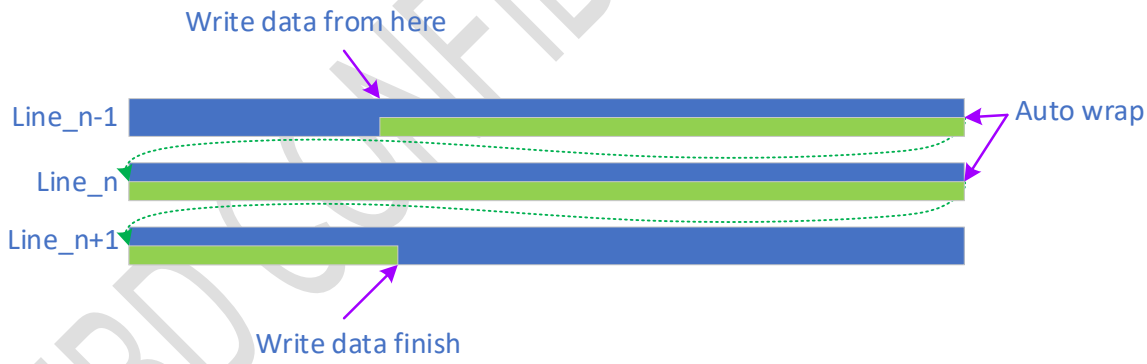
Internal Buffer is used to store frame data. Also, the data in the Buffer can be read out via SPI interface for confirmation purpose. Once the full frame data is ready in the buffer, a synchronization command is issued to enable the pixel data in the memory be loaded into the pixel array circuits.

The IC backplane can support 3 different data transfer modes for pixel data written to or read from buffer: 4-bit pixel data transferred via SPI interface, 4-bit pixel data transferred via QSPI interface and 1-bit pixel data transferred via QSPI interface. Customers can configure the data transfer mode by register configurations.

4.2.2 Partial refresh mechanism

Based on the way of SPI/QSPI write buffer by address, the function of pixel partial update can be realized, so as to achieve the purpose of more efficient update of panel images. Write the buffer with SPI/QSPI, which can automatically wrap lines inside the chip, so that it is more flexible to update partial data in buffer.

Figure 7 Auto wrap diagram

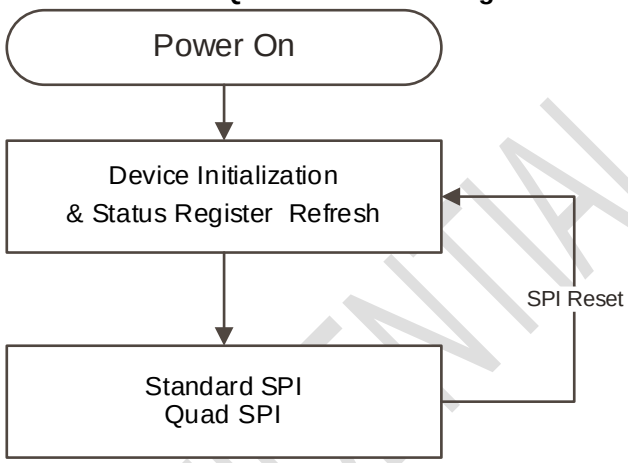


4.3 Serial Peripheral Interface (SPI)

Both standard SPI protocol and Quad SPI protocol can be supported by configuring the corresponding registers.

The IC backplane can support both standard SPI and Quad SPI interface. Customers can select one of them with corresponding commands.

Figure 8. Standard SPI & Quad SPI Status Diagram



4.3.1 Standard SPI Instructions

The JBD013VGA is accessed through an SPI compatible bus consisting of four signals: Serial Clock (SCLK), Chip Select (CSB), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI interface uses the SI input pin to write instructions, addresses or data to the device on the rising edge of SCLK. The SO output pin is used to read data or status from the device on the falling edge of SCLK.

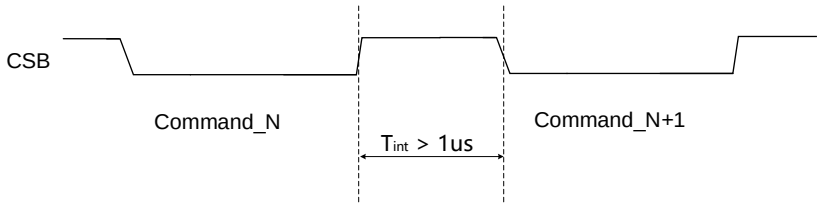
4.3.2 Quad SPI Instructions

The JBD013VGA supports Quad SPI operation when using instructions such as Quad SPI Buffer Write & Read or One-bit Quad SPI Buffer Write & Read. These instructions allow data to be transferred into or from the device at four times the rate of ordinary Serial commands. The Quad Read instructions offer a significant improvement in continuous and random-access transfer rates allowing frame data to RAM or read directly from the SPI bus. When using Quad SPI instructions, the SI and SO pins become bidirectional IO0 and IO1, and the pins IO2 and IO3 is needed respectively.

4.3.3 The timing between SPI/QSPI commands

It should be the time(T_{int}) to keep the CSB high for more than 1 us between spi/qspi commands.

Figure 9 The timing between commands



4.4 Power Management

4.4.1 Power Supply Schemes

- V_{DDIO} = 1.62 to 3.6 V: external power supply for I/Os. Provided externally through VDDIO pins. The V_{DDIO} voltage level must be provided first
- V_{DD12IO} = 1.08 to 1.32 V: external power supply for I/Os core.
- V_{DD12} = 1.08 to 1.32 V: external power supply for IC core.
- V_{DD12P} = 1.08 to 1.32 V: external power supply for IC Panel.
- V_{COM} = -1.3V~-3.0V: external power supply for IC Cathode negative voltage.

4.4.2 Low-Power Modes

The JBD013VGA Display chip supports two low-power modes to achieve the best compromise low power consumption.

- **Screen OFF**

  All the uLED display scan signals are disabled and uLED array is turned off. The panel stays in a power-saving mode.

- **Deep Power Down**

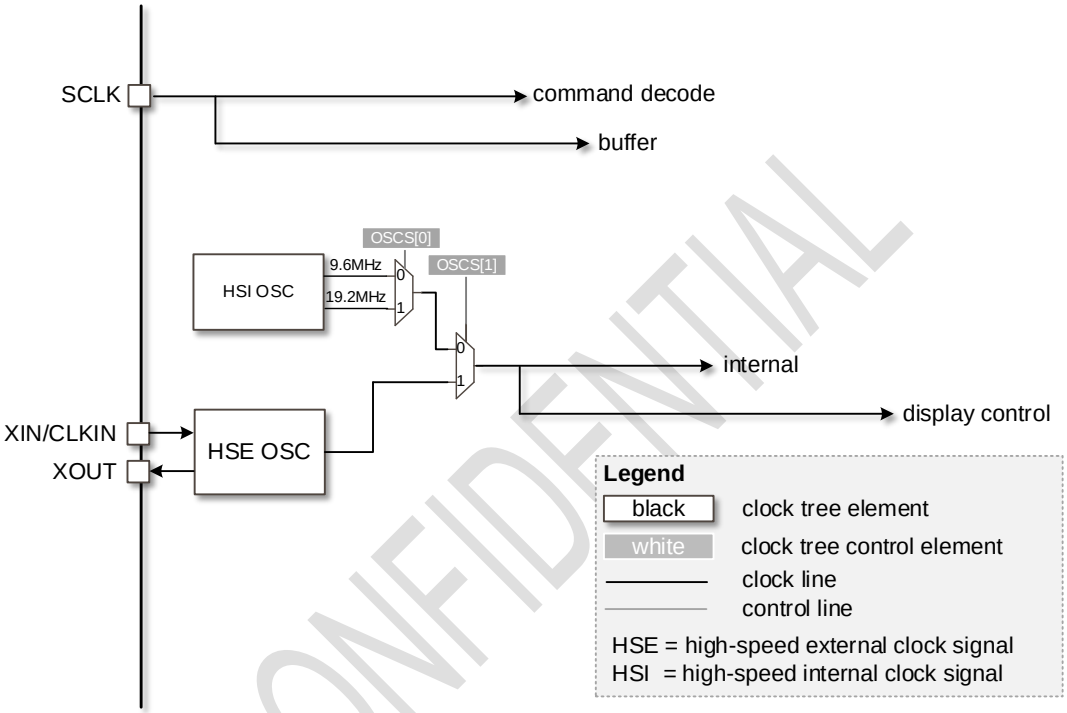
  The Deep Power Down mode is used to achieve the lowest power consumption. The internal OSC or the external crystal oscillators are switched off. Once entering Deep Power Down mode, the content in buffer and registers keeps unchanged.

  The device exits Deep Power Down mode when an external reset (RSTN pin) or Release Deep Power Down command is generated.

4.5 Clocks and Startup

System clock selection is performed on startup. However, the internal RC 9.6MHz oscillator is selected as default clock on reset. And an external clock can also be selected.

Figure 10 Clock Management of JBD013VGA



5 Memory Mapping

Figure 11 Display Pixel Row and Column location map

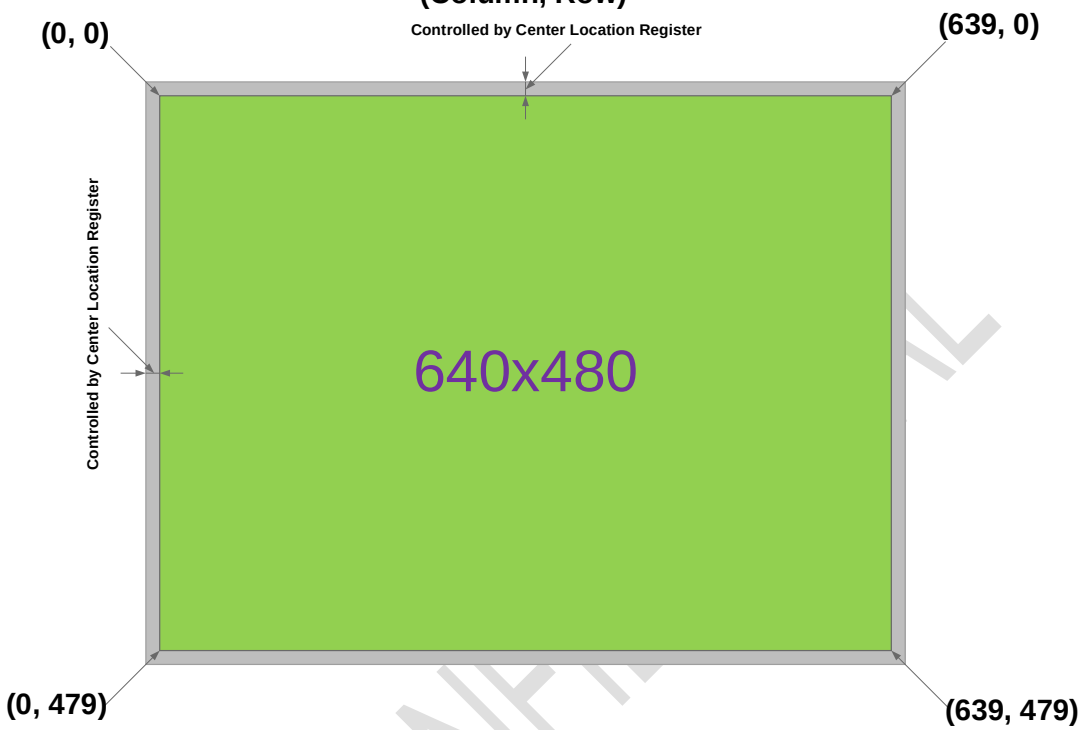
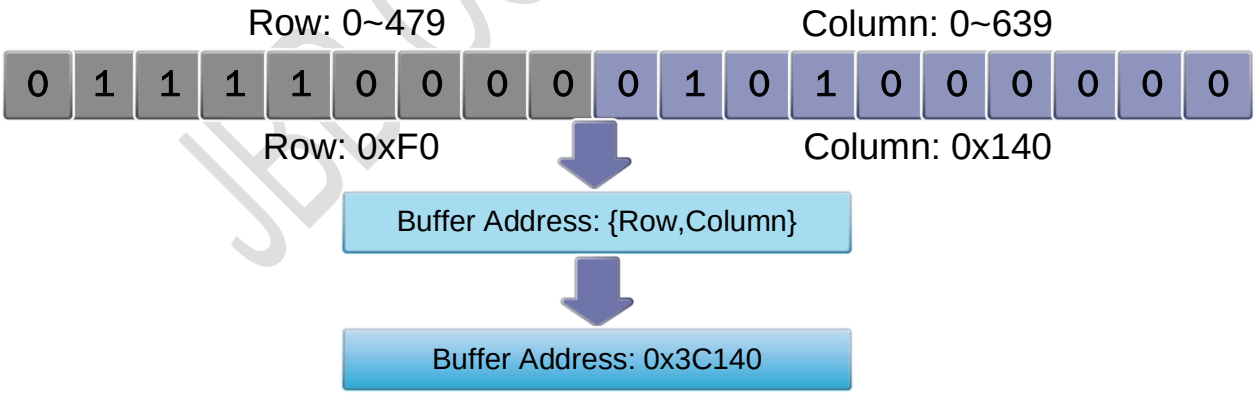


Figure 12 Buffer Address Mapping



6 Status and Configuration Registers

6.1 Registers Map

Table 3. Register Map and Reset Values

Command Control	register	7	6	5	4	3	2	1	0
Luminance Register	**Lum_H**	LUM[15:8]							
	Reset	0	0	0	1	1	0	1	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Lum_L	LUM[7:0]							
	Reset	1	1	0	0	0	1	0	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Current Register R/W	**Cur**	Reserved		CUR[5:0]					
	Reset	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Offset Register R/W	**Row**	Reserved			ROW[4:0]				
	Reset	0	0	0	0	1	1	0	0
	R/W	R0	R0	R0	R/W	R/W	R/W	R/W	R/W
	Column	Reserved			COL[4:0]				
	Reset	0	0	0	0	1	0	1	0
	R/W	R0	R0	R0	R/W	R/W	R/W	R/W	R/W
Status Register 1	**ST1**	W0	GMAEN	RFFQ[2:0]			Reserved		
	Reset	1	0	0	1	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	W0	W0	W0
Status Register 2	**ST2**	Reserved	Reserved	SPF	RFHF	PORF	SYNC_S	OSCS[1]	OSCS[0]
	Reset	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R/W	R/W	R/W	R/W

6.2 Status Registers

Command access: Status Register 1 Read (0x05H) & Write (0x01H)

Reset value: 0x90

7	6	5	4	3	2	1	0
W0	W0	RFFQ [2:0]			Reserved		
R/W	R/W	R/W	R/W	R/W	W0	W0	W0

Bits 7 **W0: Write 0 at any reset release status**

0: Disable demura function (default)

1: Enable demura function

Bits 6 **W0: Write 0 at any reset release status**

0: Disable gamma correction (default)

1: Enable gamma correction

Bits 5:3 **RFFQ** [2:0]: Panel Refresh frequency

If internal OSC 9.6MHz is selected.	If internal OSC 19.2MHz is selected.
000: 30Hz	000: 60Hz
001: 60Hz	001:120Hz
010: 90Hz (default)	010: 180Hz (default)
011: 120Hz	011: 240Hz
100: 150Hz	100: 300Hz
101: 180Hz	101: 360Hz
110: 210Hz	110: 420Hz
111: 240Hz	111: 480Hz

Bits 2:0 Reserved, if used, need to write 3'b000.

Note: Different refresh frequency(**RFFQ**) has different **luminance register** value range, as below:

000: 0~21331;

001: 0~10664;

010: 0~7109;

011: 0~5331;

100: 0~4264;

101: 0~3366;

110: 0~2907;

111: 0~2558;

Command access: Status Register 2 Read(0x35H) & Write(0x31H)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved		SPF	RFHF	PORF	SYNC_S	OSCS [1]	OSCS [0]
R/0	R/0	R	R	R/0	R/W	R/W	R/W

Bits 7:6 Reserved, must be kept at reset value.

Bits 5 **SPF**: Panel Scan Period Flag

0: Not panel scan time

1: The panel is scanning

Bits 4 **RFHF**: Reload buffer data to Pixel Latch flag

0: No reload operation

1: Reload time

Bits 3 **PORF**: Power on reset flag

0: write 0 to clean

1: Power on happened

Bits 2 **SYNC_S**: SYNC command with screen off select

0: SYNC command has screen off function(default)

1: SYNC command has no screen off function(suggestion)

Bits 1:0 **OSCS [1:0]**: Oscillator Selection

00: Internal oscillator 9.6MHz(default)

01: Internal oscillator 19.2MHz(suggestion)

1x: External Crystal/External CLKIN from Pin XIN

6.3 Luminance Register

Command access: Luminance Register Read(0x37H) & Write(0x36H)

Reset value: 0xC5

7	6	5	4	3	2	1	0
LUM [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:0 **Lum [7:0]**: Low 8 bits luminance value.

Reset value: 0x1B

7	6	5	4	3	2	1	0
LUM [15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:0 **Lum [15:8]**: High 8 bits luminance value

6.4 Current Register

Command access: Current Register Read (0x47H) & Write(0x46H)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved		CUR [5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:6 Reserved

Bits 5:0 **Cur [5:0]**: 6 bits micro LED bias current adjust value.

6.5 Offset Register

Command access: Offset Register Read(0xC1H) & Write(0xC0H)

Reset value: 0x0C

7	6	5	4	3	2	1	0
Reserved			ROW [4:0]				
R0	R0	R0	R/W	R/W	R/W	R/W	R/W

Bits 7:5 Reserved, must be kept at reset value.

Bits 4:0 **ROW [4:0]**: Row offset adjust 5 bits value.

Reset value: 0x0A

7	6	5	4	3	2	1	0
Reserved			COL [4:0]				
R0	R0	R0	R/W	R/W	R/W	R/W	R/W

Bits 7:5 Reserved, must be kept at reset value.

Bits 4:0 **COL [4:0]**: Column offset adjust 5 bits value.

7 Instructions

7.1 Device ID and Instruction Set Tables

Table 4. Manufacturer and Device Identification

MANUFACTURER ID	(MF7 – MF0)
JBD Serial Display	0xBD
Device ID	(ID15 – ID0)
JBD013VGA	0x4010

7.2 Instruction Table

Table 5. Instruction Table

Command name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Read ID Operations						
Read ID	9FH	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)		
Release power down	ABH	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)	Dummy	(MF7-MF0)
Deep Power-Down Operations						
Deep Power Down	B9H	Dummy				
Software Reset Operations						
Reset Enable	66H					
Reset	99H					
Display Operations						
Sync	97H					
Display Enable	A3H					
Display Disable	A9H					
Display Default Mode	71H					
Display UPDOWN	72H					
Display RIGHTLEFT	73H					
Luminance Setting						
Luminance Register Write	36H	LUM15-LUM8	LUM7-LUM0			
Luminance Register Read	37H	LUM15-LUM8	LUM7-LUM0			
Current Register Write	46H	CUR7-CUR0				
Current Register Read	47H	CUR7-CUR0				
Display Center Setting						
Offset Register Write	C0H	R4-R0	C4-C0			
Offset Register Read	C1H	R4-R0	C4-C0			
Buffer Operations						
SPI Buffer Write	02H	A23-A16	A15-A8	A7-A0	Dummy	D03-D00，D13-D10
SPI Buffer Read	03H	A23-A16	A15-A8	A7-A0	Dummy	D03-D00，D13-D10
Quad SPI Buffer Write	62H	A23-A16	A15-A8	A7-A0	Dummy	D03-D00，D13-D10
Quad SPI Buffer Read	63H	A23-A16	A15-A8	A7-A0	Dummy	D03-D00，D13-D10
Protect Operations						
Write Enable	06H					
Write Disable	04H					
Status & Flag Register Operations						
Write Status Register 1	01H	S17-S10				
Read Status Register 1	05H	S17-S10				
Write Status Register 2	31H	S27-S20				
Read Status Register 2	35H	S27-S20				
Write Status Register3	57H	S37-S30				
Read Status Register3	59H	S37-S30				
Check Sum Read	42H	CS15-CS8	CS7-CS0			
SELF-TEST						
ALL OFF	13H					
ALL ON	14H					
3X3 CHK I	15H					
3X3 CHK II	16H					

Note: Single commands need keep last SI/IO0 value at least 1us (Tcmdh>1us) after CSB going high.

Single commands include software reset operations, display operations, protect operations and self test operations.

Temperature sensor read refer to 7.3.27.

OTP read refer to 7.3.28.

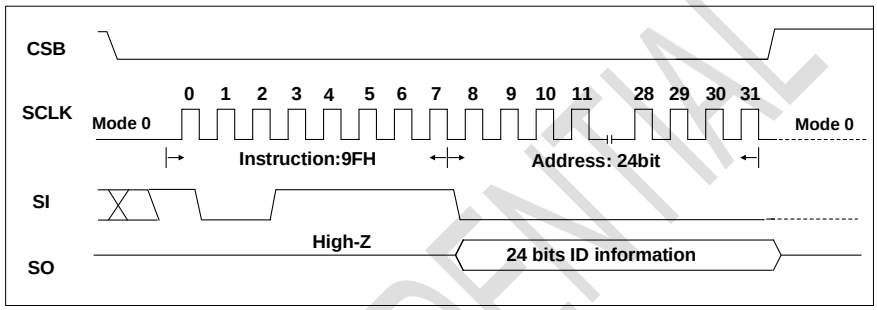
7.3 Instruction Descriptions

7.3.1 Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two Bytes of device identification.

The device is first selected by driving CSB low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CSB high at any time during data output.

Figure 13. Read ID Sequence Diagram (SPI)



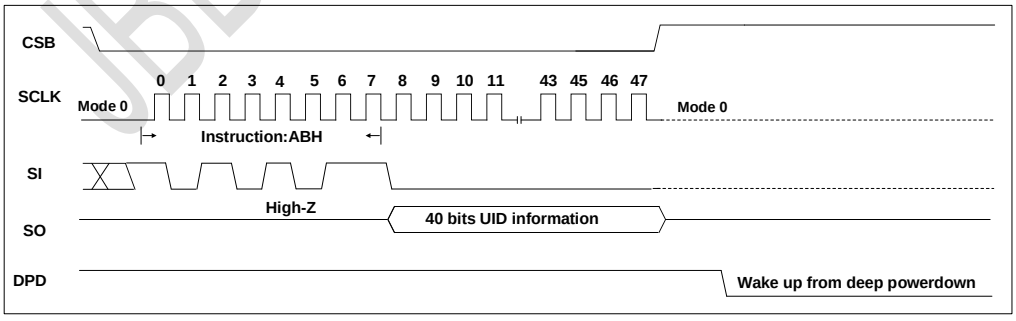
CMD	IO	Byte 1	Byte 2	Byte 3	Byte 4
RDID	SI	9FH	00H	00H	00H
	SO		(MF7-MF0)	(ID15-ID8)	(ID7-ID0)

7.3.2 Release Deep Power Down (ABH)

Release Deep Power Down sequence: CSB goes low → sending Read Unique ID command → 40bit Unique ID information Out → CSB goes high.

Release Deep Power Down is one way to wakeup IC from deep power down status.

Figure 14. Release Deep Power Down Diagram (SPI)



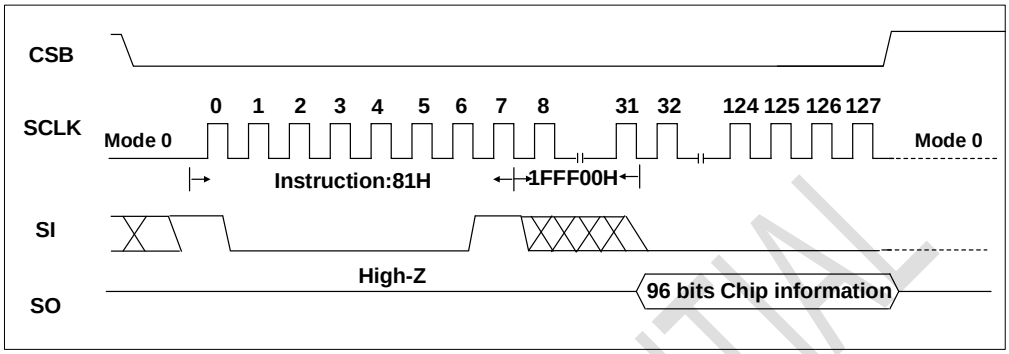
CMD	B	1	2	3	4	5	6
Release DPD	SI	ABH	00H	00H	00H	00H	00H
	SO		MF	(ID15-ID8)	(ID7-ID0)	Dummy	(MF7-MF0)

7.3.3 Read Chip Information (81H)

The Read Chip Information command read chip information that is unique to each device.

The Read Chip Information command sequence: CSB goes low → sending Read Chip Information command → 96bit chip information Out → CSB goes high.

Figure 15. Read Chip Information Sequence Diagram (SPI)



CMD	B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
RDINF	SI	81H	1FH	FFH	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H
	SO					MF	WaferID					Year	Month	Day	4in12	X_Loc	Y_Loc

7.3.4 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation (except in Continuous Read Mode) will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits.

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in SPI mode. The “Reset (99H)” command has the following sequence: CSB goes low → Sending Enable Reset command → CSB goes high → CSB goes low → Sending Reset command → CSB goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST} / t_{RST_E} to reset. During this period, no command will be accepted. Data corruption may happen when Reset command sequence is accepted by the device. It is recommended to check the Status Register before issuing the Reset command sequence.

Figure 16. Enable Reset Diagram (SPI)

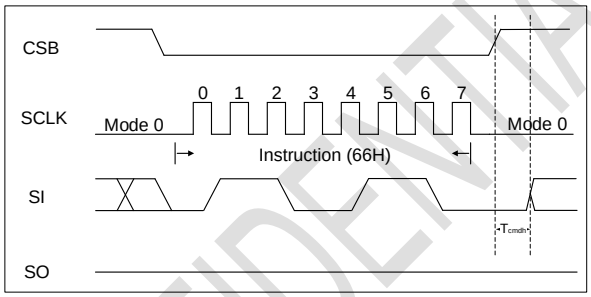
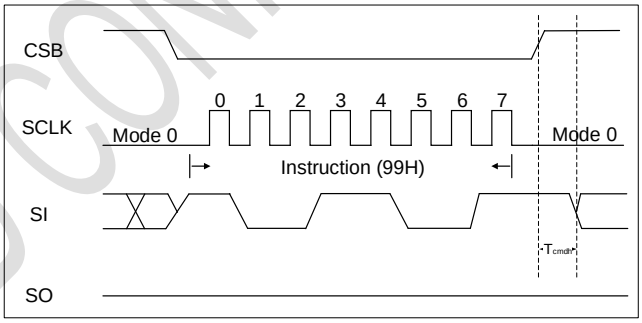


Figure 17. Reset command Diagram (SPI)



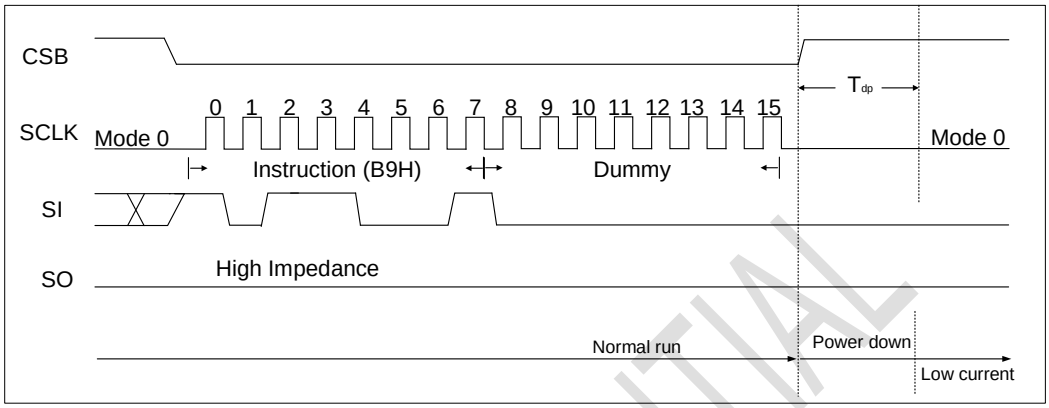
7.3.5 Deep Power-Down (DPD) (B9H)

Executing the Deep Power-Down (DPD) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all other commands. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down (ABH) or Enable Reset (66H) and Reset (99H) commands. These commands can release the device from this mode. The Release from Deep Power-Down command releases the device from deep power down mode.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power-Up. The Deep Power-Down command sequence: CSB goes low → sending Deep Power-Down command → CSB goes high. CSB must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP)

command is not executed. As soon as CSB is driven high, it requires a delay of T_{dp} (>1us) before the supply current is reduced to IC and the Deep Power-Down Mode is entered. Any Deep Power-Down (DPD) command, while other command except RESET or release from Power-Down is in progress, is rejected without having any effects on the cycle that is in progress.

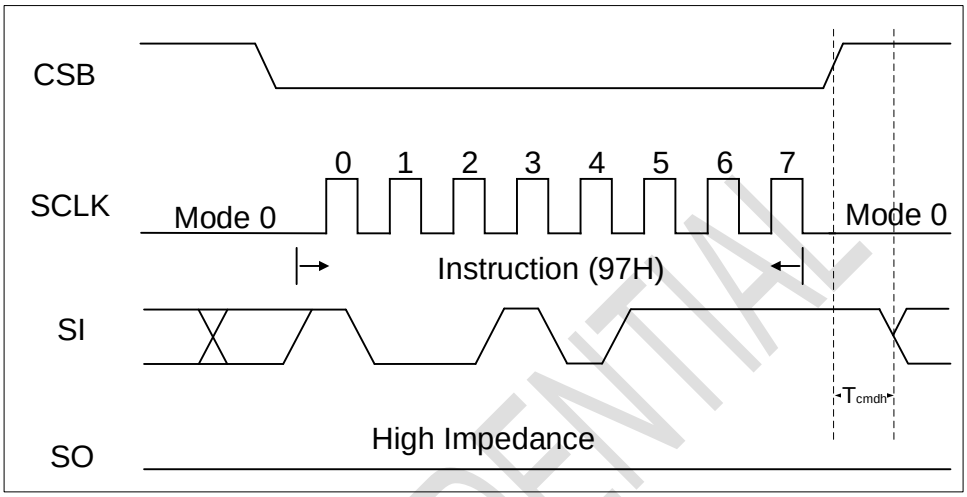
Figure 18. Deep Power-Down Sequence Diagram (SPI)



7.3.6 Sync (97H)

Reload buffer data to Pixel latch, and start to scan screen, then the screen displays normally. It is necessary to reserve 0.83ms @ 9.6MHz system clock or 0.42ms @ 19.2MHz system clock time keeping the full reloading period.

Figure 19 Sync Command Diagram



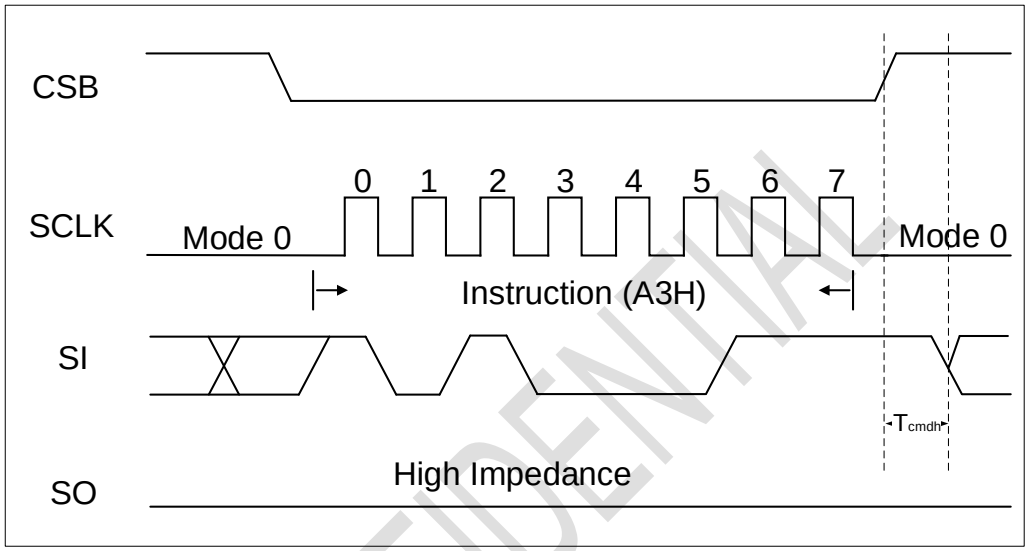
Users need to know that synchronization requires time, and data transfer to the buffer during synchronization is prohibited, which can lead to unexpected errors. The time required is as follows:

	Clock frequency(MHz)	sync time(ms)
External clock	8	1.00
	16	0.50
	20	0.40
	32	0.25
Internal OSC	9.6	0.83
	19.2	0.42

7.3.7 Display enable (A3H)

Turn on panel scan signals, the panel prepares to drive u-LEDs. And SYNC command is needed to active LEDs driving signal. The u-LED's status is based on gray value from SPI or buffer. Please avoid long-time full screen on since it will generate higher power consumption.

Figure 20 Display Enable Diagram

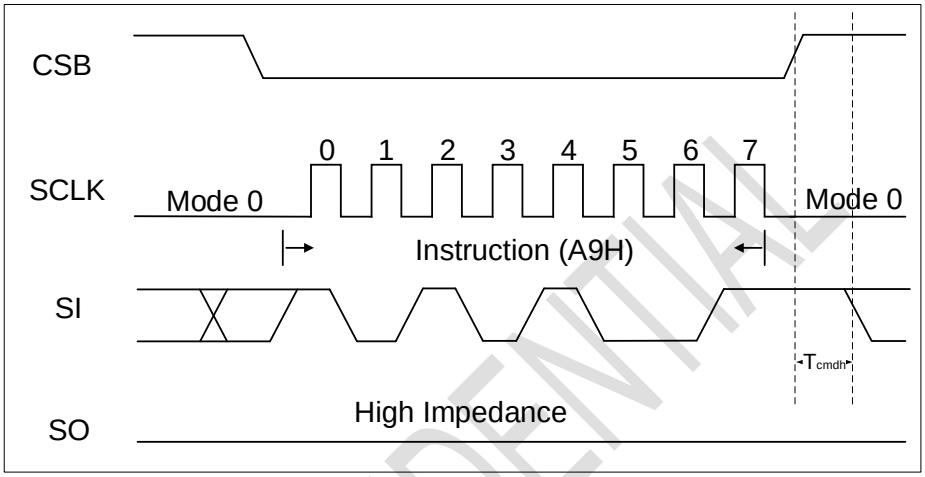


7.3.8 Display disable (A9H)

Turn off scan signal, all micro LEDs are not driven, the current will be smaller than any LED on.

In order to release from this status and restore display, Display enable and SYNC command is needed.

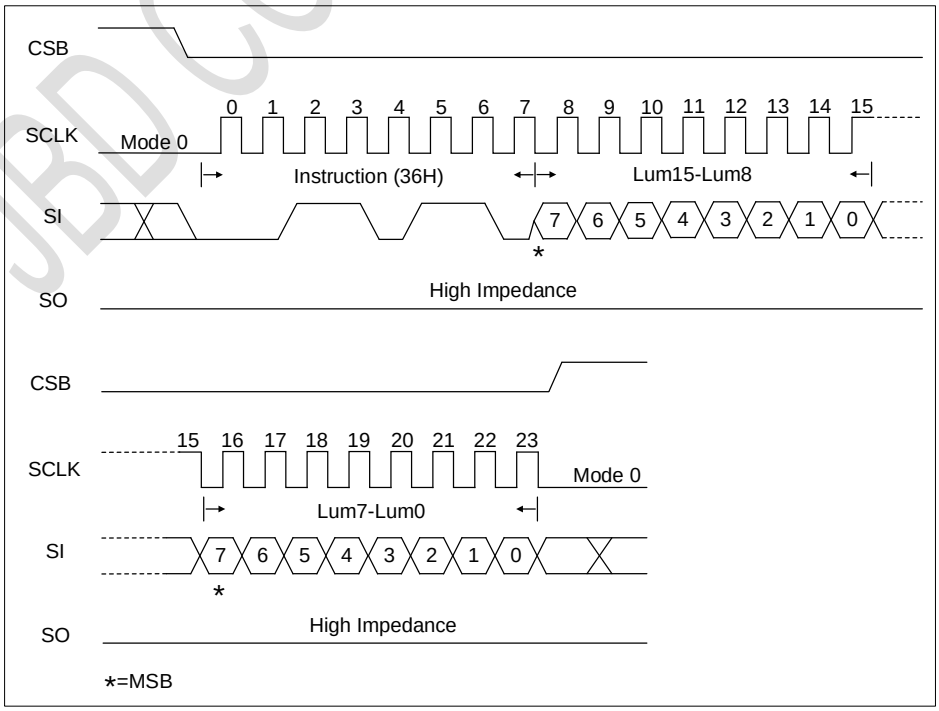
Figure 21 Display Disable Diagram



7.3.9 Luminance Register Write (36H)

Set 16 bits luminance.

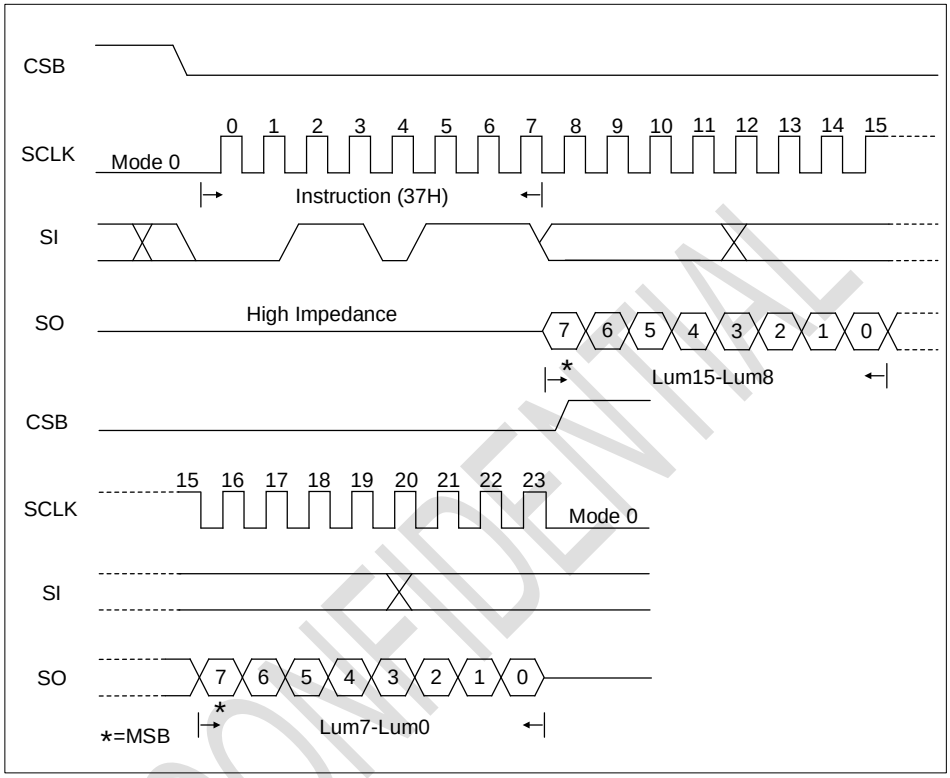
Figure 22 Luminance Register Write Diagram



7.3.10 Luminance Register Read (37H)

Read 16 bits luminance.

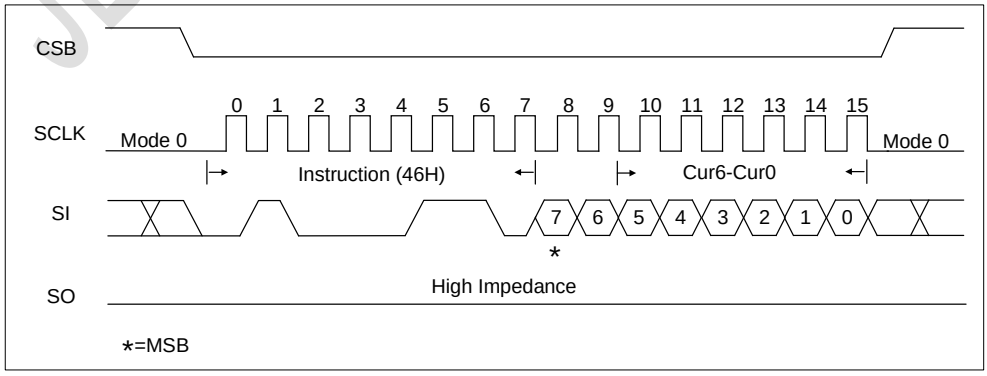
Figure 23 Luminance Register Read Diagram



7.3.11 Current Register Write (46H)

Set 8 bits register value for global current adjustment.

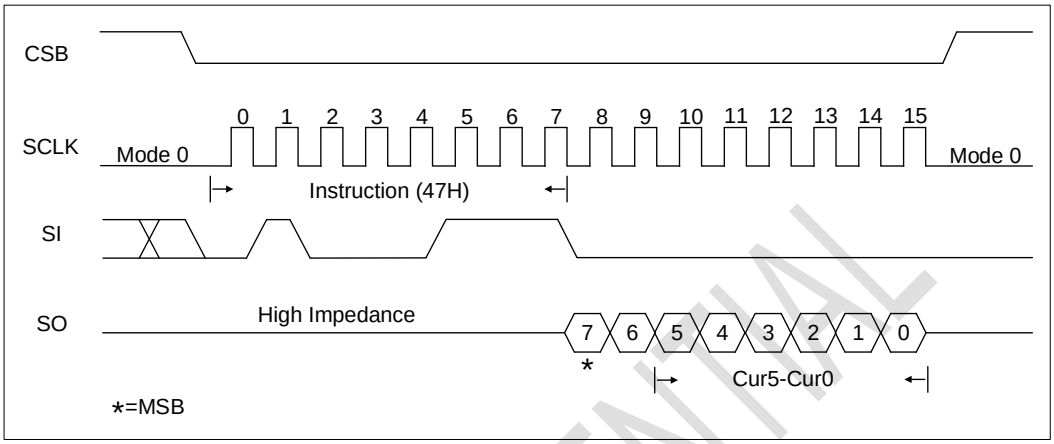
Figure 24 Current Register Write



7.3.12 Current Register Read (47H)

Read 8 bits register value for global current adjustment.

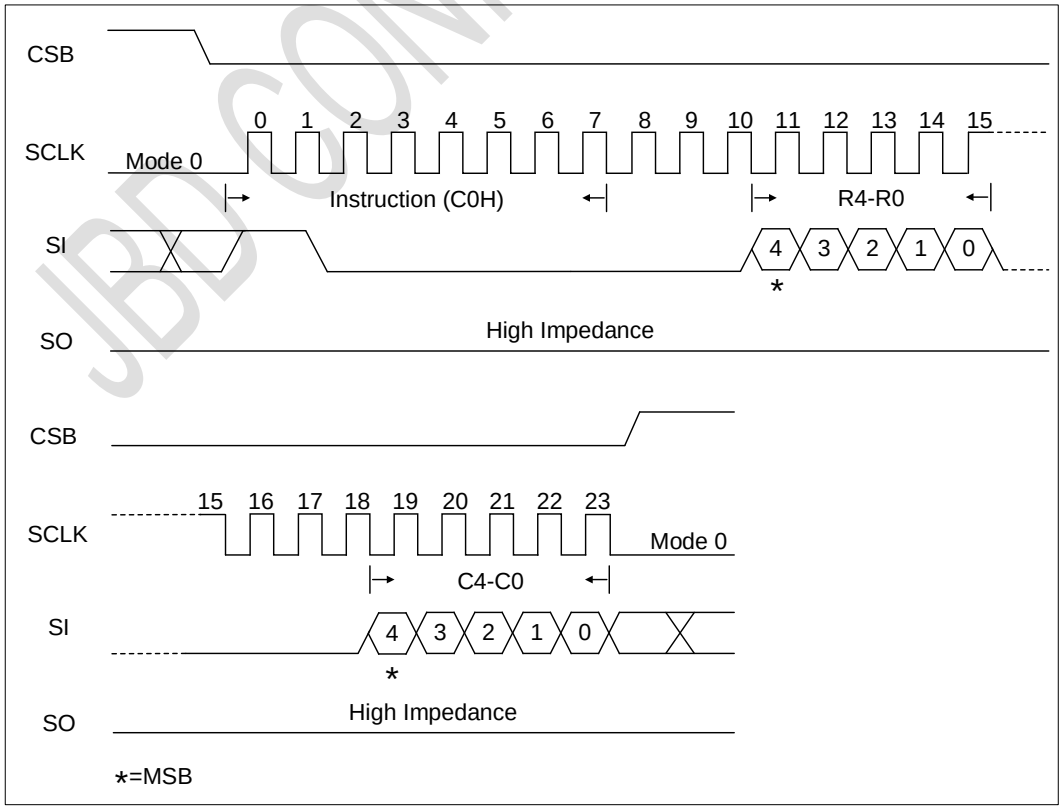
Figure 25 Current Register Read Diagram



7.3.13 Display Center Register Write (C0H)

Set the position of display zone

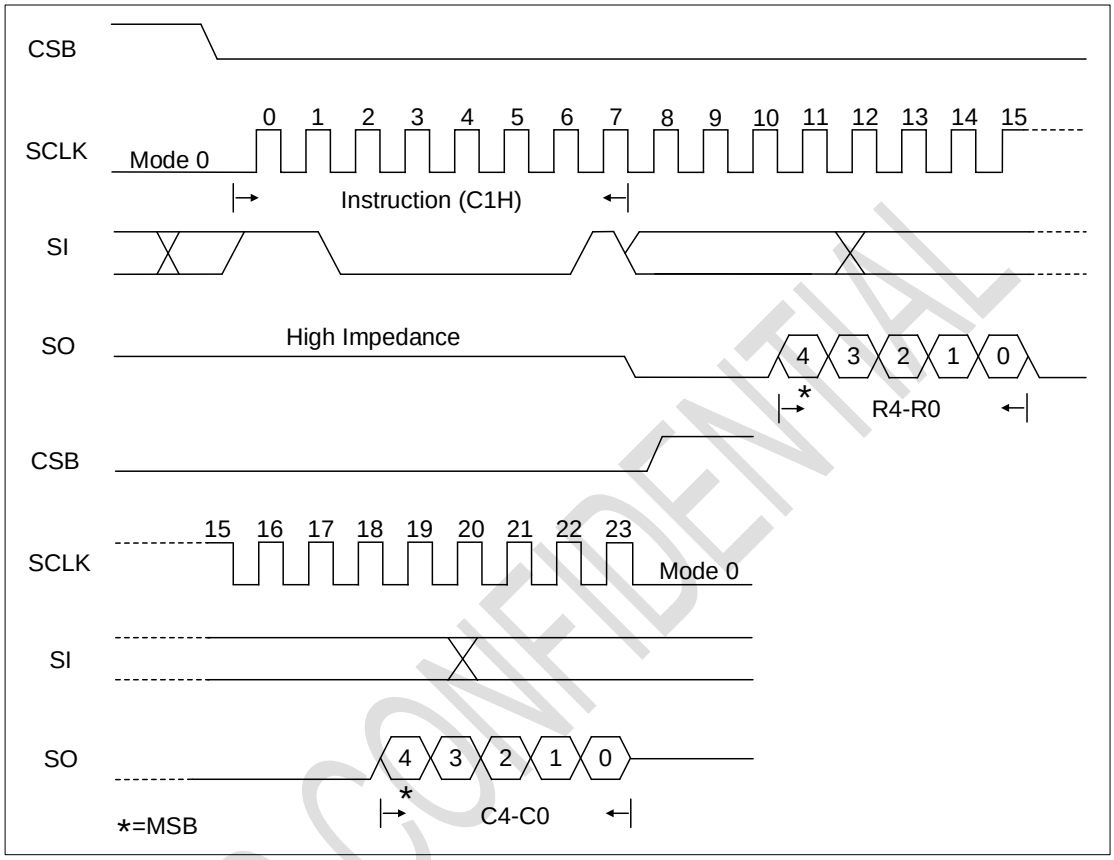
Figure 26 Display Center Register Write Diagram



7.3.14 Display Center Register Read (C1H)

Read Row & Column of display center.

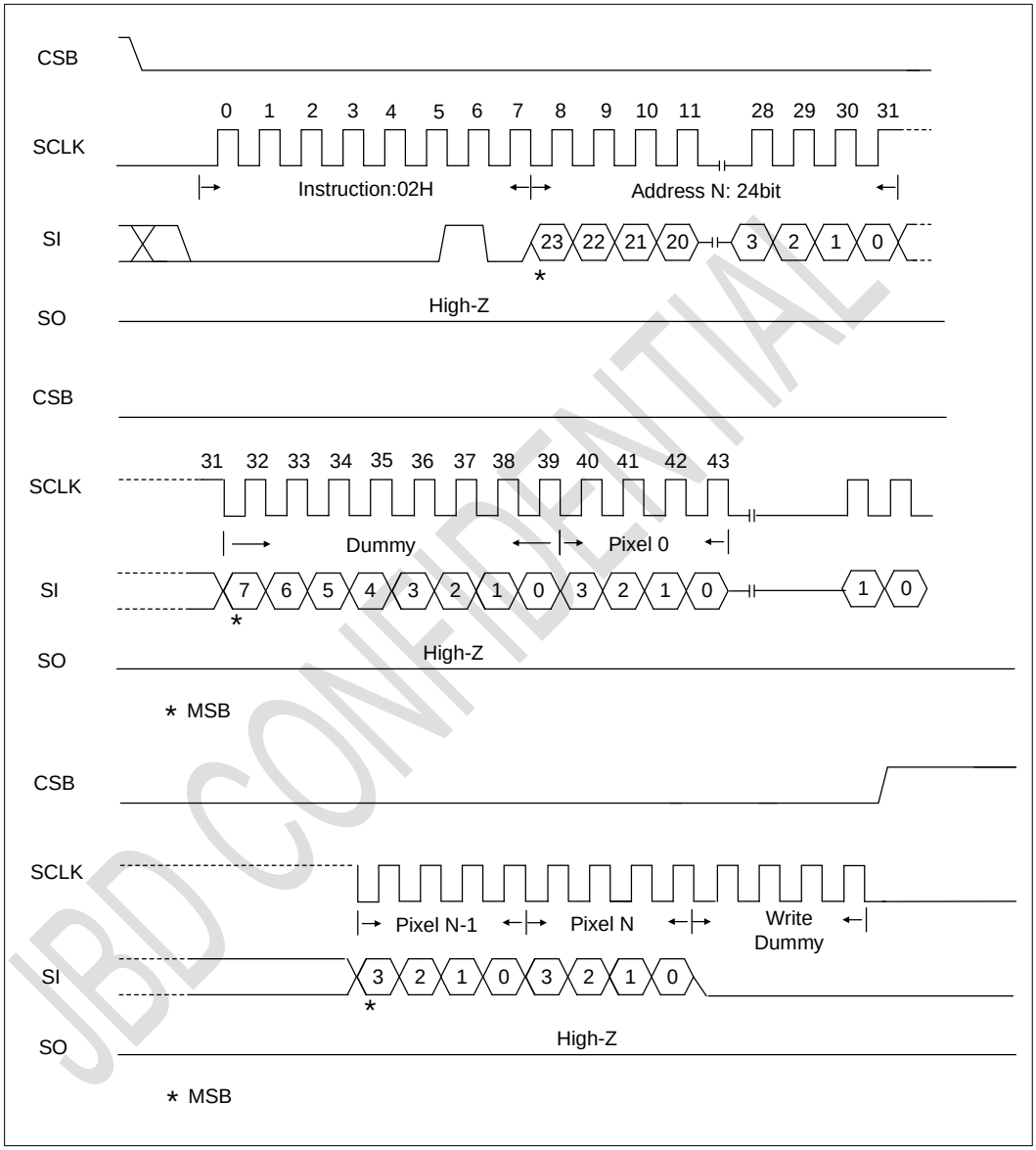
Figure 27 Display Center Register Read Diagram



7.3.15 SPI Write Buffer Data (02H)

Write Buffer Data in SPI protocol.

Figure 28 Write Buffer Data Diagram

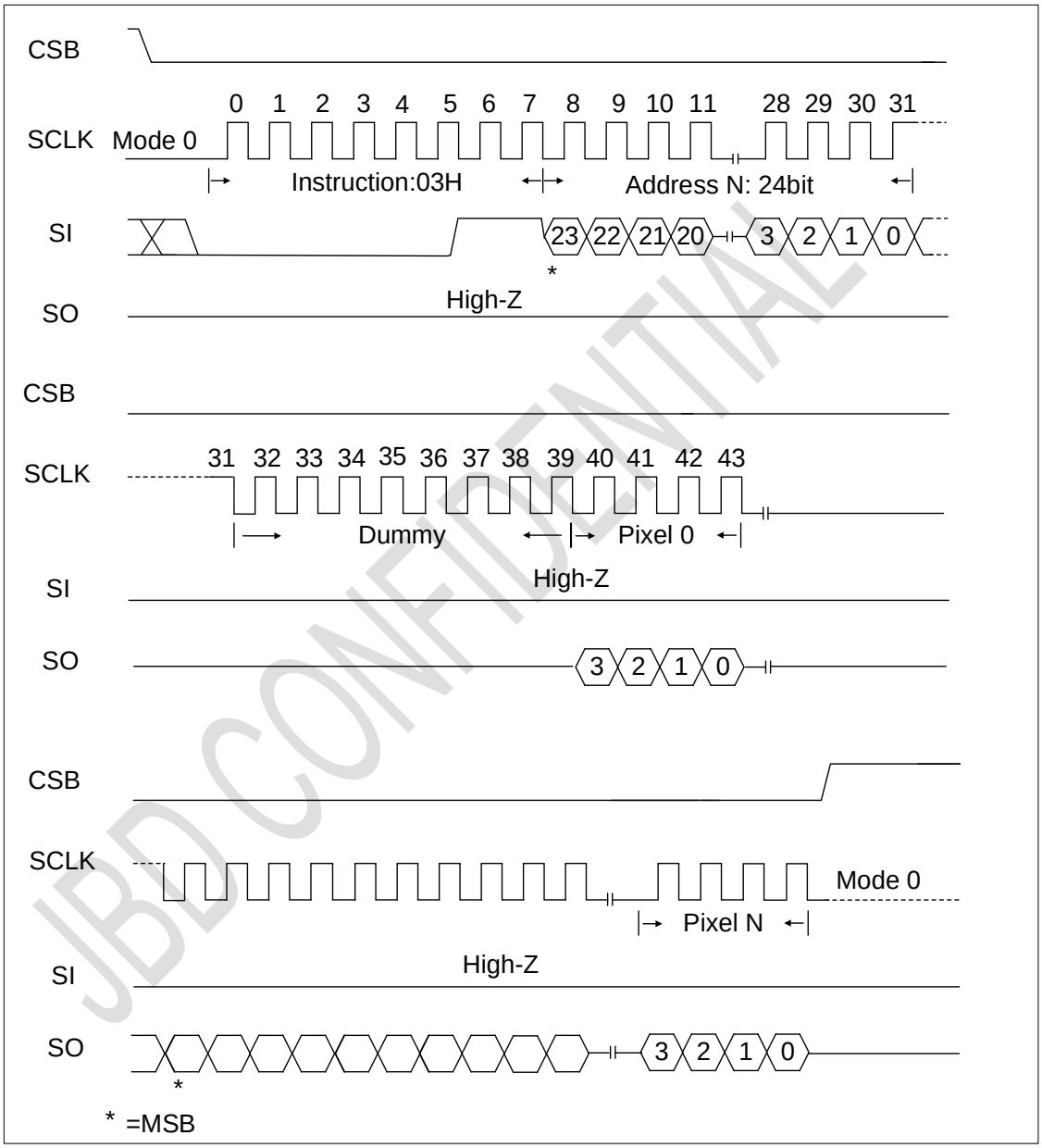


Note: Address = {5'b00000, ROW [8:0], COL [9:0]}
Final 4 dummy clocks are needed.

7.3.16 SPI Read Buffer Data (03H)

Read Buffer Data in SPI protocol.

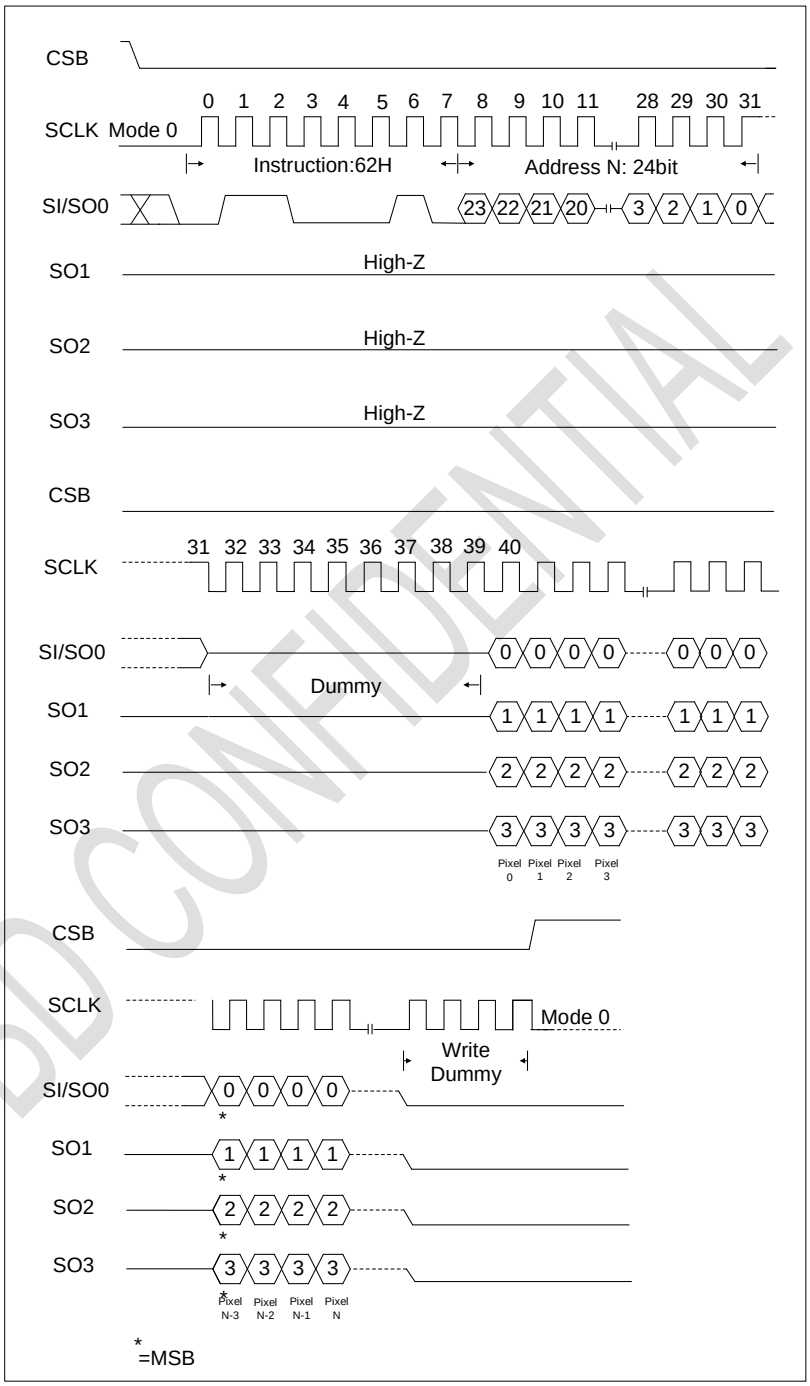
Figure 29 Read Buffer Data Diagram



7.3.17 QSPI Write Buffer Data (62H)

Fast Write Buffer Data in Quad SPI protocol.

Figure 30 Fast Write Buffer Data Quad Input Diagram

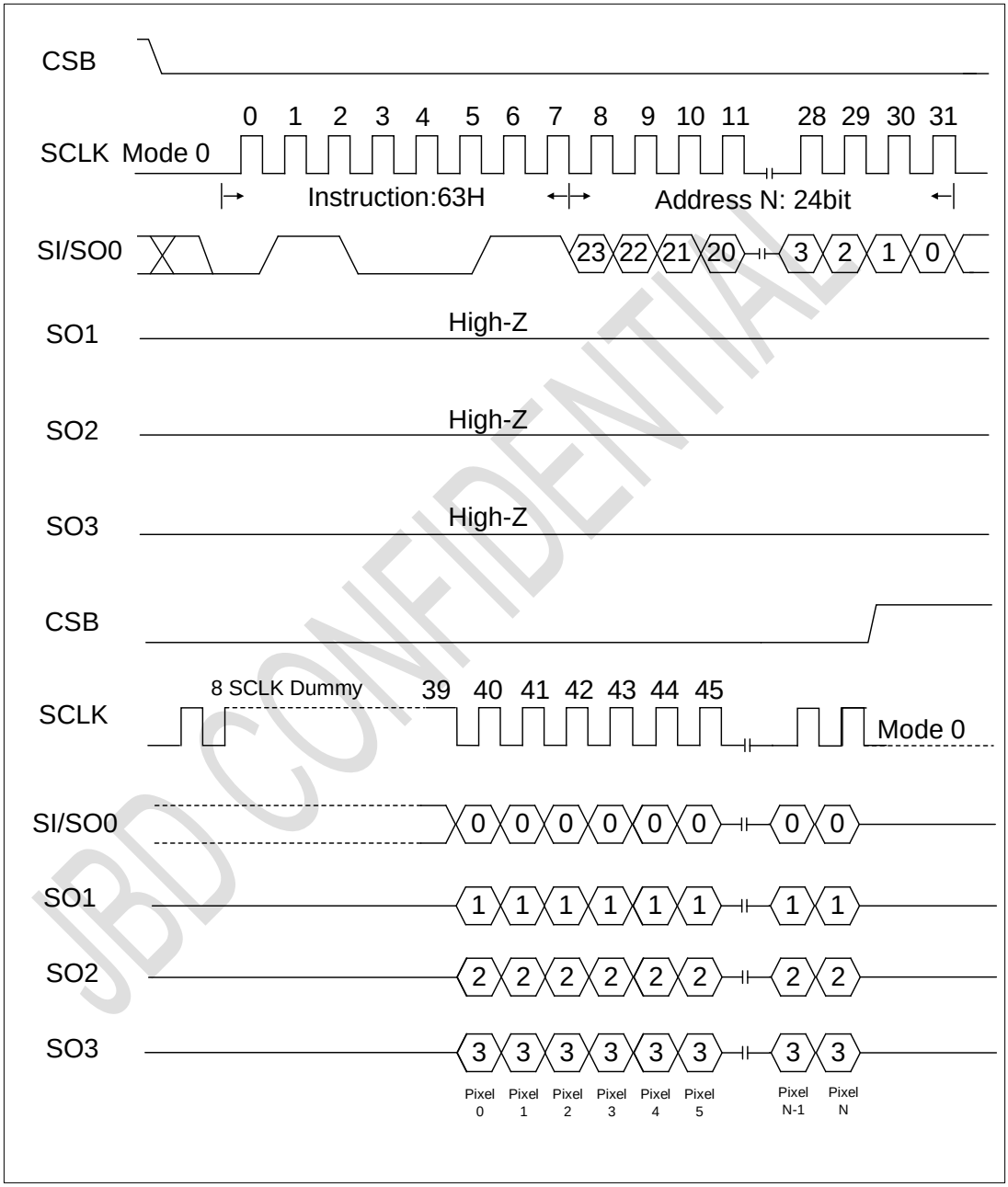


Note: Address = {5'b00000, ROW [8:0], COL [9:0]}
Final 4 dummy clocks are needed.
One SCLK transfers 1-pixel data with 4bit gray value.
N+1 is a multiple of 4

7.3.18 QSPI Read Buffer Data (63H)

Fast Read Buffer Data in Quad SPI protocol.

Figure 31 Fast Read Buffer Data Quad Output Diagram

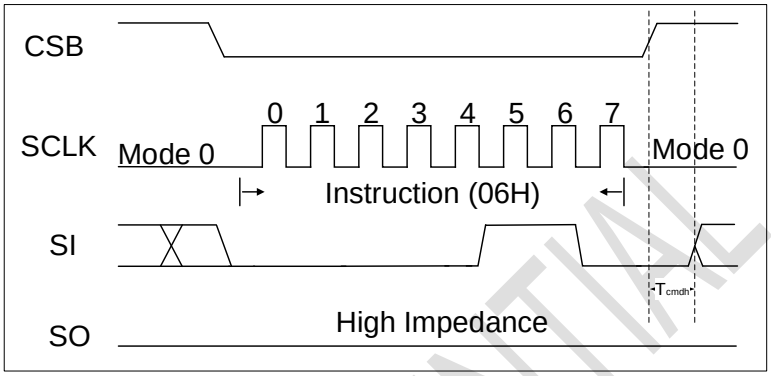


Note: One SCLK reads 1-pixel data with 4bit gray value.

7.3.19 Write Enable (06h)

The Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to 1. The WEL bit must be set prior to write status registers instruction. The Write Enable instruction is entered by driving CSB low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CSB high.

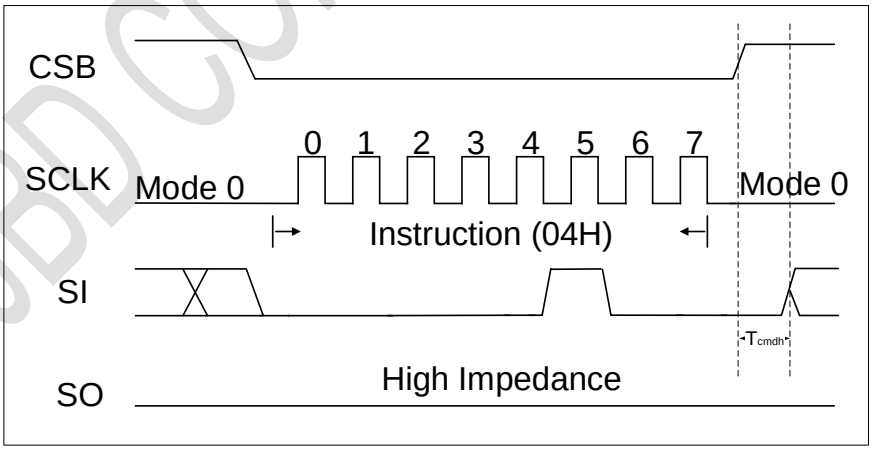
Figure 32. Write Enable Instruction for SPI Mode



7.3.20 Write Disable (04h)

The Write Disable instruction (Figure 33) resets the Write Enable Latch (WEL) bit in the Status Register to a 0, and then the status registers can’t be written. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up.

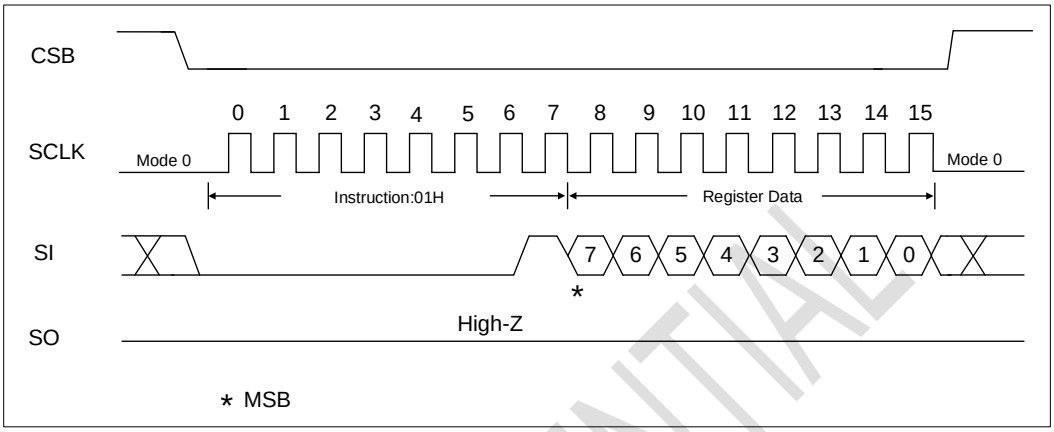
Figure 33 Write Disable Instruction for SPI Mode



7.3.21 Write Status Register 1 (01H)

Write Status Register 1.

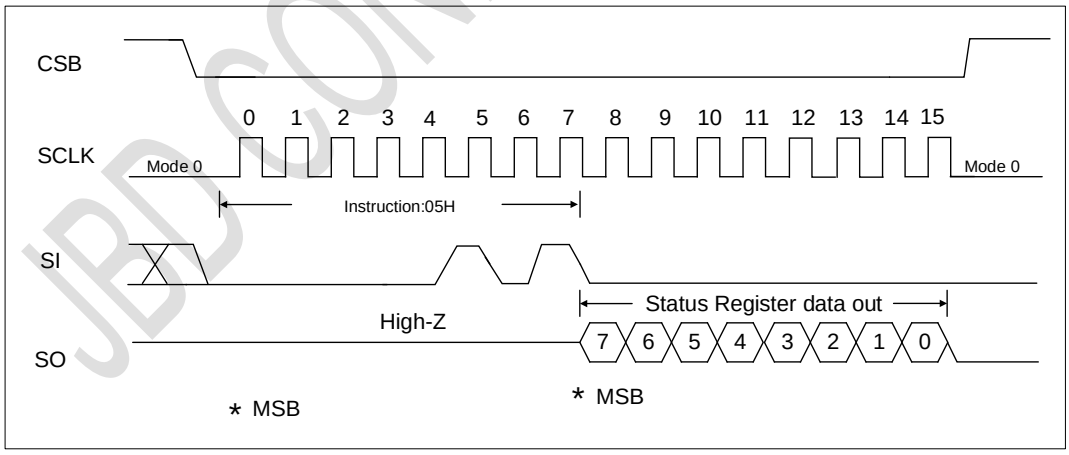
Figure 34 Write Status Register 1 Diagram



7.3.22 Read Status Register 1 (05H)

Read Status Register 1.

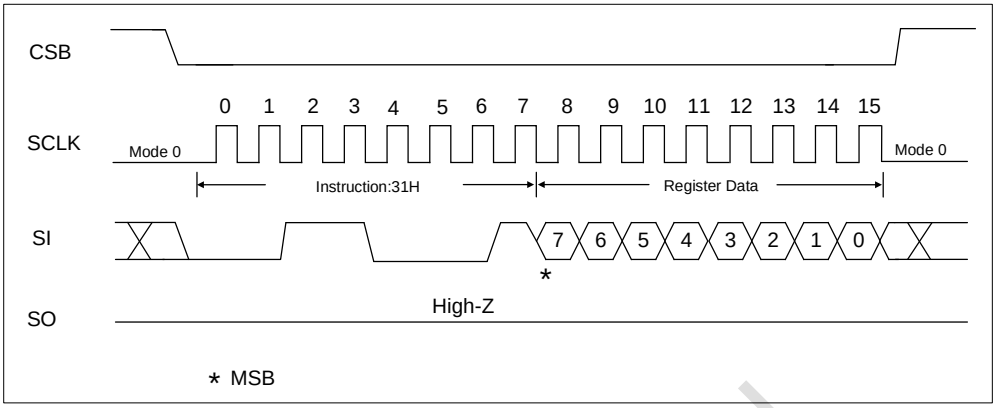
Figure 35 Read Status Register Diagram



7.3.23 Write Status Register 2 (31H)

Write Status Register 2.

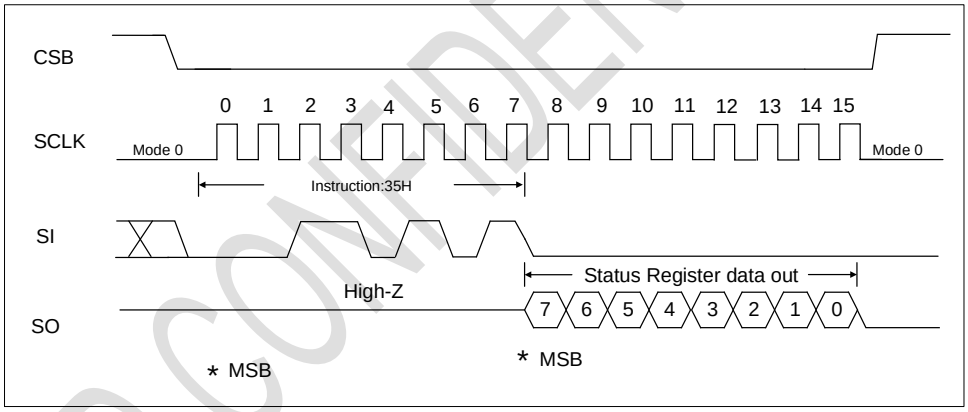
Figure 36 Write Status Register 2 Diagram



7.3.24 Read Status Register 2 (35H)

Read Status Register 2.

Figure 37 Read Status Register 2 Diagram



7.3.25 Mirror (71H/72H/73H)

Mirror command can change the image to mirror view automatically.

Command (71H) returns to default image.

Command (72H) changes image to up/down mirror view.

Command (73H) changes image to left/right mirror view.

Note: After mirror command, the SYNC command is needed.

The mirror image diagram ref *Figure 4.*

Figure 38 Mirror command Diagram 1

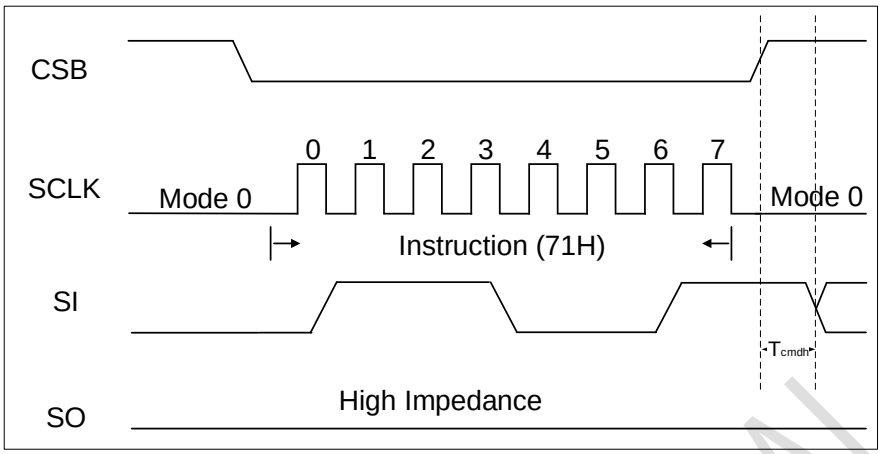


Figure 39 Mirror command Diagram 2

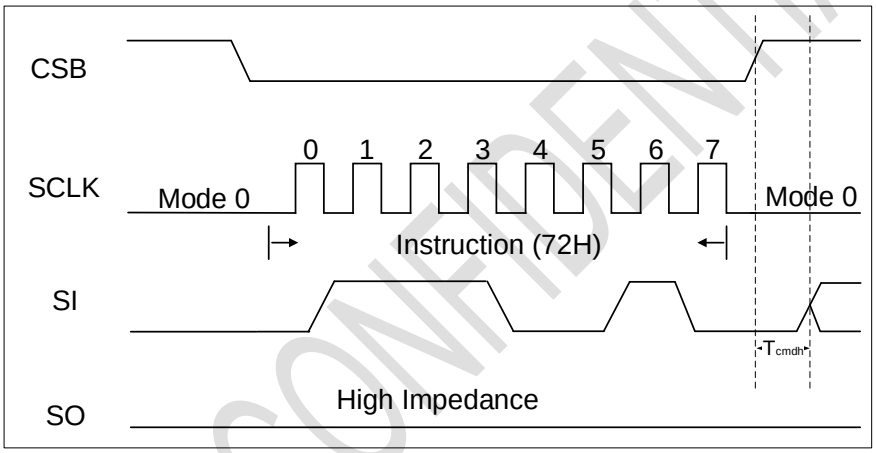
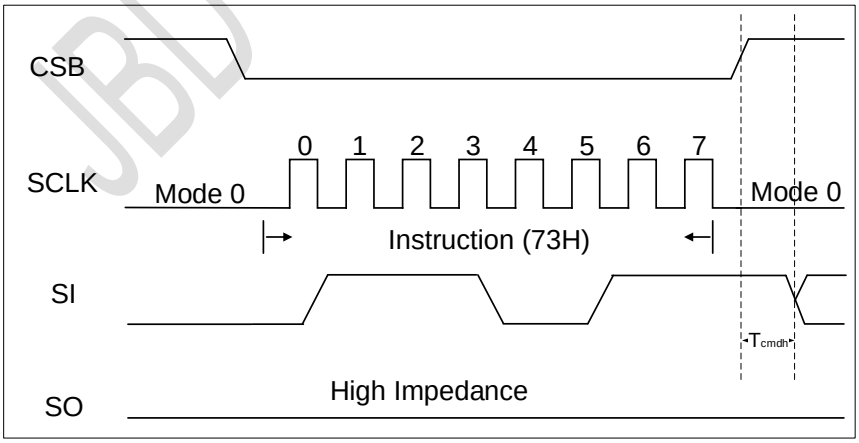


Figure 40 Mirror command Diagram 3



7.3.26 Self-Test (13H/14H/15H/16H)

Self-test command can be used to test the panel performance.

Command (13H) makes the screen all off.

Command (14H) makes the screen all on.

Command (15H) makes the screen enter 3X3 check I mode.

Command (16H) makes the screen enter 3X3 check II mode.

Note: After self-test command, the SYNC command is needed.

The self-test diagram ref *Figure 5.*

Figure 41 Self-Test command Diagram 1

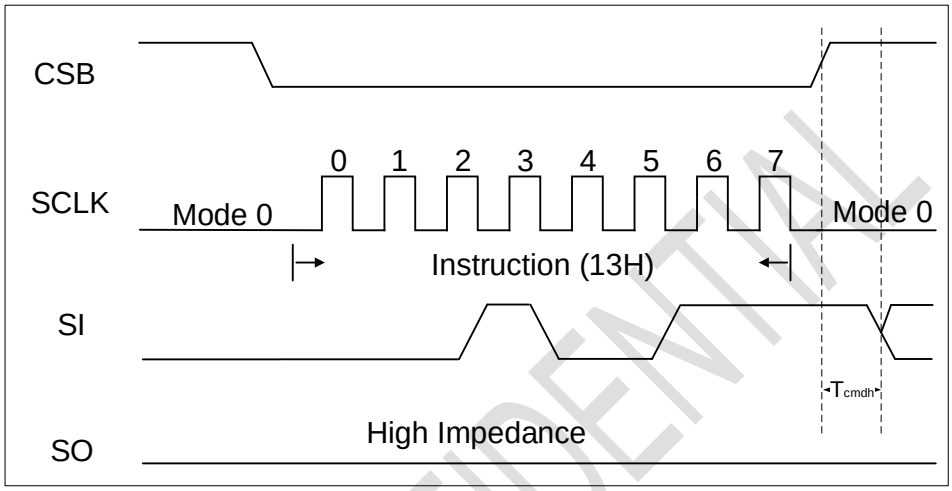


Figure 42 Self-Test command Diagram 2

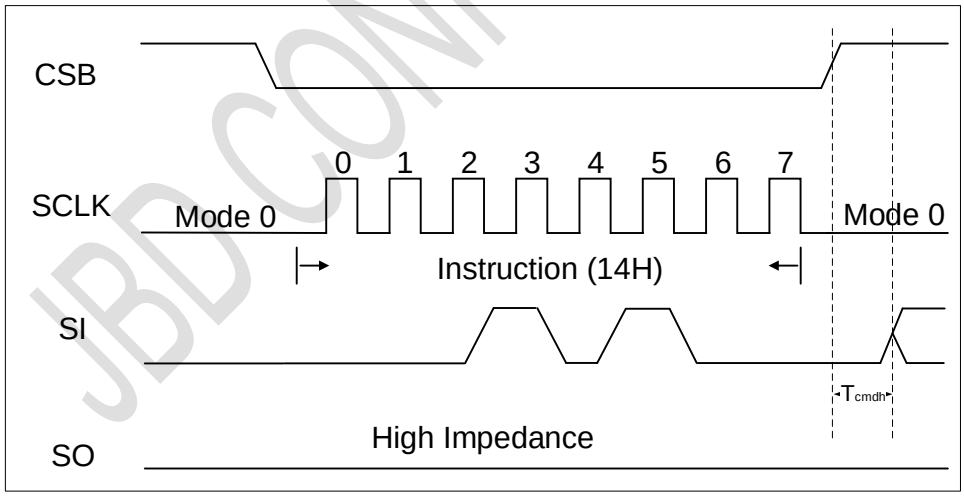


Figure 43 Self-Test command Diagram 3

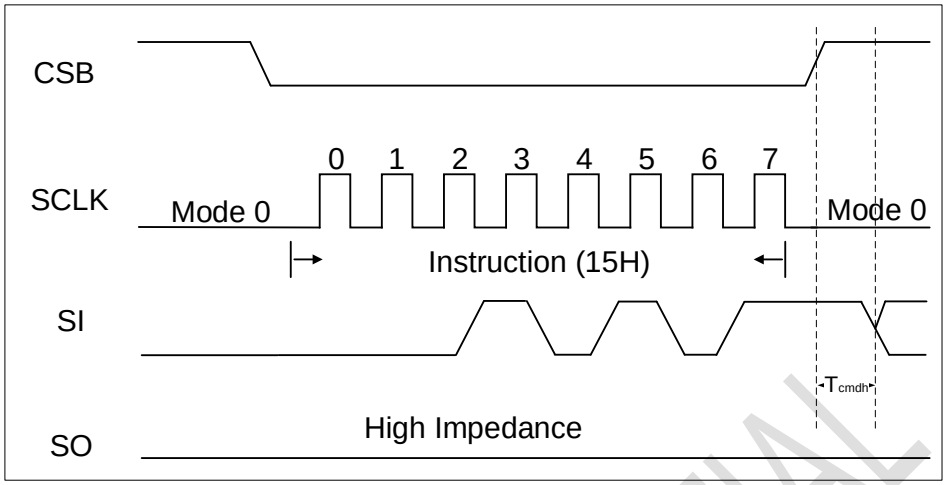
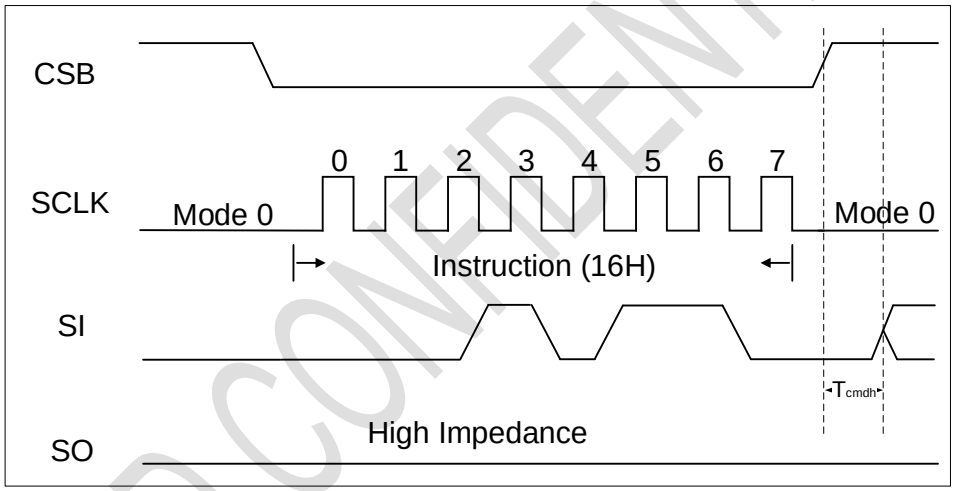


Figure 44 Self-Test command Diagram 4



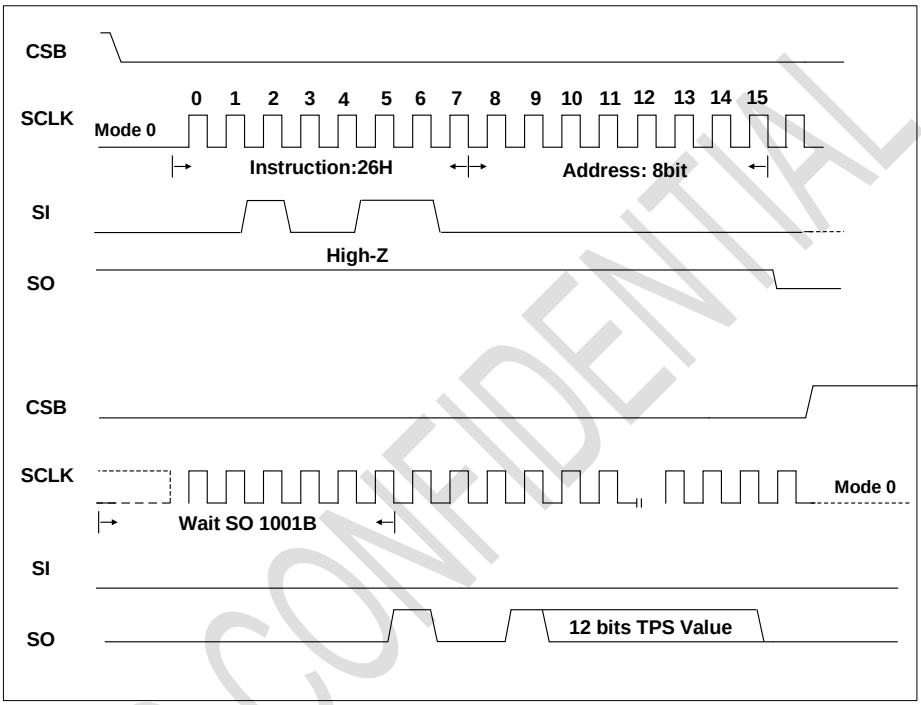
7.3.27 Temperature Sensor Read (26H)

Temperature Sensor Read command can read temperature sensor value. Users can get temperature of panel corners through corresponding calculation.

Ref *Figure 45*

Note: Address = 0x02

Figure 45 Temperature Sensor Read Command Diagram



Please check **design note** for detail.

7.3.28 OTP Read (81H)

OTP address range is from 0x0000 to 0x1FFF

Figure 46 SPI OTP Read Diagram

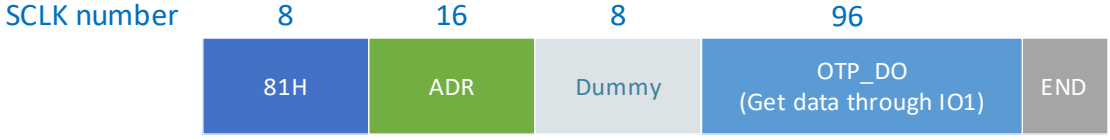
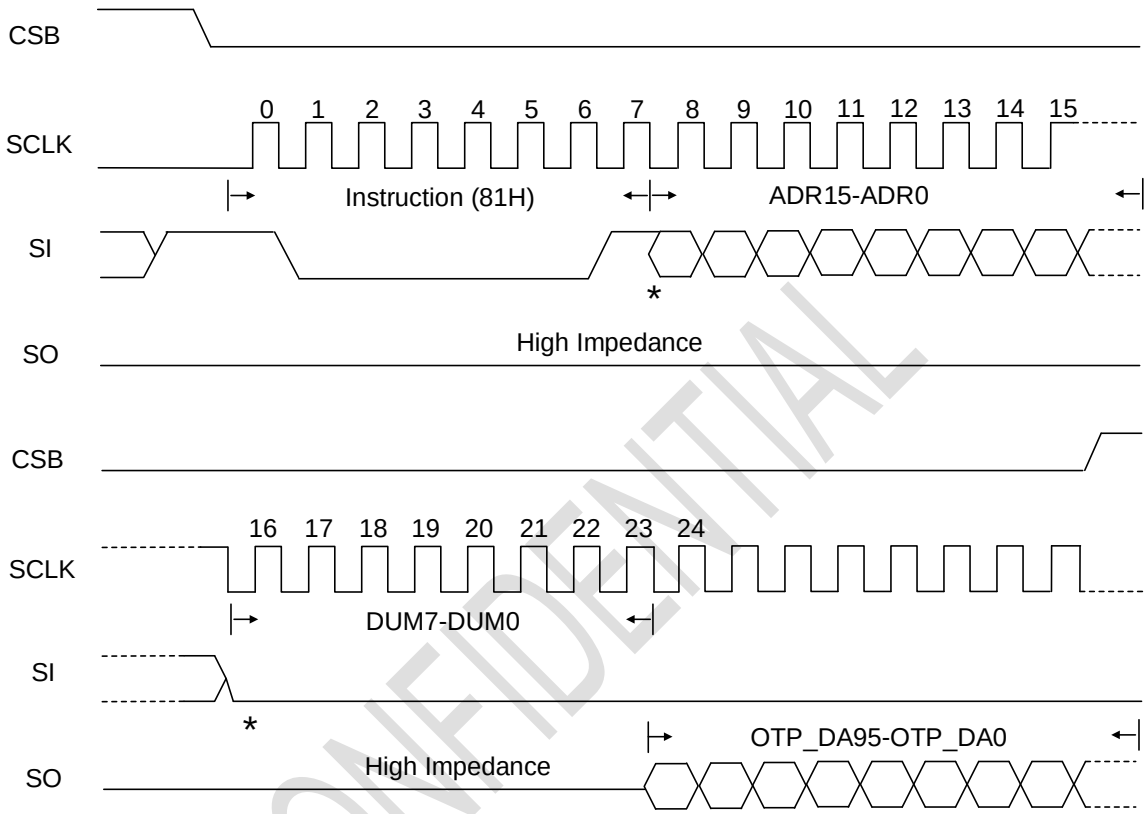


Figure 47 SPI OTP Read Wave Diagram

SPI OTP Read

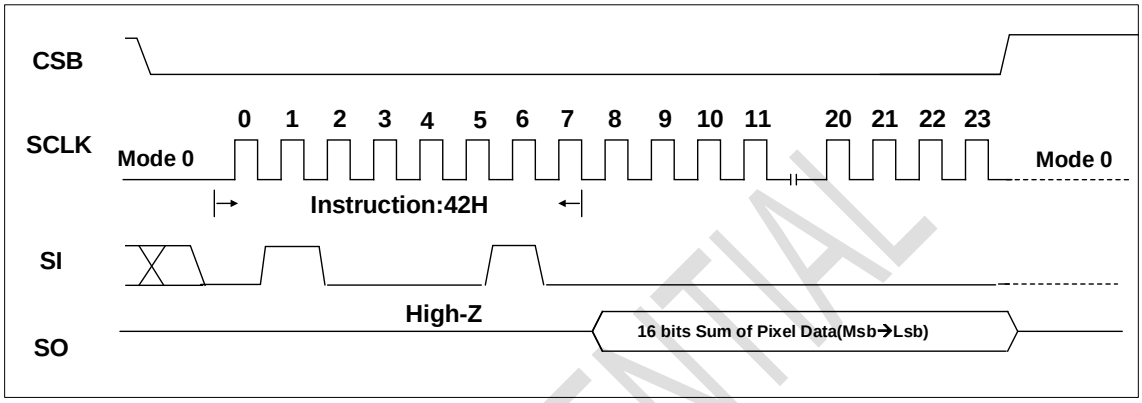


7.3.29 Read Check Sum (RDCHKS) (42H)

The Read checksum (RDCHKS) command read the sum value of pixel transfer data. A total of 16 bits is the accumulated value of the transmitted pixel data (4bits) 。

Only QSPI data calculation is supported for the cumulative result。And spi transfer data will change the sum value to last pixel data.

Figure 48. Read Sum Value Sequence Diagram (SPI)



CMD	IO	Byte 1	Byte 2	Byte 3
RDCHKS	SI	42H	00H	00H
	SO		CS[15:8]	CS[7:0]

Figure 49. Sum Value Generation Sequence Diagram (QSPI)

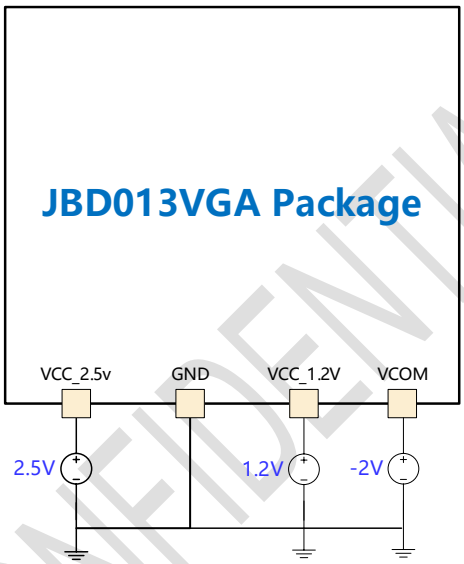
Note: 1 pixel data 4bit

8 Electrical characteristics

8.1 Power Supply Scheme

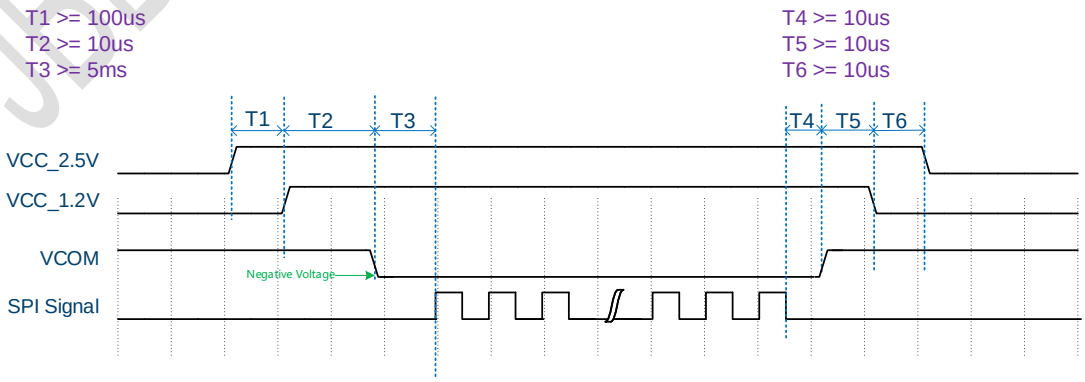
For package, pins ref Figure 59

Figure 50 Package power supply diagram

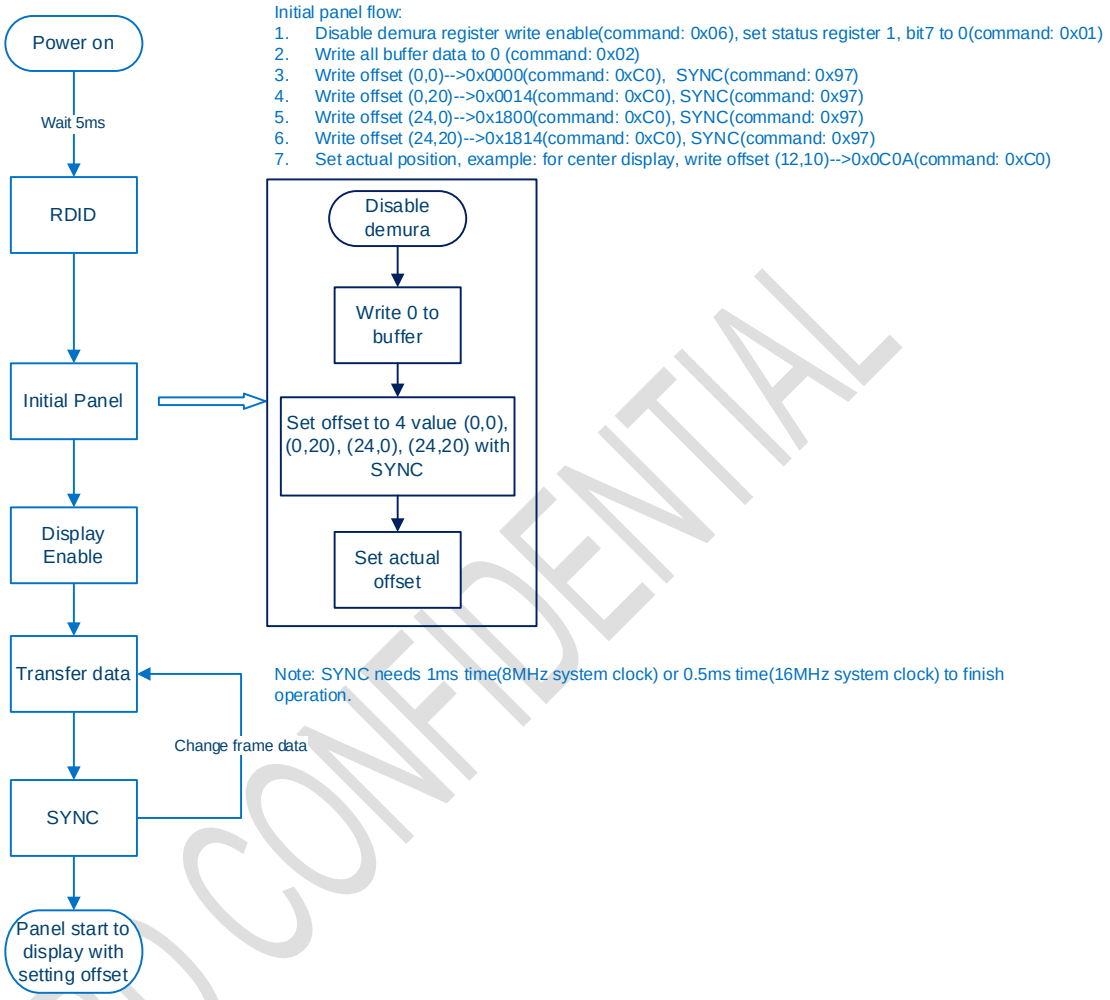


8.2 Power On/Off Sequence

Figure 51 Power On/Off Sequence Diagram for Package



8.3 Display Control Sequence



Note:

1. Config REG needs to set current at first. Demura enable default, if the function is not needed, disable the function at configuration register status. Refer to *7.3.21.* And any change in status register 1 or status register 3 will change luminance to max value, so luminance setting after the status register operation is needed.
2. Initial Panel must be done before normal operation, otherwise the edge of panel maybe lit up unexpected. Sync command is needed after setting offset, and corresponding delay is necessary.
3. Setting offset refer to *7.3.13* , offset register value mapping: (0,0) → 0x0000, (0,20) → 0x0014, (24,0)→0x1800, (24,20)→0x1814.

8.4 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in *Table 6. Voltage characteristics*, *Table 7. Thermal characteristics* may cause permanent damage to the device. These are absolute maximum ratings and regular operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDIO}–V_{SS}	External main supply voltage	-0.3	3.6	V
V_{DD12}–V_{SS}	External analog supply voltage	-0.3	1.32	V
V_{IN}	Input voltage	V_{SS} -0.3	V_{DDIO}+0.3	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$ -$V_{SS}\|$	Variations between all the different ground pins	-	50	mV

1. All main power and ground pins must always be connected to the external power supply, in the permitted range.

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–40 to +90	°C
T_J	Maximum junction temperature	125	°C

8.5 Operating Conditions

8.5.1 Recommended Operating Conditions

Table 8. General Operating Conditions

Symbol	Parameter	Min	Max	Unit
f_{HCLK}	Internal clock frequency	0	16	MHz
V_{DDIO}	Standard IO operating voltage	1.62	3.6	V
V_{DD12IO}	IO IP to internal digital voltage	1.08	1.32	V
V_{DD12}	Internal operating voltage	1.08	1.32	V
V_{DD12P}	External power supply for IC Cathode positive voltage.	1.08	1.32	V
V_{COM}	External power supply for IC Cathode negative voltage.	-3.0	-1.3	V
V_{IN}	I/O input voltage	-0.3	V_{DDIO}+0.3	V

8.5.2 Supply current characteristics

Table 9. Power Current under Normal Run

Symbol	Description	Conditions	Typ	Max	Unit
I_{DDIO}	IO supply current in Run mode	SCLK @ 32MHz	3.39	4.49	mA
I_{DD12IO}	IO to internal logic supply current in Run mode	SCLK @ 32MHz	33.5	33.7	uA
I_{DD12}	Core digital supply current in Run mode	SCLK @ 32MHz	3.33	3.55	mA
I_{DD12P}	Micro LED panel positive supply current in Run mode	SCLK @ 32MHz with full screen on	480	550	mA
I_{COM}	Micro LED panel negative supply current in Run mode	SCLK @ 32MHz with full screen on	480	550	mA

Table 10. Power Current under Deep Power Down Status

Symbol	Description	Conditions	Typ	Max	Unit
I_{DDIO}	IO Supply current in DPD mode	Deep power down, SPI stop	35.4	40.1	uA
I_{DD12IO}	IO to internal logic Supply current in DPD mode	Deep power down, SPI stop	33.5	33.7	uA
I_{DD12}	Core digital Supply current in DPD mode	Deep power down, SPI stop	0.33	0.42	mA
I_{DD12P}	Micro LED panel positive supply current in DPD mode	Deep power down, SPI stop	30.1	33.1	uA
I_{COM}	Micro LED panel positive supply current in DPD mode	Deep power down, SPI stop	30.1	33.1	uA

8.5.3 External Clock Source Characteristics

8.5.3.1 External User Clock Generated From An External Source

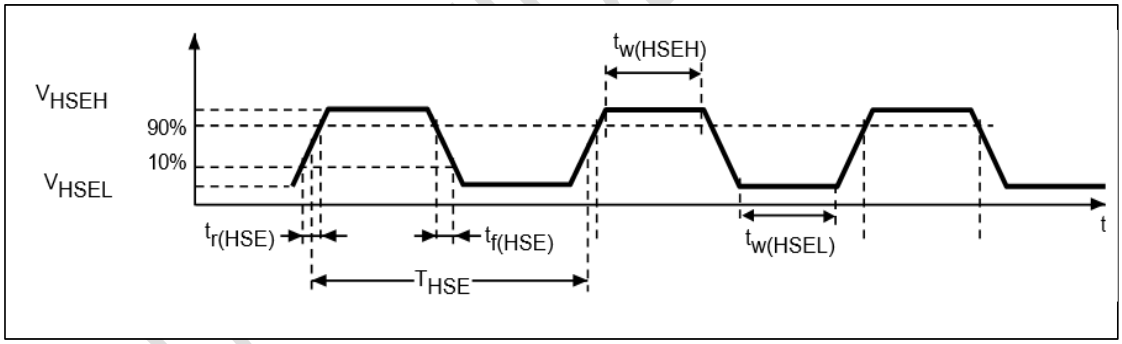
When OSC select external clock and the Crystal is switched off, external clock can input from XIN pin.

The recommended clock input waveform is shown in *Figure 52. External Clock Source AC Timing*

Table 11. External User Clock Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		8		MHz
V_{HSEH}	CLKIN input pin high level voltage	0.7 V_{DDIO}	-	V_{DDIO}	V
V_{HSEL}	CLKIN input pin low level voltage	V_{SS}	-	0.3 V_{DDIO}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	CLKIN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	CLKIN rise or fall time	-	-	20	

Figure 52. External Clock Source AC Timing Diagram



8.5.3.2 External Clock Generated From a Crystal/Ceramic Resonator

The high-speed external (HSE) clock can be supplied with an 8/16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 12. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 12. HSE Oscillator Characteristics 1

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

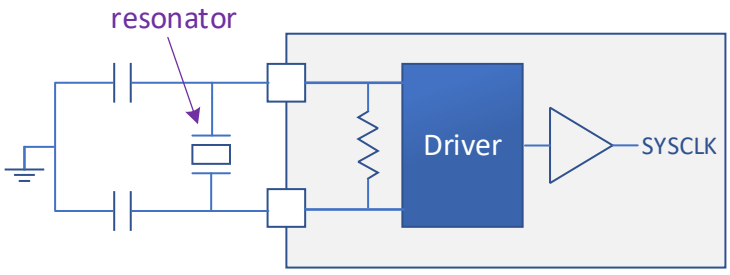
Table 13. HSE Oscillator Characteristics 2

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 1.8 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
t_{SU}(4)(HSE)	Startup time	V_{DD} is stabilized	-	2	-	Ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure* 53). CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. PCB and IC pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2.

Figure 53. Typical Application with a resonator



8.5.4 I/O Port Characteristics

8.5.4.1 General Input/Output Characteristics

Unless otherwise specified, the parameters given in *Table 14* are derived from tests performed. All I/Os are designed as CMOS- and TTL-compliant.

Table 14. I/O Static Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	All I/Os	-	-	0.3 V_{DDIO}	
V_{IH}	High level input voltage	All I/Os	0.7 V_{DDIO}	-	-	
V_{hys}	Schmitt trigger hysteresis	Input I/O	-	200(1)	-	mV
I_{lkg}	Input leakage current(2)	$V_{SS} < V_{IN} < V_{DDIO}$	-	-	0.1	µA
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.

8.5.4.2 Output Driving Current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, or sink or source up to +/- 20 mA (with a relaxed VOL/VOH).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 8.4:

8.5.4.3 Output Voltage Levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed. All I/Os are CMOS- and TTL-compliant.

Table 15. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 8 mA V_{DDIO} > 2.0 V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIO}–0.4	-	
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA V_{DDIOx} > 2.0 V	-	1.3	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIO}–1.3	-	

8.5.5 Communication Interfaces

8.5.5.1 SPI Characteristics

Unless otherwise specified, the parameters given in *Table 16* for SPI are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 8. General Operating*

Table 16. SPI Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SPI clock frequency		-	32	MHz
t_{sf2ckr}	CSB falling to sclk rising time		31.25	-	ns
t_{ckf2sr}	SCLK falling to CSB rising time		31.25	-	
t_{su}	Data input setup time		10	-	
t_h	Data input hold time		10	-	
t_{sf2ckf}	CSB falling to sclk falling time		31.25	-	
t_{ckr2sr}	SCLK rising to CSB rising time		31.25	-	
$t_{v(SO)}$	Data output valid time	after SCLK falling edge	-	10	
$t_{h(SO)}$	Data output hold time	after SCLK falling edge	0	-	
DuCy(SCK)	SPI slave input clock duty cycle		25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 54 Serial Input Timing(SCLK MD0)

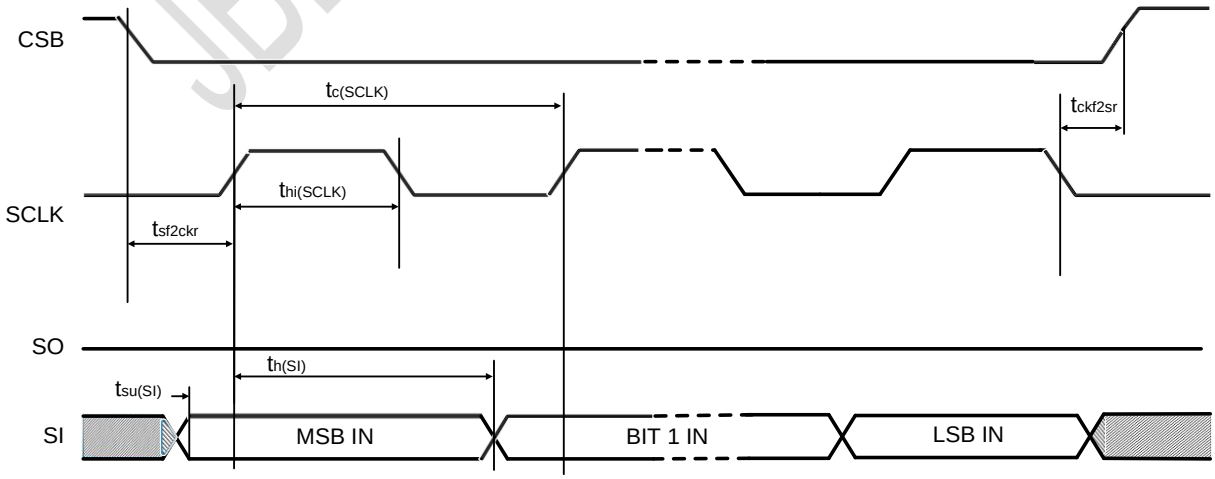


Figure 55 Serial Input Timing (SCLK MD3)

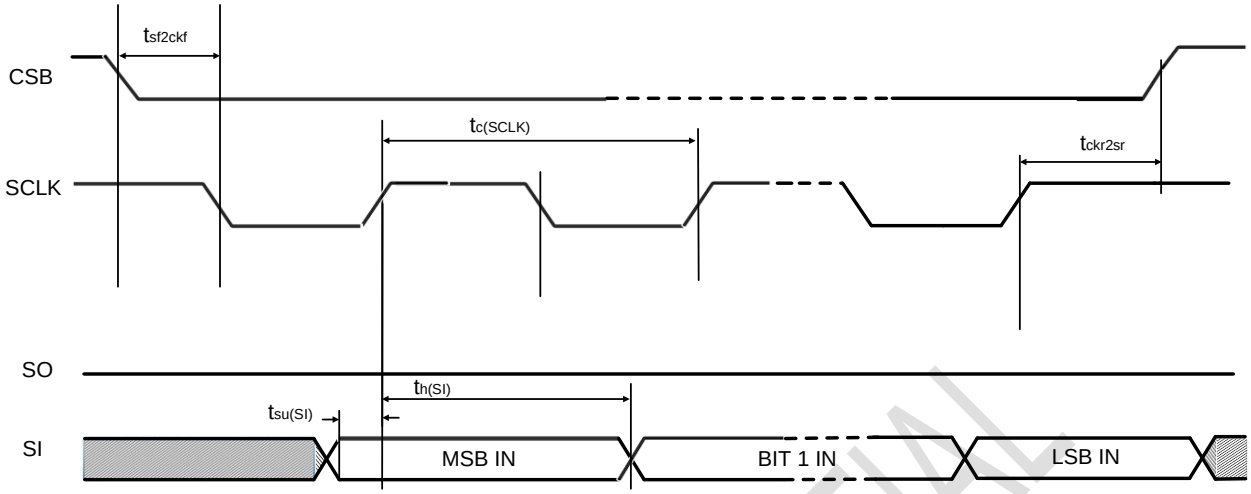
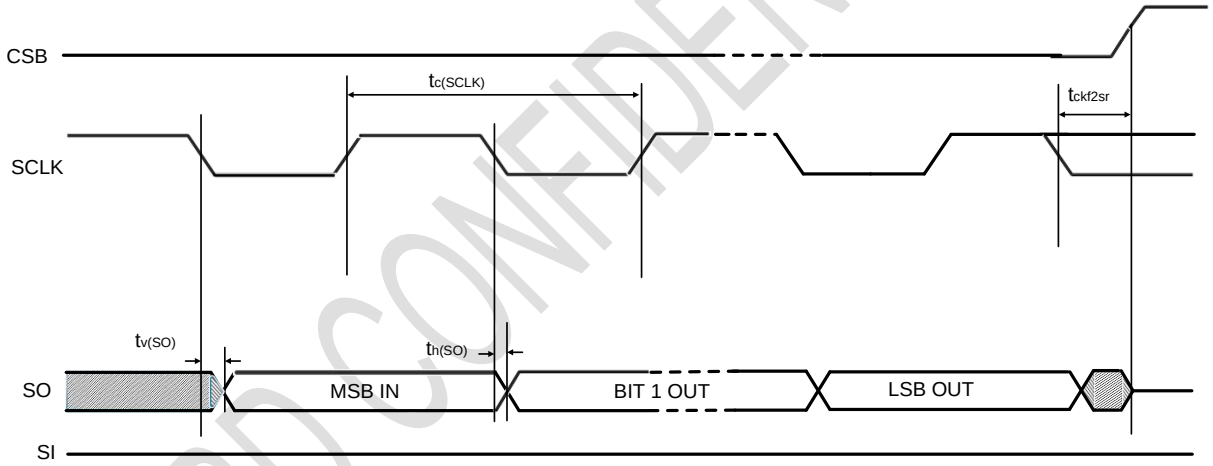


Figure 56 Serial Output Timing



9 Mechanical Specifications

9.1 Physical Specifications

Figure 57 uLED Panel Package Specifications

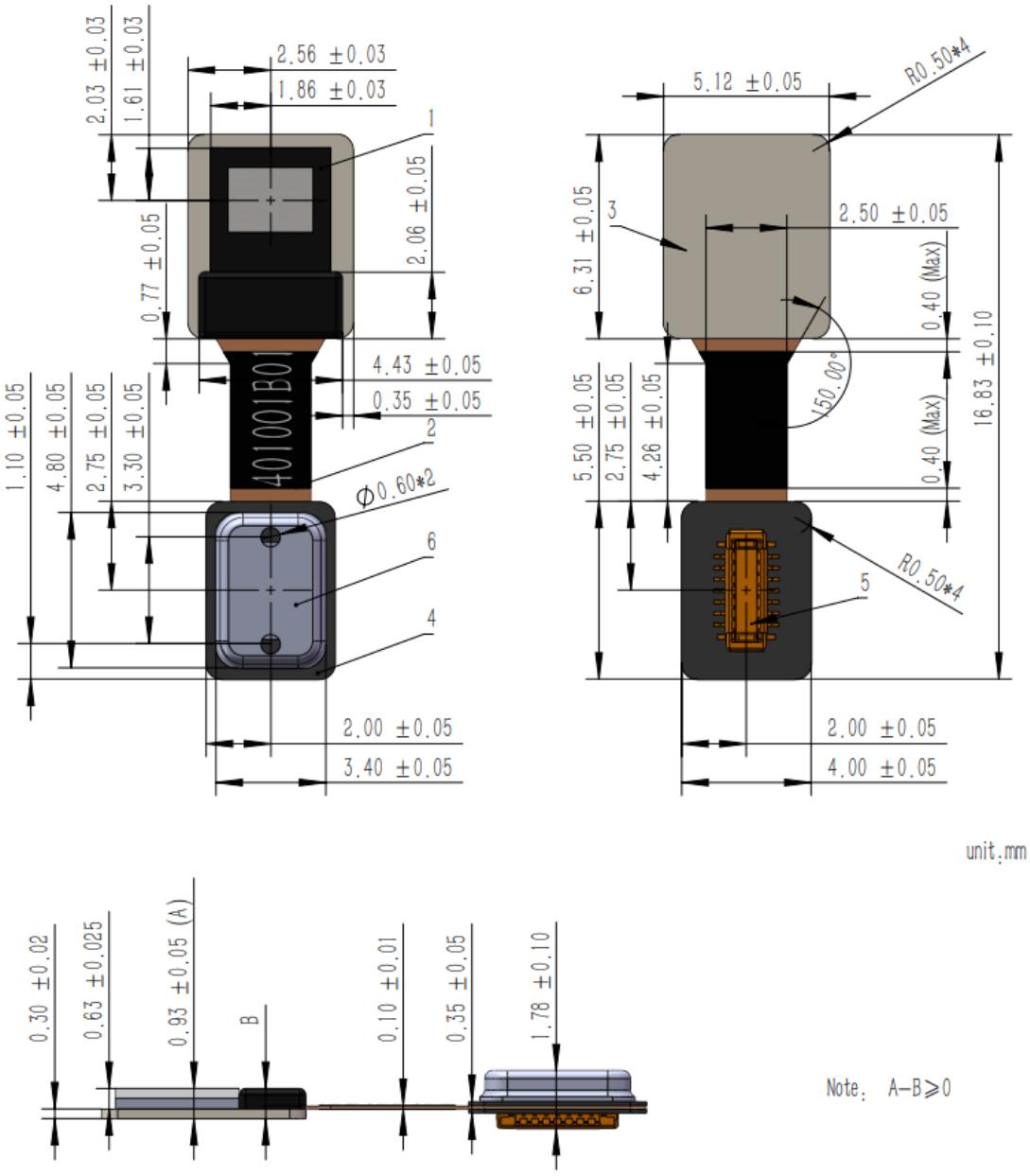


Figure 58 uLED Panel Package Outer Limit

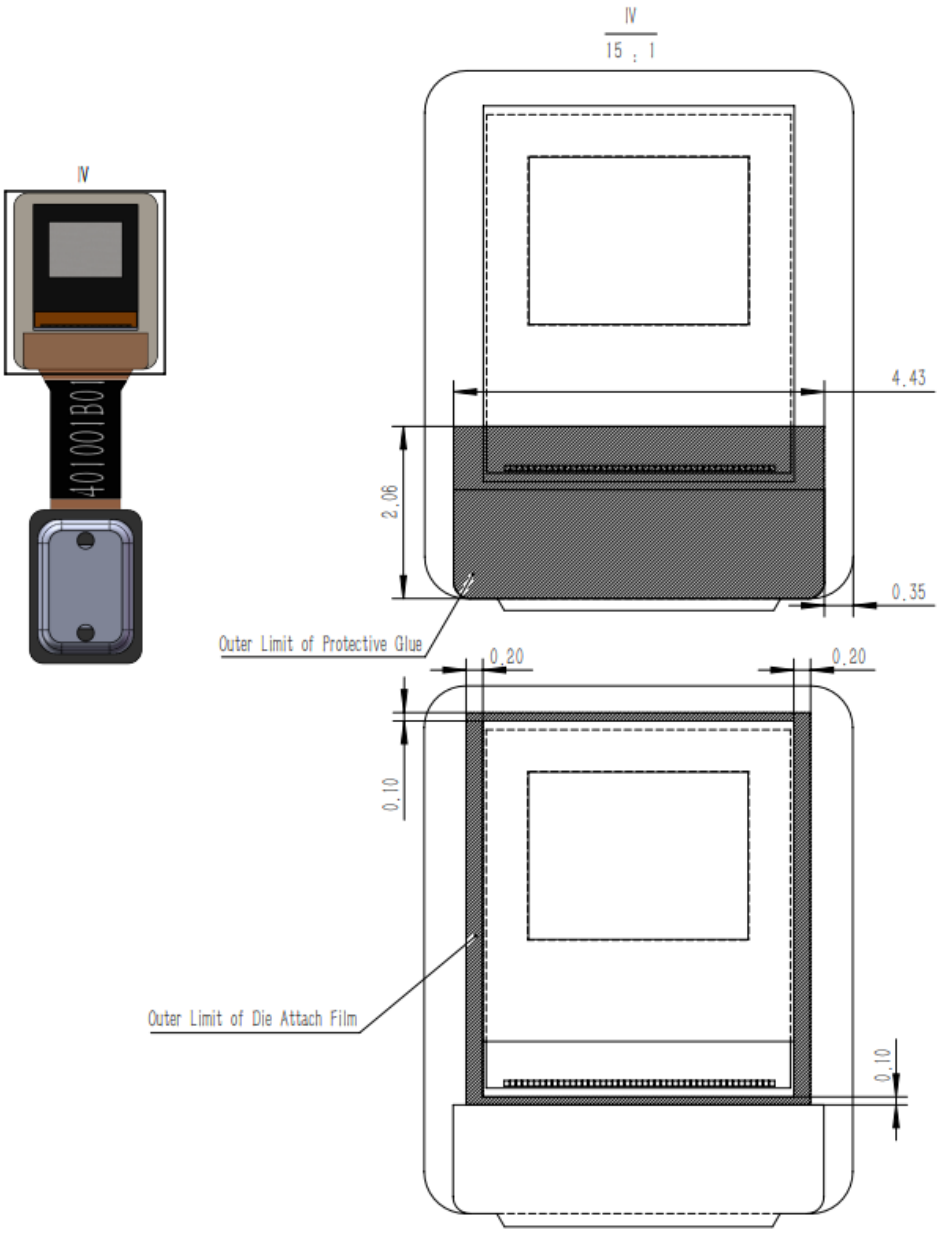
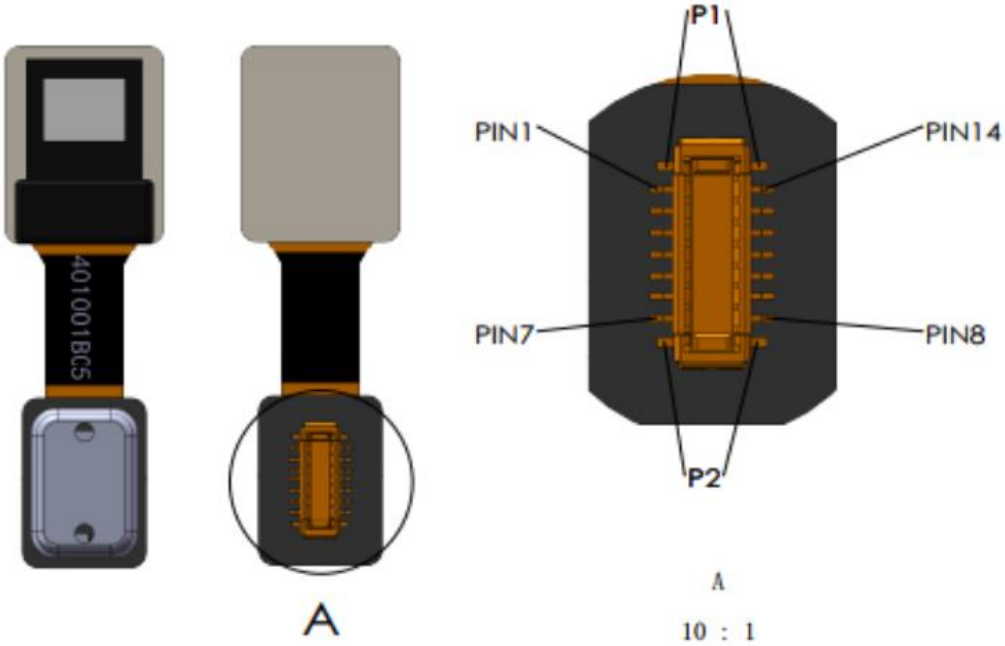


Figure 59 uLED Panel Connector Pin List



PIN No	PANEL IC	FLASH
1	XIN	
2		CS#
3	VCC	VCC
4		WP#
5	GND	GND
6	GND	GND
7	GND	GND
8	IO1	SO
9	PGMDB	
10	IO0	SI
11	CSB	
12	IO3	
13	SCLK	SCLK
14	IO2	
P1	1.2V	
P2	-2V	

9.2 Thermal Characteristics

Ref *Table 7. Thermal characteristics*

10 Revision History

Table 17. Document Revision History

Date	Revision	Changes
07-Jan-2020	1.00	Initial release.
08-Jan-2020	1.01	Updated diagram P10, P36, P37, P38, P39 Changed HSE OSC voltage from 3.3v to 2.5v at P46 Updated SPI timing P49, P50 Updated some diagrams, adjust some descriptions Update package information Adjust some diagrams, adjust some error descriptions Update instruction table P26 Update QSPI read buffer data diagram P40 Add QSPI fast write data diagram P42 Add write status register 3 content P44 Update registers description P20~P24 Update deep power down diagram P30 Update instruction set table P27 Update diagram about status register P45~P48 Adjust register table P21 Change screen on/off to display enable/disable P32 P33 Adjust header and footer Adjust current register 8bits to 6bits P21 P25 Add single command last bit keeps value description P28 and all the single command diagram Adjust display sequence description P53 Delete check sum description Change step description to GMS P21 P24 Delete Status register RFTM description P21 P22 Update package diagram P62
21-May-2021	2.03	Update VCOM voltage P52 jbdproduct Update Luminance feature P1 Update operating temperature P1 Update Max f_{HCLK} to 16Mhz on P55 Update mechanical specifications on P63~64
09-Jul-2021	2.12	Update Read UID command P30 Add Read Chip Information Command P30 Update Current Description P56 P57 Change VDD25IO range from 2.4v~2.6v to 1.62v~3.6v Update description on page 8. Update figure 55 about physical specifications Change name “cache” to “buffer”
16-Nov-2021	2.13	Update power diagram P53 Update panel mechanical specifications. Update panel connector pin list (RSTN connected to VDD25)
23-Nov-2021	2.14	Update register map P21 Change DMEN to W0 (P22), and disable internal demura function forever. Delete status register function P46 Delete 1bit operation

		Adjust instruction table P27 Adjust release deep power down diagram P28
10-Jan-2022	2.15	Update all figures of mechanical specifications
15-Mar-2022	2.16	Change VDDIO to VDD25IO in Table.11
09-Jan-2023	2.17	Adjust Internal oscillator frequency P23 Adjust scan frequency P22
08-Mar-2023	2.18	Delete reset pin description Delete IC power description P48 Add package power description P48 Update temperature sensor information P46
13-Mar-2023	2.19	Add OTP read description
20-Mar-2023	2.20	Add Sync timing description P32 Adjust RFFQ description P22 Add package diagram
30-Mar-2023	2.21	Add Partial refresh mechanism P15
23-Apr-2023	2.22	Updata diagram P11 Update diagram P64
23-Jun-2023	2.23	Import sum function P50
24-Nov-2023	2.24	Update refresh rate description P1 P8 P12 Update VDDIO typical voltage from 2.5v to 1.8v P1 P8 P57