JBD013VGA(4010) User Note

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1 Description

This use note provides supplementary note for various problem solution about 4010 (JBD013VGA).

2 Block Diagram

Figure 1. Panel IC Block Diagram

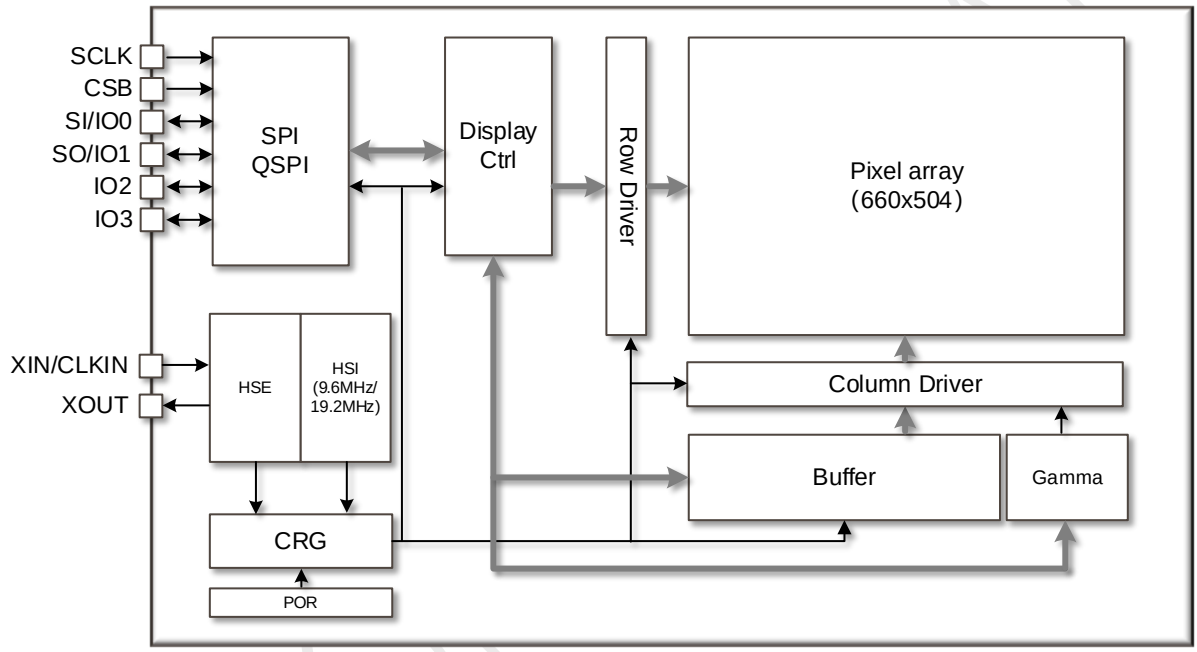
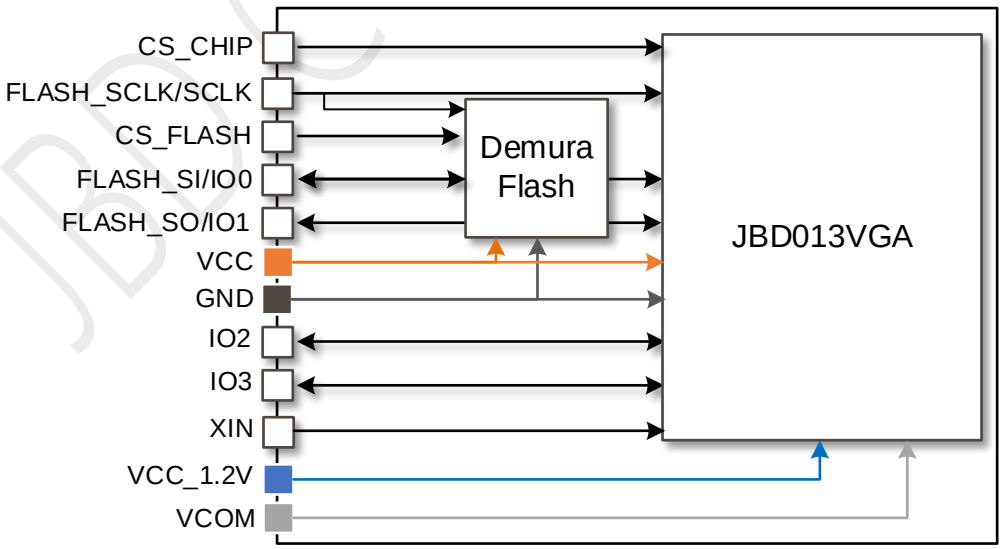


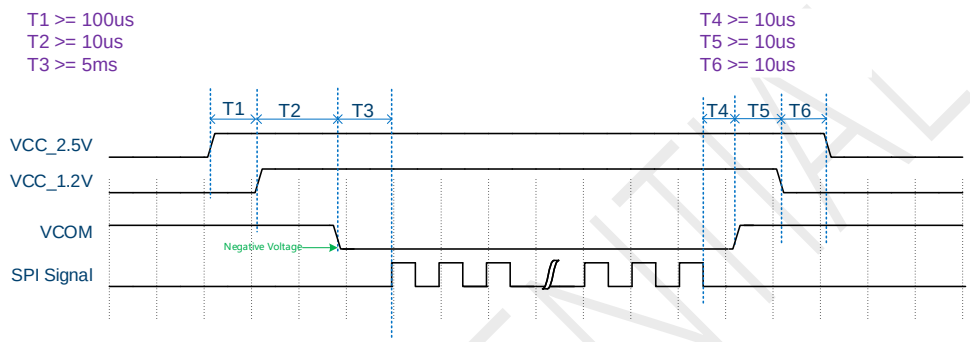
Figure 2. Package Diagram



3 Power Sequence

Package power sequence refer to the following diagram

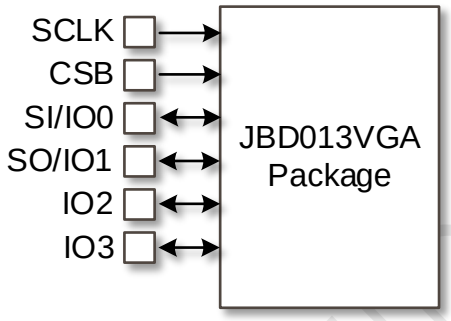
Figure 3 Power On/Off Sequence Diagram for Package



4 How to handle idle IO

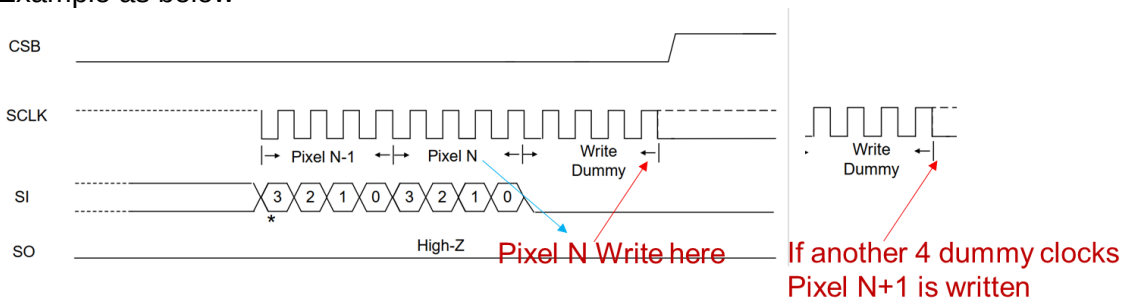
If custom use SPI control panel package only, the solution of idle IO2/IO3 refer to the following suggestion

a) IO2 and IO3 is tied to low is ok, please don't enter QSPI read command, which will induce IO2/IO3 fighting.
b) IO2 and IO3 keep floating is ok too, but may cause some leakage current.
c) The best method is tied to weak pull low with external resistor.



5 Tail dummy clock issue

As datasheet description, SPI or QSPI writing need last 4 dummy clock to finish writing. While the host end is difficult to generate such 4 dummy clocks. More like 8 dummy clocks.
Example as below



If all buffer is written from pixel 0 to the pixel N=640x480-1 with last 8 dummy clocks. and at the same time, N+1=640x480 is written which is outside of buffer address space. Then pixel(N+1) is invalid and abandoned.
If part of buffer is written, N is in the range of (0~640x480-1) with 8 dummy clocks (N is assumed as odd number). And data is sent as 0. Then the N+1 buffer space will be written to 0. this is considered as an invalid value. We suggest that the next write operation address start from N+1, then the pixel(N+1) will write a new right value.

If N is a even number, the operation has 4 dummy clocks, nothing need to do.

6 Luminance adjust issue

Luminance adjusting behavior is related with Status Register 2, bit 2 setting. As below:

Command access: Status Register 2 Read(0x35H) & Write(0x31H)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved		SPF	RFHF	PORF	SYNC_S	OSCS [1]	OSCS [0]
R/0	R/0	R	R	R/0	R/W	R/W	R/W

Bits 7:6 Reserved, must be kept at reset value.

Bits 5 **SPF**: Panel Scan Period Flag

0: Not panel scan time

1: The panel is scanning

Bits 4 **RFHF**: Reload buffer data to Pixel Latch flag

0: No reload operation

1: Reload time

Bits 3 **PORF**: Power on reset flag

0: write 0 to clean

1: Power on happened

Bits 2 **SYNC_S**: SYNC command with screen off select

0: SYNC command has screen off function

1: SYNC command has no screen off function

Bits 1:0 **OSCS [1:0]**: Oscillator Selection

00: Internal oscillator 9.6MHz

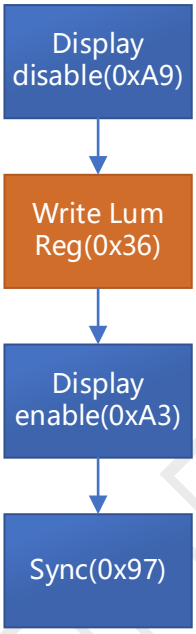
01: Internal oscillator 19.2MHz

1x: External Crystal/External CLKIN from Pin XIN

If SYNC_S is set as 0, means that SYNC command has screen off function. The luminance register can change at any time. The disadvantage is that the screen may flicker.
If SYNC_S is set as 1, means that SYNC command has no screen off function. The luminance registers value changing need to follow below flow chart.

Figure 4 Flow chart about luminance reg value change under no screen off setting

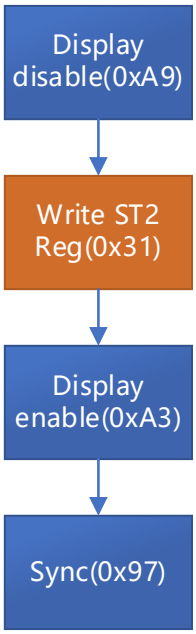
Figure 5 Change luminance register operation



7 Status register 2 adjust issue

Adjust Status register2 b2 or b1, need to follow operation below:

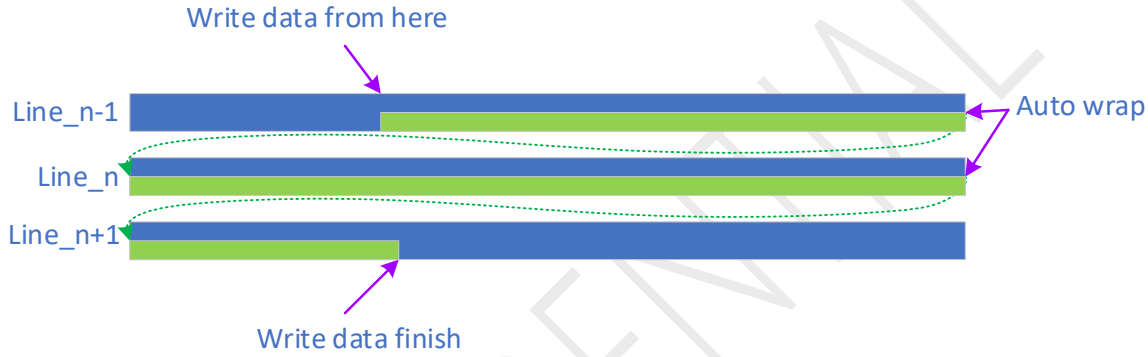
Figure 6 Change Status register 2 operation



8 Partial refresh mechanism

Based on the way of SPI/QSPI write buffer by address, the function of pixel partial update can be realized, so as to achieve the purpose of more efficient update of panel images. Write the buffer with SPI/QSPI, which can automatically wrap lines inside the chip, so that it is more flexible to update partial data in buffer.

Figure 7 Auto wrap diagram



9 Sync timing

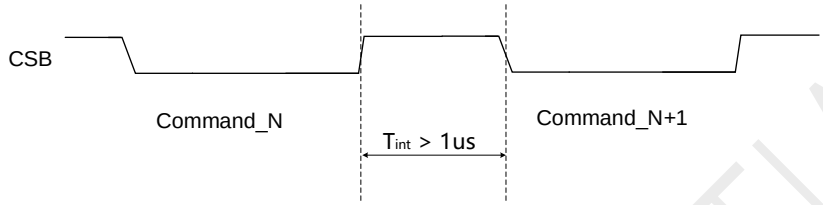
The sync time is related to the clock source frequency。Don't transfer data during sync period, which bring about data confusion. Timing as below

	Clock frequency (MHz)	sync time(ms)
External clock	8	1.00
	16	0.50
	20	0.40
	32	0.25
Internal OSC	9.6	0.83
	19.2	0.42

10 CSB(CS_CHIP) timing between commands

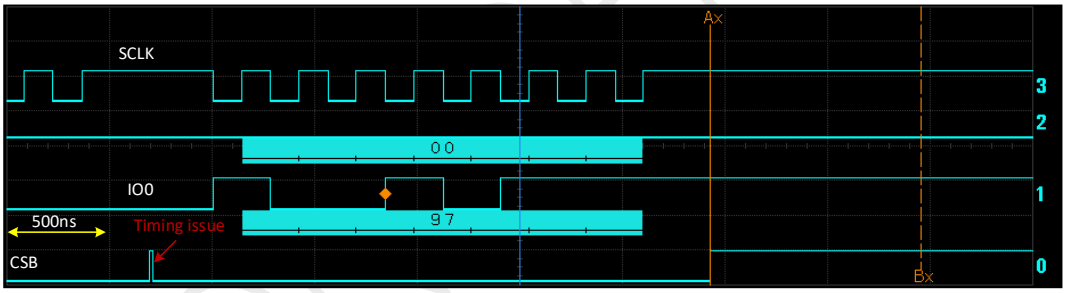
It should be the time (Tint) to keep the CSB high for more than 1 us between spi/qspi commands.

Figure 8 The timing between commands



If the timing is shorter than defined, it will induce command error which will not be accepted by panel IC.

Figure 9 Fail case scene



11 Self-refresh frequency setting

It is not recommended to set the scanning frequency to 30Hz which will induce panel flicker. Setting of 60Hz or upper is suggested.

For example:
Command 0x01 and data 0x10 set the panel refresh frequency to 90Hz.

Command detail as below:

Command access: Status Register 1 Read (0x05H) & Write (0x01H)

Reset value: 0x90

7	6	5	4	3	2	1	0
W0	GMAEN	RFFQ [2:0]			Reserved		
R/W	R/W	R/W	R/W	R/W	W0	W0	W0

Bits 7 **W0**: Write 0 at any reset release status

0: Disable demura function

1: Enable demura function (default)

Bits 6 **GMAEN**: Gamma enables.

0: Disable gamma correction (default)

1: Enable gamma correction

Note: Gamma enables only after panel initial flow

Bits 5:3 **RFFQ** [2:0]: Panel Refresh frequency

If internal OSC 9.6MHz is selected.	If internal OSC 19.2MHz is selected.
000: 30Hz (not suggestion)	000: 60Hz
001: 60Hz	001:120Hz
010: 90Hz (default)	010: 180Hz (default)
011: 120Hz	011: 240Hz
100: 150Hz	100: 300Hz
101: 180Hz	101: 360Hz
110: 210Hz	110: 420Hz
111: 240Hz	111: 480Hz

Bits 2:0 Reserved, if used, need to write 3'b000.

Note: Different refresh frequency (**RFFQ**) has different **luminance register** value range, refer to datasheet description.

12 Panel initial flow

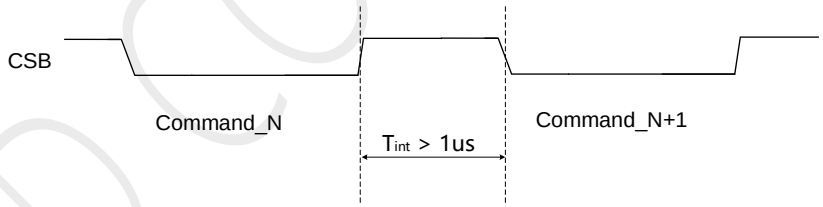
Panel initial as below

Table 1 Panel initial flow example

Time	SI(IO0)	Instructions
	0x06	Write enable
	0x01 0x10	Set Status Register 1 include disable Demura
	0x02 0x00000000… (4 bits)	Write cache data to 0
	0x97	SYNC
wait sync time	0xC0 0x0000	Write offset (0,0)
	0x97	SYNC
wait sync time	0xC0 0x0014	Write offset (0,20)
	0x97	SYNC
wait sync time	0xC0 0x1800	Write offset (24,0)
	0x97	SYNC
wait sync time	0xC0 0x1814	Write offset (24,20)
	0x97	SYNC
wait sync time	0xC0 0x0C0A	Write offset (12,10)
	0x04	Write disable

Note: Keep CSB high timing between (SPI/QSPI) command > 1us

Figure 10 The timing between commands

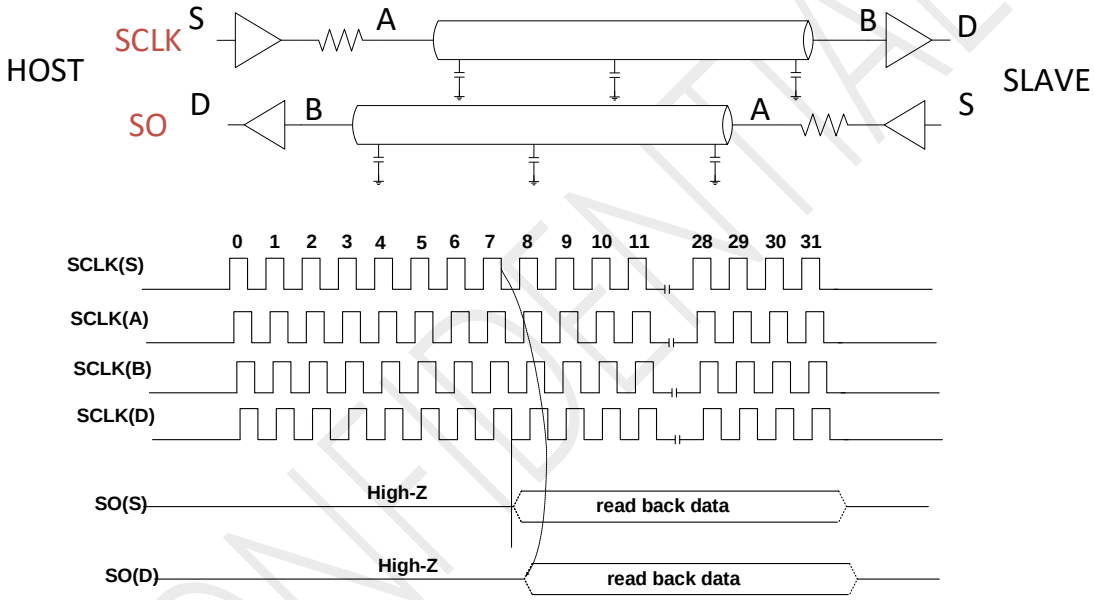


13 About SPI/QSPI speed

SPI/QSPI reading speed is limited by online parasitic capacitance.
The online delay causes limited reading speed, and the solution is as follows:

1. Reduce read speed
2. Delay data capture
3. Shorten the length of the line

Figure 11 Online delay induce read delay example



14 Demura

14.1 Demura attention

The demura function is only valid when the original value is set in the offset register. Other values will cause the Demura dislocation and cause the demura to fail. Similarly, using the image operation inside the chip will also cause demura error。

Offset Register

Command access: Offset Register Read(0xC1H) & Write(0xC0H)

Reset value: 0x0C

7	6	5	4	3	2	1	0
Reserved			ROW [4:0]				
R0	R0	R0	R/W	R/W	R/W	R/W	R/W

Bits 7:5 Reserved, must be kept at reset value.

Bits 4:0 **ROW [4:0]**: Row offset adjust 5 bits value.

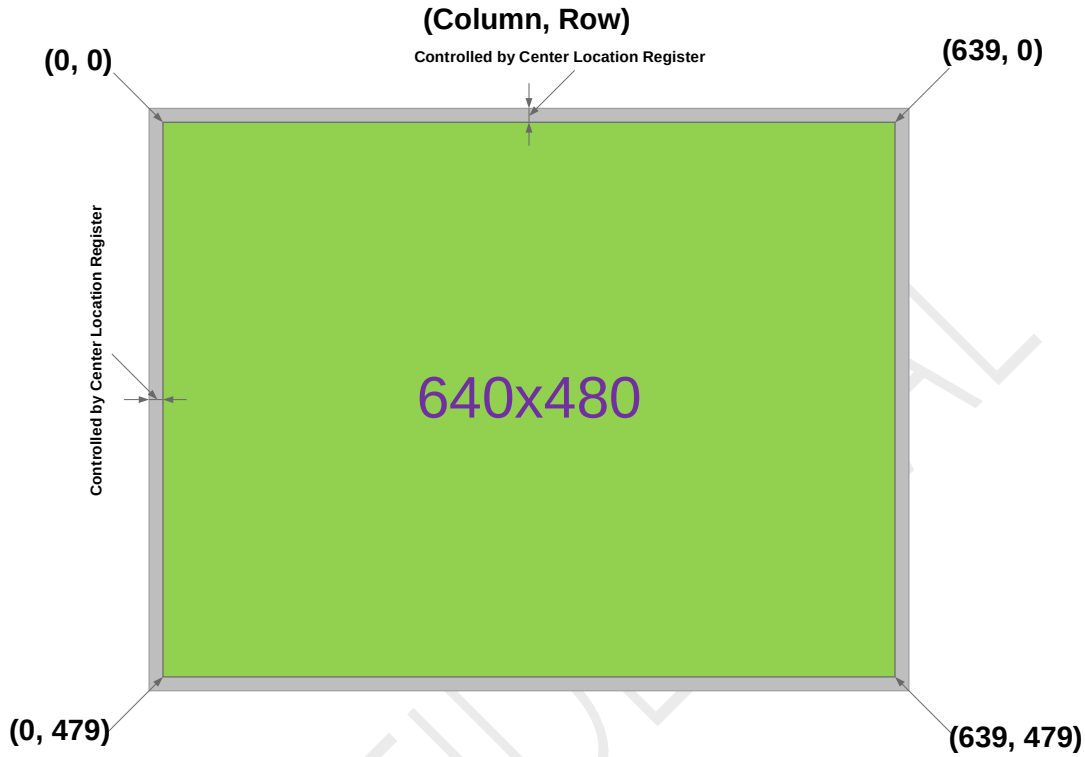
Reset value: 0x0A

7	6	5	4	3	2	1	0
Reserved			COL [4:0]				
R0	R0	R0	R/W	R/W	R/W	R/W	R/W

Bits 7:5 Reserved, must be kept at reset value.

Bits 4:0 **COL [4:0]**: Column offset adjust 5 bits value.

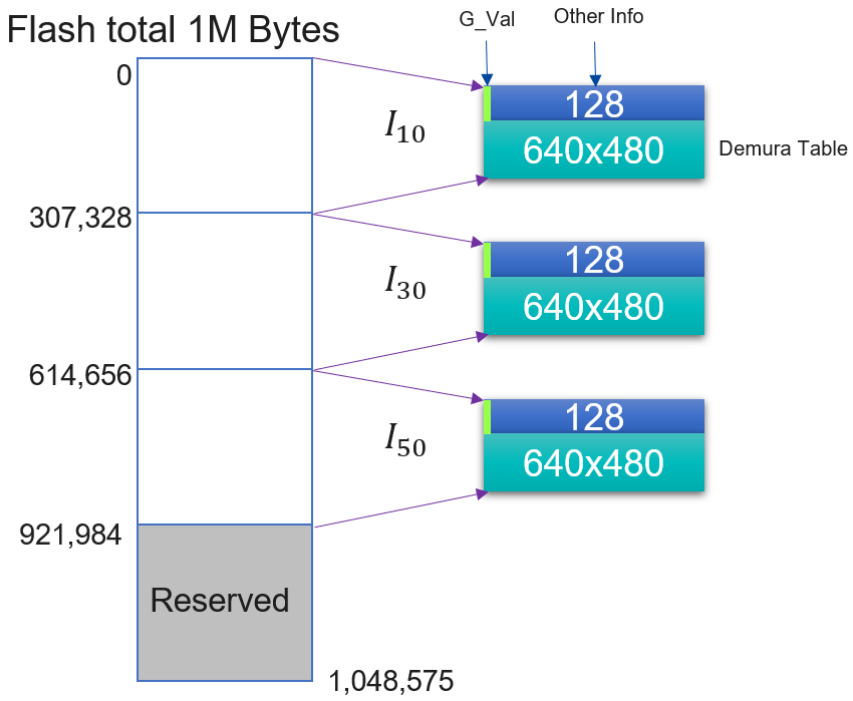
Figure 12 Panel overview



14.2 Demura flash data mapping

Only 3 current value support. I10, I30, I50.

Figure 13 Compatible Flash Memory Mapping



15 Temperature sensor

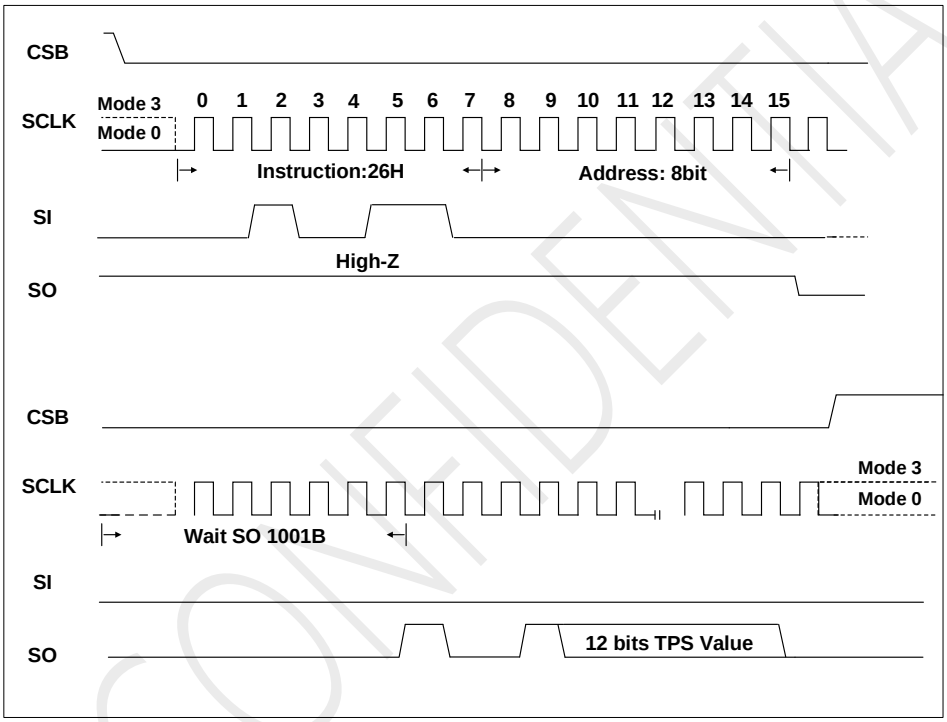
15.1 Temperature sensor value acquisition

Temperature Sensor Read command can read temperature sensor value. Users can get temperature of panel corners through corresponding calculation.

Ref *Figure 14*

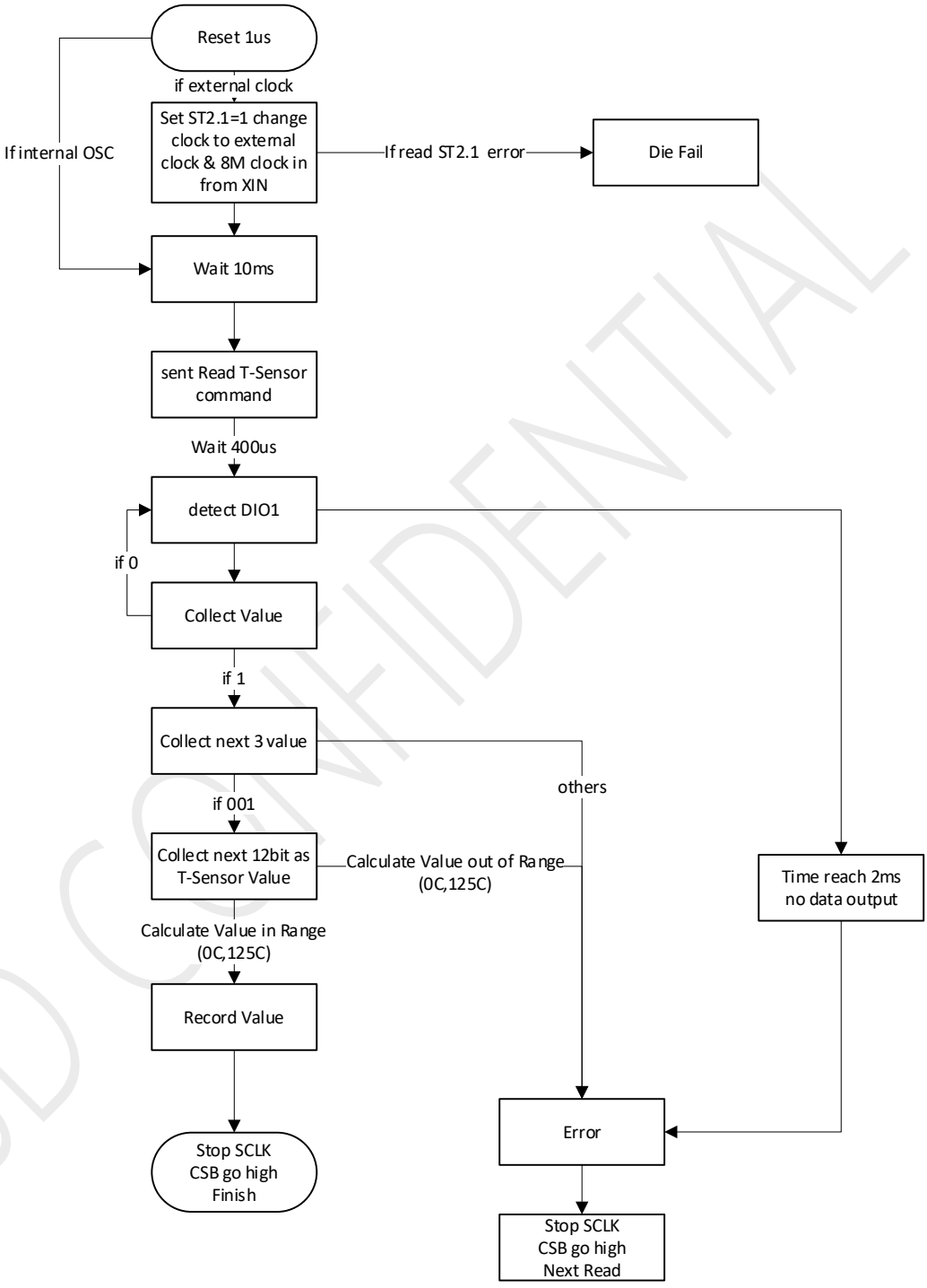
Note: Address = 0x02

Figure 14 Temperature Sensor Read Command Diagram



The reading process is shown in the figure. The read value is recorded as the current temperature from internal temperature sensor (Tv). This is a 12-bits value.

Figure 15 Temperature sensor value read flow



15.2 Temperature value calculation

During the CP test, the values of 30 ℃ and 80 ℃ will be burned in the OTP and recorded as T_{30} and T_{80}. Recording position in OTP as below:

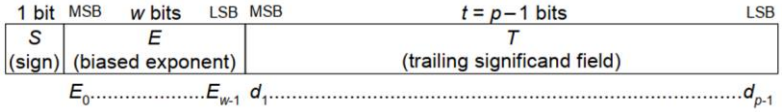
Mapping Table	MSB		~~~~~~~~~			~~~			~~~			~~~			~~~			~~~~~~~~~		LSB
Address Hex	95	94	~~~~~~~~~		64	63	~~~	48	47	~~~	32	31	~~~	24	23	~~~	12	11	~~~~~~~~~	1	0
0x1FE0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	30C T3 Sensor value		
0x1FE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	80C T3 Sensor value		
0x1FE2	0	0	0	0	0	K value						1/K value								

K and 1/K value are recorded as floating-point number base on IEEE(754-2019) Standard.

a) 1-bit sign S

b) w-bit biased exponent $E = e + bias$

c) $(t = p - 1)$-bit trailing significand field digit string $T = d_1 d_2 \ldots d_{p-1}$; the leading bit of the significand, d_0, is implicitly encoded in the biased exponent E.



The current temperature(T) calculation formula is as below

$$T = \frac{(T_v - T_{30}) * 50}{T_{80} - T_{30}} + 30$$

If calculated by K or 1/K

$$K = \frac{T_{80} - T_{30}}{50}$$

$$T = \frac{(T_v - T_{30})}{K} + 30$$

or $T = (T_v - T_{30}) * (1/K) + 30$

16 About IO voltage and VDDIO

As panel IC 4010, the VDDIO range from 1.68v~3.6v is acceptable. And must keep IO high value is same as VDDIO.

Figure 16 Input/Output diagram

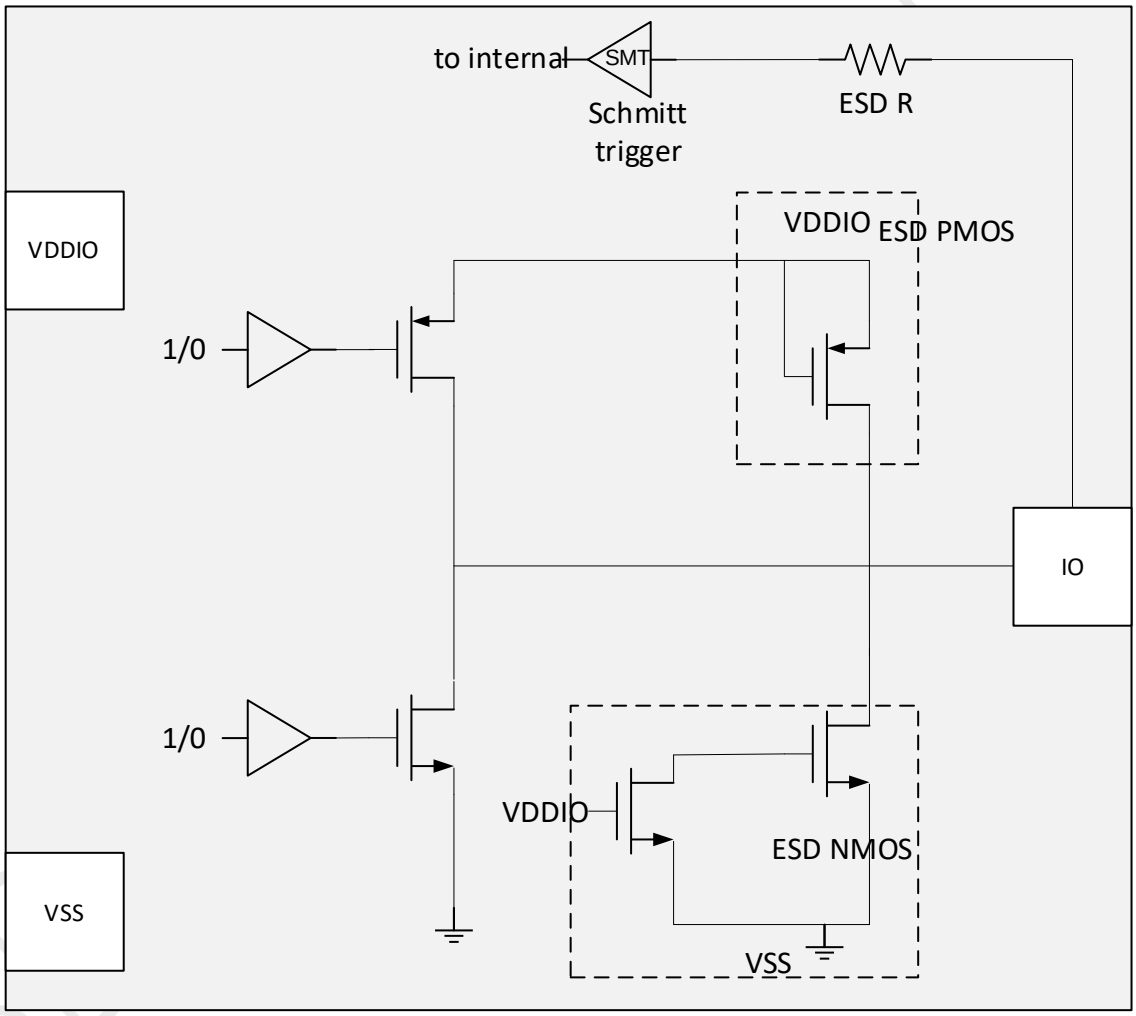


Figure 17 Input diagram

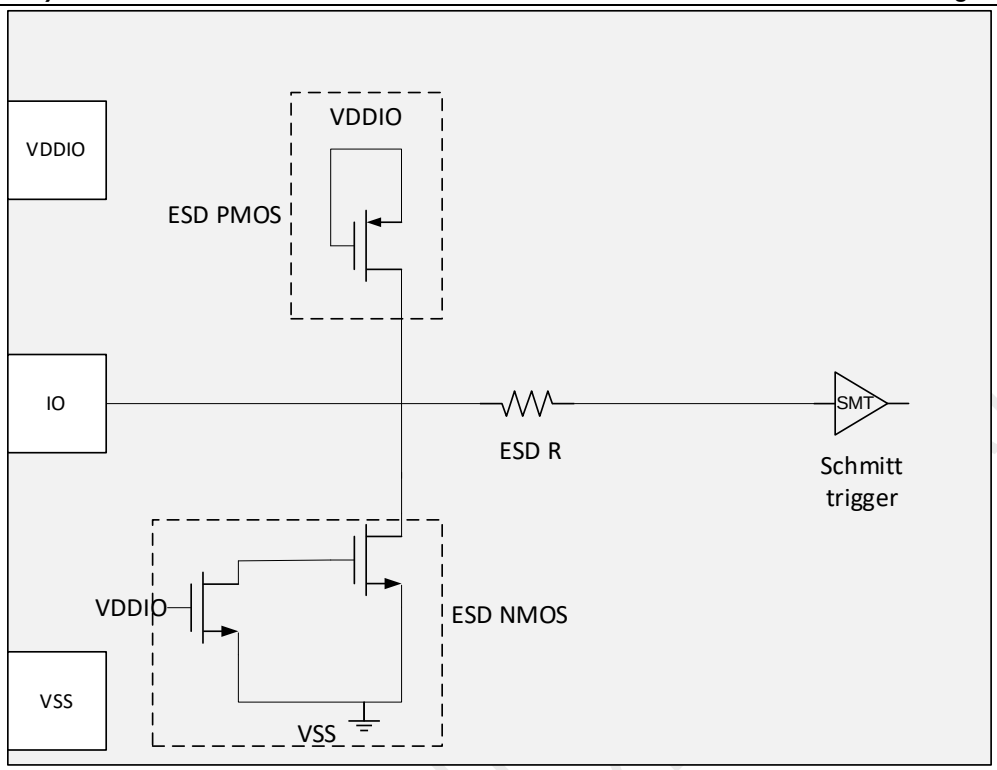
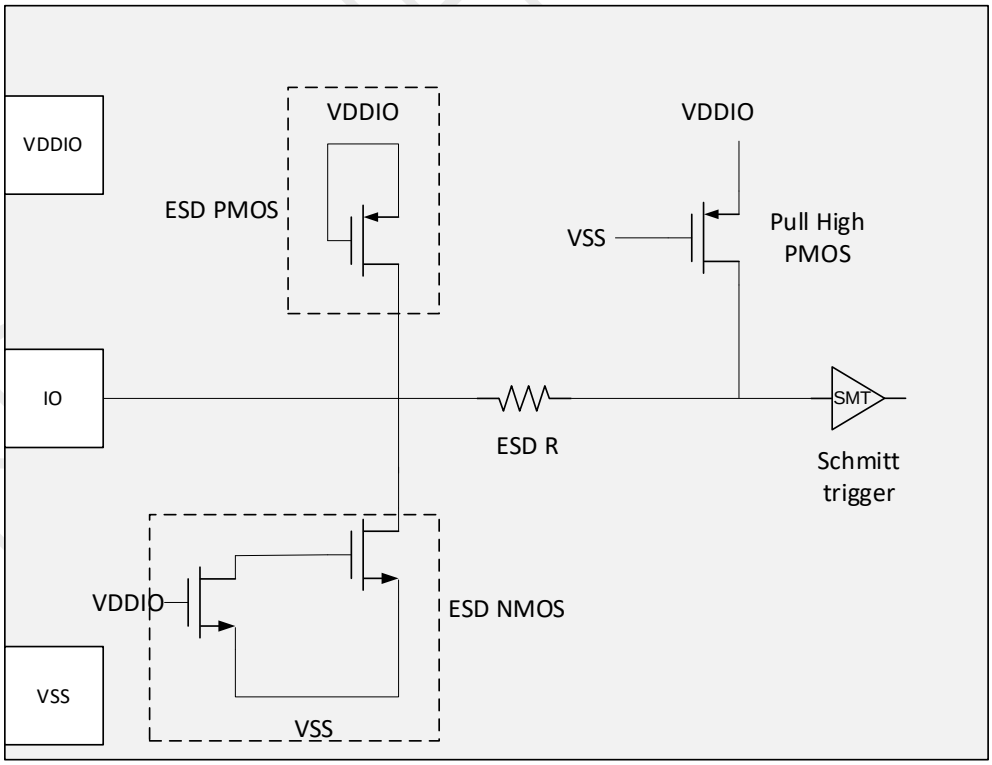


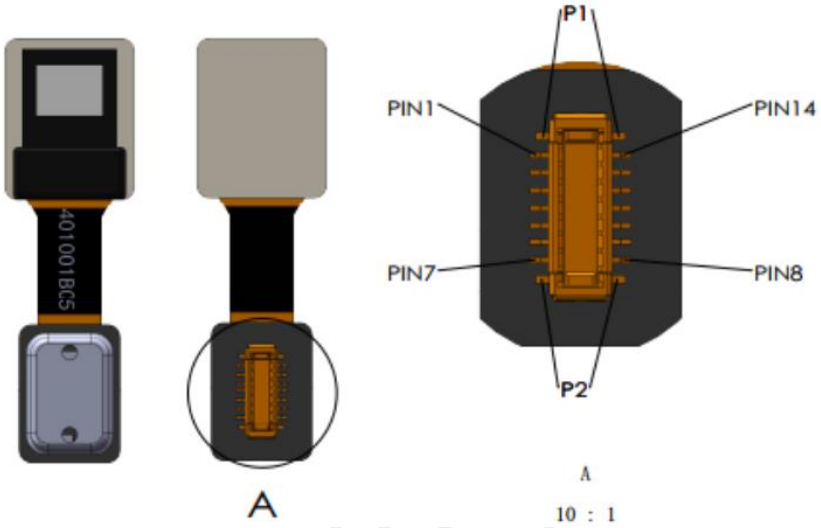
Figure 18 Input with pull high diagram



17 About special pin description

As panel package incidental flash, the WP# pin need connect to customer board ground for protect flash error writing or erasing under complex environment.
Pin 9 is a special pin for programming OTP, and don't connect any other signal line.

Figure 19 uLED Panel Connector Pin List



PIN No	PANEL IC	FLASH
1	XIN	
2		CS#
3	VCC	VCC
4		WP#
5	GND	GND
6	GND	GND
7	GND	GND
8	IO1	SO
9	PGMDB	
10	IO0	SI
11	CSB	
12	IO3	
13	SCLK	SCLK
14	IO2	
P1	1.2V	
P2	-2V	

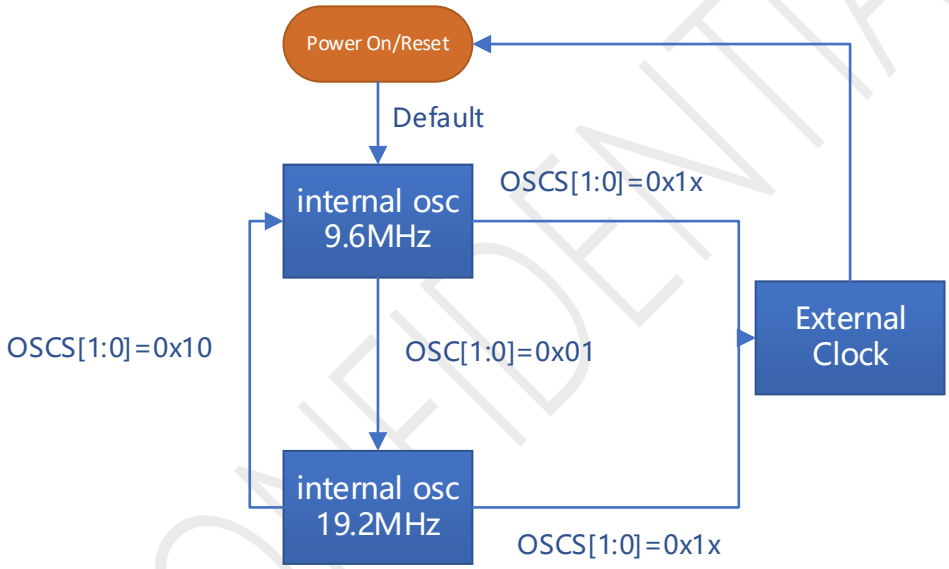
18 About clock switch

Status registers 2, bit1 and bit0 are used for setting system clock source. The setting method as below:

Bits 1:0 OSCS [1:0]: Oscillator Selection
00: Internal oscillator 9.6MHz(default)
01: Internal oscillator 19.2MHz(suggestion)
1x: External Crystal/External CLKIN from Pin XIN

The setting flow need to follow below methods.

Figure 20 System clock setting flow



19 Revision History

Table 2 Document Revision History

Date	Revision	Changes
21-Apr-2023	0.09	Internal version
05-Dec-2023	0.12	1.Add WP# control of package P25 2.Add clock change note P26 3. Delete Package List and Connector chapters
14-Dec-2023	0.13	1.Add Status register adjust issue chapters