MicroConverter® 12-Bit ADCs and DACs with Embedded High Speed 62-kB Flash MCU

Silicon Anomaly List — ADuC841/ADuC842/ADuC843

A. This Anomaly List represents the known bugs, anomalies and work-arounds for the ADuC841/ADuC842/ADuC843 MicroConverter parts.

B. The Anomaly listed, apply to all ADuC841/ADuC842/ADuC843 packaged material branded as follows:

Third Line: **F21 <date code>**

C. Analog Devices Inc. is committed, through future silicon revisions to continuously improve silicon functionality. Analog Devices Inc. will use its best endeavors to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended work-arounds outlined in this document.

D. ADuC841/ADuC842/ADuC843 Silicon Anomaly List Revision History :

Revision	Date	Relevance	Silicon Status	# of Bugs Reported
C	May 2004	All Silicon branded Third Line: F21 <date code>	Release	5 Errata

REV C May 2004

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1. SPI INTERFACE [er006]:

Background:
The SPI can either be used on the standard pins or can be moved to P3.3, P3.4 and P3.5 by setting the MSPI bit in CFG841/CFG842. When the MSPI bit is set P3.3 should be MISO, P3.4 MOSI and P3.5 SCLOCK.

Issue A:
By setting the MSPI bit the P3.3, P3.4 and P3.5 have the following configuration.
P3.3 = MISO, P3.4 = SCLOCK, P3.5 = MOSI

Work-Around A:
None.

Issue B:
When the ADuC841/ADuC842/ADuC843 is set up as an SPI slave the device may receive or transmit bytes incorrectly.

Work-Around B:
None

Related Issues:
None

2. READING/WRITING TO DATAFLASH/EE [er007]:

Background:
There are 4kB of DATAFLASH/EE which can be used for non-volatile storage.

Issue:
If an interrupt occurs during a DATAFLASH/EE read or write operation, code execution may resume at a random program memory address.

Work-Around:
Disable all interrupts prior to a read or write operation. This can be done by setting the EA bit to 0.

Related Issues:
None

3. PWM OPERATION [er008]:

Background:
The PWM output rate is determined by the PWMxH and PWMxL registers for the PWM0 and PWM1 outputs.

Issue:
Modifying RAM address 2EH will cause the PWM timer to be reloaded.

Work-Around:
For Assembly code: Do not use memory location 2EH
For C code: Assign a dummy variable to location 9AH using the following code

```
idata unsigned int ui32Dummy[2] _at_ 0x2E;
```

Related Issues:
None

4. WDT OPERATION [er009]:

Background:
The ADuC841, ADuC842, and ADuC843 incorporate a Watchdog Timer. The purpose of the WDT is to ensure the part is never stuck in an endless loop by generating either a hardware reset or an interrupt event that vectors to the WDT ISR.

Issue:
If the WDT generates an interrupt as opposed to a hardware reset, and if the ISR subsequently sets up the WDT to time out to a hardware reset, the reset is ignored.

Work-Around:
Ensure that a double write to the WDCON is executed inside the ISR with the first write being a reset of the WDT. For example:

```
void isr_wdt( void ) interrupt 11
{
WDWR = 1;         // This first WDT write is required to get the WDT to work inside the ISR.
WDCON  = 0x60;// Reset WDT.
WDWR = 1;         // Now set the WDT to the required 1s timeout
WDCON  = 0x62;// select reset after 1000mS
while(1);
}

void main(void)
{
EA = 0;
WDWR = 1;         // Allow write to WDCON
WDCON = 0x6A;       // timeout=1000mS, WDT enable, WDT ISR Interrupt
while (1);
}
```

Related Issues:
None

5. LEVEL TRIGGERED EXTERNAL INTERRUPT OPERATION [er010]:

Background:
The ADuC841/ADuC842/ADuC843 incorporate two external interrupt sources (INT0 & INT1) that can be configured to respond to either an edge event or a level event.

Issue:
If an interrupt occurs on the INT0 or INT1 pins and is then removed within one core instruction cycle, the interrupt vector address that is generated may be incorrect resulting in a vector to 0000H. This effectively restarts code execution.

Work-Around:
To ensure that this does not occur all source for a level trigger must be kept low for a minimum of 9 core clock cycles.

Related Issues:
None

ADuC841/ADuC842/ADuC843 Silicon Anomaly Revision History

Errata #	Description	Status
Updated on Rev F. Silicon		
er001	**MODE 0 UART OPERATION**	**FIXED**
er002	**USE OF THE EXTENDED STACK POINTER**	**FIXED**
er003	**USE OF I2C IN SLAVE MODE WITH STOP INTERRUPT ENABLED**	**FIXED**
er004	**USE OF I2C IN SLAVE MODE WITH STOP INTERRUPT DISABLED**	**FIXED**
er005	**I2C DATA TRANSFER**	**FIXED**