MicroConverter® Multichannel 24-/16-Bit ADCs with Embedded 62 kB Flash and Single-Cycle MCU

Silicon Anomaly Sheet

ADuC845/ADuC847/ADuC848

This anomaly list represents the known bugs, anomalies, and workarounds for the ADuC845, ADuC847, and ADuC848 MicroConverter products. The ADuC845/ADuC847 packaged material is branded as follows:

First Line ADuC845BS or ADuC845BCP
ADuC847BS or ADuC847BCPP
Third Line A2Y and B2W

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended workarounds outlined here.

ADUC845/ADUC847/ADUC848 SILICON ANOMALY SHEET REVISION HISTORY

Revision	Date	Relevance	Silicon Status	Number of Bugs Reported
B.0	April 2004	All silicon branded ADUC845BS or ADuC845BCP ADuC847BS or ADuC847BCP Third Line: A2Y and B2W	Sample	8

ANOMALIES

1. SPI Slave Mode Interface [er001]

Background:	The SPI serial interface is available on Pins P2.0, P2.1, P2.2, and P2.3. These pins represent SCLOCK, MOSI, MISO, and SS, respectively. The control SFR for SPI is SPICON.
Issue:	When the ADuC845/ADuC847/ADuC848 are set up as SPI slave devices, they may receive bytes incorrectly.
Workaround:	Incorporate checksums into all communication with the ADuC845/ADuC847 slave. If an error occurs, it is necessary to reset the slave via the SPE bit in SPICON and retransmit the data from the master.
Related Issues:	None.

2. Interrupts During Reading/Writing to Data FLASH/EE [er002]

Background:	There are 4 kB of DATAFLASH/EE that can be used for nonvolatile data storage.
Issue:	If an interrupt occurs during a DATAFLASH/EE read or write operation, code execution following the ISR may resume at a random program memory address.
Workaround:	Disable all interrupts prior to a read or write operation. This can be done by setting the EA bit to 0.
Related Issues:	None.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

3. PWM Operation [er003]

Background:	The PWM output rate is determined by the PWMxH and PWMxL registers for the PWM0 and PWM1 outputs.	
Issue:	Modifying RAM address 2EH causes the PWM timer to be reset.	
Workaround:	For Assembly code:	Do not use memory location 2EH.
	For C code:	Assign a dummy variable to location 2EH using the following code..... `idata unsigned int ui32Dummy[2] _at_ 0x2E;`
Related Issues:	None.	

4. I²C Operation [er004]

Background:	The I2CDAT register is used to read or write data to the I²C bus. The I2CDAT register has an SFR address of 9AH.	
Issue:	During an I²C transfer, if a user accesses the RAM address 9AH, the contents of the I2CDAT SFR can be modified.	
Workaround A:	For Assembly code:	Do not use memory location 9AH.
	For C code:	Assign a dummy variable to location 9AH by using the following code thereby preventing C from using it. `idata unsigned int ui32Dummy[2] _at_ 0x9A;`
Related Issues:	None.	

5. ADC Noise [er005]

Background:	The ADuC845 incorporates two 24-bit S-? ADCs, and the ADuC847 and ADuC848 incorporate a 24-bit and 16-bit S-? ADC, respectively. These ADCs are specified for typical noise performance as described in the relevant noise tables of the data sheet.
Issue:	ADC noise performance degrades when operating at maximum MCU clock frequency as determined via the CD bits in the PLLCON SFR.
Workaround:	For the duration of an ADC conversion, the CD bits should be set to 0x3 or greater. Note that the default CD setting is 0x3
Related Issues:	None.

6. Watchdog Timer [er006]

Background:	The ADuC845, ADuC847, and ADuC848 incorporate a Watchdog Timer. The purpose of the WDT is to ensure the part is never stuck in an endless loop by generating either a hardware reset or an interrupt event that vectors to the WDT ISR.
Issue:	If the WDT generates an interrupt as opposed to a hardware reset, and if the ISR subsequently sets up the WDT to time out to a hardware reset, the reset is ignored.

Workaround:	Ensure that a double write to the WDCON is executed inside the ISR with the first write being a reset of the WDT. For example:
	`void isr_wdt( void ) interrupt 11`
	`{`
	`  WDWR = 1;  // This first WDT write is required to get the WDT to work inside the ISR.`
	`  WDCON  = 0x60;// Reset WDT.`
	`  WDWR = 1;  // Now set the WDT to the required 1s timeout`
	`  WDCON  = 0x62;// select reset after 1000mS`
	`  while(1);`
	`}`
	`void main(void)`
	`{`
	`  EA = 0;`
	`  WDWR = 1;  // Allow write to WDCON`
	`  WDCON = 0x6A; // timeout=1000mS, WDT enable, WDT ISR Interrupt`
	`  while (1);`
	`}`

Related Issues:	None.

7. Stack Pointer in ULOAD Mode [er007]

Background:	When starting user code, the stack pointer should, by default, be initialized to Address 07h.
Issue:	In ULOAD mode, the stack pointer defaults to 03h causing conflict between ram locations R4 to R7 and the stack.

Workaround:	Manually change in code the stack pointer address to 07h or to the address that is required upon entry to ULOAD mode, that is,
	`MOV SP, #07h`
	or
	`SP = 0x07;`

Related Issues:	None.

8. Level Triggered Interrupt Operation [er008]

Background:	The ADuC845/7/8 incorporate two external interrupt sources (INT0 & INT1) that can be configured to respond to either an edge event or a level event.
Issue:	If an interrupt occurs on the INT0 or INT1 pins and is then removed within one core instruction cycle, the interrupt vector address that is generated may be incorrect resulting in a vector to 0000H. This effectively restarts code execution.
Workaround:	To ensure that this does not occur the level triggered interrupt source must be kept low for a minimum of 9 core clock cycles.
Related Issues:	None.

ADuC845/ADuC 847/ADuC 848 SILICON ANOMALY REVISION HISTORY

Anomaly No.	Description	Status
er001	SPI Slave Mode Interface	Pending
er002	Interrupts During Reading/Writing to DATAFLASH/EE	Pending
er003	PWM Operation	Pending
er004	I^2C Operation	Pending
er005	ADC Noise	Pending
er006	Watchdog Timer	Pending
er007	Stack Pointer in ULOAD Mode	Pending
Er008	Level Triggered Interrupt Operation	Pending