MicroConverter® Technical Note – uC016
Migrating to the ADuC832 from the ADuC812

Introduction

The ADuC832 is an upgrade to the ADuC812. Its additional features include 62kB program flash, 2kB on chip RAM and 4kB data flash. Full details of the additional features of the ADuC832 are detailed in technote uC017.

To migrate an application from the ADuC812 to the ADuC832 there a number of hardware and software changes which need to be addressed. There are a few registers which are defined differently from the original ADuC812. This document is designed to allow an ADuC812 user modify their system quickly and efficiently.

Modifications

The following features and their control registers operate in a different manner:

ADC Operation
- ADCCON1
- ADCCON2
- ADCCON3
- Input stage and sampling capacitor.

Voltage Reference Connection
- Driving in an external reference
- Using the internal reference externally in the application

Power Supply Monitor
- PSMCON

Interrupt Structure
- IE2

Watchdog Timer
- WDCON

Flash Programmming/Erase
- ETIM1,ETIM2

SPI Timing
- SPICON

Port 3
- Drive Capability of Port 3

PLL
- PLLCON

ADC Operation

ADCCON1: This register controls the conversion and acquisition times, hardware conversion modes and power-down modes.

On the ADuC832 this register has been redefined as follows

ADCCON1.7	ADC Mode (1=ON, 0=OFF)
ADCCON1.6	External Vref select bit (0=On-Chip Reference)
ADCCON1.5	ADC clock divider bit
ADCCON1.4	ADC clock divider bit
ADCCON1.3	Acquisition time select bit
ADCCON1.2	Acquisition time select bit
ADCCON1.1	Timer 2 convert enable
ADCCON1.0	External CONVST enable

The differences from the ADuC812 are
- The ADC on the ADuC832 has just one power control bit which determines whether it is power on or not.
- ADCCON1.6 is set by the user if using an external reference.
- The ADC Clock divider ratios are now 8,4,16,32.
- The CONVST input in DMA will generate one ADC conversion per trigger, this differs from the ADuC812 where the CONVST input in DMA mode would trigger continuous conversions for the DMA block. The CONVST input in normal mode operates the same as per the ADuC812

The rest of the bits in the register have the same function as in the ADuC812 controlling the acquisition time

ADCCON2: The ADCCON2 register controls ADC channel selection and conversion modes.
On the ADuC832 this control register operates in the exact same manner as the ADuC812. There are additional channels which may be selected on the ADuC832.

CS3	CS2	CS1	CS0	CH#
1	0	0	1	DAC0
1	0	1	0	DAC1
1	0	1	1	AGND
1	1	0	0	VREF

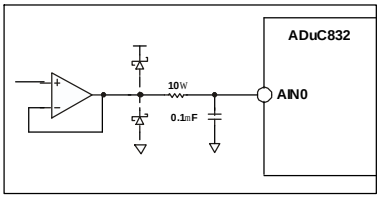
ADCCON3: The ADCCON3 register controls the operation of various calibration modes as well as giving an indication of ADC busy status.

It is defined as follows

ADCCON3.7	Busy indicator flag (0=ADC not active)
ADCCON3.6	Gain calibration disable bit (0=gain cal enabled)
ADCCON3.5	Number of averages selection bit
ADCCON3.4	Number of averages selection bit [15,1,31,63]
ADCCON3.3	Offset calibration disable bit (0=offset cal enabled)
ADCCON3.2	Calibration mode (0=device cal, 1=system cal)
ADCCON3.1	Calibration type (0=offset cal, 1=gain cal)
ADCCON3.0	Start calibration

The differences from the ADuC812 are
- On the ADuC812 this register was used only to give the ADC busy status. This register is used to control ADC calibration on the ADuC832 as well as the busy status flag.

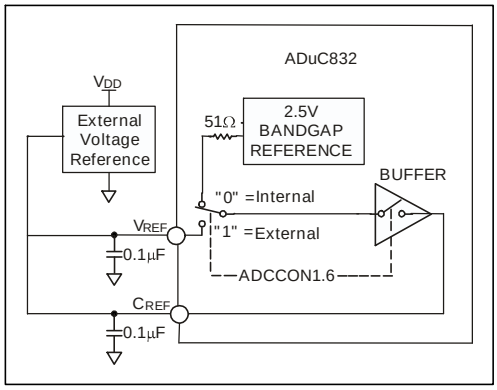
Input Stage to the ADC: On the ADuC812 the internal sampling capacitor was 2Pf. On the ADuC832 this internal sampling capacitor is now 32Pf. This means that a larger external capacitor is required on the input as shown in the diagram below.



Voltage Reference

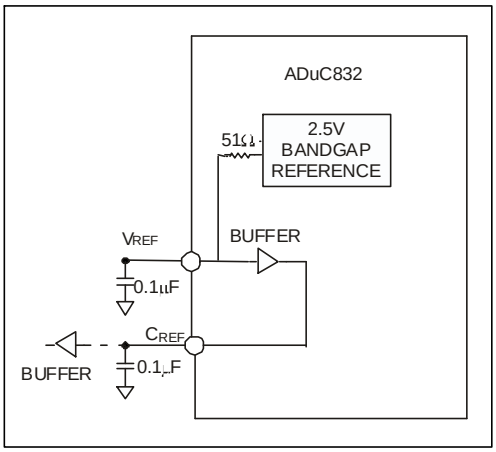
Connecting an external reference: On the ADuC812 to connect in an external reference theVref pin was overdriven. This method can still be used with the ADuC832. This allows backwards compatibility with the ADuC812. Note that ADCCON1.6 should be set to select the internal refernce if this method is used allowing the internal reference to be overdriven. Note that this method introduces a gain error which will then have to be calibrated out.

The recommend method for connecting in an external reference is as shown below. This does not introduce a gain error as in the previous case.



Using the internal refernce: On the ADuC812 to use the internal refernce as a reference to external circuitry the Vref pin was used. This can be used to maintain compatibility with the ADuC812 however there is a gain error between this an the reference used for the ADC conversions.

The recommended method is to use the Cref pin as shown below.



Power Supply Monitor

PSMCON: This register controls the operation of the power supply monitor which monitors both the DVdd supply levels.

On the ADuC832 this register has been redefined as follows

PSMCON1.7	RESERVED
PSMCON1.6	PSM Status bit (1=normal / 0=fault)
PSMCON1.5	PSM Interrupt bit
PSMCON1.4	Trip Point Select bit
PSMCON1.3	Trip Point Select bit [4.37V,3.08V,2.93V,2.63V]
PSMCON1.2	RESERVED
PSMCON1.1	RESERVED
PSMCON1.0	PSM Enable control (0=Off, 1=On)

The differences from the ADuC812 are

- The trip point at 4.63V has been removed
- The AVDD/DVDD fault indicator has been removed since AVDD and DVDD have to remain within 0.3V.

Interrupt Structure

IE2: This register is the secondary interrupt enable register.
To reflect the changes below this register is referred to as **IEIP2** in all documentation relating to the ADuC832

On the ADuC832 this register has been redefined as follows

IEIP2.7	RESERVED
IEIP2.6	Priority of the Time Interval Counter Interrupt
IEIP2.5	Priority of the Power Supply Monitor Interrupt
IEIP2.4	Priority of SPI Interrupt
IEIP2.3	RESERVED – This bit must contain 0
IEIP2.2	Enable Time Interval Counter Interrupt
IEIP2.1	Enable Power Supply Monitor Interrupt
IEIP2.0	Enable SPI Interrupt

The differences from the ADuC812 are

- 3 priority bits are now contained in this register for the Timer Interval Counter (new feature), Power Supply Monitor and SPI interface
- 1 extra enable bit IEIP2.2 is added to enable interrupts for the Time Interval Counter

Watchdog Timer

WDCON: This register controls the operation of the Watchdog Timer whose purpose is to generate a device reset or interrupt within a reasonable amount of time if the MicroConverter enters an erroneous state.

On the ADuC832 this register has been redefined as follows

WDCON.7 PRE3 Watchdog timeout selection bits
WDCON.6 PRE2
WDCON.5 PRE1
WDCON.4 PRE0 [15.6,31.2,62.5,125,250,500,1000,2000,0.0ms]
WDCON.3 WDIR Watchdog interrupt response bit
WDCON.2 WDS Watchdog status flag (1=Watchdog timeout)
WDCON.1 WDE Watchdog enable control (0=disabled)
WDCON.0 WDWR Watchdog write enable (set to enable write)

The differences from the ADuC812 are

- On the ADuC812 the watchdog timer was clocked by a 64kHz R/C oscillator. On the ADuC832 the watchdog timer is clocked directly by the 32.768kHz external crystal.
- To write to the watchdog enable bit the watchdog write enable must be set first.
- On the ADuC812 to refresh the watchdog WDR1 and WDR2 were set sequentially. On the ADuC832 to refresh the watchdog the WDE bit must be set within the watchdog timeout period.

Flash Programming/Erase

ETIM1,ETIM2: These registers control the Flash/EE erase and program timing. On power up on the ADuC812 these registers are set to the appropriate values for a 11.0592MHz crystal. If the user is using a different crystal value the user was required to modify these registers according to the formula

ETIM2,ETIM1 = 100uS * Fosc

On the ADuC832 the Flash/EE program and erase times are fixed and do not need to be modified by the user.

SPICON

SPI Timing: On the ADuC812 the SPI bit rate select bits gave a bit rate of fosc/[4,8,32,64]. On the ADuC832 the SPI bit rate can be fcore/[2,4,8,16]

Port 3

Drive Capability of Port 3: On the ADuC812 port 3 was specified to sink 8mA. On the ADuC832 port 3 is specified to sink 4mA.

PLL

On the ADuC812 the core was clocked directly by the external crystal. On the ADuC832 there is an internal PLL which generates the core frequency. This PLL locks onto an external 32.768kHz crystal.

PLLCON: This register controls the operation of the PLL. The core frequency is determined by the CD bits contained in PLLCON i.e PLLCON.2, PLLCON.1, PLLCON.0

PLLCON.7 Oscillator powerdown control bit (0=normal)
PLLCON.6 PLL lock indicator flag (0=out of lock)
PLLCON.5 (this bit must contain 0)
PLLCON.4 (this bit must contain 0)
PLLCON.3 “Fast interrupt” control bit (0=normal)
PLLCON.2 3-bit clock divider value, “CD” (default=3)
PLLCON.1 fcore = 16.777216MHz/ 2^{CD}
PLLCON.0