

# MicroConverter® Technical Note – uC017 Additional Features of the ADuC83x Family

#### Introduction

The ADuC83x family are pin compatible upgrades to previous MicroConverter products. They include all the features of their predecessors plus a host of new and improved features.

 Part
 Upgrade

 ADuC812
 ADuC831

 ADuC816
 ADuC836

 ADuC824
 ADuC834

These new features include

- Increased Program Flash (8k to 62k)
- Increased Data Flash (640 bytes to 4kBytes)
- Increased RAM (256 bytes to 2304 Bytes)
- Additional support for High Level Programming
- Pulse Width Modulator Outputs (PWM).
- Dedicated Baud Rate Timer.
- On chip POR
- Time Interval Counter (new to ADuC831)

This technote gives a summary of the new features

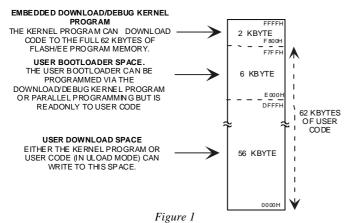
# New Features of the ADuC83x Family

# **Memory Features**

#### **Increased Program Memory**

• 62kB On-Chip Flash/ EE Memory

The increased 62kB of program memory offers users increased integration removing the need for external EEPROM and latch. The program memory is arranged as shown in Figure 1 below.



As with the previous generation parts there is a 2kB Embedded download/debug kernel which downloads code to the part. The kernel can download to the entire memory space and also implements a single pin emulator/debugger. The kernel is primarily designed to interface with ADI tools such as the Windows Serial Downloader and Debugger.

The program memory allows users to implement a bootloader in a protected user bootloader space, details of this and example bootloader code are available in technote uC007. The user bootloader space can only be downloaded to from the kernel or in parallel programming and is seen as ROM to user code, thus protecting the bootloader.

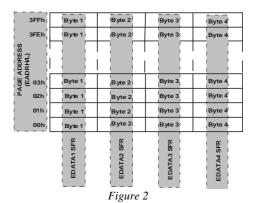
#### **Increased Data Memory**

#### • 4Kb On-Chip Flash/EE Data Memory

This represents an increase of over six times the dataflash/EE. This along with the fact that unused program memory may be used as data memory makes the ADuC83x family ideal for datalogging applications.

On the previous parts the dataflash was accessed via the EADRL register. In order to access the extended flash space an addition register is required. This is EDATAH.

When accessing the dataflash the flash has the following structure. It is arranged in pages of 4 bytes as shown in Figure 2.



#### Increased RAM

#### 2304 Bytes On-Chip Data Ram

This extra RAM is enabled via the CFG83x.0 bit. If enabled this extra RAM is seen by user code as external RAM as shown in Figure 3.

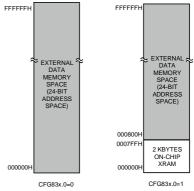


Figure 3

MicroConverter Tech Note – uC017 <a href="http://www.analog.com/microconverter">http://www.analog.com/microconverter</a>



# MicroConverter® Technical Note – uC017 Additional Features of the ADuC83x Family

### **High Level Language Programming Features**

- Dual Data Pointer
- Extended Stack Pointer

The extended stack pointer extends the stack pointer by 3 bits allowing the stack to use additional internal XRAM. This allows the stack to overflow from FFH to 100H.

The Dual Data Pointer allows more efficient code size and execution along with some useful features such as auto increment and auto decrement.

The combination of these features along with the extra RAM and Program memory allows for greater ease of programming in higher level languages such as C.

The C compiler available from Keil Software (<a href="http://www.keil.com">http://www.keil.com</a>) supports the dual data pointer and extended stack pointer. An evaluation copy of this compiler is available as part of the MicroConverter Quickstart development system.

# **Pulse Width Modulator Block (PWM)**

- 2 PWM Outputs
- Flexible Configuration
- · Choice of output pins

The PWM can be configured as a  $\Sigma\Delta$  DAC with up to 16-bits of resolution or as a PWM with variable resolution. The PWM is widely programmable in terms of input clock, clock dividers and PWM mode to give a highly flexible PWM.

On the ADuC831 and ADuC832 additional flexibility is provided by allowing the user to choose the PWM output pins . The output pins that the PWM uses are determined by the CFG83x register, they can be either P2.6 and P2.7 or P3.3 and P3.4. The PWM can be configured to give either a single or dual output.

# Timer 3 - Dedicated Baud Rate Generator

- Generates very accurate baud rates
- Frees up other timers

Timer 3 can be used instead of timer1 or timer2 for generating the baudrate, allowing a much wider range of baud rates to be accurately obtained. For example 230400 and 115200 baud can be obtained with a 0.1% error on all parts. Timer 3 also frees up the other three timers allowing them to be used for different applications.

Timer 3 uses a programmable fractional divider to divide down the core clock into a wide range of clocks. 115200 Baud could not be obtained on the ADuC816 and ADuC824 but now this Baud Rate and higher can be obtained on the ADuC83x family.

### **Internal Power On Reset (POR)**

Removes need for external POR IC

The predecessors of the ADuC83x parts required an external POR circuit to be implemented. The inclusion of a robust internal POR on the ADuC83x family removes the need for this.

#### **Time Interval Counter**

- Wake up from Power Down
- Time Long Intervals (up to 255 hours)

This feature is new on the ADuC831 which is an upgrade to the ADuC812. Previous parts the ADuC816 and ADuC824 have this feature as does their upgrades the ADuC834 and ADuC836.

A time interval counter is provided on-chip for counting longer intervals than the standard 8051-compatible timers are capable of. The TIC is capable of timeout intervals ranging from 1/128th second to 255 hours.

Furthermore, this counter is clocked by an internal R/C oscillator rather than the external crystal and has the ability to remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required.

If the ADuC831 is in power-down with the Time Interval Counter interrupt enabled, the Time Interval Counter is capable of 'waking up' the ADuC831 and executing code in the TIC interrupt routine.

A simplified block diagram of the TIC is shown in Figure 4.

