

İHSAN DOĞRAMACI BILKENT UNIVERSITY DEPARTMENT OF COMPUTER SCIENCE CS223

DIGITAL DESIGN

FPGA Guitar Hero

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March 5, 2016

1 Description of the Project

This is an FPGA implementation of the famous Play Station game Guitar Hero. This project will be implemented with System Verilog using a Basys3 board.

The main principle of the game is to match the patterns that appears on the screen with the inputs that will be given by the user via buttons. There are 5 lines of patterns and each should be pressed when the symbol of that line (colors blue red green yellow and orange) is synchronized with the line below, the corresponding button for the symbol will be pressed to match the color. An example UI is shown in Figure 1.

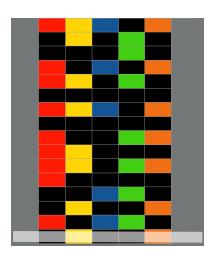


Figure 1: Example UI, as it can be seen, the buttons corresponding to yellow and orange should be pressed since it's corresponding colors are intersecting with the white line

When the pattern is mismatched some points will be reduced from the player's score. If player loses some certain amount of points, the game will end. Else it will continue until the pattern is finished. If the user does a certain amount of the pattern right he will receive stars which will be implemented as leds.

2 Equipment to be used

- Basys 3 Board.
- Seven Segment Display on the Basys3 Board

- Breadboard on the Beti Board (for the display of the leds.
- Modular Breadboard (for the buttons to be modular) -Will buy it from Konya Sokak-
- VGA Monitor -The one in the lab will be used-
- 5 Leds -Will buy it from Konya Sokak-
- 5 Buttons -Will buy it from Konya Sokak-
- Resistors for the buttons and the leds -Will buy it from Konya Sokak-
- Some Jumpers -Will buy it from Konya Sokak-

3 Deliverables of The Project

3.1 Progress report

Deliverables	Due date
Block diagram and description of the blocks of the project	April 11, 2016
Some of the System Verilog Code (and other codes if used)	April 11, 2016
Block table describing what they do for all of the blocks.	April 11, 2016
List of differences in the project proposal (if any)	April 11, 2016

3.2 Final Report and Demo

Deliverables	Due date
Block diagram and description of the blocks of the project	May 5, 2016
Top level block diagram description, timing of the inputs and outputs.	May 5, 2016
System Verilog Code (and other codes if used)	May 5, 2016
Data sheets for the hardware	May 5, 2016
Circuit diagrams	May 5, 2016
Other used codes and references	May 5, 2016
Oral presentation about the project and the demonstration of the project	May 5, 2016
Pear grading forms	May 5, 2016
System Verilog code will be uploaded to Unilica	May 5, 2016