# CS415 Homework Assignment 4: Virtual Memory and Scheduling

#### 1 Problems

#### 1.1 Problem 1

(20 pts) A process references five pages A, B, C, and D in the following order: A;B;D;A;B:C;D;E.

The Virtual Memory Manager (VMM) is using the first-in, first out replacement strategy. How many frames will be swapped to/from memory is the process is allocated three physical memory frames? Repeat for four frames.

#### 1.2 Problem 2

(20 pts) A process contains eight virtual pages on disk and is assigned a fixed allocation of four physical frames in main memory.

The program accesses memory pages in the following order:

1,0,2,2,1,7,0,1,2,0,3,0,4,5,1,5,2,4,5,6,7,6,2,4,2,7,3,3,2,3

- 1. Show what virtual frames are stored in the physical frames as the process accesses memory if the VMM uses a FIFO replacement strategy. Assume the physical frames are empty when the process starts. Compute the hit ratio in main memory.
- 2. Now do the same thing for when the VMM uses LRU replacement. Compute the hit ratio.
- 3. Given the respective hit ratios, would FIFO replacement approximate LRU replacement for this memory trace? Why or why not?

#### 1.3 Problem 3

(20 pts) Suppose a page replacement string for a process has a working set of M frames, initially all empty. The page reference string is of length P with N distinct page numbers in it.

- 1. What is a lower bound on the number of page faults (justify your answer)?
- 2. What is an upper bound on the number of page faults (again, justify your answer)?

#### 1.4 Problem 4

(20 pts, 5 pt. per algorithm) Consider the following workload:

Thread	Burst	Priority	Arrival
	Time		Time
T1	$50 \mathrm{ms}$	2	$0 \mathrm{ms}$
T2	$20 \mathrm{ms}$	1	20ms
Т3	100ms	4	$40 \mathrm{ms}$
T4	$40 \mathrm{ms}$	2	$60 \mathrm{ms}$

Show how the threads would be scheduled using FCFS, SRT, non-preemptive priority and round robin with a 30ms quantum.

### 1.5 Problem 5

(20 pts) The Rather Annoying Intern comes to you with a suggestion for a new scheduling policy for scheduling processes that is a RR scheme where the contents of the ready queue are pointers to PCB of a process.

- 1. What would be the effect of pointing two pointers to the same process in the ready queue?
- 2. Does the Rather Annoying Intern have a good idea or a bad idea (in other words, what are the advantages or disadvantages of this scheme)?
- 3. Explain to the Really Annoying Intern how you can change the standard RR algorithm to achieve the same effect.

## 2 Submission instructions

You will need to document your submission in a short report that includes responses to questions and any supporting source code. Please attach this report, in PDF format, to your submission in Blackboard.