

Peripherals for an FPGA development environment

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The project consists of preparing a setup that supports the joint operation of some DE10-Lite peripherals within the logisim-evolution framework. Eventually, new users should be able to use some of the peripherals from within logisim-evolution in download mode; simulation models or techniques would be considered if time allows.

Some peripherals that connect through the GPIO are already functional and will be used as starting point. Specifically, the method allowing integrating a 16x2 LCD driver modelled in VHDL into logisim-evolution has been prepared.

Two additional peripherals are of interest, namely a) the UART interface to a PC, and b) the on-board VGA interface. Which of the two cases should be started first is part of the study.

Development method

1. study of the basic tutorial from Terasic. Implementation of given examples and understanding of the components of an application. Installation of a working software environment.
2. study of existing projects using the UART and the VGA interface. Projects should preferably be developed in VHDL and must target the DE10-Lite platform.

One (or more) existing projects should be selected from the web (e.g., Github) for example, <https://github.com/hildebrandmw/de10lite-hdl/tree/master> or from Terasic projects database. Special care must be taken regarding the reliability and licensing.

A new project must be developed that can be inspired from these existing works and that fits the requirements of an application that must be defined. For example, display some of the parameters that are recorded by the acceleration sensor, at choice.

In the case of the UART interface to the PC, first a VHDL UART must be implemented in logisim-evolution and internally interfaced. Then, a protocol analyzer is used to guarantee that the data is correctly processed through the TX. Furthermore, a UART to USB cable will be used to connect to the PC; a USB sniffer will be used to monitor the data. Finally, PC software must be developed that displays the data in a graphical user interface, using Qt or a multiplatform environment that supports Qt, Python-Qt in anaconda3.

3. the VHDL blocks must be inserted into logisim-evolution as external modules. An interface must be prepared for them such that they can be connected to any sort of additional digital system on-board the MAX10 FPGA.
4. a full application must be developed in logisim-evolution that makes use of the new peripheral modules as a library.
5. the possibility of simulating the behavior of the accelerometer will be assessed. This can be as a model of as another module that sends identical data as the accelerometer.
6. if time permits, the second module should be developed following the same method.