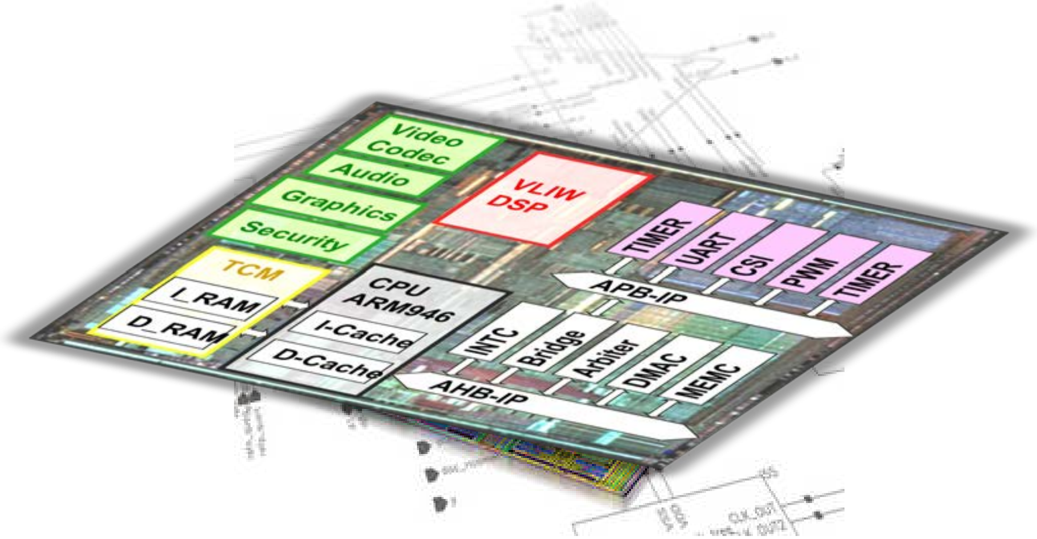
ECE 695R:
SYSTEM-ON-CHIP DESIGN

Module 2: HW/SW Partitioning
Lecture 2.5: Avalon System: Memory-Mapped Interface I



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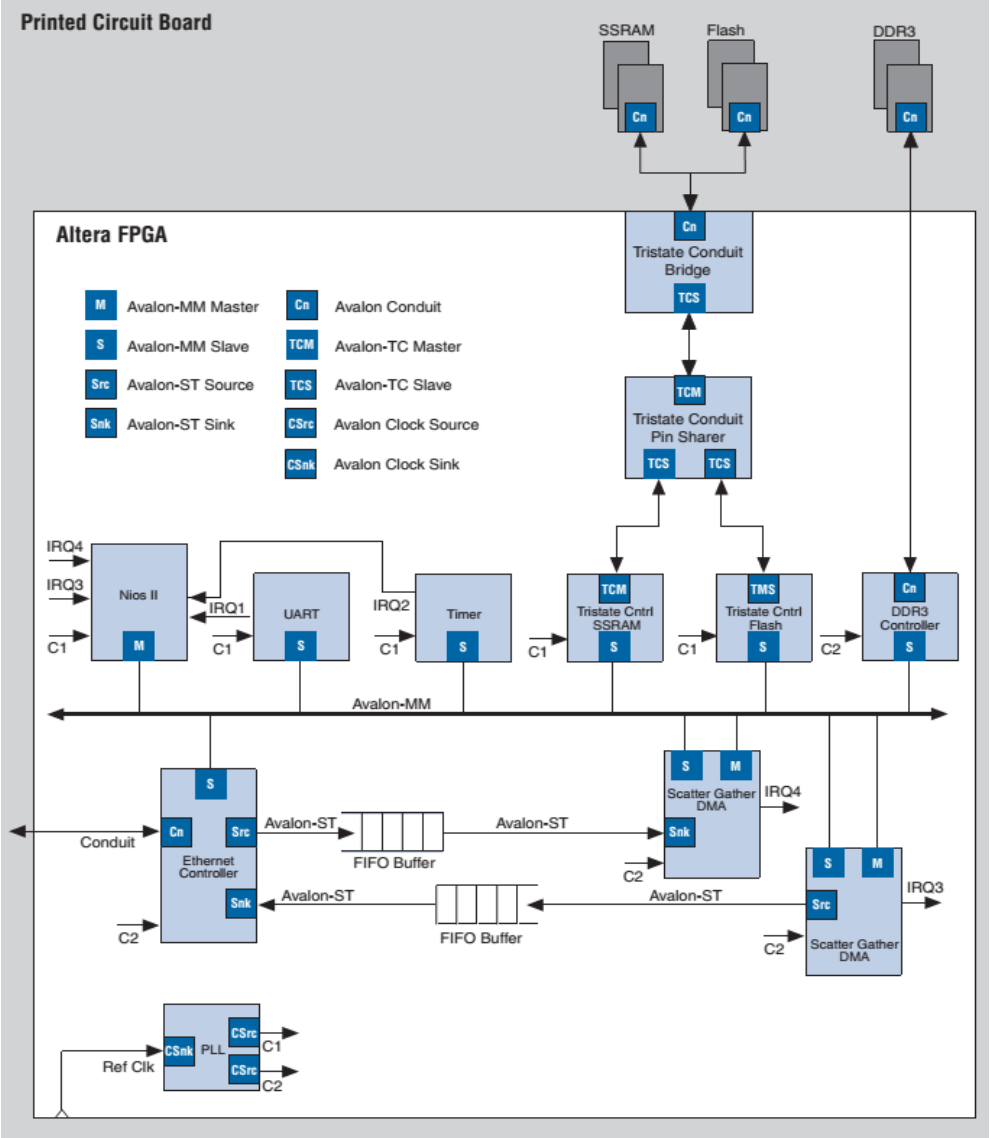
Fall 2014, ME 1052, T Th 12:00PM-1:15PM

Outline

- HW/SW interfacing basics
- Avalon system interconnect fabric
- Avalon-MM memory-mapped interface

Avalon Interfaces and System Interconnect Fabric

- Standard for interconnecting Nios-based systems
- Consists of different interface types



Avalon Interfaces

- **Avalon Memory Mapped Interface** (Avalon-MM)—an address-based read/write interface for master–slave connections.
- **Avalon Streaming Interface** (Avalon-ST)—an interface that supports the unidirectional flow of data, including multiplexed streams, packets, and DSP data.
- **Avalon Memory Mapped Tristate Interface**—an address-based read/write interface to support off-chip peripherals. Multiple peripherals can share data and address buses to reduce the pin count of an FPGA and the number of traces on the PCB.
- **Avalon Clock/Reset**—an interface that drives or receives clock and reset signals to synchronize interfaces and provide reset connectivity.
- **Avalon Interrupt**—an interface that allows components to signal events to other components.
- **Avalon Conduit**—an interface that allows signals to be exported out at the top level of an SOPC Builder system where they can be connected to other modules of the design or FPGA pins.

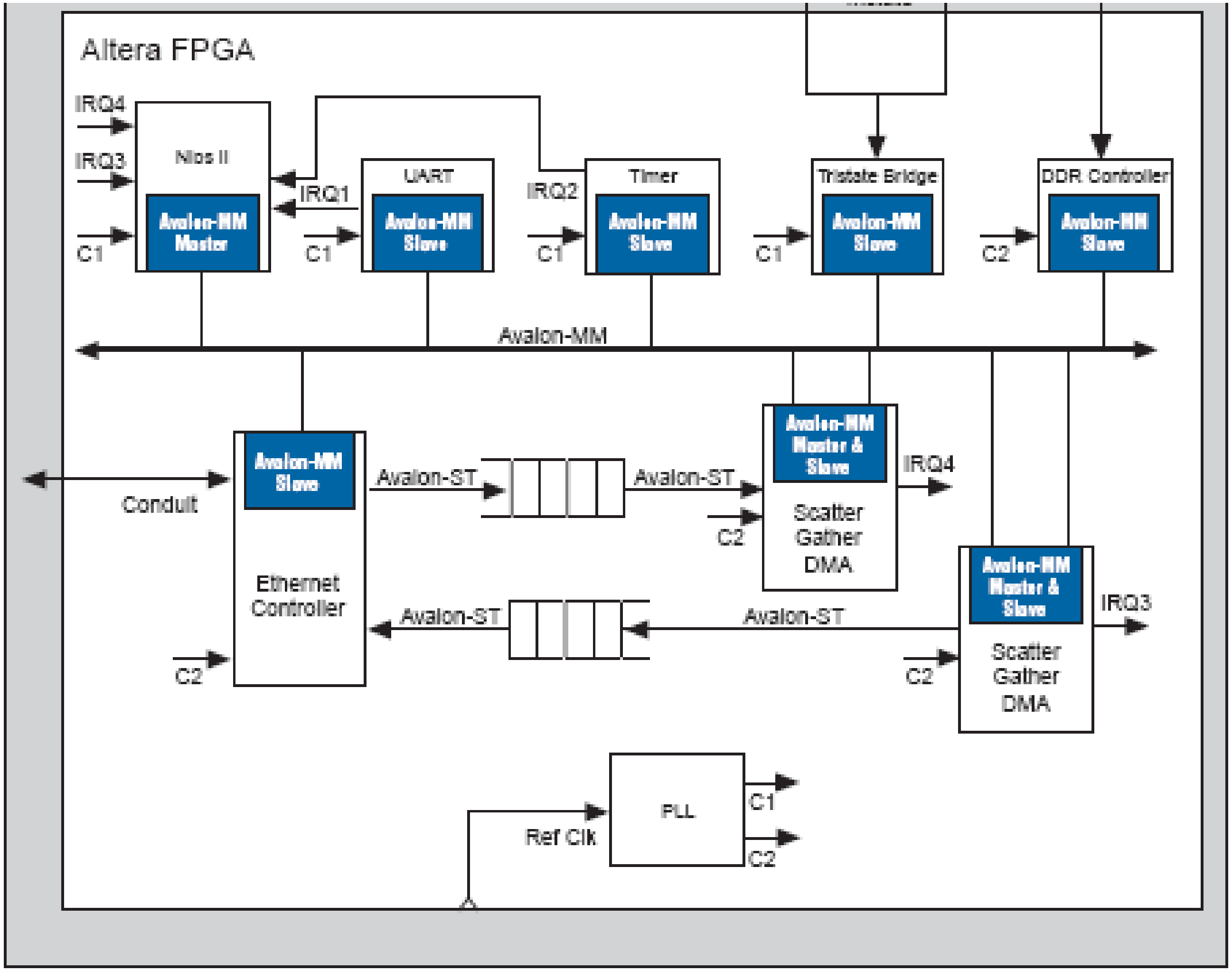
Describing components in terms of standard interfaces facilitates automated integration / interconnection (as in QSys)

Further Reading

- Avalon Interface Specification
- Hardware Acceleration and Co-processing, Altera Embedded Design Handbook, Chapter 8
- Creating Qsys components, Chapter 8 of the Quartus Manual.

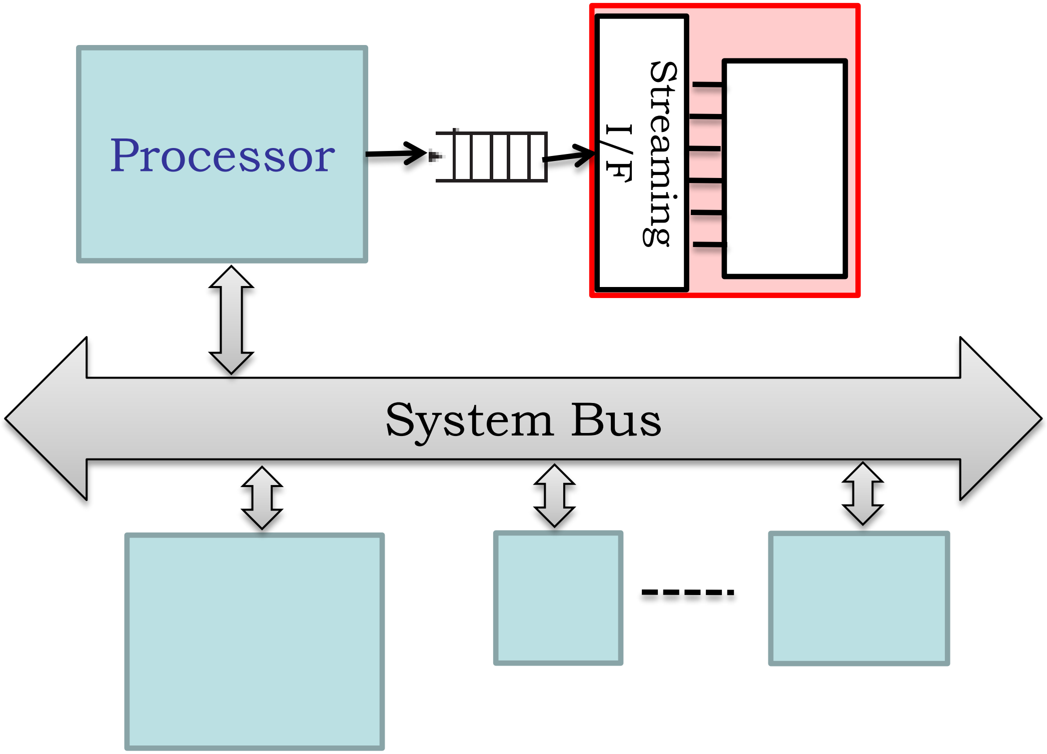
Avalon-MM and Avalon-ST

- Standard for interconnecting Nios-based systems
- Memory-mapped interface: Avalon-MM
- Streaming interface: Avalon-ST



HW/SW Interfacing: Streaming Interfaces

- Unidirectional interfaces that can support high-bandwidth, low-latency transfers

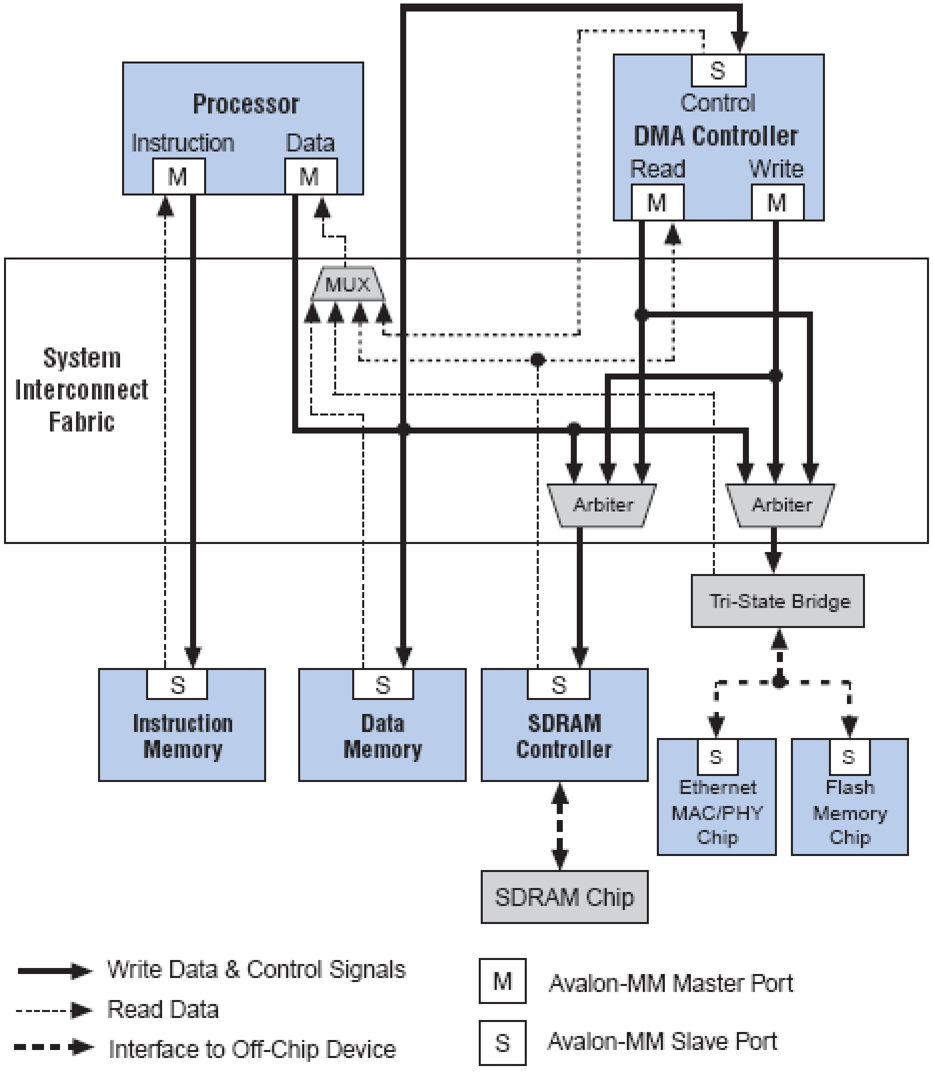


Outline

- HW/SW interfacing basics
- Avalon system interconnect fabric
- Avalon-MM memory-mapped interface

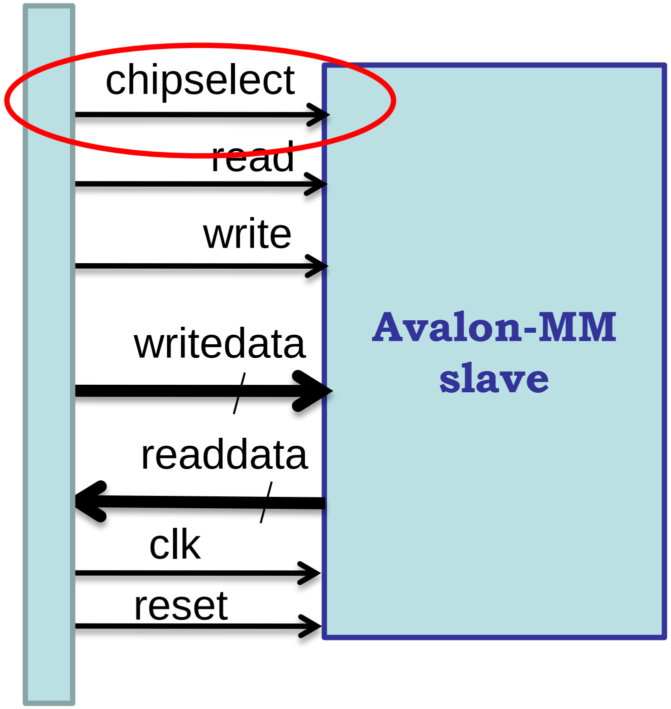
Avalon-MM Memory mapped interface

- Transactions between components look like memory transactions
- Components mapped to a "memory" space
- Each component can have Master or Slave ports
  - **Masters** can initiate transactions
  - **Slaves** can only respond to transactions



Slave Interfaces

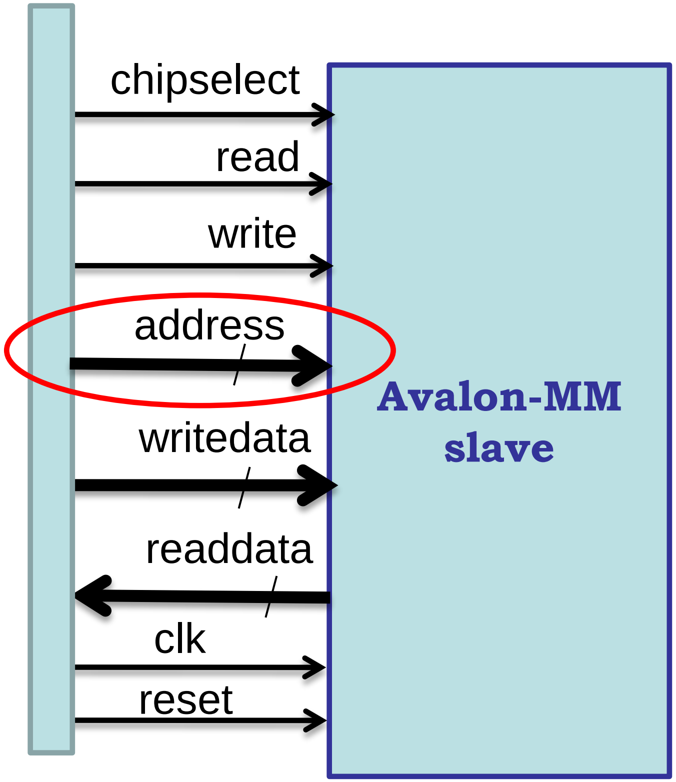
- Simplest case: Slave does not need internal addressing
- “chipselect” or “begintransfer” signal is used to notify slave when it is being accessed
- Read, Write signals indicate type of transaction
- readdata / writedata are the data lines



Question: How is the chipselect generated?

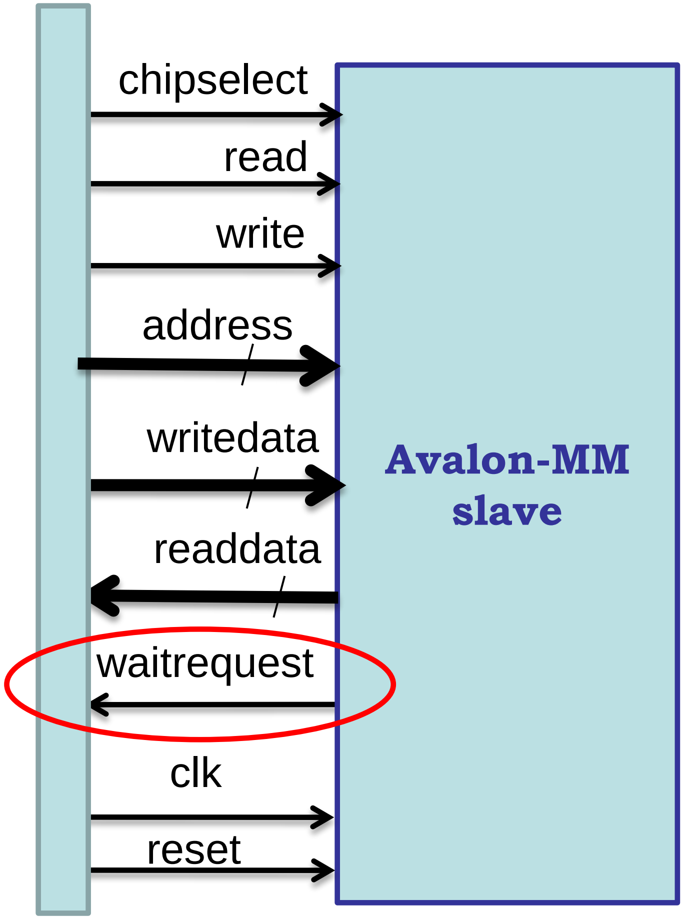
Slave Interfaces

- In general, slaves may use all or a range of the bus address bits for internal addressing
- Examples:
  - – bus_address[31:0]
  - – slave_address[5:0]



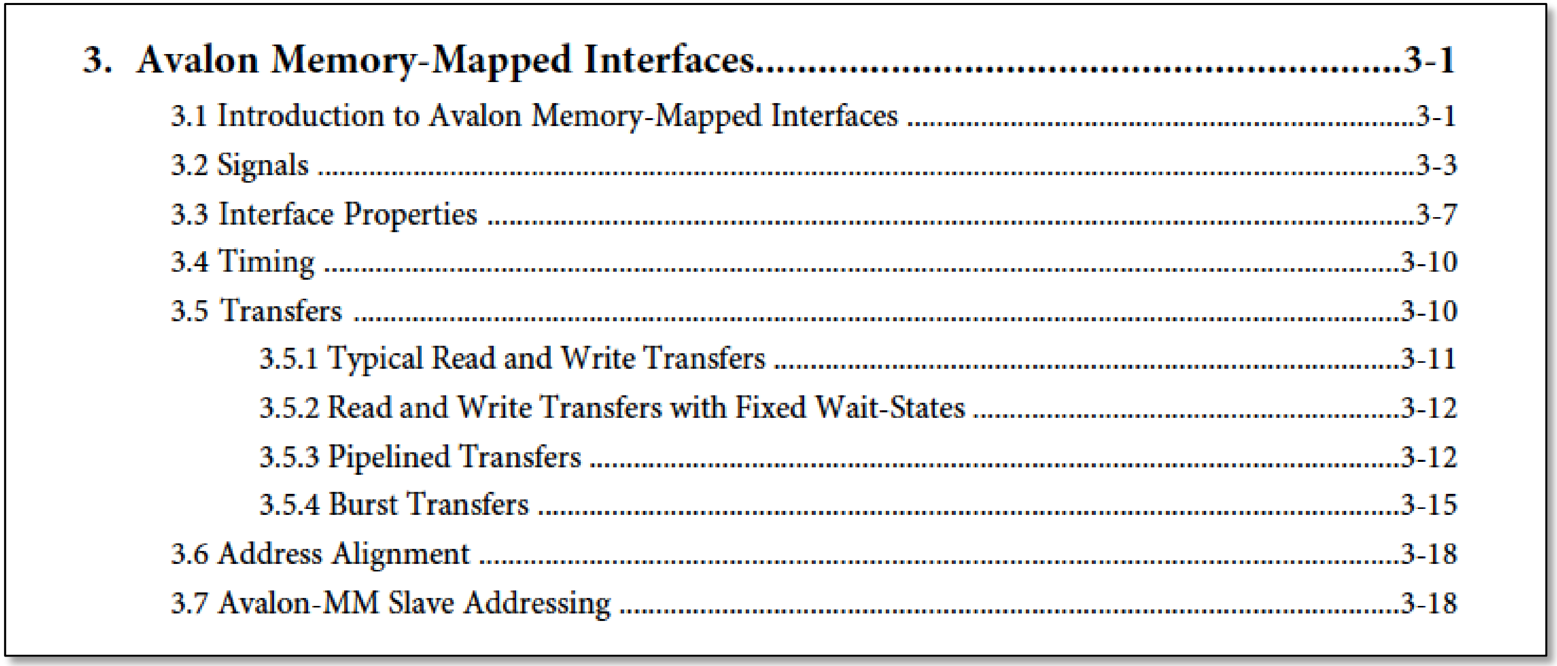
Slave Interfaces – Wait Request

- Normally, a slave MUST respond to a transaction at the next clock cycle.
- How can a slave respond if it is unable to complete the request?
  - Assert a “wait” signal that tells the bus and the master that the slave is not ready



Complete Slave Interface

- See Avalon Interface Specification document



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http://www.altera.com/literature/manual/mnl_avalon_spec.pdf