Develop Your Projects

During development, you can use the Vivado Design Suite. You can implement project files in your project. Run.bat file will be used only evaluation phase by us.

Arrange Environment Files

- Open Run.bat file using the text editor.
- You must arrange the first line according to the installation directory. Under the installation directory, there must be a "settings64.bat" file. You should give this file path in the first line.

```
Run.bat
1    call C:\Xilinx\Vivado\2017.4\settings64.bat
2
3    set folder=Simulation_Files
4    mkdir %folder%
5    copy "RAM.mem" "%folder%/RAM.mem"
6    cd "%folder%"
7
8    ::Register 16 Simulation
9    call xvlog ../Register16bit.v
10   call xvlog ../Register16bitSimulation.v
11   call xvlog ../Helper.v
12   call xelab -top Register16bitSimulation -snapshot reg16sim -debug typical
13   call xsim reg16sim -R
```

Example Submission Files

The required project files are given under "ExampleSubmission.zip" files. You must use these modules **without** changing names. The explanation for each file is given below. **The files must be the same as given.** Please do not put files in a folder. **If you do not submit it as ExampleSubmission.zip, the evaluation may not execute. You may get ZERO points.**

Name	Explanation	Require Edit
Register16bit.v	16-bit Register Module	YES
Register16bitSimulation.v	Simulation Test Bench of 16-bit Register Module.	You can add new tests to the given test scenario.
Register32bit.v	32-bit Register Module	YES
Register32bitSimulation.v	Simulation Test Bench of 32-bit Register Module.	You can add new tests to the given test scenario.
RegisterFile.v	Register File Module	YES
RegisterFileSimulation.v	Simulation Test Bench of Register Module	You can add new tests to the given test scenario.
AddressRegisterFile.v	Address Register File Module	YES
AddressRegisterFileSimulation.v	Simulation Test Bench of Address Register Module	You can add new tests to the given test scenario.

InstructionRegister.v	Instruction Register Module	YES
InstructionRegisterSimulation.v	Simulation Test Bench of Instruction Register Module	You can add new tests to the given test scenario.
DataRegister.v	Data Register File Module	YES
DataRegisterFileSimulation.v	Simulation Test Bench of Data Register Module	You can add new tests to the given test scenario.
ArithmeticLogicUnit	Arithmetic Logic Unit Module	YES
ArithmeticLogicUnitSimulation.v	Simulation Test Bench of Arithmetic Logic Unit Module	You can add new tests to the given test scenario.
Memory.v	Memory Module	NO
RAM.mem	The data file of memory module	Add the simple program to the RAM. You can add new tests to the given test scenario.
ArithmeticLogicUnitSystem.v	Arithmetic Logic Unit System Module	YES
ArithmeticLogicUnitSystemSimulation.v	Simulation Test Bench of Arithmetic Logic Unit System Module	You can add new tests to the given test scenario.
CPUSystem.v	CPU System Module	YES
CPUSystemSimulation.v	Simulation Test Bench of CPU System Module	You can add new tests to the given test scenario.
Helper.v	Helper module for the simulation modules.	NO
Run.bat	Execution Script of Testbench Files	Only first line
Report.pdf	Report file of the Project 1	You must replace it with your report.
GroupMembers.xlsx	Student Numbers and Names of the group members. (If your teammate does not make any contribution, please **DO NOT WRITE** his/her name.)	YES. Don't change file type.

Run TestBench

- Open Command Prompt.
- Go to the project directory to arrange for submission.
- Write "Run.bat" command. Click Enter.

```
PS C:\Users\OMURFE\Vivado\ExampleSubmissionTest> .\Run.bat

C:\Users\OMURFE\Vivado\ExampleSubmissionTest>call C:\Xilinx\Vivado\2017.4\settings64.bat
The system cannot find the path specified.
        1 file(s) copied.
INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/OMURFE/Vivado/ExampleSubmissionTest/Register16bit.v" into library work
INFO: [VRFC 10-311] analyzing module Register16bit
INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/OMURFE/Vivado/ExampleSubmissionTest/Register16bitSimulation.v" into library work
INFO: [VRFC 10-311] analyzing module Register16bitSimulation
INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/OMURFE/Vivado/ExampleSubmissionTest/Helper.v" into library work
INFO: [VRFC 10-311] analyzing module FileOperation
INFO: [VRFC 10-311] analyzing module CrystalOscillator
Vivado Simulator 2017.4
Copyright 1986-1999, 2001-2016 Xilinx, Inc. All Rights Reserved.
Running: C:/Xilinx/Vivado/2017.4/bin/unwrapped/win64.o/xelab.exe -top Register16bitSimulation -snapshot reg16sim -debug typical
Multi-threading is on. Using 14 slave threads.
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module work.CrystalOscillator
Compiling module work.Register16bit
Compiling module work.FileOperation
Compiling module work.Register16bitSimulation
Built simulation snapshot reg16sim

****** Webtalk v2017.4 (64-bit)
  **** SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017
  **** IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017
    ** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

source C:/Users/OMURFE/Vivado/ExampleSubmissionTest/Simulation_Files/xsim.dir/reg16sim/webtalk/xsim_webtalk.tcl -notrace
INFO: [Common 17-206] Exiting Webtalk at Mon Mar 17 04:00:37 2025...

****** xsim v2017.4 (64-bit)
  **** SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017
  **** IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017
    ** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

source xsim.dir/reg16sim/xsim_script.tcl
# xsim {reg16sim} -autoloadwcfg -runall
Vivado Simulator 2017.4
Time resolution is 1 ps
run -all
--------------------------------------
Register16bit Simulation Started
[PASS] Test No: 1, Component: Q, Actual Value: 0x00000025, Expected Value: 0x00000025
[PASS] Test No: 2, Component: Q, Actual Value: 0x00000024, Expected Value: 0x00000024
[PASS] Test No: 3, Component: Q, Actual Value: 0x00000025, Expected Value: 0x00000025
[PASS] Test No: 4, Component: Q, Actual Value: 0x00000026, Expected Value: 0x00000026
Register16bit Simulation Finished
```

- Under the "Simulation_Files" folder created by "Run.bat", there are "debug.txt" and "evaluation.csv" files. The "debug.txt file consists of testbench results for you. You should fix your design in case there are failed cases. The "evaluation.csv" file consists of the same results for the automatic evaluation system.