GEBZE TECHNICAL UNIVERSITY

ELECTRONIC ENGINEERING

ELEC-237 ELECTRONICS

LABORATORY-I

EXPERIMENT 2
OPERATIONAL AMPLIFIER IMPERFECTIONS AND APPLICATIONS

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1.Voltage and Current Offsets

1.1 Offset Measurement:

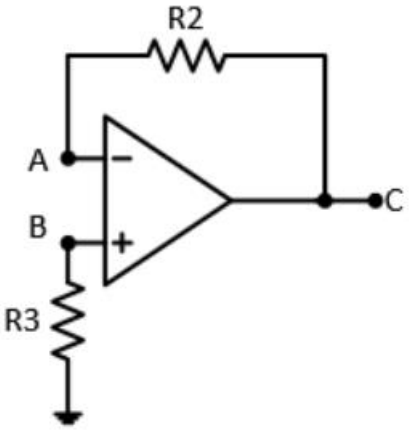


Figure 1:A circuit for the measurement of offsets:

Assemble the circuit as shown in Figure 2. Adjust the power supplies to ±10V. Measure VC for R2=R3=1MΩ (Resistors should be matched within 2% tolerance). Then, short circuit R3 and measure VC and as R3 is shorted, add R1=1kΩ to ground from the negative input and measure VC. Put your measurement results to Table 1.

Theorical Informations:

Offset voltage is the differential input voltage that would have to be applied to force the op amp's output to zero volts. Typical offset voltages range from mV down to μV, depending on the op amp model. Offset can be modeled as an internal dc source connected to the input of the op amp. Changing power supply voltage and common mode voltage will affect input offset voltage.

Input Bias Current – IB , is the current flowing into the inputs of an op amp. These currents can be modeled as a current source connected to each input, as shown in this figure. Ideally, the two input bias currents would be equal to each other and would cancel. In reality, though, they are not equal, and the difference of these currents is defined as input offset current. If the input offset current is low, it's possible to match the impedances connected to each input and cancel the offset developed from the input bias currents.

Input bias current and input offset current also affect the net offset voltage seen for a given amplifier. The voltage offset due to these currents is separate from the input offset voltage parameter and is related to the impedance of the signal source and of the feedback and input impedance networks, such as the two resistors used in the basic inverting and non-inverting amplifier configurations. FET -input op-amps tend to have lower input bias currents than bipolar -input op-amps, and hence incur less offset of this type.

First Circuit Statement 1:

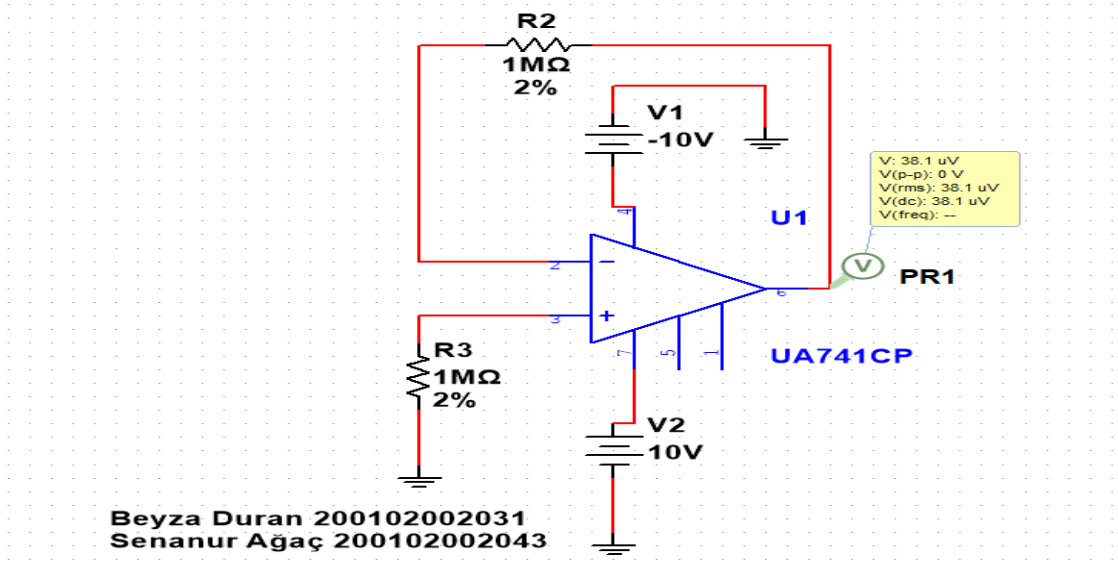


Figure 2:When R1 is open circuit and resistors R2 and R3 are 1MΩ

First Circuit Statement 2:

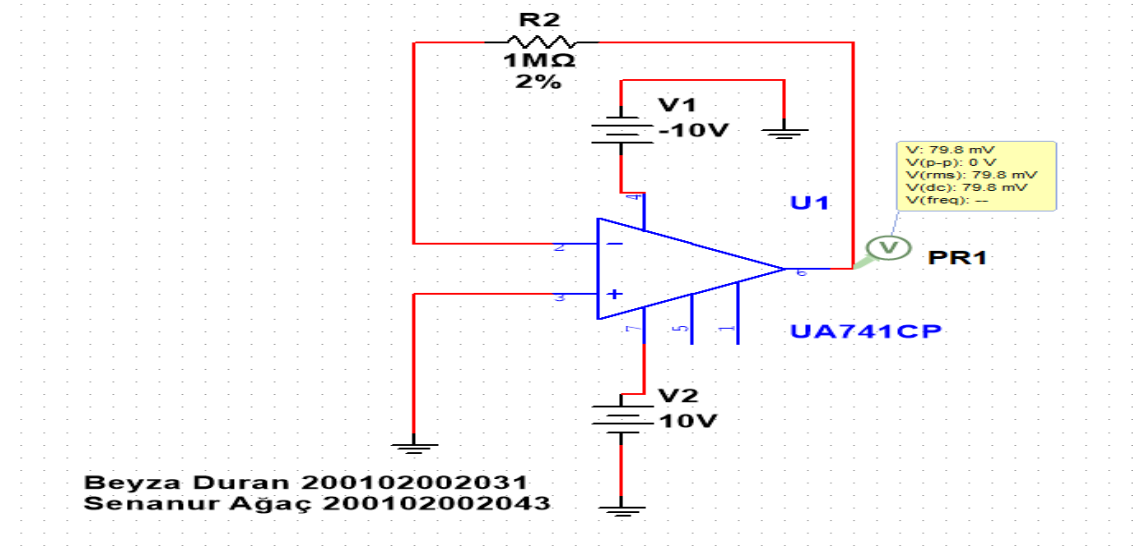


Figure 3:When R1 is open circuit and R2 is 1MΩ and R3 is short circuit

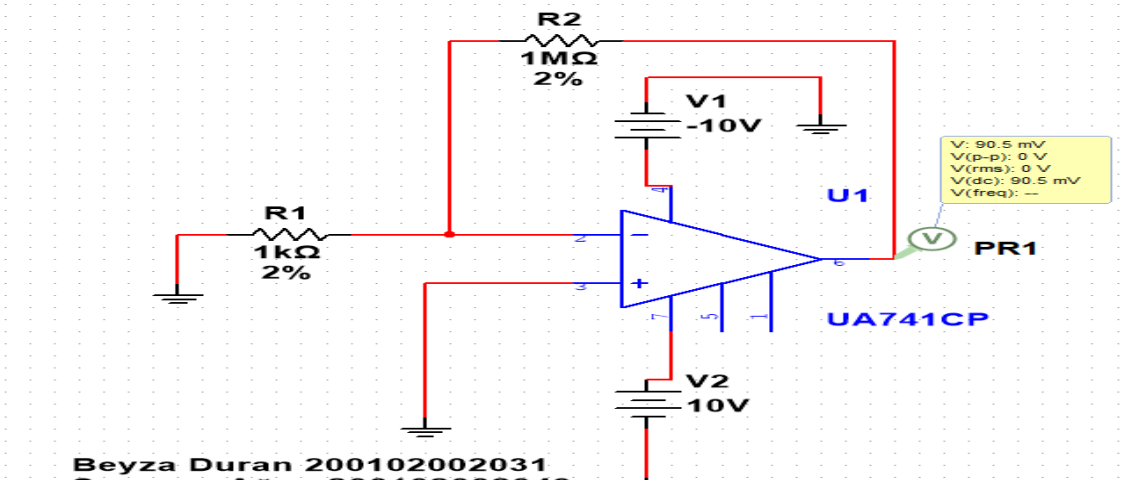


Figure 4:When R1 is 1 kΩand R2 is 1MΩ and R3 is shorted

First Circuit Statement 3:

Table 1: MultiSim measurements

	$R_3 = 1\ M\Omega$ $R_1 = \infty$	$R_3 = 0$ $R_1 = \infty$	$R_3 = 0$ $R_1 = 1\ k\Omega$
V_C	38.1 µV	79.8 mV	90.5 mV

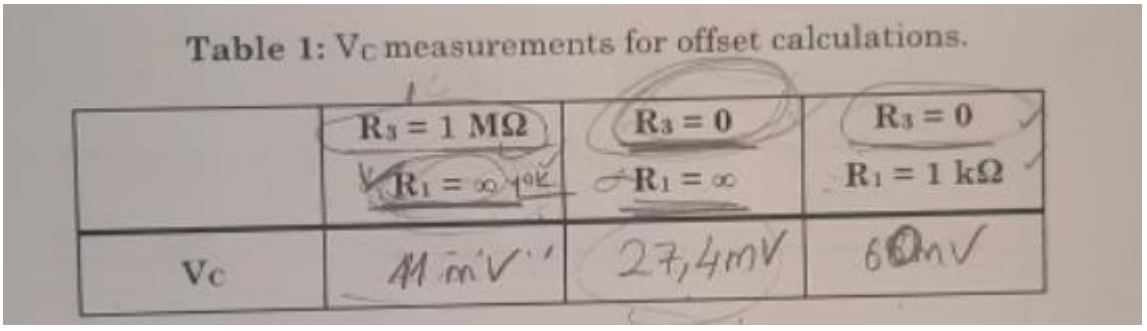


Figure 5: Experiment measurements

CALCULATIONS:

Offset voltage, offset current and bias current are calculated for the first circuit in Table 1.

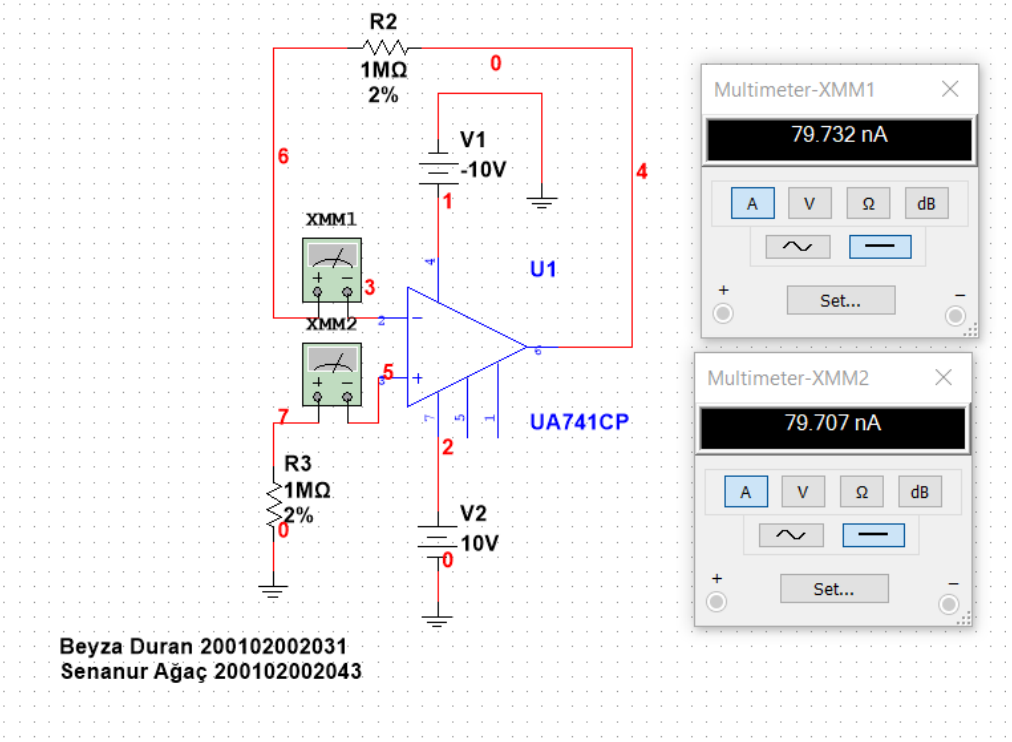


Figure 6: Input currents measured to find the wanted values

$$V_C = A_V . V_{os} + R_2 . (I_{IB} + \frac{I_{OS}}{2})$$

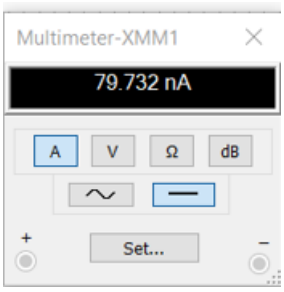
$$V_C = A_V . V_{os} + R_2 . I_{OS}$$

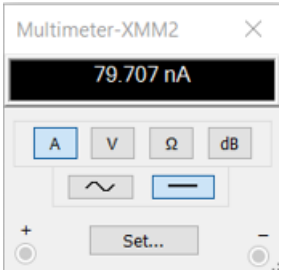
	$R_3 = 1\ M\Omega$ $R_1 = \infty$
V_C	38.1 µV

Considering these conditions, starting from Vc (output voltage) and gain, the input currents of the opamp were found in the simulation program and accordingly offset current and bias current were found.

$$R_2 = 1\,M\Omega\,, R_3 = 1M\Omega\;and\;R_1 = \infty$$

$$I_{OS} = B_1 - B_2 \quad , \quad I_{IB} = \frac{I_{B1} + I_{B2}}{2}$$

I_{B1} => 

I_{B2}=> 

$$I_{OS} = B_1 - B_2 = 79.732\,nA - 79.707\,nA = 0.025nA =$$

$$2.5 \times 10^{-8}\,mA$$

$$I_{IB} = \frac{I_{B1} + I_{B2}}{2} = \frac{79.732 + 79.707}{2} = \frac{0.025}{2}$$

$$= 0.0125\,nA = 1.25 \times 10^{-8}\,mA$$

$$A_V = \frac{R_f}{R_{in}} = \frac{R_2}{R_1} = \frac{1M\Omega}{\infty} = 0$$

$$V_C = A_V\,.V_{os} + R_2.(I_{IB} + \frac{I_{OS}}{2})$$

$$V_C = 0\,.V_{os} + 1000k\Omega.(1.25 \times 10^{-8}\,mA + \frac{2.5 \times 10^{-8}\,mA}{2})$$

$$V_C = 2.5 \times 10^{-5}\,V$$

As we calculated above, the input currents of the opamp were found and the offset current and bias current values were found through the given formulas. In addition, the value of Vc, which is the output voltage, has been confirmed with the values here and is very close.

2.Compensated Miller Integrator

2.1 Integrator Offset Control:

The input current is offset by a negative feedback current flowing in the capacitor, which is generated by an increase in output voltage of the amplifier. The output voltage is therefore dependent on the value of input current it has to offset and the inverse of the value of the feedback capacitor. The greater the capacitor value, the less output voltage has to be generated to produce a particular feedback current flow. The input impedance of the circuit is almost zero because of the Miller effect. Hence all the stray capacitances (the cable capacitance, the amplifier input capacitance, etc.) are virtually grounded and they have no influence on the output signal.

The important information in this part is that in DC steady state, the capacitor behaves like an open circuit. The DC gain of the ideal circuit is therefore infinite. To counter this, a large value resistor must be connected in parallel with the capacitor. A resistor of 100kΩ is installed in the circuit given in Figure 7.

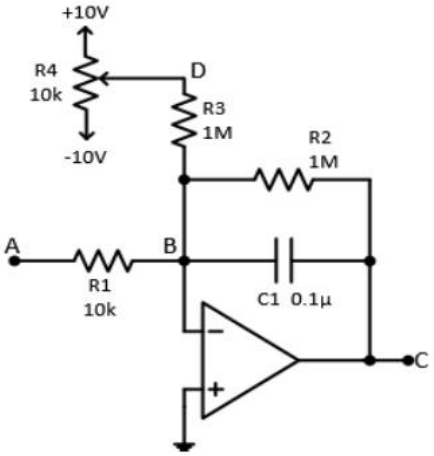


Figure 7 : A compansated integrator.

Assemble the circuit as shown in Figure 3. Adjust the power supplies to ±10V.

a) With node A open, and measuring VC, adjust R4 to make VC =0 V.

→ In this case, the circuit was set up as in figure 8 and the values were measured in line with the requirements.

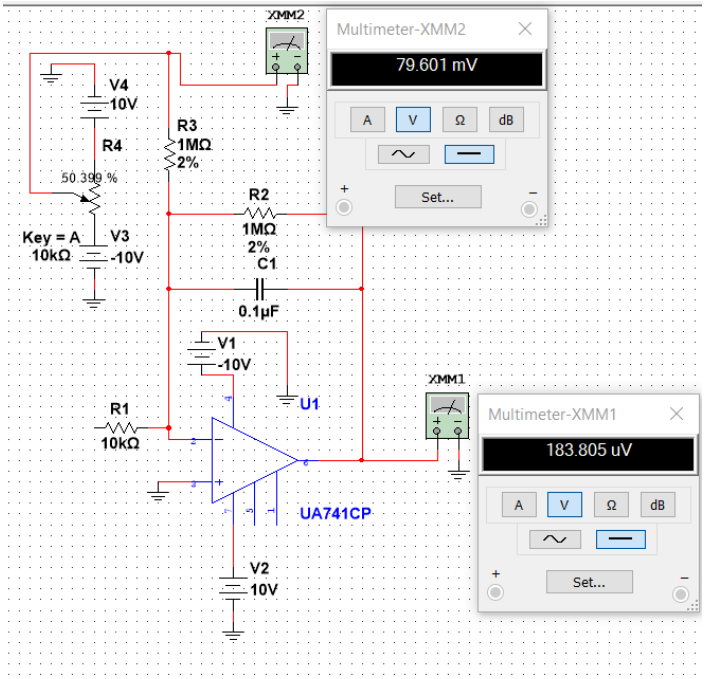


Figure 8: Solution of a) in simulation

R4= 50.399% at the value where Vc value is approximately 0V.

a) Ground node A. Measure node C and node D.

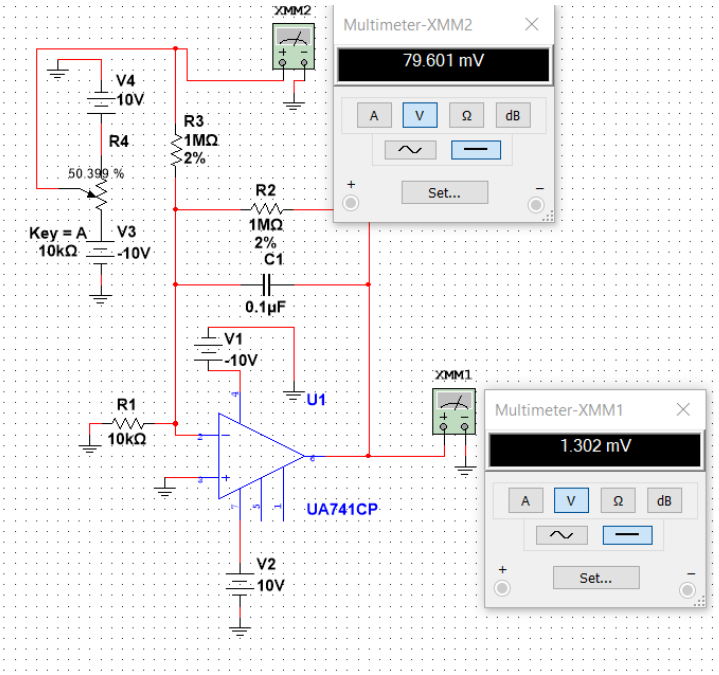


Figure 9: Solution of b) in simulation

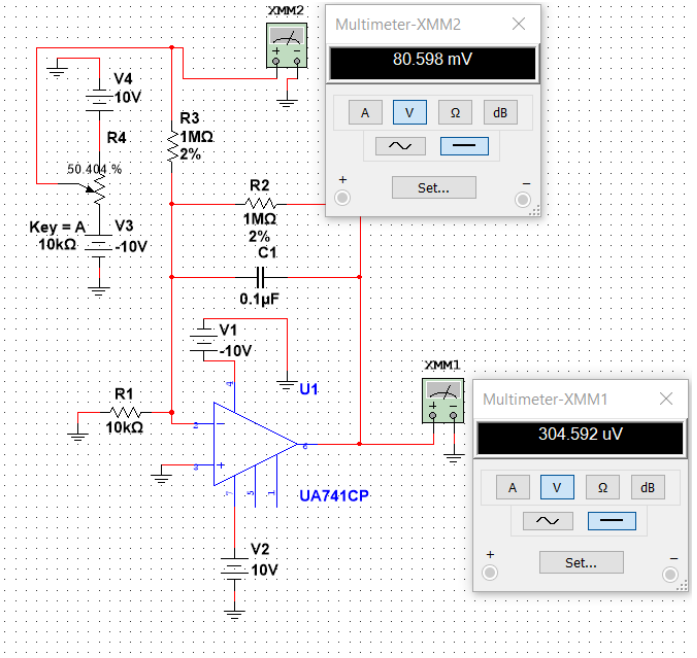


Figure 10 : Solution of c) in simulation

Point A is connected to ground and R4 = 50.404% when Vc = 0V.

Table 3: Compensation measurements.

	a)	b)	c)
Vc	79.601 mV	79.601 mV	80.598 mV
V_D	183.805 uV	1.302 mV	304.592 uV

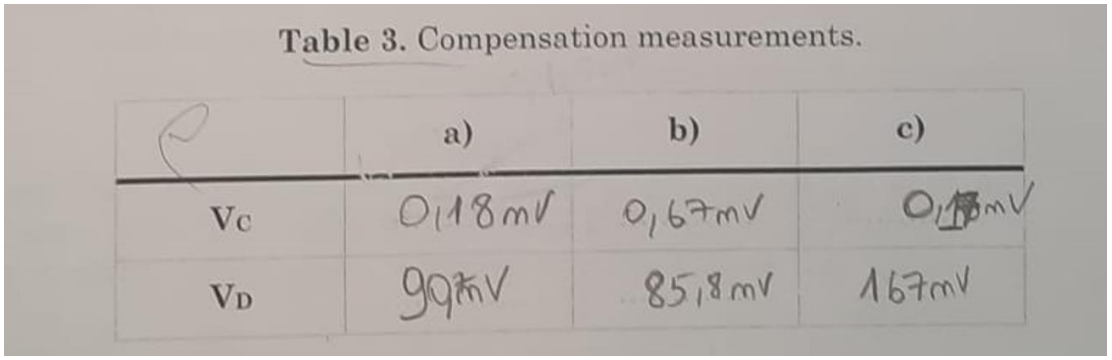


Figure 11: Experiment results

2.2 Integrator Operation:

Use the circuit as shown in Figure 3 with compensation adjusted in 2.1. Connect a function generator to input A.

a) Adjust the generator to provide a 1 kHz symmetric square wave at input A of 1 Vpp amplitude Measure A and C. Sketch the waveforms, noting peak amplitudes and relative timing

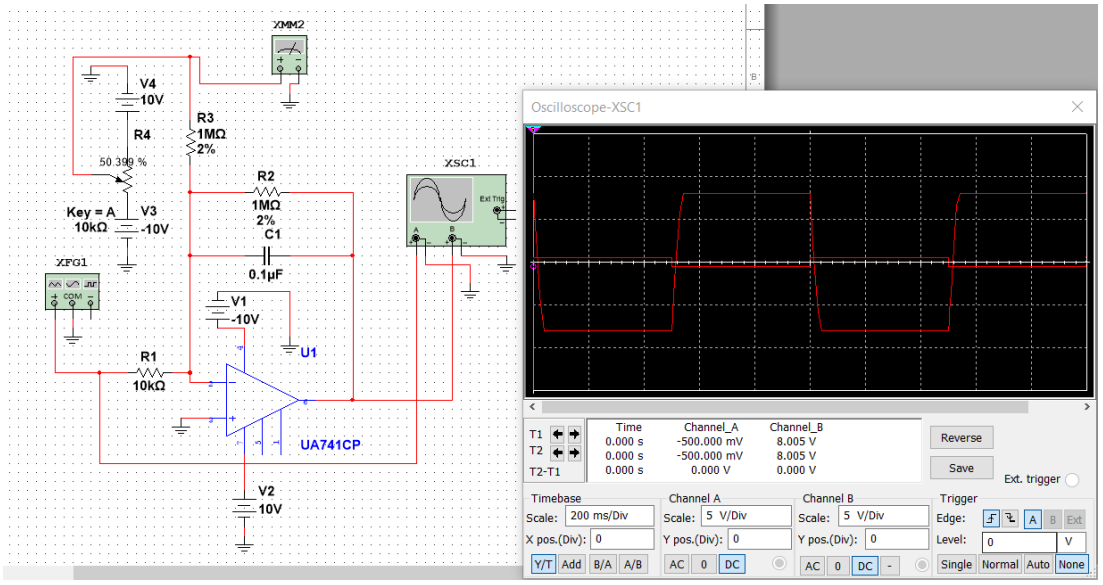


Figure 12 : Solution of a) in simulation

Waveform of 5V /div - 200 ms / div

b) Switch the generator to provide a 1 Vpp sine wave at input A. Sketch the waveforms, noting the peak amplitude and relative timing.

Waveform of 5V /div - 200 ms / div

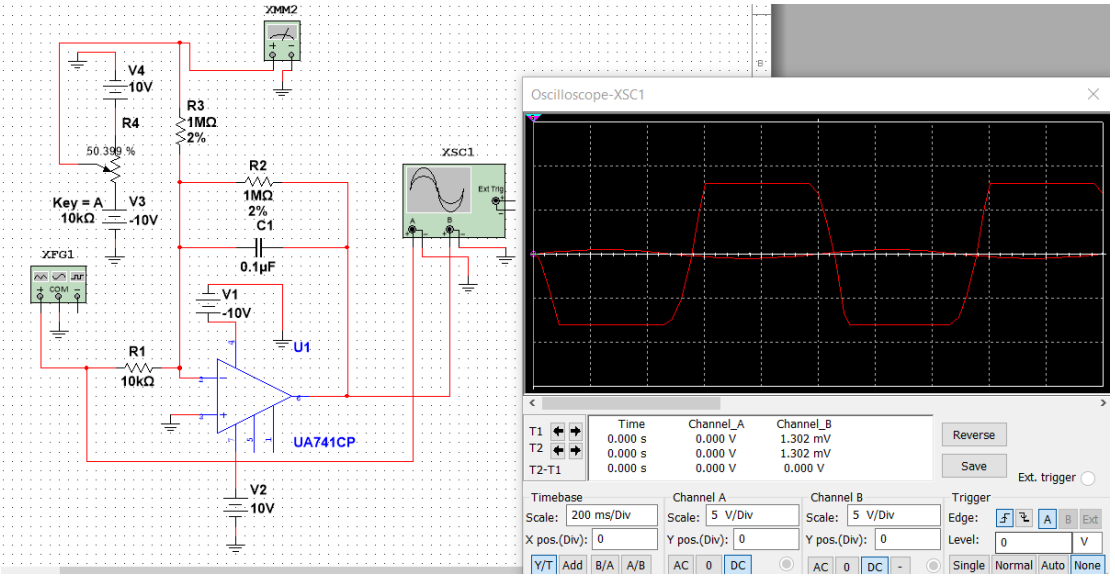


Figure 13 : Solution of b) in simulation

3.1 Small Signal Frequency Response:

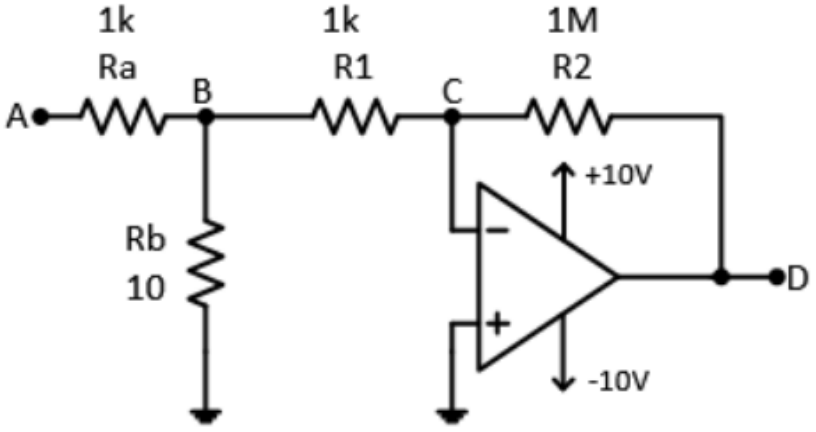


Figure 14: A high-gain inverting amplifier for frequency measurement.

Assemble the circuit as shown in Figure 4. Adjust the power supplies to ±10V. Connect a function generator to input A at 100 Hz.

a) Measure nodes A and D. Adjust the generator amplitude to provide a peak output at node D of 2 Vpp at 100 Hz.

b) Raise the frequency of the generator to the value at which vD is reduced by 3dB (to $1/\sqrt{2} = 0.707$ of its 100 Hz value). Note the frequency as f4. [Make sure that the voltage at node A has remained at its initial value as established in a).]

c) Increase the frequency to 10 f4. Measure the peak-to-peak output value.

d) Change resistor R2 from 1MΩ to 100kΩ and repeat a), b), c).

Put your measurement results to Table 4 & 5.

A small-signal model is an AC equivalent circuit in which the nonlinear circuit elements are replaced by linear elements whose values are given by the linear approximation of their characteristic curve near the bias point

a) R2=1MΩ

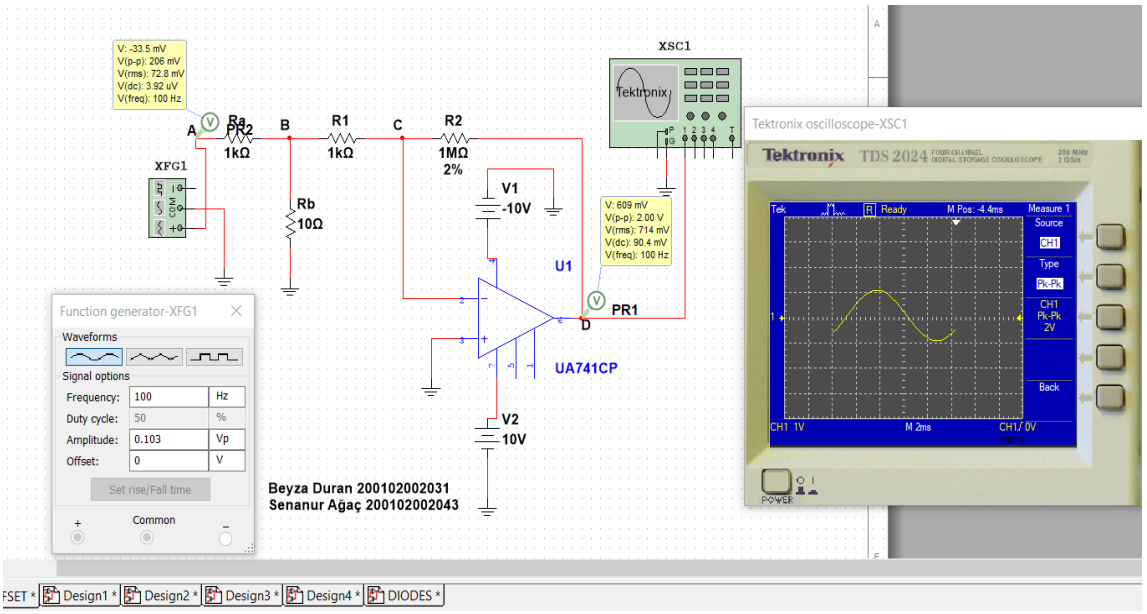


Figure 15: Finding the amplitude value that makes VD 2V at a frequency of 100 hertz

b)

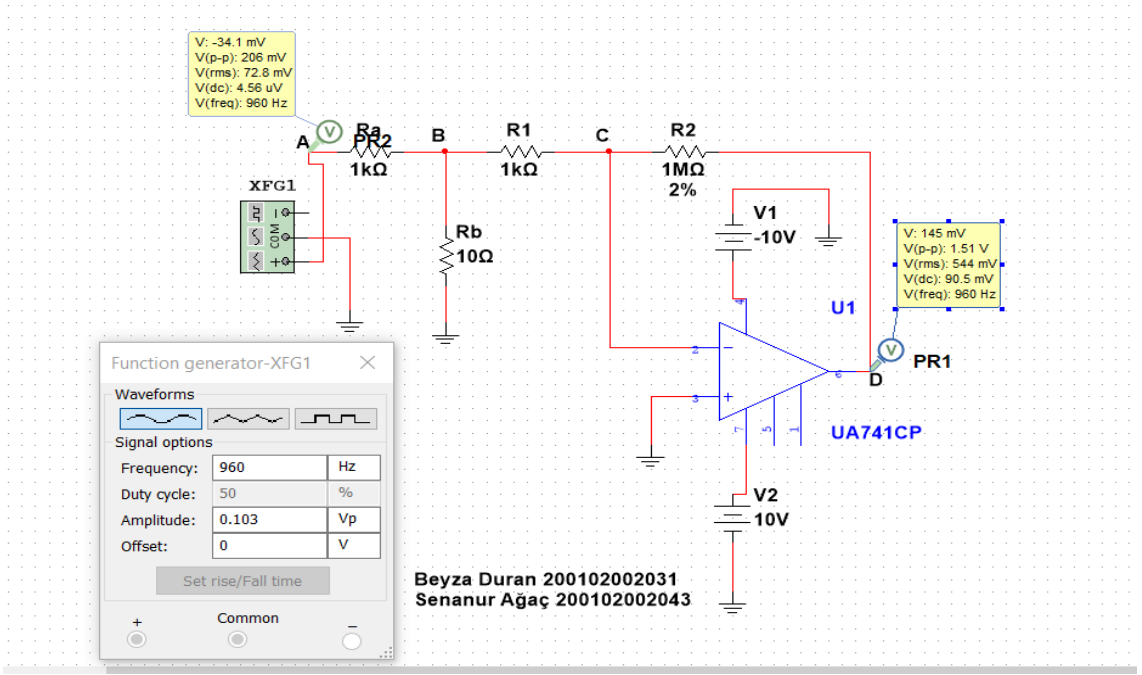


Figure 16: Solution of b) in simulation

c)

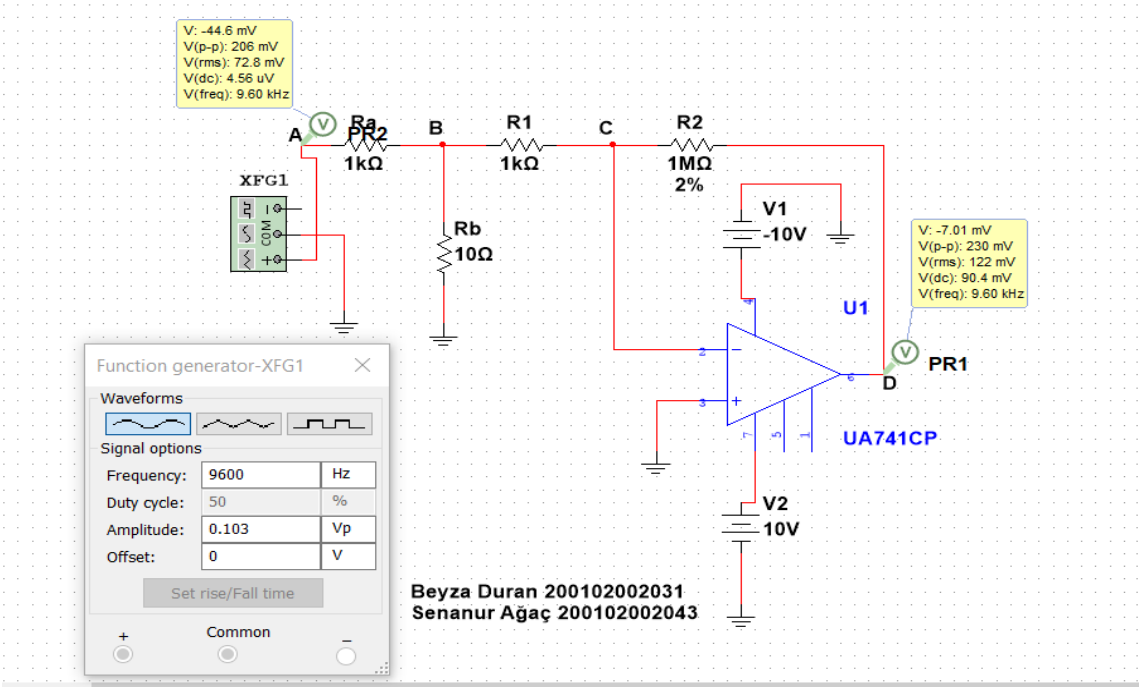


Figure 17 : : Solution of c) in simulation

Table 4: Multisim Measurements

$R_2 = 1M\Omega$	a)	b)	c)
v_A	206 mV	206 mV	206 mV
v_D	2 V_{pp}	1.51 V	230 mV
f_4	100 Hz	960 Hz	9.6kHz

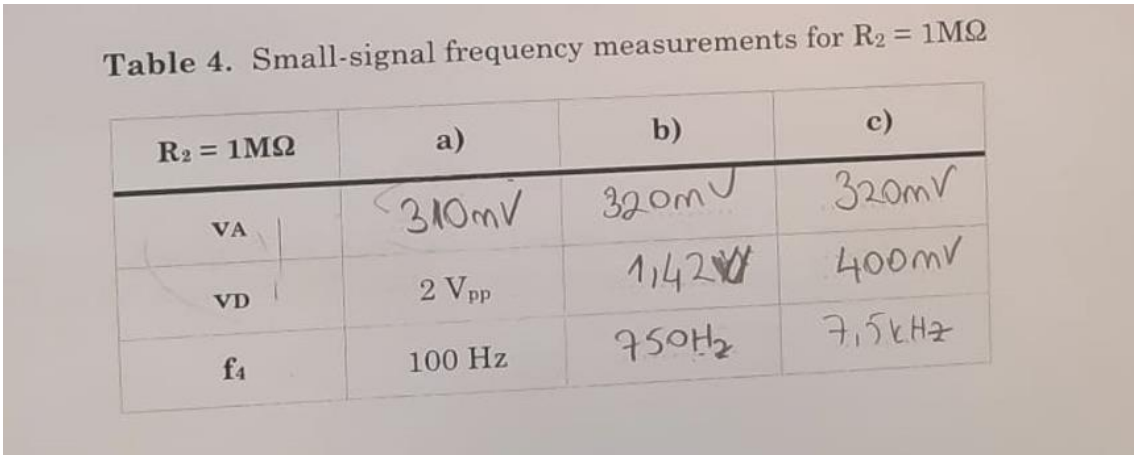


Table 4. Small-signal frequency measurements for $R_2 = 1M\Omega$

$R_2 = 1M\Omega$	a)	b)	c)
v_A	310mV	320mV	320mV
v_D	2 V_{pp}	1,42V	400mV
f_4	100 Hz	750Hz	7,5kHz

Figure 18: Experiment results

Implementation of the circuit for 100 kΩ :

a)

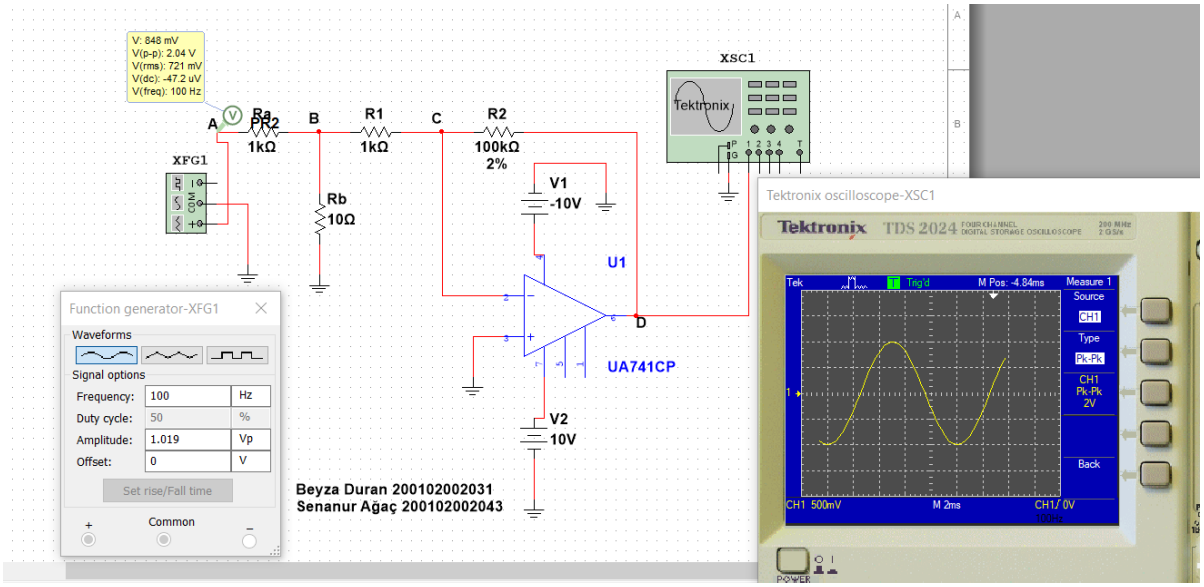


Figure 19: Solution of a) in simulation

b)

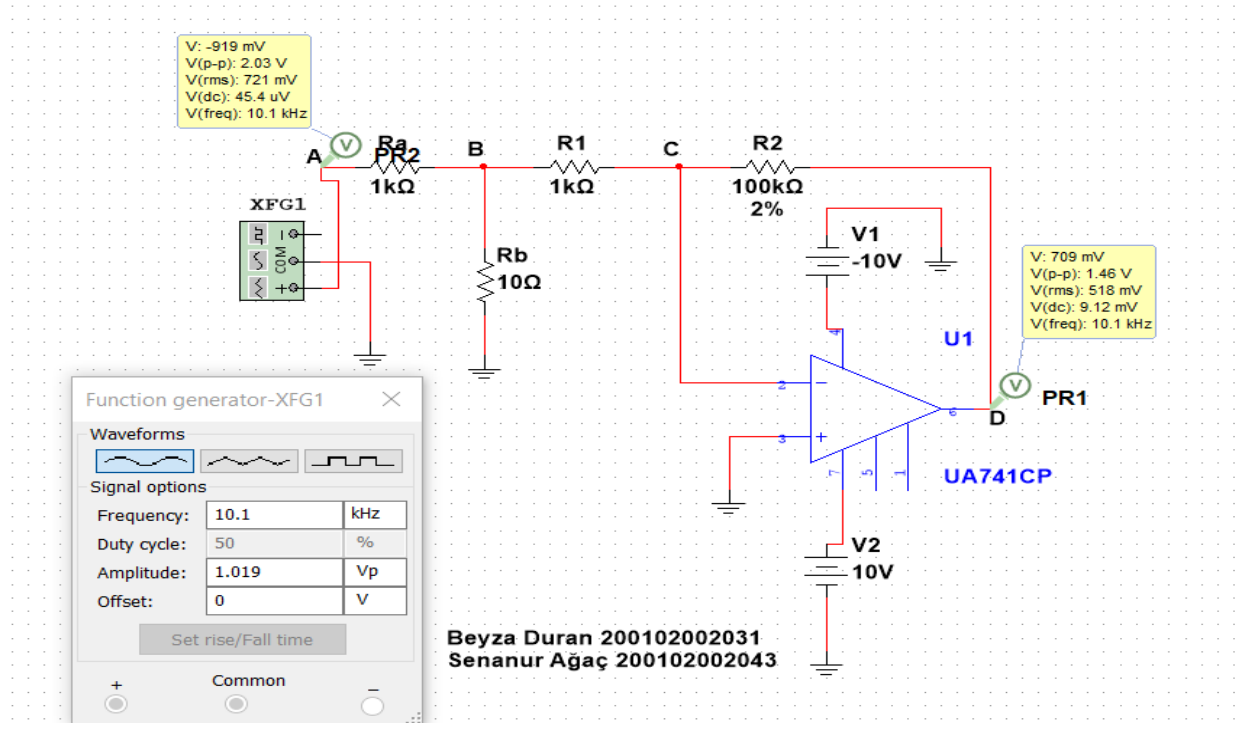


Figure 20 : Solution of b) in simulation

c)

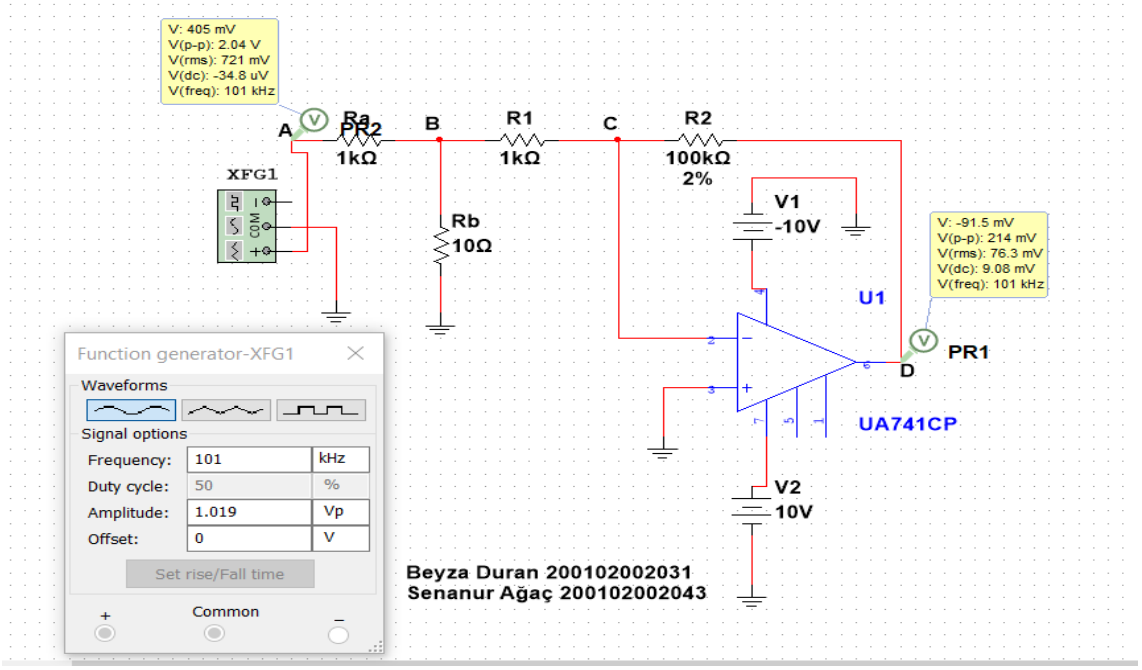


Figure 21 : Solution of c) in simulation

R_2 = 100kΩ	a)	b)	c)
v_A	**2.04 V**	**2.04 V**	**2.04 V**
v_D	2 V_{pp}	**1.46 V**	**214 mV**
f_4	100 Hz	**10.1 kHz**	**101 kHz**

Table 5 : Small signal frequency measurements for R2= 100k

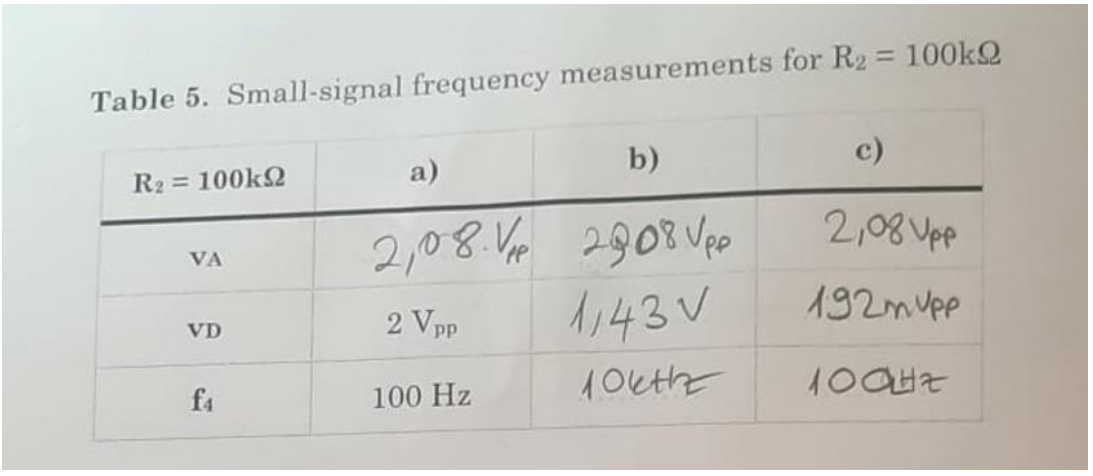


Table 5. Small-signal frequency measurements for R_2 = 100kΩ

R_2 = 100kΩ	a)	b)	c)
v_A	2,08 V_{pp}	2,08 V_{pp}	2,08 V_{pp}
v_D	2 V_{pp}	1,43 V	192 mV$_{pp}$
f_4	100 Hz	10kHz	100Hz

Figure 22 : Experiment results

3.2 Slew-rate limiting:

The output of an operational amplifier can only change by a certain amount at any given time. This limit is called the op-amp's slew rate, and although slew rate is not always mentioned, it can be a critical factor in ensuring an amplifier can provide an output that is a faithful representation of the input. The op-amp slew rate can limit the performance of the circuit if the slew rate requirement is exceeded. If the rotation speed is exceeded, it may distort the waveform and prevent the input signal from being faithfully displayed on the output.

One of the numbers specified in the datasheets for operational amplifiers is the slew rate and some calculations need to be made to check this and ensure that the particular op amp device can handle the output change rate requested from it. In some applications where speed is required and the output needs to change rapidly, the slew rate of the operational amplifier is can have a significant impact on the overall performance of the circuit and the design must accommodate it.

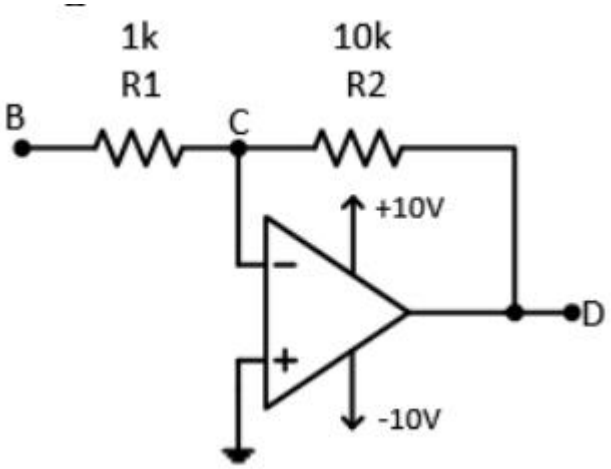


Figure 23 : A circuit for evaluatig slew rate

Assemble the circuit as shown in Figure 5. Adjust the power supplies to ±10V.Connect a function generator to input B at 1 kHz.

a) Measure nodes B and D. Adjust the generator amplitude to provide a peak output at node D of 0.2 Vpp at 1 kHz

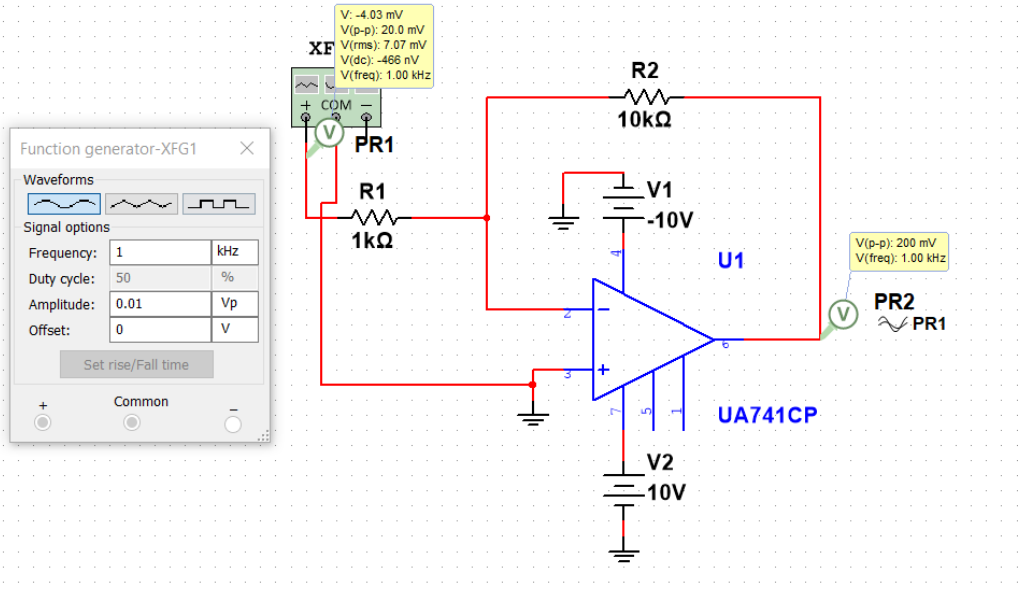


Figure 24: Solution of a) in simulation

b) Raise the frequency of the generator to the value at which vD is reduced by 3dB (to $1/\sqrt{2} = 0.707$ of its 1 kHz value). Note the frequency as f5. Verify that it's 100 times that in E3.1 b), namely 100 f4.

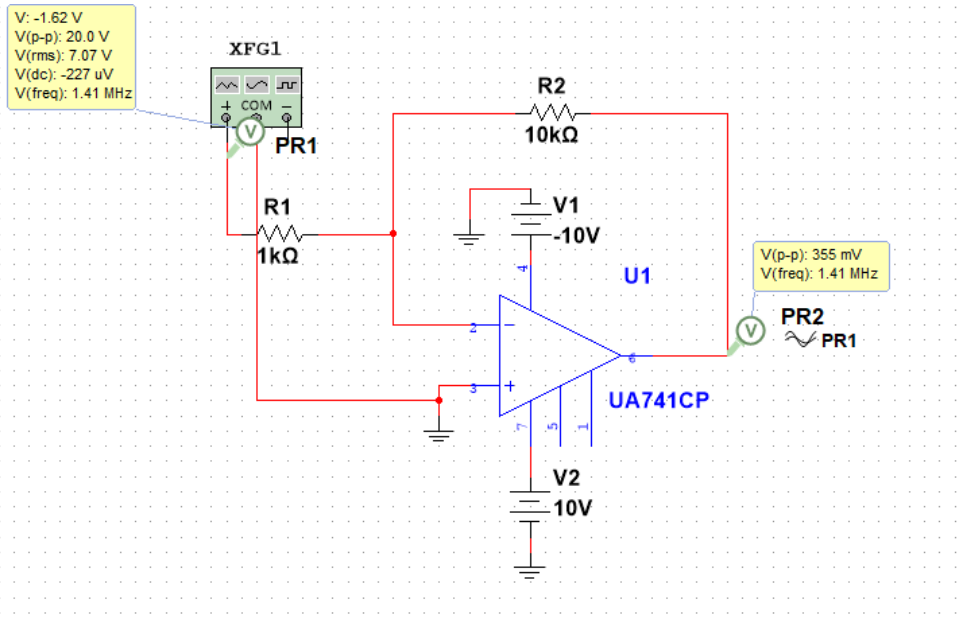


Figure 25: Solution of b) in simulation

f5 = 1.41 Mhz

frequency is set as specified and f5 is found.

c) Reduce the frequency to 1 kHz. Raise the input signal amplitude until vD reaches 8 Vpp. Note vB.

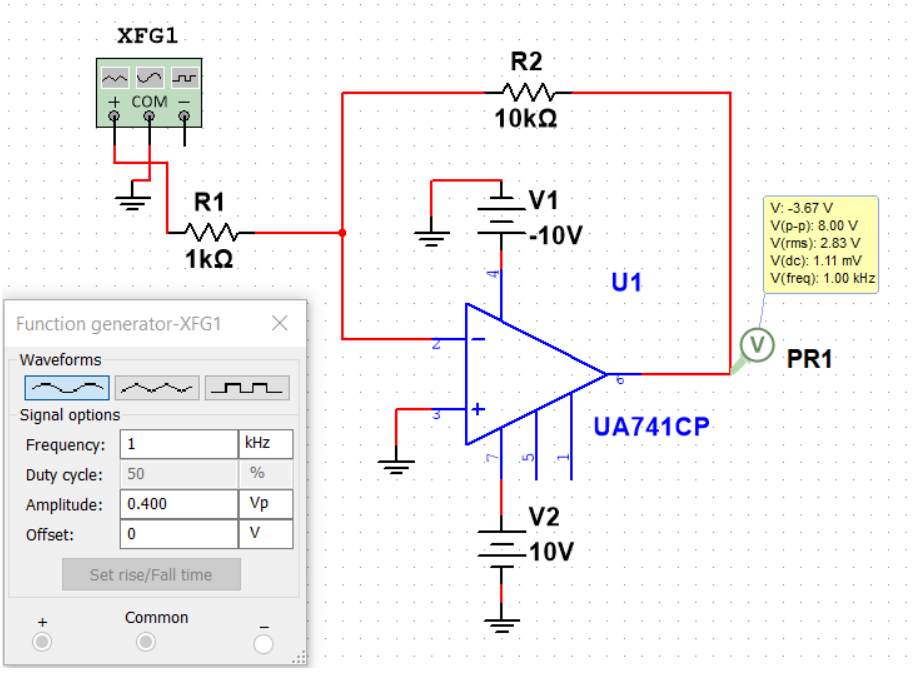


Figure 26 : Solution of c) in simulation

It was found that Vb value should be 0.4 vP(0.8 Vpp) in order to get the output voltage as Vd = 8V Vpp.

vB = 0.4 Vp

d) Keeping vB fixed and observing vD, raise the frequency until vD falls to 0.707 of its low-frequency value. Note the frequency as f6; Sketch the waveform.

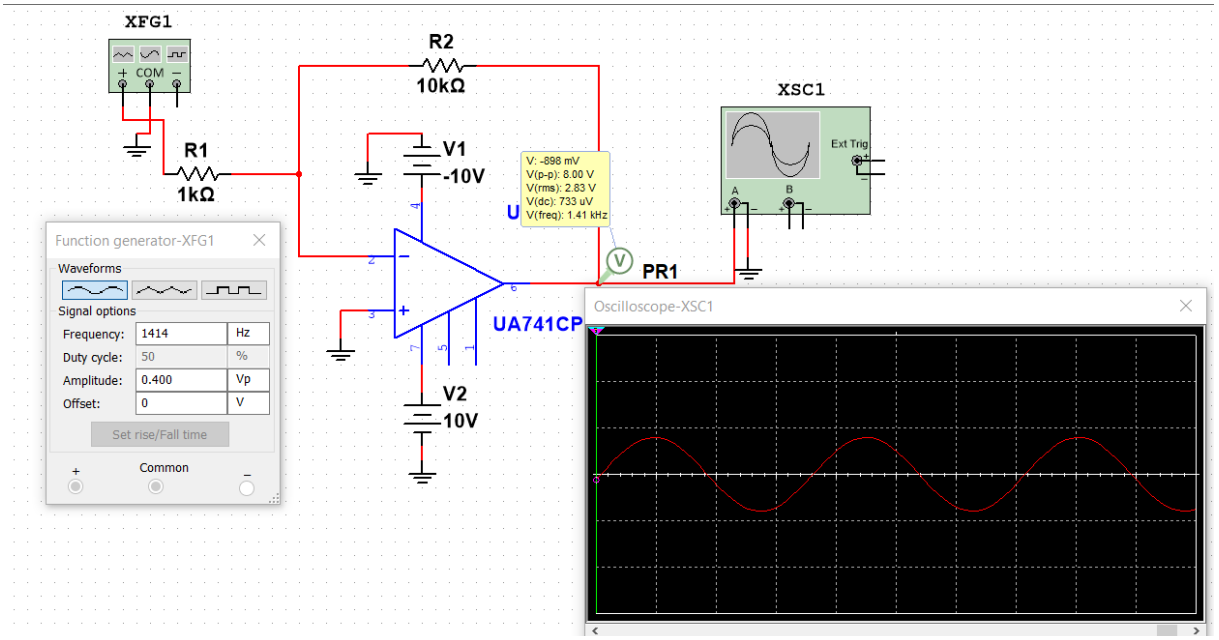


Figure 27 : Solution of d) in simulation (wavefrom)

f6 =1.41 kHz

e) Lower vB to half its former value. What does vD become? Sketch the waveform.

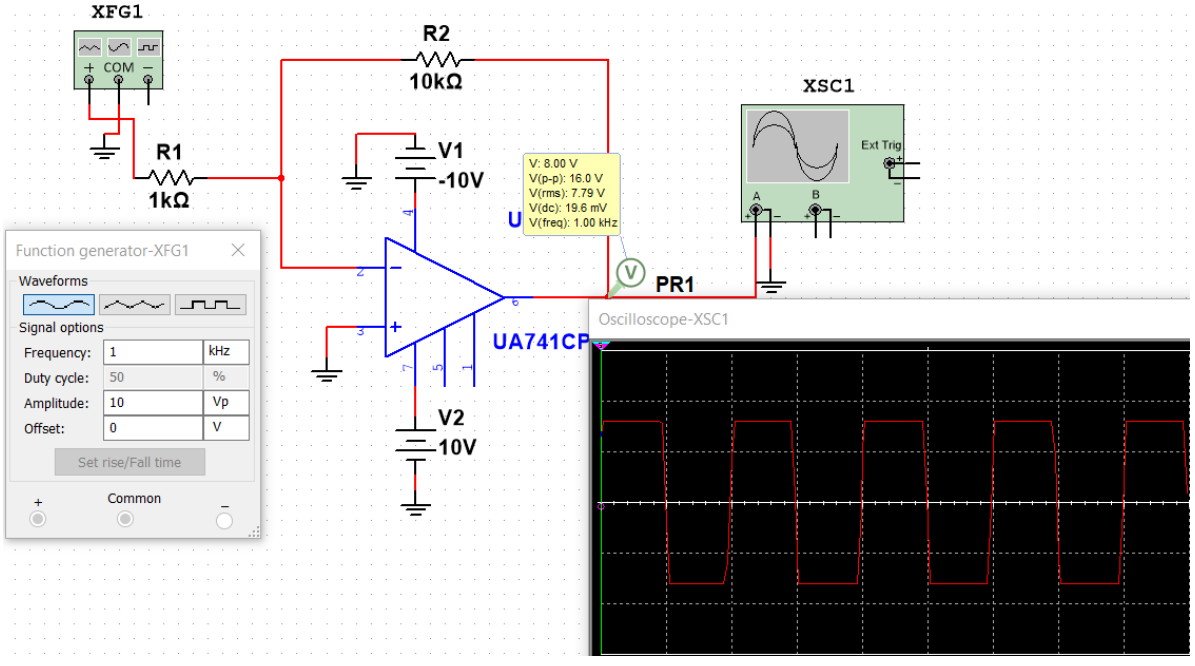


Figure 28 : Solution of e) in simulation

Vd = 16.0 V Vpp

a) Measure nodes B and D. Adjust the generator amplitude to provide a peak output at node D of 0.2 V_{pp} at 1 kHz.

b) Raise the frequency of the generator to the value at which v_D is reduced by 3dB (to $1/\sqrt{2} = 0.707$ of its 1 kHz value). Note the frequency as f_5. Verify that it's 100 times that in E3.1 b), namely 100 f_4.

$f_5 =$ 80kHz

c) Reduce the frequency to 1 kHz. Raise the input signal amplitude until v_D reaches 8 V_{pp}. Note v_B.

$v_B =$ 800mVp

d) Keeping v_B fixed and observing v_D, raise the frequency until v_D falls to 0.707 of its low-frequency value. Note the frequency as f_6; Sketch the waveform.

$f_6 =$ .....

Figure 29: Experiment results