GEBZE TECHNICAL

UNIVERSITY

ELECTRONIC

ENGINEERING

ELEC-237

ELECTRONICS LABORATORY-I

EXPERIMENT 4

Bipolar Transistor Basics

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1.Component Familiarization and Identification

1.1 Establishing Device Currents (npn):

- Analysis of the circuit:

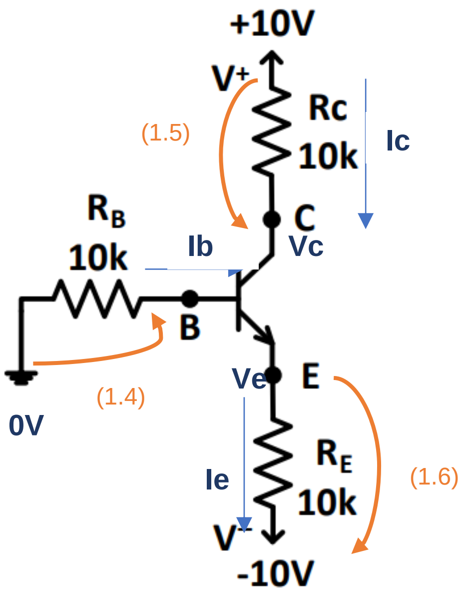


Figure 1 : A flexible biasing circuit.

Equation region

➔ $Ie = Ic + Ib$ (KCL) (1.1)

➔ $\beta = \frac{Ic}{Ib}$ $and\ \alpha = \frac{Ic}{Ie}$ (1.2)

➔ $so\ ;\ \beta = \frac{\alpha}{1-\alpha}$ (1.3)

➔

➔ $\frac{0V - Vb}{10k} = Ib$ (1.4)

➔ $\frac{10V - Vc}{10k} = Ic$ (1.5)

➔ $\frac{Ve - (-10V)}{10k} = Ie$ (1.6)

The analysis of the circuit is made as given in the equation region and Figure 1.

- Question :

Connect the circuit as shown in Figure 1, with the supplies carefully adjusted to ±10.00V. Note the exact values of resistors using your DVM and try to choose well-matched (with a 1% tolerance) resistors.

Measure the voltages at B, E, and C with respect to ground, using your DVM. Using these measurements, calculate VBE, IB, IC, IE, α, β. Fill Table 1.

- Simulation :

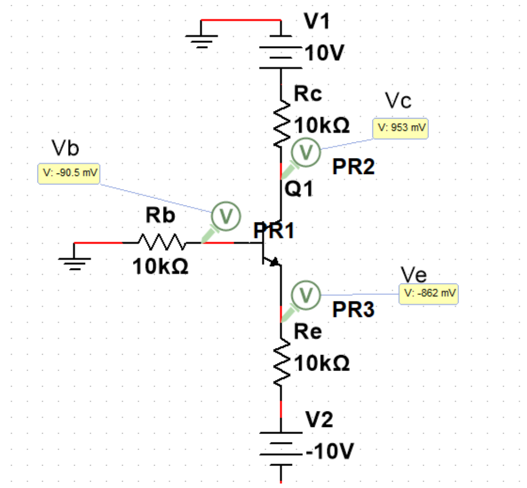


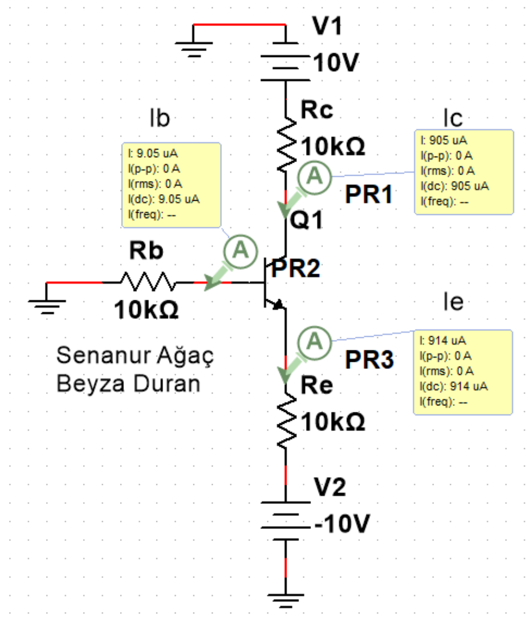
Figure 2 : Simulation for Vb,Vc,Ve

Vc = 953 mV

Vb = -90.5 mV

Ve = -862 mV

With the simulation made on Multisim, the voltage results are as shown below.



Ic = 905 uA

Ib = 9.05 uA

Ie = 914 uA

With the simulation made on Multisim, the voltage results are as shown below.

Figure 3 : Simulation result for Ib,Ic,Ie

Results :

Simulation :

V_B	V_C	V_E	V_{BE}	I_B	I_C	I_E	α	β
-90.5mV	953 mV	-862mV	771.5mV	9.05uA	905uA	914 uA	0.99	100

Table 1 : Operating points of the BJT in Figure 1(Simulation)

Experiment :

Table 1. Operating points of the BJT in Figure 1.

$I_c = \beta \cdot I_B$

V_B	V_C	V_E	V_{BE}	I_B	I_C	I_E	α	β
-36.3mV	0.707V	-608mV	0.601V	2.07μA	951μA	+953.8μA	0.997	459

601mV

$\beta = 459$

When both tables were compared, it was seen that the values were compatible with the results, although they were not exactly the same.

1.2 Identifying the Controlling Junction and Junction Current:

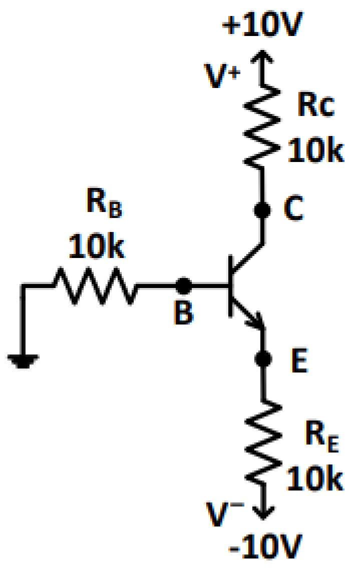


Figure 4: A flexible biasing circuit

a) Raise V- to -5V, and measure the voltages at B, E, and C with respect to ground, using your DVM. Repeat the calculation steps in 1.1 and fill Table 2.

b) With V- = -5V, lower V+ to +5V, and repeat a).

a)

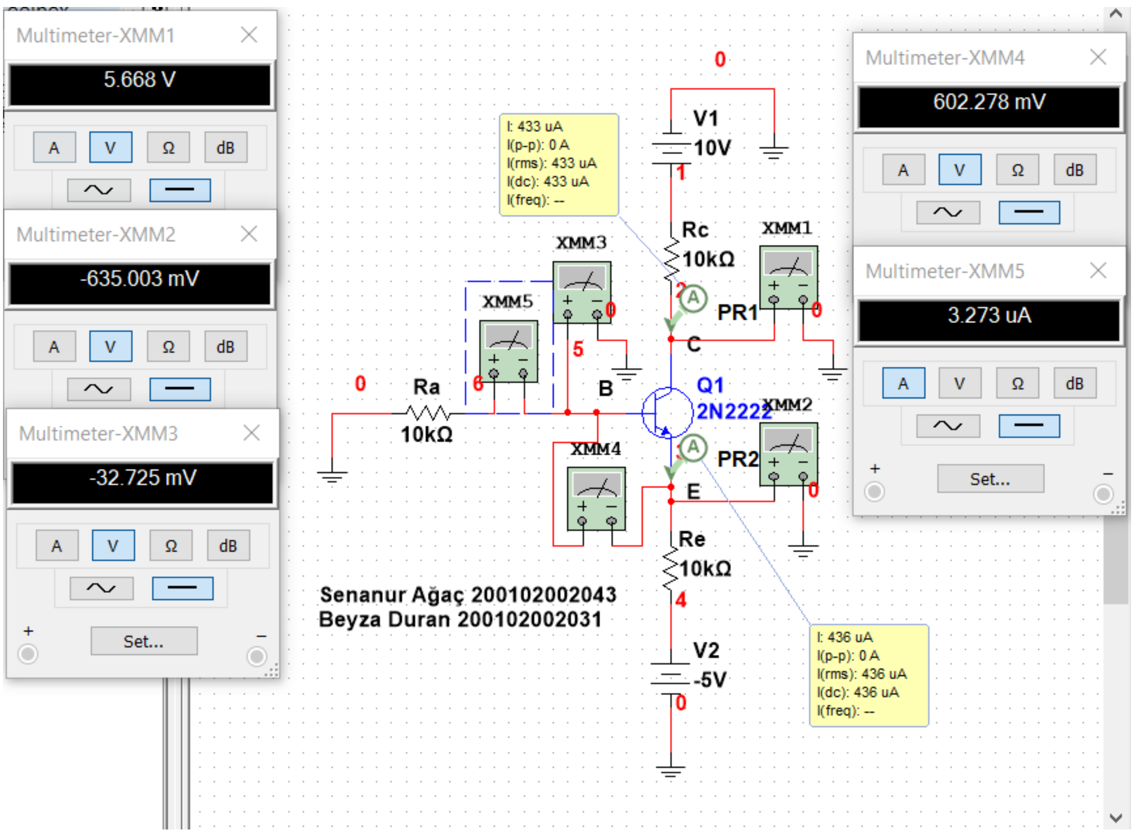


Figure 5: $V^{+} = 10\ V$, $V^{-} = -5V$

b)

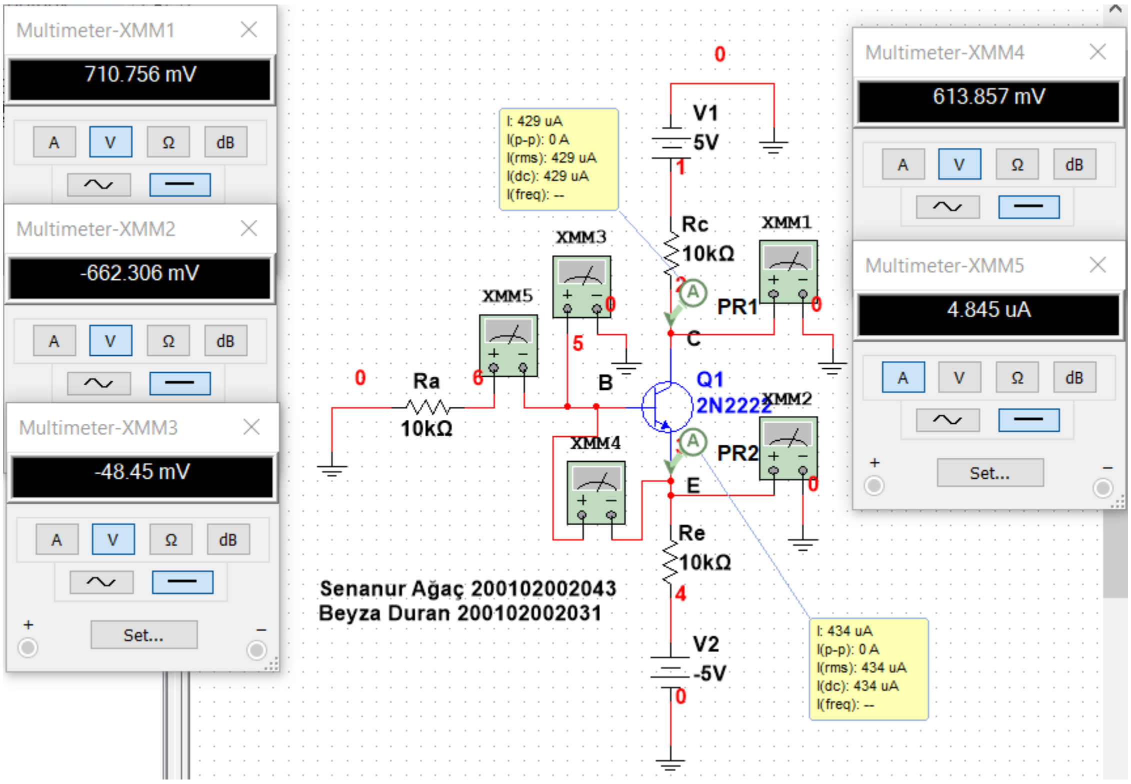


Figure 6: $V^+ = 5$ V , $V^- = -5$V

Tablo 2: Operating points of the BJT in Figure 1 with different supply voltages.

	V_B	V_C	V_E	V_{BE}	I_B	I_C	I_E	α	β
$V^- = -5V$ $V^+ = +10V$	**-33mV**	**5.668V**	**-635mV**	**602mV**	**3.273 μA**	**436 μA**	**433μA**	**133**	**0.99**
$V^- = -5V$ $V^+ = +5V$	**-48mV**	**711 mV**	**-662mV**	**614mV**	**4.845 μA**	**429 μA**	**434 μA**	**89**	**0.99**

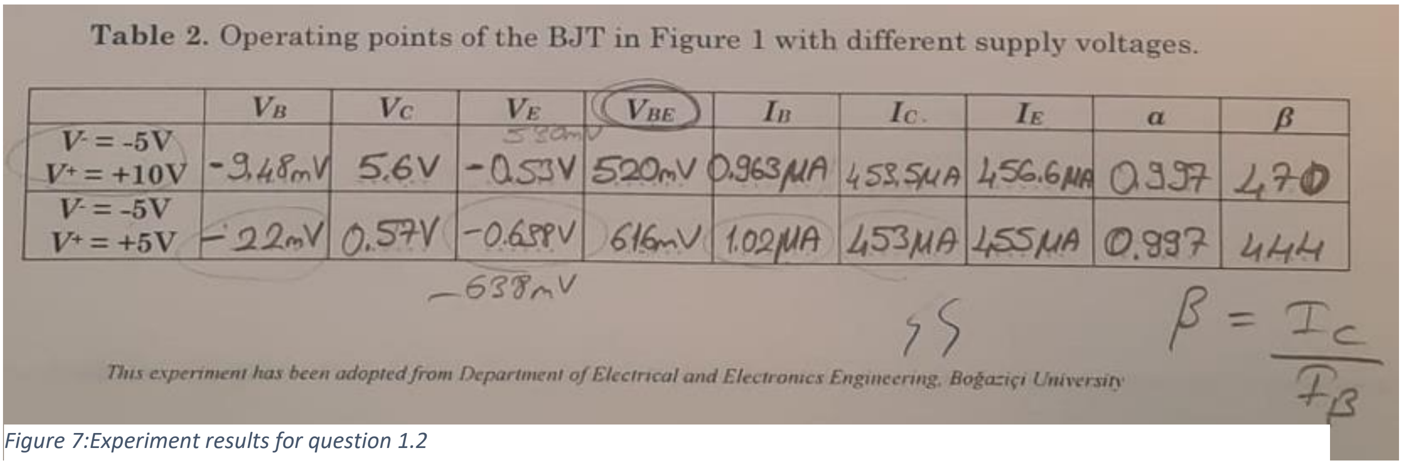


Table 2. Operating points of the BJT in Figure 1 with different supply voltages.

	V_B	V_C	V_E	V_{BE}	I_B	I_C	I_E	α	β
$V^- = -5V$ $V^+ = +10V$	-9.48mV	5.6V	-0.53V	520mV	0.963μA	453.5μA	456.6μA	0.997	470
$V^- = -5V$ $V^+ = +5V$	-22mV	0.57V	-0.638V	616mV	1.02μA	453μA	455μA	0.997	444

530mV

-638mV

55

$\beta = \frac{I_C}{I_B}$

This experiment has been adopted from Department of Electrical and Electronics Engineering, Boğaziçi University

Figure 7:Experiment results for question 1.2

2.Other, Less-Stable Biasing Schemes

2.1 Base-Current Bias:

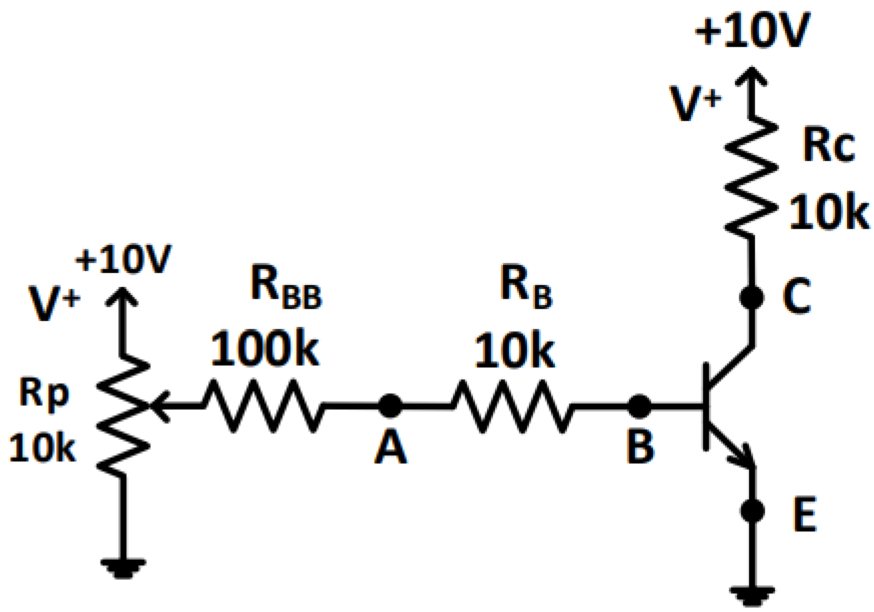


Figure 8: A bad base-current-biasing circuit

a) Measure the voltage at node C, adjusting potentiometer RP until VC = +5V.
b) Measure the voltages at nodes A and B with your DVM.
c) While measuring VC, heat the transistor. Note the new value of VC.
d) Remove the transistor (carefully). Insert another one in its place; repeat the parts b) and c) without changing the potentiometer resistance RP.

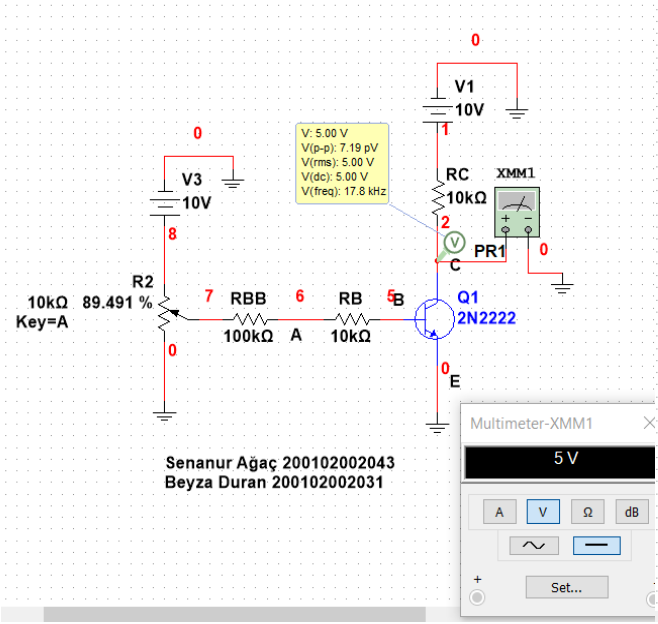


Figure 94: The value of the potentiometer when Vc is 5 V

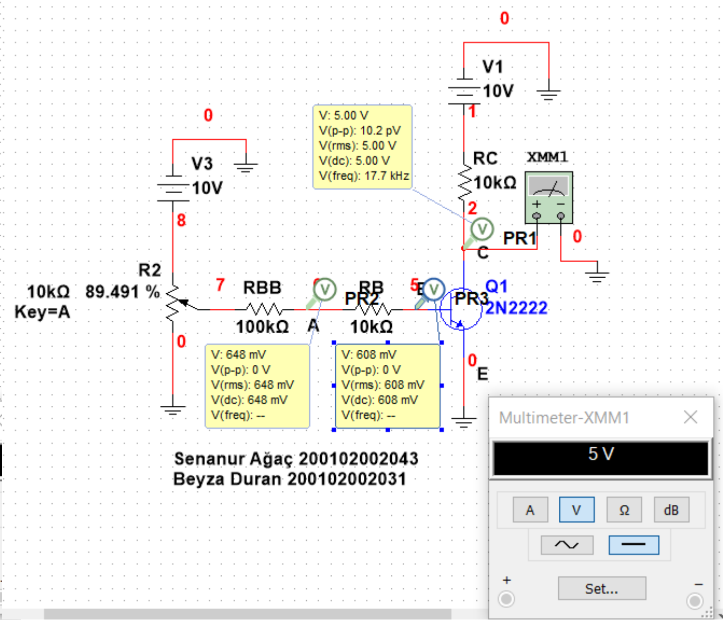


Figure 10: Measuring A and B node voltages

Tablo 3: Operating points of BJT in Figure ? under different temperature conditions.

Node Voltage	Transistor 1	Transistor 2
V_A	648 mV	648 mV
V_B	608 mV	608 mV
V_{C_cold}	5 V	5 V
V_{C_hot}		

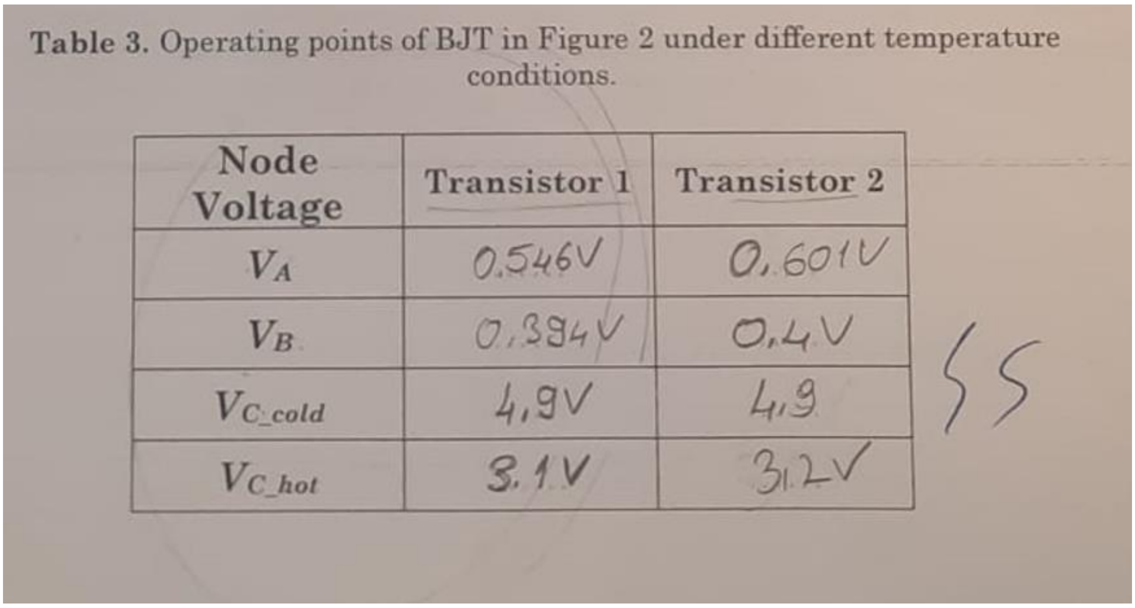


Table 3. Operating points of BJT in Figure 2 under different temperature conditions.

Node Voltage	Transistor 1	Transistor 2
V_A	0.546V	0.601V
V_B	0.394V	0.4V
V_{C_cold}	4,9V	4,9
V_{C_hot}	3.1V	3.2V

Figure 11: Experimental results fort he question 2.1

Transistor Biasing : Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

The steady state operation of a transistor depends a great deal on its base current, collector voltage, and collector current values and therefore, if the transistor is to operate correctly as a linear amplifier, it must be properly biased around its operating point. Establishing the correct operating point requires the selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions. The correct biasing point for a bipolar transistor, either NPN or PNP, generally lies somewhere between the two extremes of operation with respect to it being either “fully-ON” or “fully-OFF” along its DC load line. This central operating point is called the “Quiescent Operating Point”, or **Q-point** for short.

- 2.2 Fixed Base-Emitter-Voltage Biasing

Question :

Note, this is clearly the worst bias design of all, unless the desire is to create an electronic thermometer! Connect the circuit as shown in Figure 3.

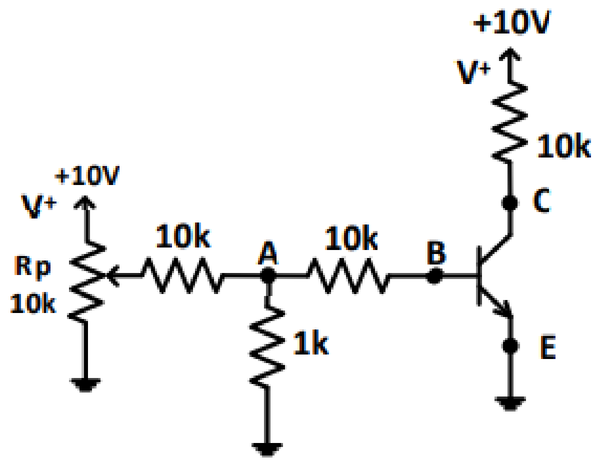


Figure 12 : A bad base-voltage-biasing circuit.

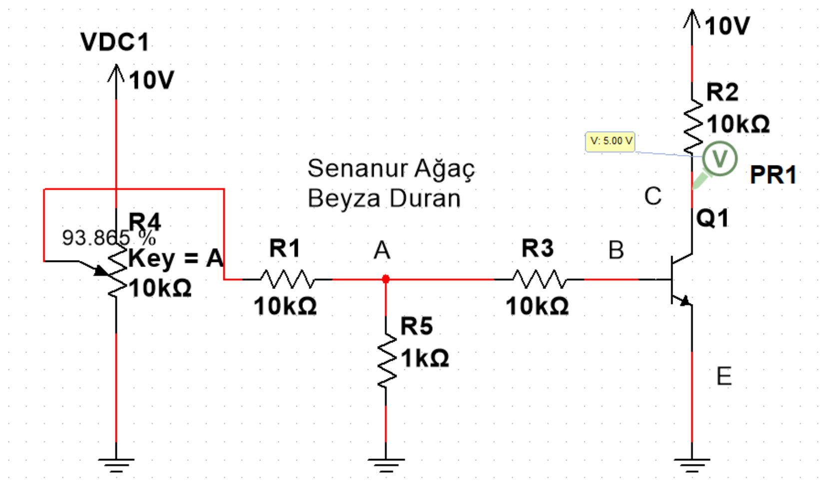
a) Measure the voltage at node C, adjusting potentiometer RP until VC = +5V.

b) Measure the voltages at nodes A and B with your DVM.

c) While measuring VC, heat the transistor (ask your TA for a soldering iron). Note the new value of VC.

- Simulation

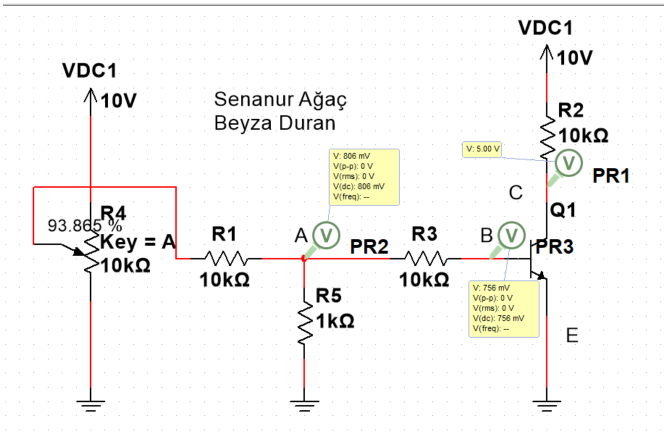
a)



In the simulation, the value of Rp was constantly changed and when Rp = 93.865%, it was seen that the Vc value was 5V.

Figure 13 : Simulation result for a)

b)



Va = 806 mV and Vb = 756 mV in simulation, when Vc is kept constant at 5V (without changing Rp).

Figure 14: Simulation result for b)

c)

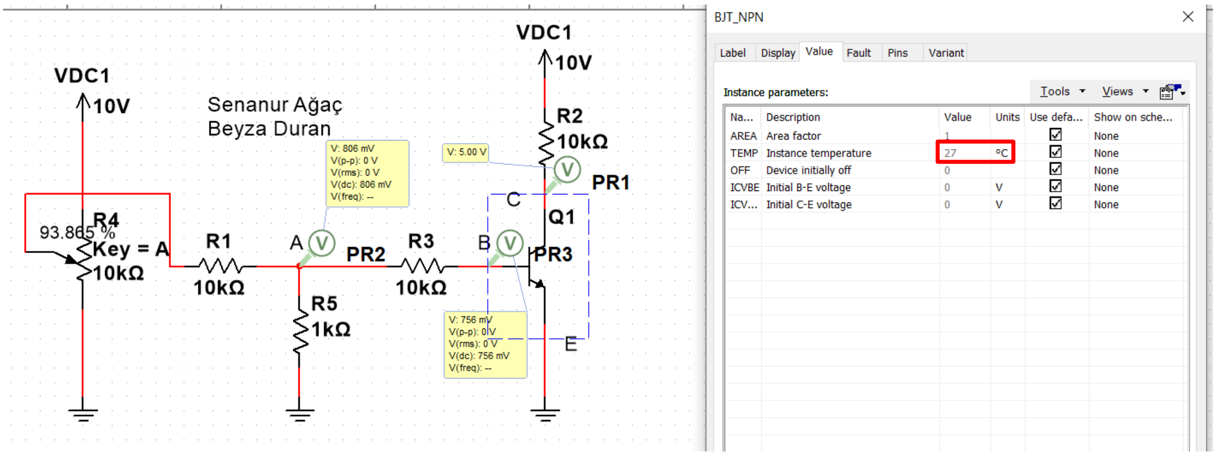


Figure 15 : Simulation result for c) – cold

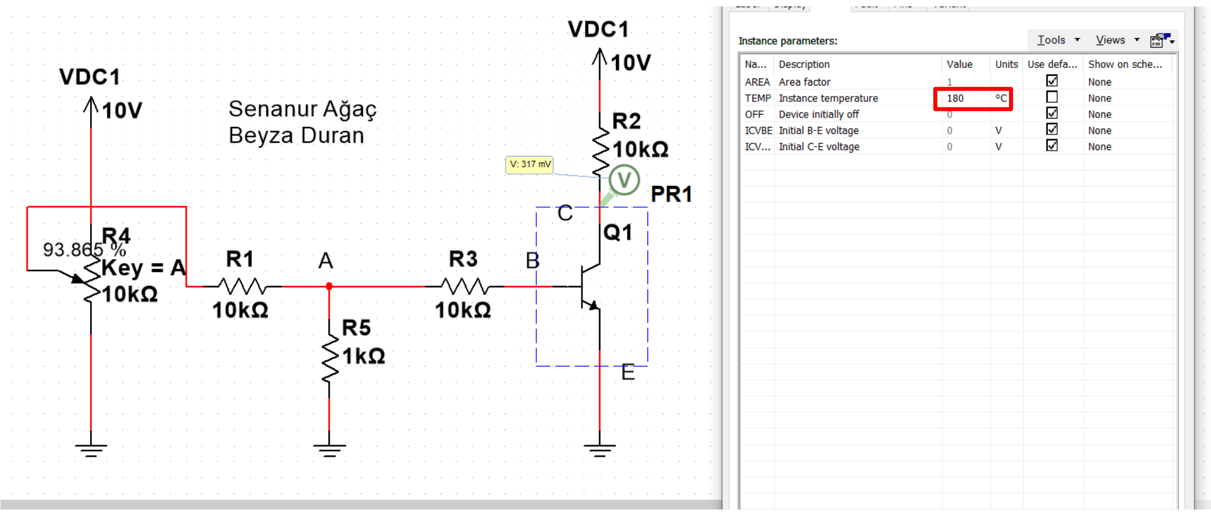


Figure 16: Simulation result for c) – hot

In the simulation, when the BJT was 27 °C, Vc was measured and found to be 5v (Figure 7). Then the temperature was increased to 180 °C and it was observed that the Vc value decreased to 317 mV. As a result, it was found that the voltage Vc decreased as the temperature of Bjt increased.

Results *:*

Sİmulation :

VA	806 mV
VB	756 mV
VC_cold	5V
VC_hot	317 mV (180 C°)

Table 4 : Operating points of BJT in Figure 3 under different temperature conditions.

Experiment :

Table 4. Operating points of BJT in Figure 3 under different temperature conditions.

51

V_A	0.590V
V_B	0.585V
V_{C_cold}	4.9V
V_{C_hot}	2.6V

It has been observed that the results measured in the experiment and the results found in the simulation are similar. The reason for the difference in the vc_hot value is that the degree value selected in the simulation is much higher.

3.The BJT as Amplifier

While the circuit shown in Figure 4 uses a rather bad bias design, being a combination of base-current and base-voltage biasing, it is relatively convenient for the measurement of gain of a particular transistor under stable environmental conditions. Incidentally, the presence of the potentiometer RP is, generally speaking, a sure sign of less-than-ideal design.

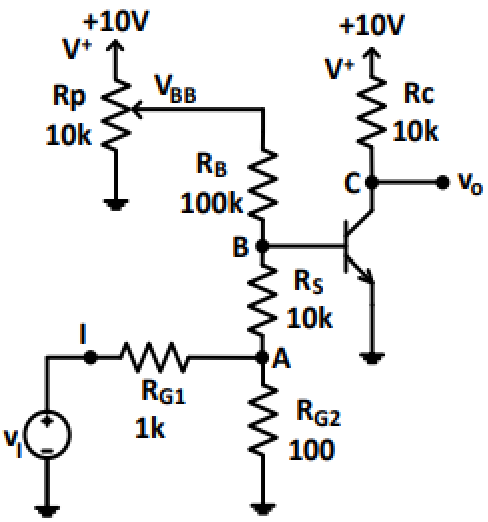


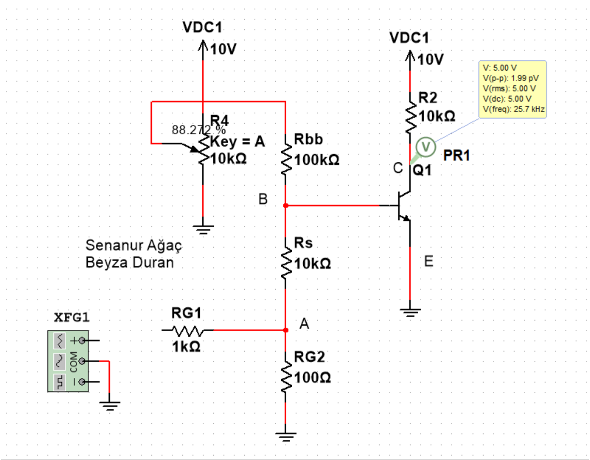
Figure 17 : A badly-biased but otherwise-interesting amplifier.

3.1 Voltage Gain and Input Resistance:

Connect the circuit as shown in Figure 9.

a) While vi open, adjust RP so that the DC voltage at C is 5V. Note the exact value of VC using your DVM.

→Simulation :



It has been observed that for Vc to be 5V when Vi is open, Rp must be 88.272%.

Vc= 5V

Figure 17 : Simulation result for a)

b) Connect the waveform generator to node I with vi is a sine wave at 1KHz. Using both channels of your oscilloscope, adjust the input-signal amplitude so that vC is a sine wave with 2Vpp amplitude. Note the peakto-peak value of the input signal.

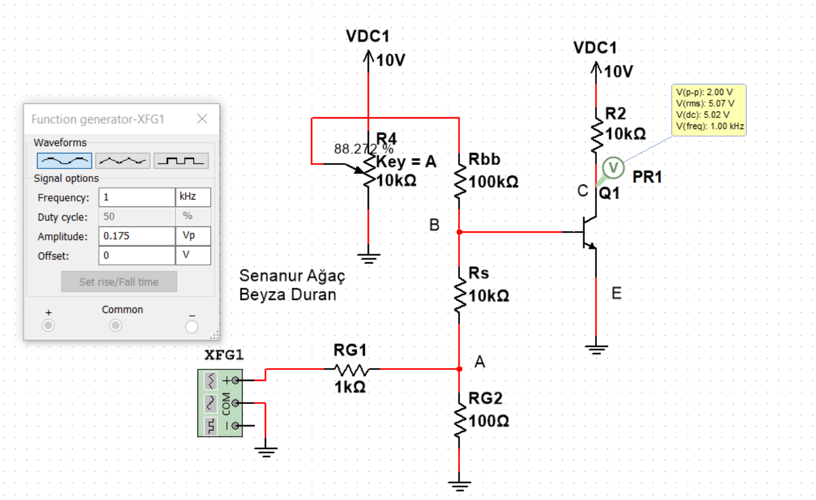
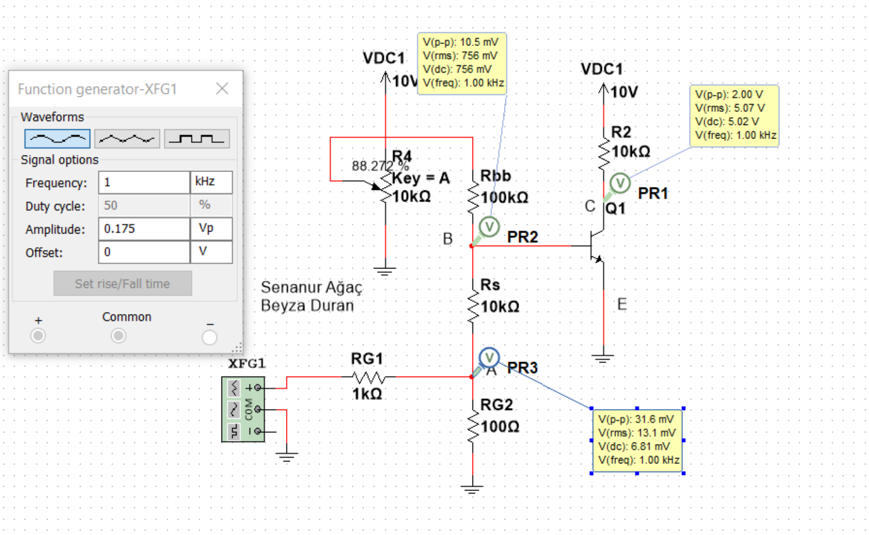


Figure 18 : Simulation result for b)

Provided that the Rp value remains the same, a voltage source Vi is connected at 1 Khz frequency and the Vi value is adjusted until Vc becomes 2 Vpp. Vi value was found to be 0.35 Vpp in simulation.

Vi = 0.35 Vpp

c)



Vb = 10.5 mVpp

Va = 31.6 mVpp

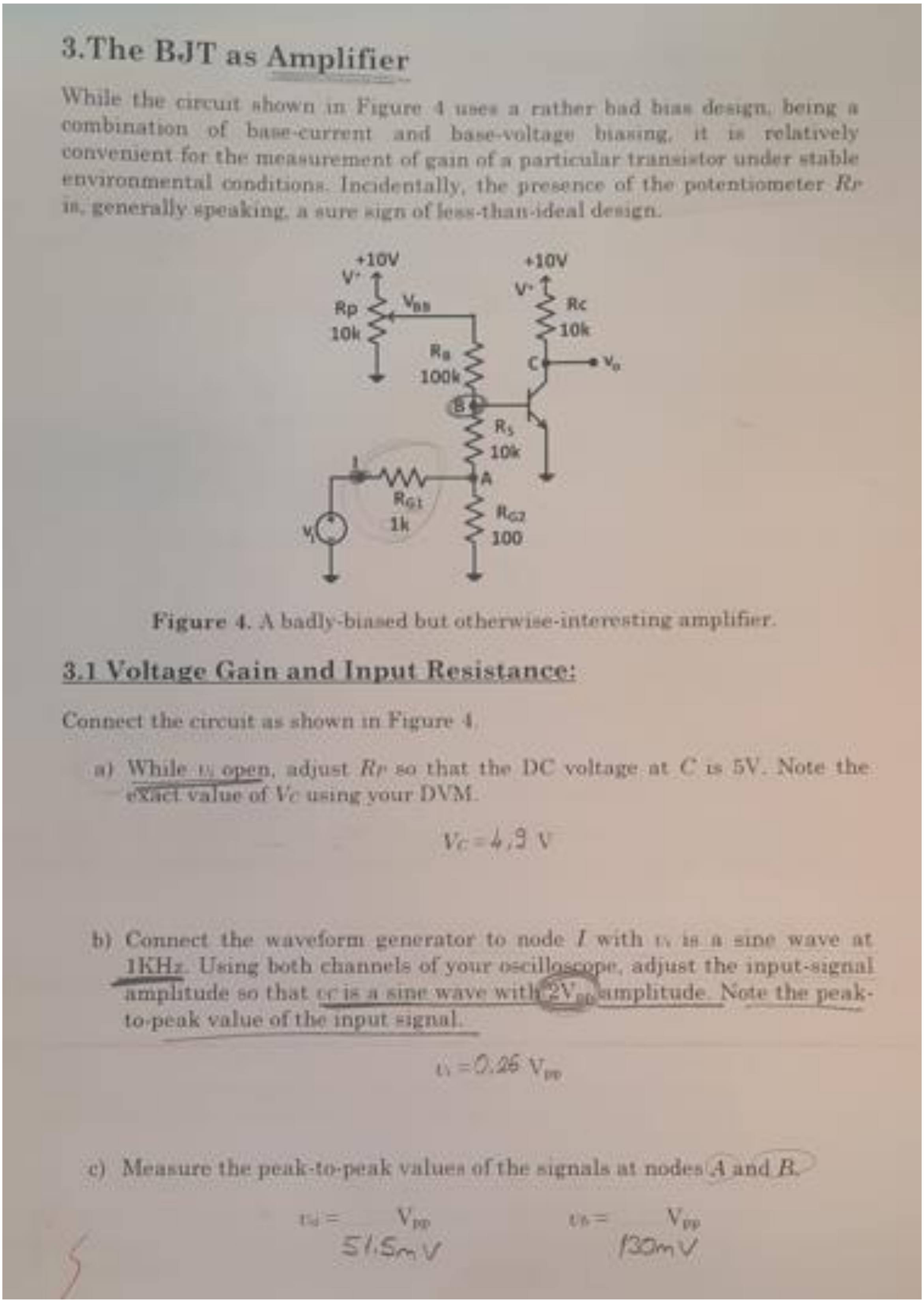
Calculate the voltage gains vo/vb, vo/va, vo/vi, and the current into the base ib, and thereby Rinb. (Rinb is the resistance that is seen by looking from node B through the base of the BJT. Because Rinb is quite small comparing with the RB + RP which is approximately 100kΩ, ib can be regarded as the current passing through RS.)

CALCULATION AREA

- $\frac{vo}{vb} = \frac{2Vpp}{10.5\ mV} = 190.47\ V/V$
- $\frac{vo}{va} = \frac{2Vpp}{31.6\ mV} = 63{,}3\ V/V$
- $\frac{vo}{vi} = \frac{2Vpp}{0.35Vpp} = 5.74\ V/V$

vo/vb =$190.47\ V/V$	vo/va=$63{,}3\ V/V$	vo/vi=$5.74\ V/V$	ib = 2. 1 uA	Rinb = 999.001 miliohm

Experiment results:



3.The BJT as Amplifier

While the circuit shown in Figure 4 uses a rather bad bias design, being a combination of base-current and base-voltage biasing, it is relatively convenient for the measurement of gain of a particular transistor under stable environmental conditions. Incidentally, the presence of the potentiometer R_P is, generally speaking, a sure sign of less-than-ideal design.

Figure 4. A badly-biased but otherwise-interesting amplifier.

3.1 Voltage Gain and Input Resistance:

Connect the circuit as shown in Figure 4.

a) While v_i open, adjust R_P so that the DC voltage at C is 5V. Note the exact value of V_C using your DVM.

V_C = 4,9 V

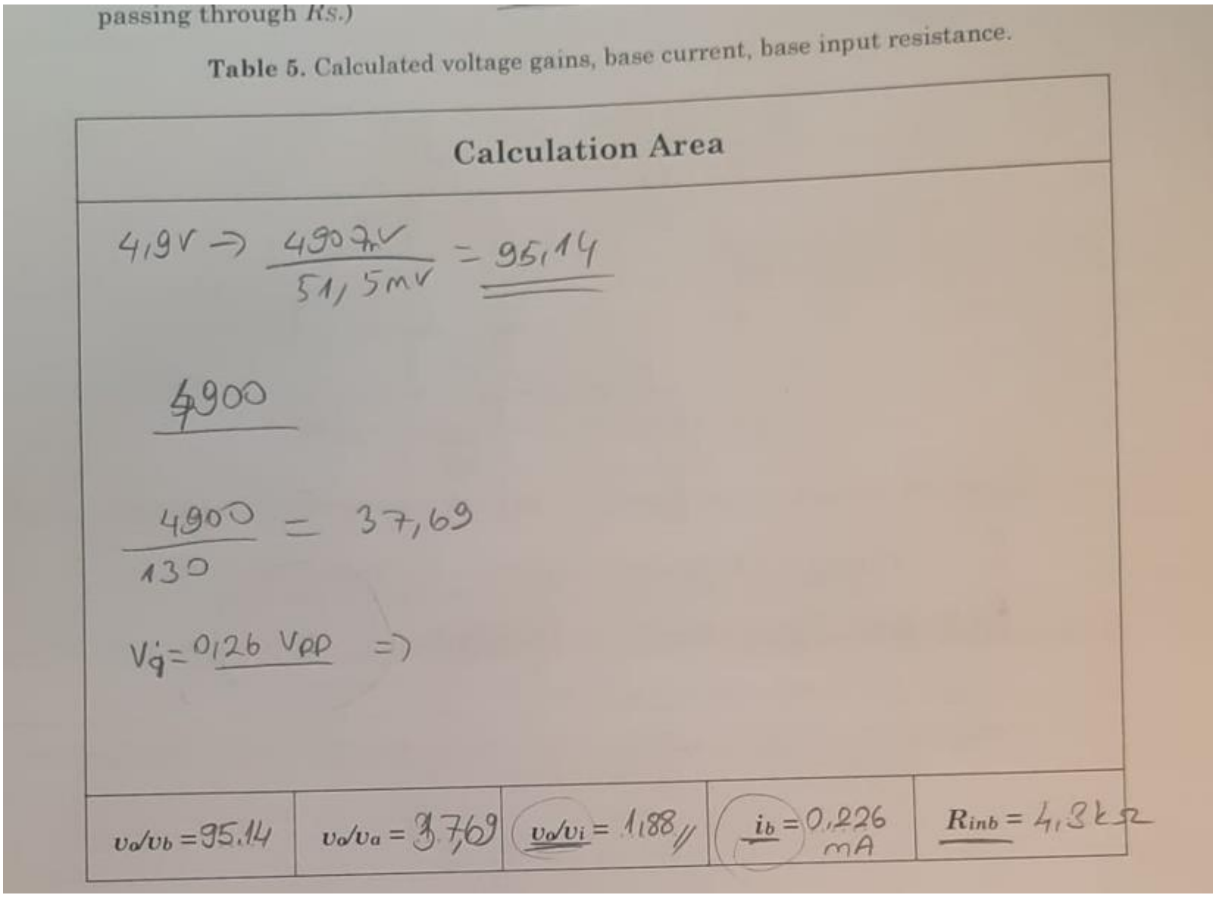
b) Connect the waveform generator to node I with v_i is a sine wave at 1KHz. Using both channels of your oscilloscope, adjust the input-signal amplitude so that v_C is a sine wave with $2V_{pp}$ amplitude. Note the peak-to-peak value of the input signal.

v_i = 0.26 V_{pp}

c) Measure the peak-to-peak values of the signals at nodes A and B.

v_a = V_{pp} 51.5mV v_b = V_{pp} 130mV

Figure 19 : Experiment result for a) b) and c)



passing through R_S.)

Table 5. Calculated voltage gains, base current, base input resistance.

Calculation Area				
$4{,}9V \rightarrow \frac{4900mV}{51{,}5mV} = 95{,}14$ $\underline{4900}$ $\frac{4900}{130} = 37{,}69$ $V_g' = 0{,}126\ V_{PP} \Rightarrow$				
$v_o/v_b = 95.14$	$v_o/v_a = 37{,}69$	$v_o/v_i = 1{,}88$	$i_b = 0{,}226\ mA$	$R_{inb} = 4{,}3k\Omega$

Figure 20 : Calculation area

3.2 Large Signal Distortion:

Use the same configuration as in Figure 4. Adjust for VC = 5V as directed in 3.1 step a) above.

a) Measure the voltages at nodes C and I with your dual-channel oscilloscope. Adjust the input-signal amplitude so that vC is a sine wave with 1Vpp amplitude. Note the peak-to-peak value of the input signal.

vi = 0.98 Vpp

b) Set both channels of node C and I on AC coupling. Adjusting the volt/division and dc level settings of the channels, try to overlap two signals as exact as possible. Note the phase of node C with respect to I

$\Phi = 0°$

c) Raise the input voltage slowly, while observing the voltages at nodes I and C. Observe that the gain will start to change slightly at some point. Note the necessary values to the table below.

a)

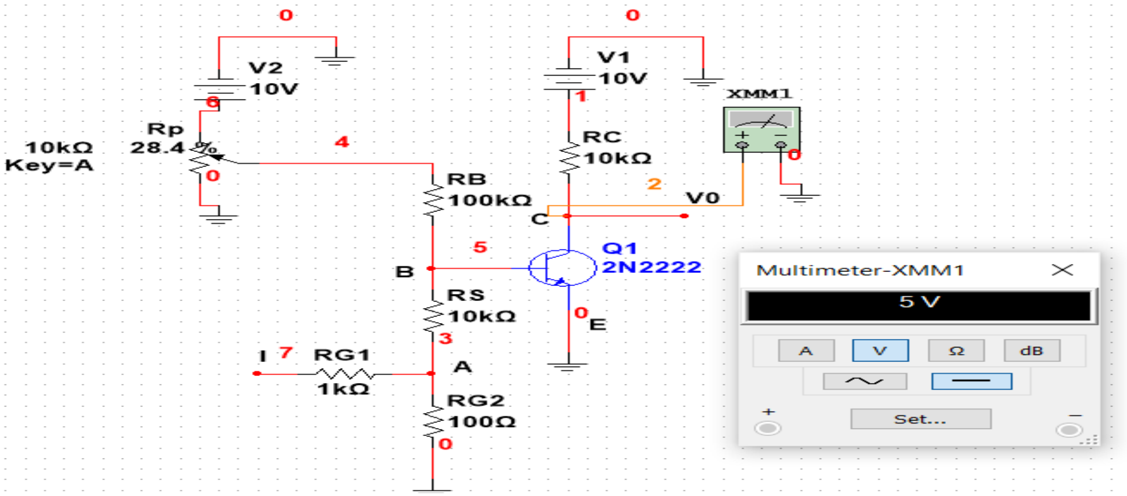
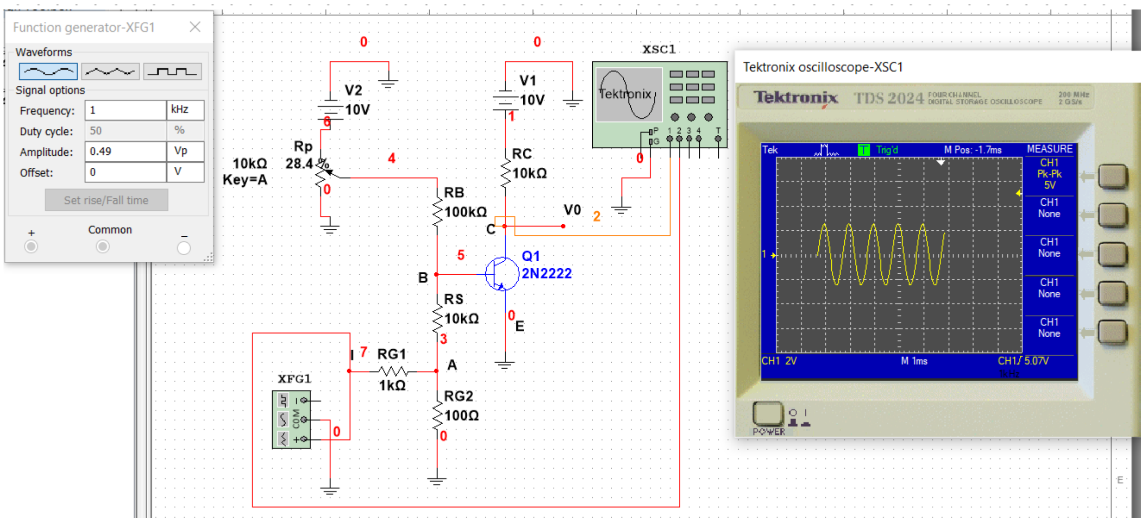


Figure 21: Adjusting the potentiometer to make the Vc voltage value 1 Vpp



Display of the amplitude value that will make the Vc voltage value 5V on the function generator (Vpp = 2X 0.49=0.98V)

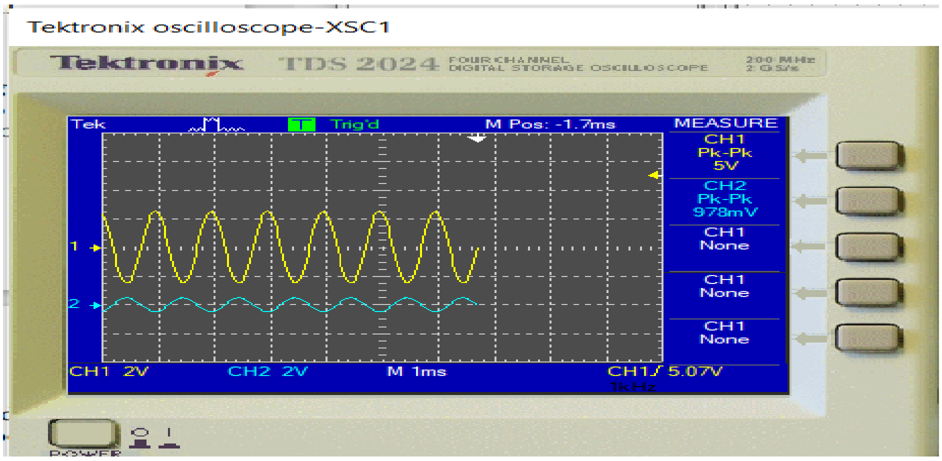


Figure 21: Measuring voltages at nodes C and I (CH1= C, CH2=I)

b) The time difference between the C and I waves is so small that the phase angle p is found as;

$$\Phi = 360 \times \Delta t \times f = 0°$$

c)

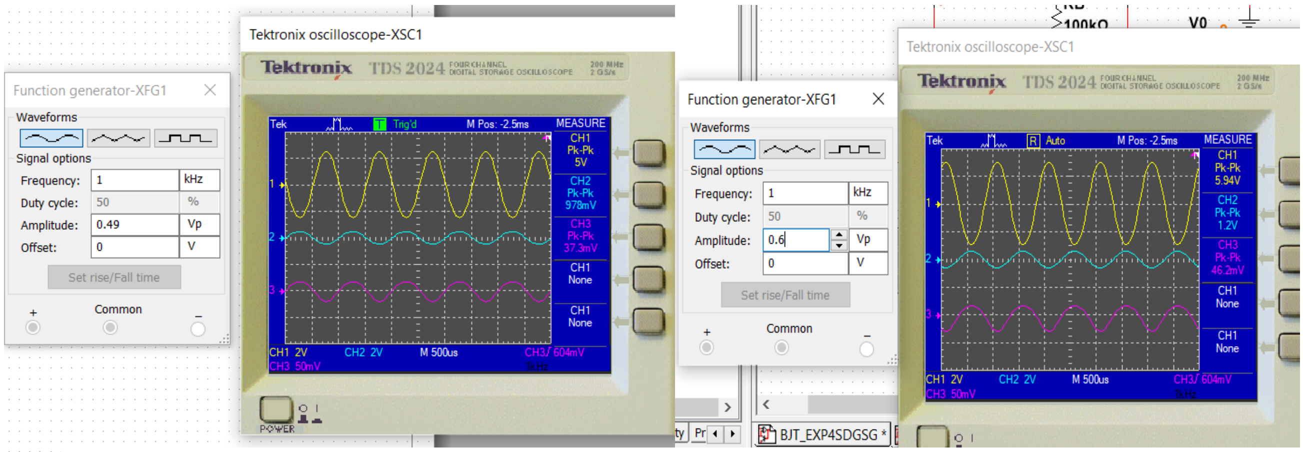


Figure22: slowly increasing the input voltage

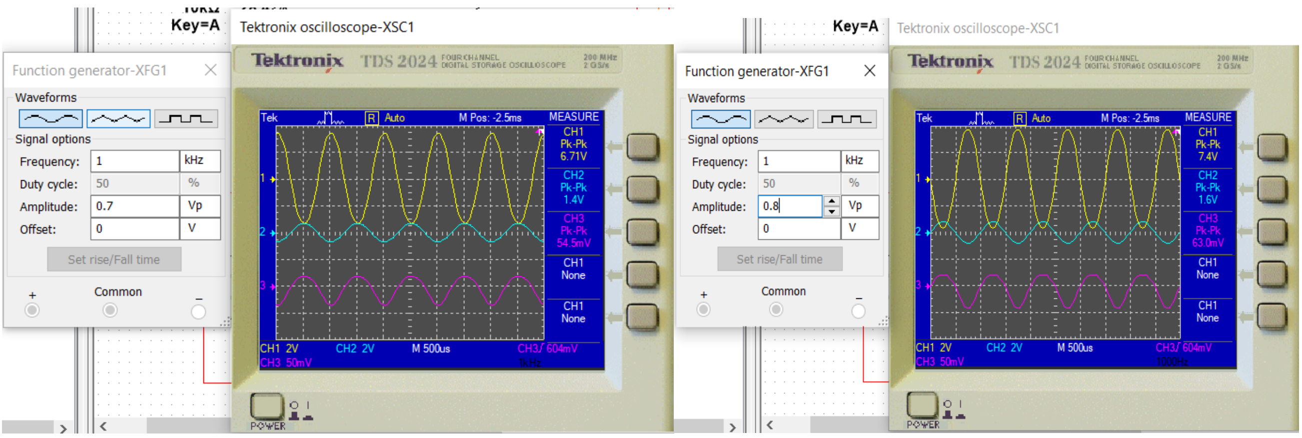


Figure 23: slowly increasing the input voltage

3.2 Large Signal Distortion:

Use the same configuration as in Figure 4. Adjust for $V_C = 5V$ as directed in 3.1 step a) above.

a) Measure the voltages at nodes C and I with your dual-channel oscilloscope. Adjust the input-signal amplitude so that v_C is a sine wave with $1V_{pp}$ amplitude. Note the peak-to-peak value of the input signal.

$v_i =$ 85, V_{pp}

b) Set both channels of node C and I on AC coupling. Adjusting the volt/division and dc level settings of the channels, try to overlap two signals as exact as possible. Note the phase of node C with respect to I.

$\Phi =$ 1,100µs

This experiment has been adopted from Department of Electrical and Electronics Engineering, Boğaziçi University

Figure 24: Experimental results

c) Raise the input voltage slowly, while observing the voltages at nodes I and C. Observe that the gain will start to change slightly at some point. Note the necessary values to the table below.

Table 6. AC voltage measurements to observe large-signal distortion.

Situation	v_c	v_i	v_b
Gain just changing	......V_{pp}	......V_{pp}	......V_{pp}

d) Now, set only the channel of the output node on DC coupling. Then, keep increasing the input until you see the point positive or negative peak of the output flattens. Note the necessary values for that input level and then increase until you see the other peak flatten. Fill the table below accordingly.

Table 7. AC voltage measurements to observe output swing of amplifier in Figure4.

	DC Coupling		AC Coupling	
Situation	v_c		v_i	v_b
Pos. peak limit	......V_{pp}	Pos. peak value: V	......V_{pp}	......V_{pp}
Neg. peak limit	......V_{pp}	Neg. peak value: V	......V_{pp}	......V_{pp}

Figure 25: Unfortunately, this part of the experiment was not performed during the experiment.