

DEPARTMENT OF ELECTRONICS ENGINEERING

ELEC366 COMMUNICATIONS LABORATORY

EXPERIMENT-6



1. GOAL

In this experiment, you will learn how to perform binary phase shift keying (BPSK) modulation & demodulation and quadrature phase shift keying (QPSK) modulation & demodulation.

2. BACKGROUND

2.1 Binary Phase Shift Keying Modulation

AM and FM modulation schemes can be used to transmit digital signals and this allows for the channel to be shared. As digital data forms the message instead of speech and music, it is preferred that these two systems are called ASK and FSK instead.

Note that ASK uses the digital data's 1s and 0s to switch a carrier between two amplitudes. FSK uses the 1s and 0s to switch a carrier between two frequencies. An alternative to these two methods is to use the data stream's 1s and 0s to switch the carrier between two phases. This is called Binary Phase Shift Keying (BPSK). Figure 9.1 shows what a BPSK signal looks like time-coincident with the digital signal that has been used to generate it.

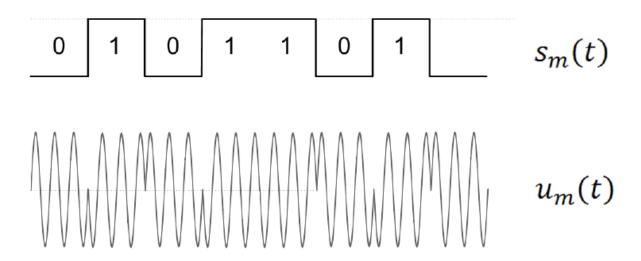


Figure 9.1: BPSK modulated signal

Notice that, when the change in logic level causes the BPSK signal's phase to change, it does so by 180°. For example, where the signal is travelling towards a positive peak the change in logic level causes it to reverse direction and head back toward the negative peak (and vice versa).

You may find it difficult to see at first but look closely and you'll notice that alternating halves of the BPSK signal's envelopes have the same shape as the message. This indicates that BPSK



is actually double-sideband suppressed carrier (DSBSC) modulation. That being the case, BPSK generation and the recovery of the data can be handled by conventional DSBSC modulation and demodulation techniques.

With a choice of ASK, FSK and BPSK you might be wondering about which system you'll most likely see. All other things being equal, BPSK is the best performing system in terms of its ability to ignore noise and so it produces the fewest errors at the receiver. FM is the next best and AM is the worst. On that basis, you'd expect that BPSK is the preferred system. However, it's not necessarily the easiest to implement and so in some situations FSK or ASK might be used as they are cheaper to implement. In fact, FSK was used for cheaper dial-up modems.

Binary Phase Shift Keying (BPSK) is a digital modulation technique. In this way, modulated signals can have discrete phase for a given digital input and it is constant for a symbol period. A BPSK modulator is shown in Figure 9.2.

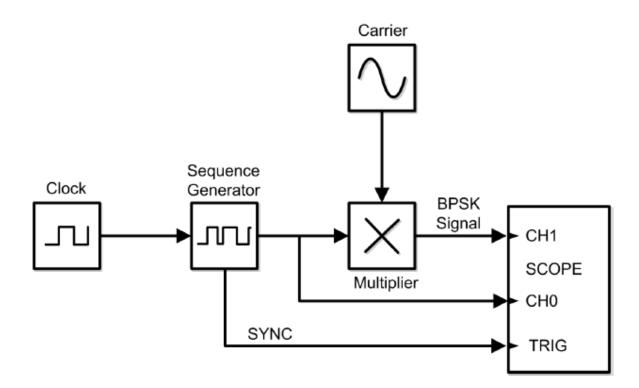


Figure 9.2: Block diagram of BPSK modulator



2.2 Binary Phase Shift Keying Demodulation

Demodulation process for a BPSK signal can be implemented by the following block diagram.

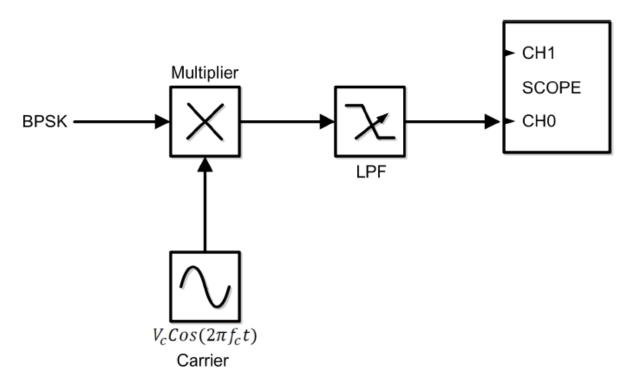


Figure 9.3: BPSK demodulator block diagram

BPSK modulation is a robust technique for distortion of the amplitude.

2.3. Quadrature Phase Shift Keying Modulation

As its name implies, quadrature phase shift keying (QPSK) is a variation of binary phase shift keying (BPSK). Recall that BPSK is basically a DSBSC modulation scheme with digital information for the message. Importantly though, the digital information is sent at a symbol rate of one bit at a time. QPSK is a DSBSC modulation scheme also but it sends has a symbol rate of two bits at a time (without the use of another carrier frequency).

As QPSK sends two bits of data at a time, it's tempting to think that QPSK is twice as fast as BPSK but this is not so. Converting the digital data from a series of individual bits to a series of bit-pairs necessarily halves the data's bit-rate. This cancels the speed advantage of sending two bits at a time.

So why bother with QPSK? Well, halving the data bit rate does have one significant advantage. The amount of the radio-frequency spectrum required to transmit QPSK reliably is half that required for BPSK signals. This in turn makes room for more users on the channel.



At the input to the modulator, the digital data's even bits (that is, bits 0, 2, 4 and so on) are stripped from the data stream by a "bit-splitter" and are multiplied with a carrier to generate a BPSK signal (called I). At the same time, the data's odd bits (that is, bits 1, 3, 5 and so on) are stripped from the data stream and are multiplied with the same carrier to generate a second BPSK signal (called Q). However, the Q signal's carrier is phase-shifted by 90° before being modulated. This is the secret to QPSK operation.

This "even/odd" labelling is somewhat arbitrary however is useful for our purposes of maintaining track of each bit stream.

Modulation process for Quadrature Phase Shift Keying (QPSK) is described in Figure 9.4.

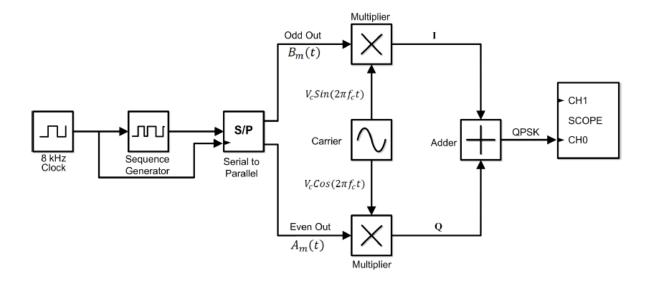


Figure 9.4: QPSK modulator block diagram

2.4. Quadrature Phase Shift Keying Demodulation

The two BPSK signals are then simply added together for transmission and, as they have the same carrier frequency, they occupy the same portion of the radio-frequency spectrum. While this suggests that the two sets of signals would be irretrievably mixed, the required 90° of phase separation between the carriers allows the sidebands to be separated by the receiver using phase discrimination. Figure 9.5 shows the block diagram of the mathematical implementation of QPSK demodulation.

Notice the arrangement uses two product detectors to simultaneously demodulate the two BPSK signals. This simultaneously recovers the pairs of bits in the original data. The two signals are cleaned-up using a comparator or some other signal conditioner then the bits are put back in order using a 2-bit parallel-to-serial converter.



To understand how each detector picks out only one of the BPSK signals and not both of them, recall that the product detection of DSBSC signals is "phase sensitive". That is, recovery of the message is optimal if the transmitted and local carriers are in phase with each another. But the recovered message is attenuated if the two carriers are not exactly in phase. Importantly, if the phase error is 90° the amplitude of the recovered message is zero. In other words, the message is completely rejected.

The QPSK demodulator takes advantage of this fact. Notice that the product detectors in Figure 9.5 share the carrier but one of them is phase shifted 90°. That being the case, once the phase of the local carrier for one of the product detectors matches the phase of the transmission carrier for one of the BPSK signals, there is automatically a 90° phase error between that detector's local carrier and the transmission carrier of the other BPSK signal. So, the detector recovers the data on the BPSK signal that it's matched to and rejects the other BPSK signal.

Demodulation process for a QPSK signal can be implemented by the following block diagram for I and Q signals.

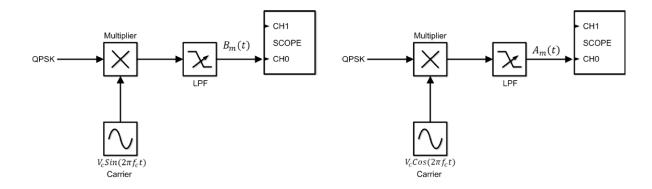


Figure 9.5: QPSK demodulator block diagram



Signal constellations for PSK modulation is given in Figure 9.6. M is the modulation order.

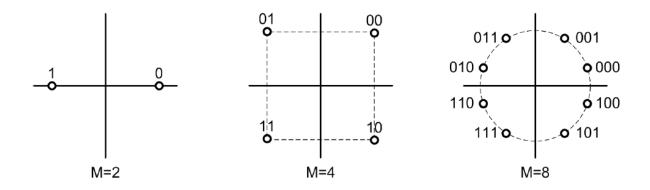


Figure 9.6: Signal constellations of PSK modulation

3. PROCEDURE

3.1. Generating an BPSK signal

 (via USB). Set the control mode of TETRA-BB to PC. Run the TETRA-BB soft front panel (SFP). After selecting the "Exp. 9 - FSK and PSK Modulation & Demodulation" experiment from the menu, TETRA-BB software will provide guidance for the steps of implementing PSK modulation, whose block diagram and the required TETRA-BB connections are shown in Figure 9.7.a. (steps 9-12 in Carefully plug the Emona Communications board into the NI ELVIS III ensuring that it is fully engaged both front and back. Ensure that you have connected the NI ELVIS III to the PC using the USB cable and that the PC is turned on. Turn on the Application Board Power button by pressing it once and confirm that it is illuminated. The LEDs on the board should also be illuminated. If they are not, then switch the unit off 	Red Set	Blue Set
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• Master Signal (Cosinus) = 100kHz.	(SFP). After selecting the "Exp. 9 - FSK and PSK Modulation & Demodulation" experiment from the menu, TETRA-BB software will provide guidance for the steps of implementing PSK modulation, whose block diagram and the required TETRA-BB connections are shown in Figure 9.7.a. (steps 9-12 in	 engaged both front and back. Ensure that you have connected the NI ELVIS III to the PC using the USB cable and that the PC is turned on. Turn on the Application Board <i>Power</i> button by pressing it once and confirm that it is illuminated. The LEDs on the board should also be illuminated. If they are not, then switch the unit off immediately and check for connection or insertion errors. Open the Instrument Launcher software in your browser and select the required instruments. Modify the set-up as shown in figure



Adjust the oscilloscope panel yourself.

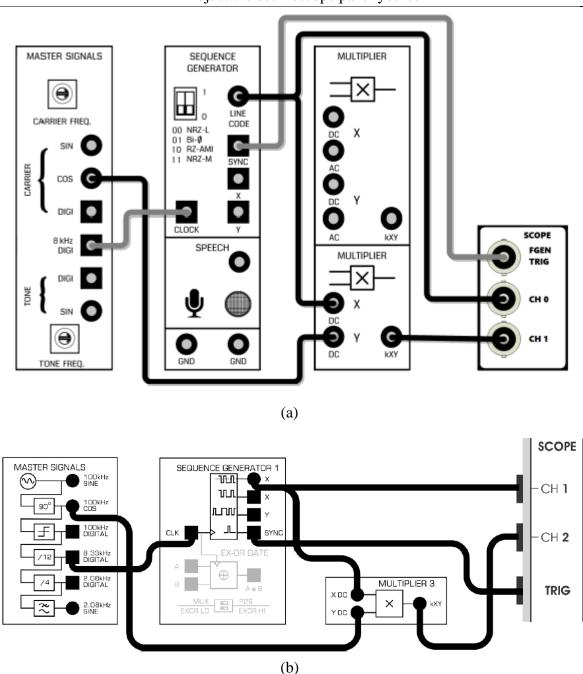


Figure 9.7. Wiring of (a) TETRA-BB (b) EMONAS hardware blocks to generate an BPSK signal.

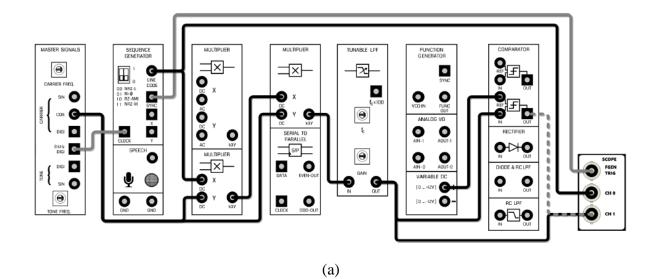
- 1. Measure rate of bits by using oscilloscope (Rb= 1/(Ts)) , ...
- 2. Observe the modulated signal and input signal in time domain ,.....
- 3. Measure the symbol period Ts of the modulated signal by using oscilloscope. Then, calculate the frequency bandwidth B = 1/(2Ts) of the modulated signal \Box .



4. Stop oscilloscope. Switch from oscilloscope to DSA in TETRA-BB SFP (red set) or enable the FFT mode of the Oscilloscope instrument (blue set). Adjust DSA and FFT mode settings as given below. Observe the frequency spectrum of BPSK modulated signal.

3.2. Demodulating an BPSK Signal

Red Set	Blue Set
• Select the "Exp. 9 - FSK and PSK	Modify the set-up as shown in figure
Modulation & Demodulation" experiment from the menu, TETRA-BB software will provide guidance for the steps of implementing demodulation of a PSK signal, whose block diagram and the required TETRA-BB connections are shown in Figure 9.8.a (steps 13-19 in the TETRA-BB SFP)	9.8.b.
Master Signal (Cosinus) = 100kHz.	
Adjust the oscilloscope panel yourself.	





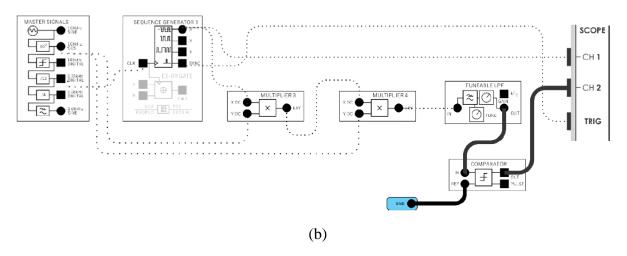


Figure 9.8. Wiring of (a) TETRA-BB (b) EMONAS hardware blocks to demodulate an BPSK signal.

- 5. Observe input and output ports of the tunable low pass filter. Adjust cutoff frequency and gain of the low pass filter.

3.3. Generating an QPSK signal

Red Set

- Please turn on the power of TETRA-BB and ELVIS platform. Then, connect the ELVIS platform to PC (via USB).
- Set the control mode of TETRA-BB to PC.
- Run the TETRA-BB soft front panel (SFP). After selecting the "Exp. 9 FSK and PSK Modulation & Demodulation" experiment from the menu, TETRA-BB software will provide guidance for the steps of implementing QPSK modulation, whose block diagram and the required TETRA-BB connections are shown in Figure 9.9.a (steps 20-29 in the TETRA-BB SFP).

Blue Set

- Ensure that the NI ELVIS III Application Board power button at the top left corner of the unit is OFF (not illuminated).
- Carefully plug the Emona Communications board into the NI ELVIS III ensuring that it is fully engaged both front and back.
- Ensure that you have connected the NI ELVIS III to the PC using the USB cable and that the PC is turned on.
- Turn on the Application Board *Power* button by pressing it once and confirm that it is illuminated. The LEDs on the board should also be illuminated. If they are not, then switch the unit off immediately and check for connection or insertion errors.



- Open the Instrument Launcher software in your browser and select the required instruments.
- Modify the set-up as shown in figure 9.9.b.
- Master Signal (Cosinus and Sinus) = 100 kHz.
 - Digital Signal = 2 kHz.
 - Adjust the oscilloscope panel yourself.

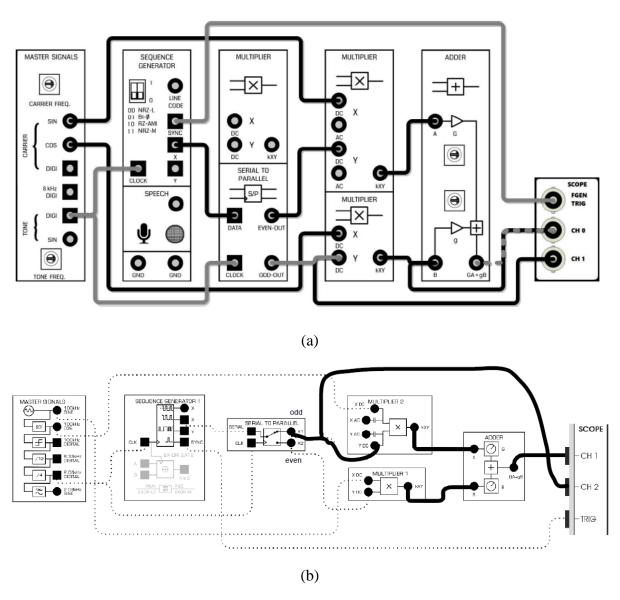


Figure 9.9. Wiring of (a) TETRA-BB (b) EMONAS hardware blocks to generate an QPSK signal.

7. Set adder gain parameters to 1. Carrier frequency is 100 kHz. Measure bit rate using oscilloscope , . .



- 9. Measure the symbol period Ts of the modulated signal by using oscilloscope. Then, calculate the frequency bandwidth B = 1/(2Ts) of the modulated signal
- 10. Stop the oscilloscope. Switch from oscillator to DSA in TETRA-BB SFP to observe frequency spectrum. Observe the frequency bandwidth by using DSA (red set) or FFT Mode (blue set). Draw the frequency spectrum of the modulated signal

3.4. Demodulating an QPSK signal

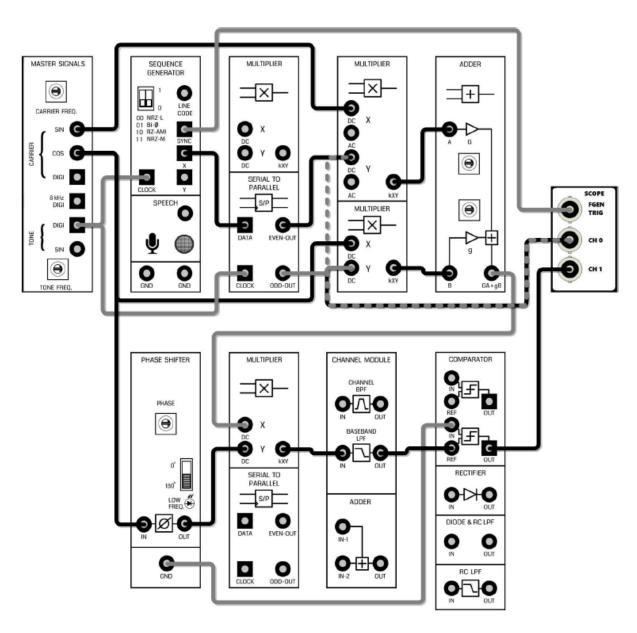
Red Set Please turn on the power of TETRA-BB and ELVIS platform. Then, connect the ELVIS platform to PC (via USB).

- Set the control mode of TETRA-BB to PC.
- Run the TETRA-BB soft front panel (SFP). After selecting the "Exp. 9 -**FSK** and PSK Modulation Demodulation" experiment from the menu, TETRA-BB software will provide guidance for the steps of implementing demodulation of a OPSK signal, whose block diagram and the required **TETRA-BB** connections are shown in Figure 9.10.a (steps 30-37 in the TETRA-BB SFP).

Blue Set

- Ensure that the NI ELVIS III Application Board power button at the top left corner of the unit is OFF (not illuminated).
- Carefully plug the Emona Communications board into the NI ELVIS III ensuring that it is fully engaged both front and back.
- Ensure that you have connected the NI ELVIS III to the PC using the USB cable and that the PC is turned on.
- Turn on the Application Board *Power* button by pressing it once and confirm that it is illuminated. The LEDs on the board should also be illuminated. If they are not, then switch the unit off immediately and check for connection or insertion errors.
- Open the Instrument Launcher software in your browser and select the required instruments.
- Modify the set-up as shown in figure 9.10.b.
- Master Signal (Cosinus and Sinus) = 100 kHz.
 - Digital Signal = 2 kHz.
 - Adjust the oscilloscope panel yourself.





(a)



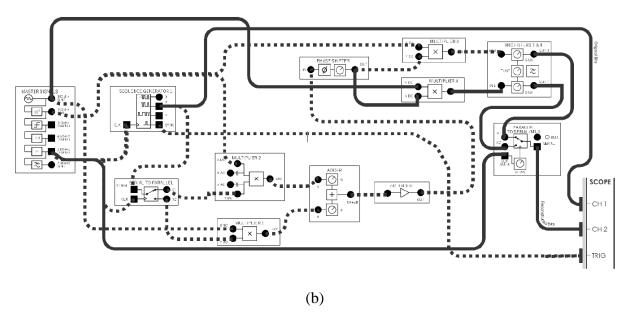


Figure 9.10. Wiring of (a) TETRA-BB (b) EMONAS hardware blocks to demodulate an QPSK signal.

Blue Set (only)

- Modify the set-up as shown in Figure 9.10.b.
- Note: The Parallel to Serial module **X1 and X2 inputs** should be <u>approximately equal</u> at approximately 4Vpp each. We will now <u>balance the inputs by turning the GAIN knobs on the RRC FILTER 3 and RRC FILTER 4 modules</u>.
- Plug Scope <u>CH 1</u> into the <u>Parallel to Serial module **X1 input**</u>. Change the Scope Time per division setting to <u>20ms</u>.
- With the Scope running, examine the Scope <u>Volts peak peak</u> measurement for <u>Channel 1</u>. Starting with the <u>RRC FILTER 3</u> module <u>GAIN knob turned fully counterclockwise</u>, <u>slowly turn</u> the RRC FILTER 3 module <u>GAIN knob clockwise until the Scope Volts peak peak measurement is approximately **4.0V**.</u>
- Plug Scope <u>CH 1</u> into the <u>Parallel to Serial module **X2 input**.</u> With the Scope running, examine the <u>Scope Volts peak peak</u> measurement for <u>Channel 1</u>. Starting with the <u>RRC FILTER 4</u> module <u>GAIN knob turned fully counterclockwise</u>, <u>slowly turn</u> the RRC FILTER 4 module <u>GAIN knob clockwise until the Scope Volts peak peak</u> measurement is approximately **4.0V**.
- <u>Plug Scope CH 1</u> into the <u>Sequence Generator 1</u> module <u>Unipolar X output</u>. Plug Scope CH 2 into the Parallel to Serial module SERIAL output.
- Turn the Parallel to Serial module ALIGN knob fully counterclockwise.



Red Set (only)

- Modify the set-up as shown in Figure 9.10.a.
- Set input signal frequency in the phase shifter block. Adjust the phase shifter to regenerate odd bits. Observe I signal and demodulated signal using oscilloscope ,