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EXPERIMENT 5

MOSFET Measurement and Applications

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1.Device Parameters

Throughout the experiments, we will be using a 4007 MOS array package whose layout is shown in Figure 1. Note that the substrate connections (reached via #7 and #14) are distributed to each respective transistor – p type substrate to NMOS and n type substrate to PMOS transistors. Also note that one NMOS and one PMOS transistor come with their substrate readily connected to their sources. Throughout the measurements, ensure substrate pins are connected to respective DC voltages at all times.

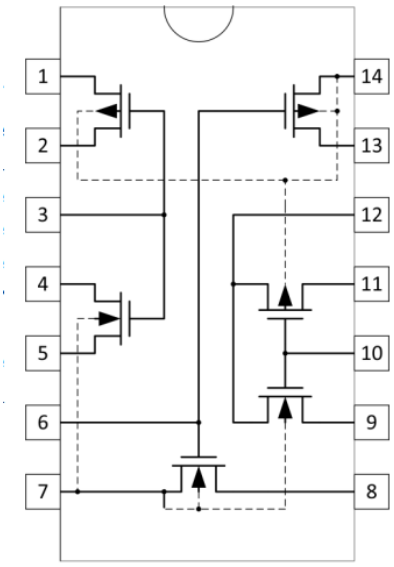
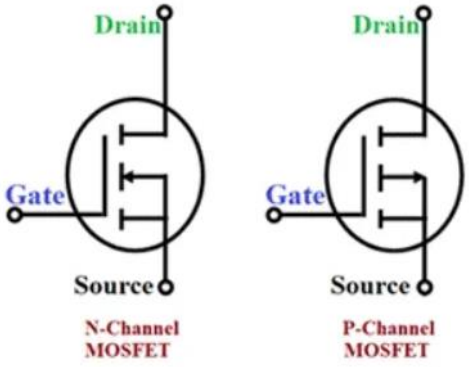


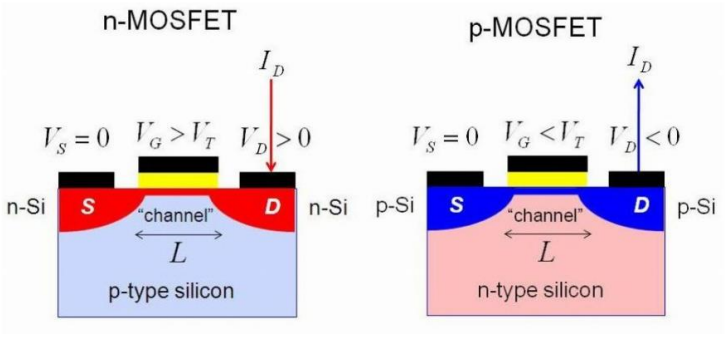
Figure 1: Layout of 4007 MOS array.

Theoretical Research

The word MOSFET stands for Metal Oxide Semi-conductor Field Effect Transistor and it means metal oxide semiconductor field effect transistor, an improved variant of field effect transistors (FET). MOSFETs also have 3 legs. These legs are called gate, drain and source.

According to the materials used in the mosfet channel areas, there are two types as N type mosfet and P type mosfet. According to the way of working, mosfets; There are two types as enhancement mosfets and depletion (depletion - reducing channels) mosfets. The structures of n-channel and p-channel mosfets are shown below.





Types of Mosfets

Deplation mosfets are normally "ON" type mosfets, that is, when the voltage applied to the gate terminal is 0 V, there is some current flow between the S and D terminals. This amount of current increases as the voltage applied from the gate leg of the mosfet increases in the positive direction. As the voltage applied to the gate leg of the mosfet increases in the negative direction, the amount of current passing between the S and D terminals decreases.

Enhancement mosfets are mosfets that are normally in the "OFF" state, as opposed to attenuating channel mosfets. As long as no voltage is applied to the G terminal of the enhancement mosfets, no current flows between the D and S terminals.

Modes of operation

For an *enhancement-mode, n-channel MOSFET*, the three operational modes are:

Cutoff, subthreshold, and weak-inversion mode (n-channel MOSFET)

When $V_{GS} < V_{th}$:
where V_{GS} is gate-to-source bias and V_{TH} is the threshold voltage of the device.

Triode mode or linear region, also known as the ohmic mode[96][97] (n-channel MOSFET)

When $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$:

The transistor is turned on, and a channel has been created which allows current between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{{V_{DS}}^2}{2} \right] (1 + \lambda V_{DS})$$

where μn is the charge-carrier effective mobility,W is the gate width,L is the gate length and Cox is the gate oxide capacitance per unit area. The transition from the exponential subthreshold region to the triode region is not as sharp as the equations suggest.

Saturation or active mode[98][99] (n-channel MOSFET)

When $V_{GS} > V_{th}$ and $V_{DS} \geq (V_{GS} - V_{th})$:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} [V_{GS} - V_{th}]^2 [1 + \lambda (V_{DS} - V_{DSsat})] .$$

To be more clear;

p-MOSFET(D):: (I-V) Equations

Cut off Mode	**Drain current**	$i_D = 0$
	Gate to Source Voltage	$V_{GS} > V_{TP}$
	Gate to drain Voltage	(.)
Linear Mode	**Linear Drain current ($\|V_{DS}\| < 1V$)**	$i_D \cong k_p \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{TP}) V_{DS}$
	Triode Drain current	$i_D = k_p \left(\frac{W}{L}\right) \cdot \left[(V_{GS} - V_{TP}) V_{DS} - V_{DS}^2/2\right]$
	Gate to Source Voltage	$V_{GS} < V_{TN}$
	Gate to drain Voltage	$V_{GD} < V_{TN}$
Saturation Mode	**Drain current**	$i_D = \frac{1}{2} k_p \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{TP})^2$
	Drain current with λ	$i_D = \frac{1}{2} k_p \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{TP})^2 \cdot (1 + \lambda \cdot V_{DS})$
	Gate to Source Voltage	$V_{GS} < V_{TP}$
	Gate to drain Voltage	$V_{GD} > V_{TP}$
Linear/Saturation Boundary	**Drain to Source Voltage**	$V_{DS} = V_{GS} - V_{TP}$

p-MOSFET(D):: Parameters

Process parameter [A/V^2]	$k_p = \mu_p C_{ox}$
Current Gain	$\beta_p = k_p \cdot \left(\frac{W}{L}\right)$
Early Voltage	$\lambda = \frac{1}{V_A}$
Body Effect Parameter	$\gamma = -\sqrt{2qN_d}\,/\,C_{ox}$
Oxide Capacitance	$C_{ox} = \frac{K_{ox}\,\epsilon_o}{t_{ox}}$
Threshold Voltage	$V_{TP} = V_{TO} + \gamma\left(\sqrt{2\phi_f + \lvert V_{SB}\rvert} - \sqrt{2\phi_f}\right)$
Zero Potential Current ($V_{GS} = 0$)	$I_{DSS} \equiv \frac{\beta_p}{2}\lvert V_{TP}\rvert^2$
Depletion p-MOSFET Threshold	$V_{TP} > 0$

Cut Off	$V_{SG} \le \lvert V_T\rvert$	$I_{SD} = 0$
Linear	$V_{SG} > \lvert V_T\rvert,\ V_{SD} \le V_{SG} - \lvert V_T\rvert$	$I_{SD} = \mu_p C_{ox} \frac{W}{L}\left[(V_{SG} - \lvert V_T\rvert)V_{SD} - \frac{V_{SD}^2}{2}\right](1 + \lambda V_{SD})$
Saturation	$V_{SG} > \lvert V_T\rvert,\ V_{SD} > V_{SG} - \lvert V_T\rvert$	$I_{SD} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(V_{SG} - \lvert V_T\rvert)^2(1 + \lambda V_{SD})$

1.1 Measuring Device Thresholds:

Question :

a) Selecting pin #1 as source terminal (a PMOS device), assemble the circuit shown in Figure 2. Ensure both substrate pins are connected. Use 10 V as supply. Measure the voltage from A to ground (VA). Estimate Vtp.

b) Repeat the measurement with drain and source interchanged: Use pin #2 as source terminal.

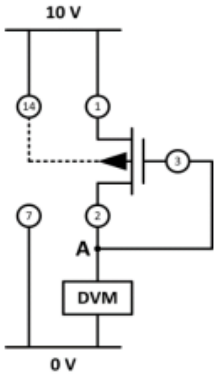


Figure 2: Setup to measure

c) Start with the configuration in Figure 2. Shunt node A to ground with a 1 kΩ resistor (note down its exact value). Break the gate-drain connection and connect the gate to an adjustable voltage source. Carefully and slowly adjust the gate voltage so that the VSG is swept through the values given in the table below. Note VA and calculate ID. Estimate Vtp as the voltage allowing a ID > 10 µA for this technology.

Considering the conditions required in the question, the circuit was established and measurements were made during the experiment. These measurements are listed in the table below.

Table 1. DC voltage measurements and threshold voltage estimations of single transistor.

Pin # as Source	V_A	V_{tp}
#1 (a)	9,52V	0,148 V
#2 (b)	9,55	0,145 V

First of all, Pin1 and 10V were connected and Va value was measured. Then, for option b, pin2 and 10V are connected. During this process, the connection between pin2 and pin3 is disconnected, a connection is established between pin3 and pin1 and Va is measured again. Va values are written in the desired places in the table above. Vth value is calculated as 10V-Va.

As a result, it has been understood that the same results will be obtained with different pins. The reason for the small errors in between is due to the non-ideal experimental environment.

Table 2. DC voltage measurements, current calculations and threshold voltage estimations with different source-to-gate voltages.

V_{SG} (V)	0.0	0.2	0.4	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	V_{tp}
V_A	0,04 mV	0,03 mV	0,02 mV	0,02 mV	0,01 mV	0,51 mV	5mV	81 mV	146 mV	0,36 V	0,48 V	0,7 V	1,02 V	
I_D	0,04 mA	0,03 mA	0,02 mA	0,01 mA	0,01 mA	0,51 mA	5 mA	0,181 mA	146 mA	0,36 mA	0,48 mA	0,7 mA	1,02 mA	1,8 mA

For option c, a 1kohm resistor is installed in parallel to node A. The gate-drain connection (pin1/2-pin3) is disconnected and an adjustable voltage source is attached to the gate. The desired VSG values are given in the table. For example, for 0.2V Vsg value in the table, it is necessary to set the gate voltage as 9.8V.

Connections and measurements were made taking these into account. It is seen in the table that the Vsg value increases with a greater acceleration after exceeding 1.8V. And at this point the Id value is greater than 10 µA as requested in the question. So Vtp can be considered as 1.8 V. It has exited saturation mode in this range.

1.2 Measuring Device Conductivity (Transconductance) Parameter, kp:

Question :

Continue using the configuration in Figure 2. Ensure both substrate pin connections remain intact.

a) Measure and note VA for pin #1.

b) Shunt the node A to ground with a resistor RD (around 10 kΩ or lower) so that VA drops by a fixed amount, such as 1 V. You can use a potentiometer or a resistor box to do the resistance adjustment. Measure VA and the resistance you applied for each case. Using the parameters at hand and the Vtp you estimated in part 1.1

c), calculate the transconductance parameter kp = μpCox(W/L) for each case. Do not forget to consider the transistor operation region while doing your calculations. c) Repeat with pins #11 and #14 used as source terminals.

Table 3. DC voltage measurements, current calculations and threshold voltage estimations for p-channel device

Pin # as source	#1	#11	#14
V_A (when open)	9,54V	9,52	9,51
V_A (shunted by R_D)	7,47V	7,5V	7,52V
R_D (manually set)	10kΩ	10kΩ	10kΩ
$k_p = \mu_p C_{ox}(W/L)$ (calculated)	15,5	15,3	15,2

First of all, it is connected to Va pin1 as desired in option A. Then, point A was connected to ground by a 10kohm resistor and Va value was measured again. And then the Kp value was calculated over the formula given in the theoretical calculation part and written in the desired place in the table. The same operations are done for pin11 and pin14. It has been observed that there are small errors between them.

1.3 Measuring n Channel Device Parameters:

Question :

Selecting pin #4 as source terminal (an NMOS device), assemble the circuit shown in Figure 3.

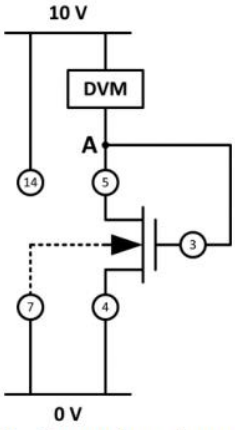


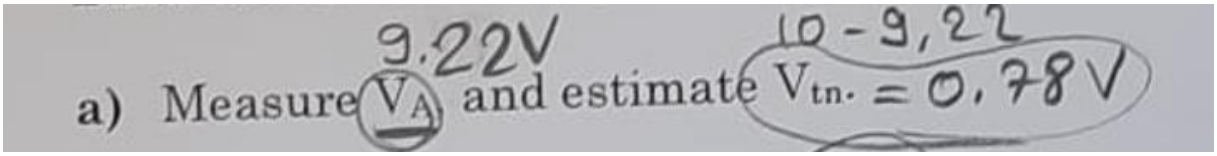
Figure 3: Setup to measure V_{tn}. Pin numbers given are in accordance with part a).

Ensure both substrate pin connections remain intact.

a)Measure VA, and estimate Vtn.

b) Shunt node A to VDD with a 1 kΩ resistor (note down its exact value). Break the gate-drain connection and connect the gate to an adjustable voltage source. Adjust the gate voltage so that the VGS is swept through the values given in the table below. Note VA and calculate ID. Estimate Vtn as the voltage allowing a ID > 10 μA for this technology.

c) Return to configuration in Figure 3. Shunt node A by a resistor 1 kΩ. Use a similar resistance adjustment method as you did in 1.2. Measure VA and the resistance you applied. Calculate kn using a way similar to the one you used to calculate kp.



In part a of the question, the desired Va voltage was measured and found as given in the figure. The treshold voltage was obtained by subtracting it from the source voltage, 10 V.

Table 4. DC voltage measurements, current calculations and threshold voltage estimations with different gate-to-source voltages.

V_{GS} (V)	0.0	0.2	0.4	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	V_{tn}
V_A	0.01 mV	0.01 mV	0.02 mV	0.03 mV	0.05 mV	0.12 mV	1.52 mV	8.02 mV	68 mV	191.8 mV	290 mV	0.56 V	0.76 V	61 mV
I_D	0,01 nA	0,01 nA	0,02 nA	0,03 nA	0,05 µA	0,12 µA	1,52 µA	8,2 µA	68 µA	191,8 µA	290 µA	0,56 mA	0,76 mA	68 µA

For option b, a 1kohm resistor is installed in parallel to node A. The gate-drain connection (pin5-pin3) is disconnected and an adjustable voltage source is attached to the gate. The desired VGS values are given in the table.

Connections and measurements were made taking these into account. It is seen in the table that the Vsg value increases with a greater acceleration after exceeding 1.2V. And at this point the Id value is greater than 10 µA as requested in the question. The Threshold voltage was found to be 61 mV.

Table 5. DC voltage measurements, current calculations and threshold voltage estimations for n-channel device

Pin # as source	V_A (open)	V_{tn} (calculated)	V_A (shunted)	R_D	I_D	$k_n = \mu_n C_{ox}(W/L)$
4	9,22V	0,76V	2,15V	1kΩ		

First of all, it is connected to Va pin4 as desired in option A. Then, point A was connected to ground by a 1kohm resistor and Va value was measured again. And then the Kn value was calculated over the formula given in the theoretical calculation part and written in the desired place in the table.