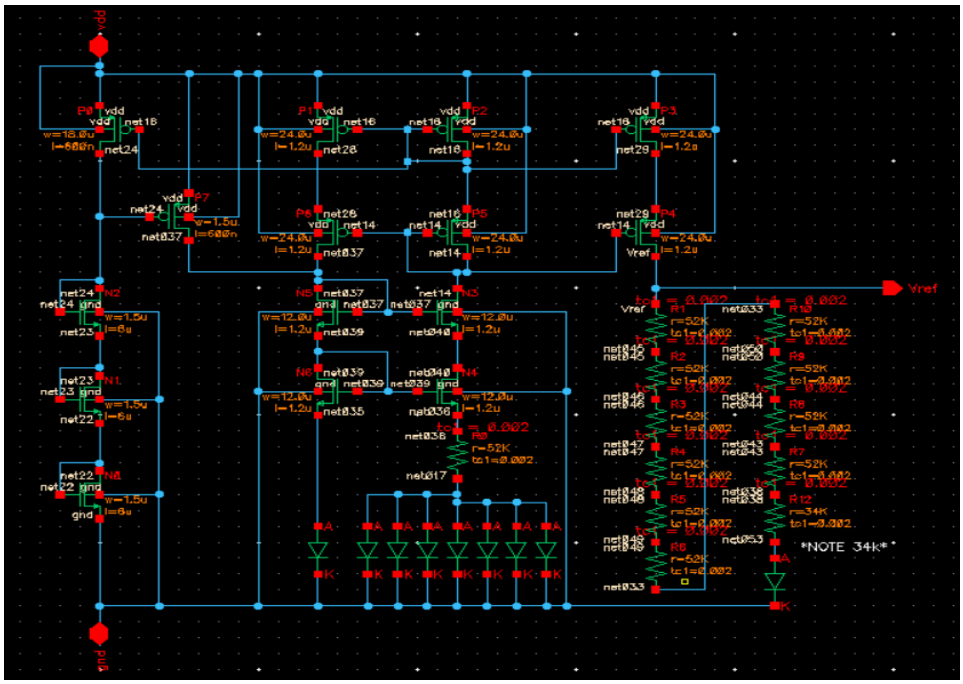
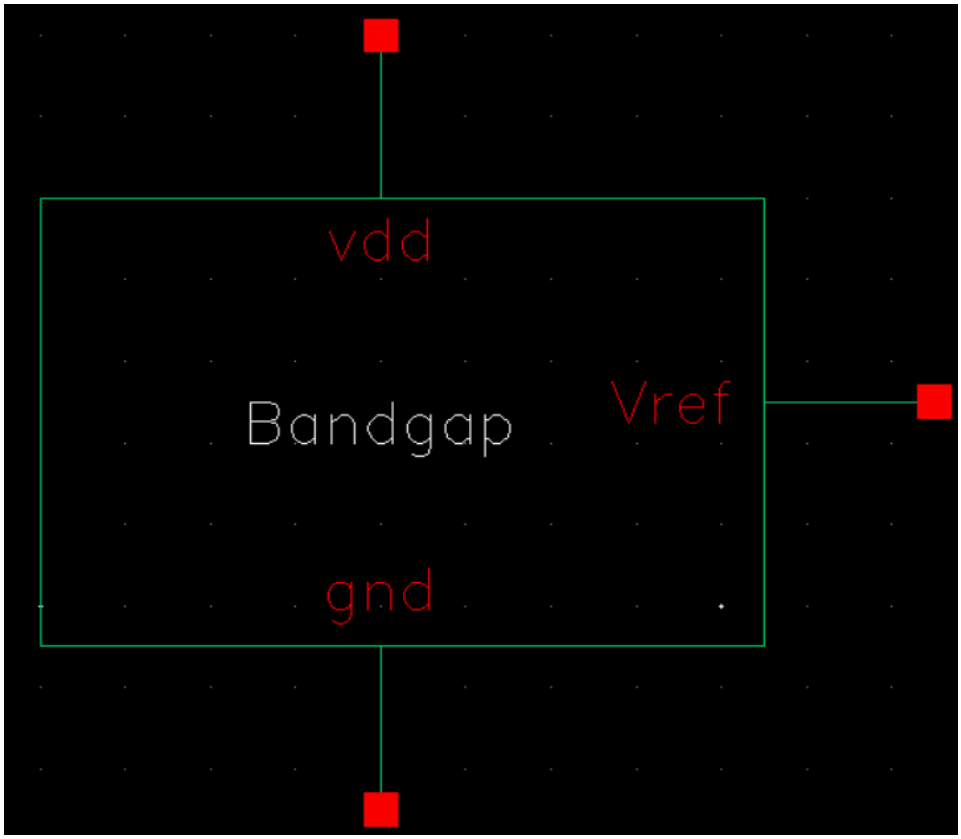
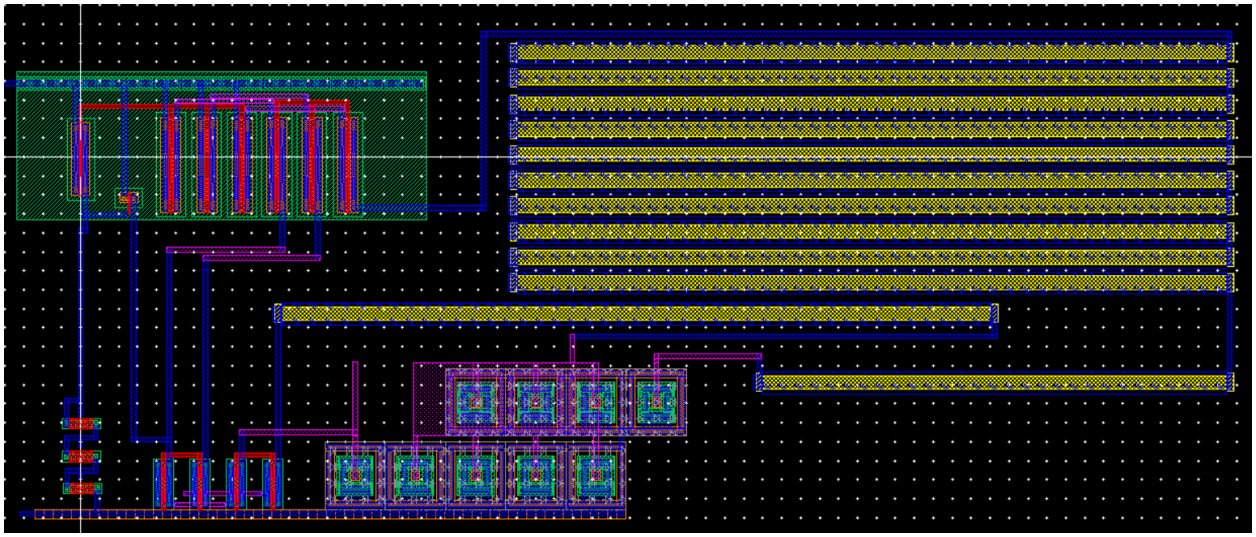
1. **Bandgap**

Schematic and symbol

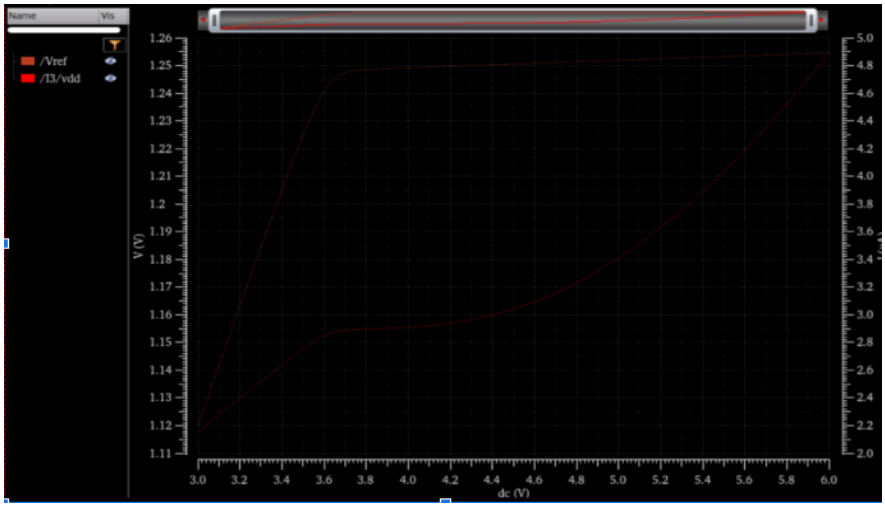




Layout

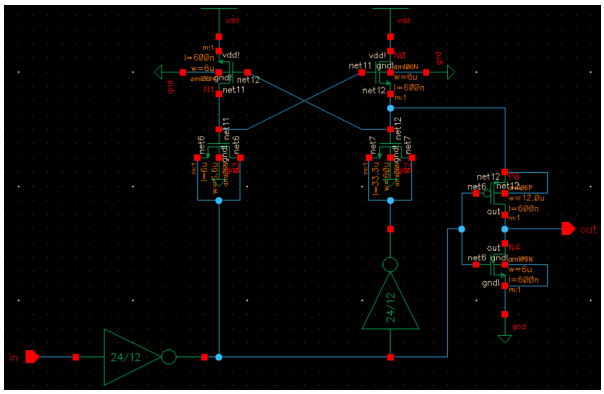


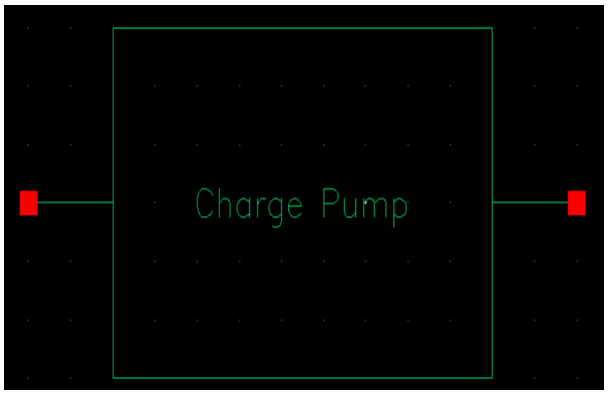
The bandgap is designed to generate a stable reference voltage (Vref) independent of temperature, supply voltage, and process variations. It utilizes the fundamental bandgap property of silicon (~1.1 eV) to create a voltage that remains consistent across operating conditions. The diodes at the bottom exploit the temperature-dependent forward voltage drop (CTAT characteristic), while other circuit elements, such as resistors and transistors, generate a proportional-to-absolute-temperature (PTAT) voltage. By carefully combining these CTAT and PTAT components, the circuit achieves temperature compensation, resulting in a stable Vref, typically around 1.2V for silicon. The resistor network scales currents and voltages to balance the contributions, while the transistors (likely part of current mirrors and amplifiers) ensure proper biasing and functionality. The simulation results below show that the lowest the power supply can go before the output voltage drops is 3.6 volts. This specific design pulls a 2.6 uA current that increases as the power supply increases.



2. Charge Pump

Schematic and Symbol





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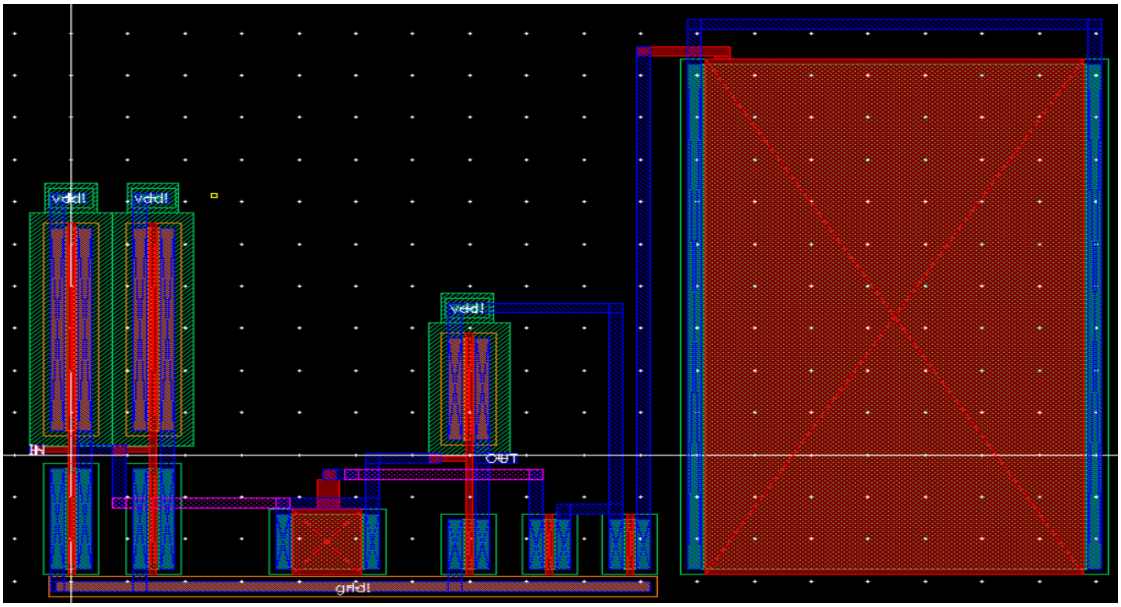
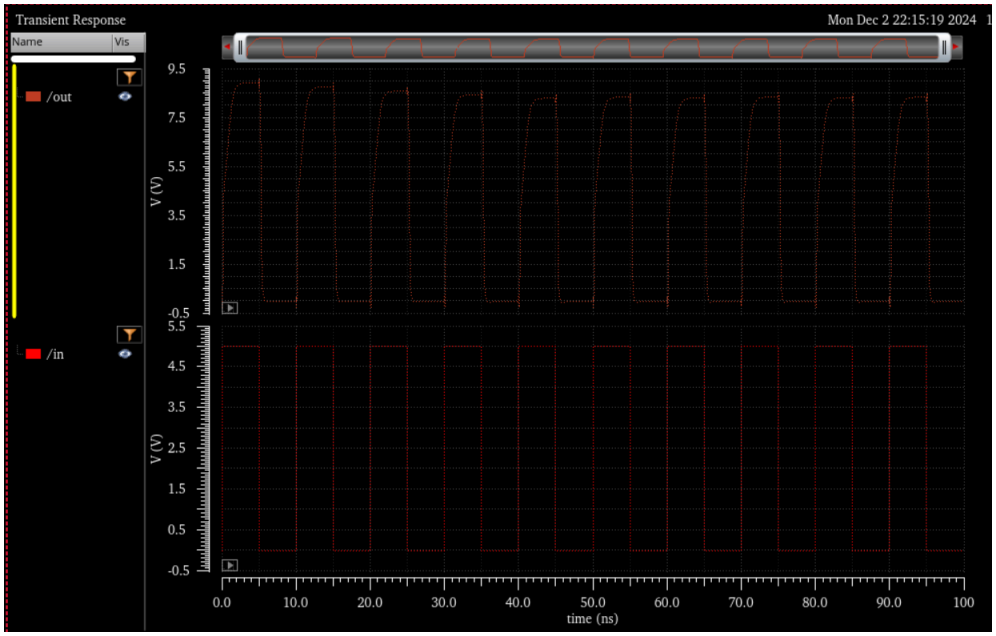


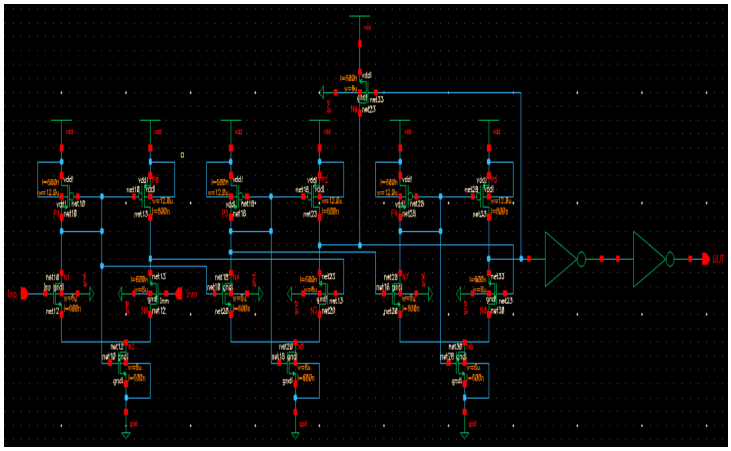
The created charge pump is a DC-DC converter that uses capacitors as energy storage elements and switches, often implemented with MOSFETs, to transfer and multiply charge to generate higher, lower, or inverted voltage levels. In the provided schematic, the circuit appears to be a cross-coupled charge pump, where pairs of MOSFETs alternate the charging and discharging phases of capacitors. The cross-coupled configuration ensures complementary operation of the switches, driven by an input clock or signal, to efficiently transfer charge. The capacitors store and redistribute energy, allowing the circuit to produce a boosted, inverted, or regulated voltage at the output. This design is commonly used in applications requiring compact, low-power solutions for generating specific voltage levels, such as powering small devices or creating negative supply voltages.

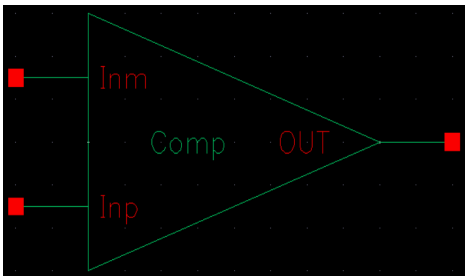


This is the simulation of the charge pump with a pulse of 0V to 5V. Shown the out climbs and peaks at around 9 volts while following the oscillations of the input voltage in.

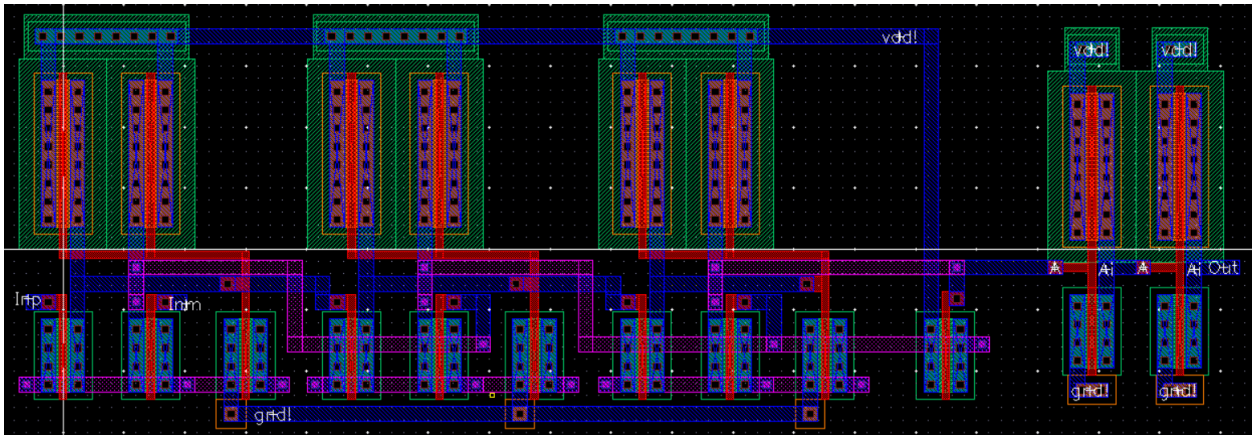
3. Comparator

Schematic and symbol



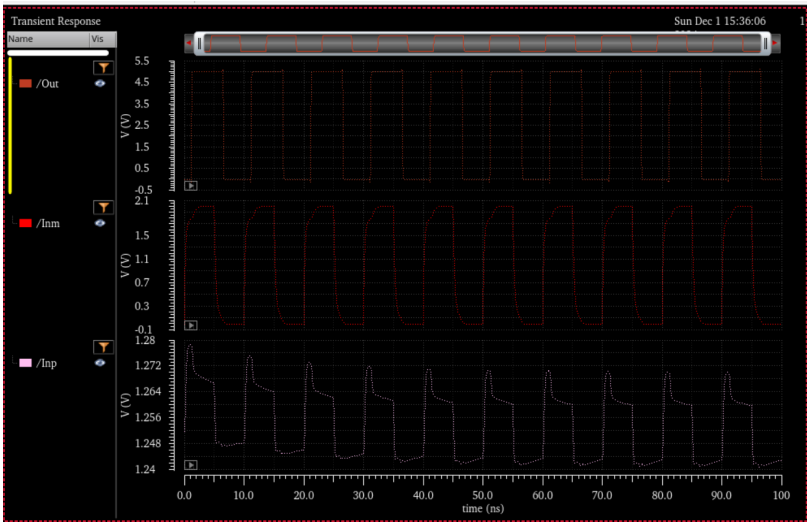


Layout



In digital integrated circuit design, a **comparator** is a circuit that compares two input voltages (or currents) and outputs a digital signal indicating which input is larger. It is commonly used in applications like analog-to-digital converters (ADCs), signal processing, and clock signal generation.

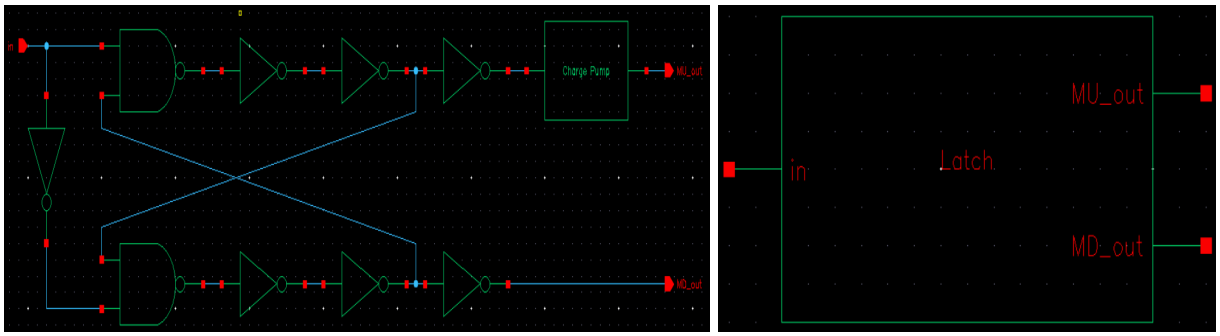
Referring to the provided schematic, which features cascaded stages of logic and switching elements, the circuit likely incorporates comparator functionality. The inverters near the output suggest that the circuit is conditioning or amplifying signals to produce a clean digital output. In this design, the comparison between **Inp** comes from a RC circuit (voltage divider with a decoupling capacitor) that provides a voltage of 3.125V into the comparator, with the **Inm** which comes from the bandgap output which is 1.25V.



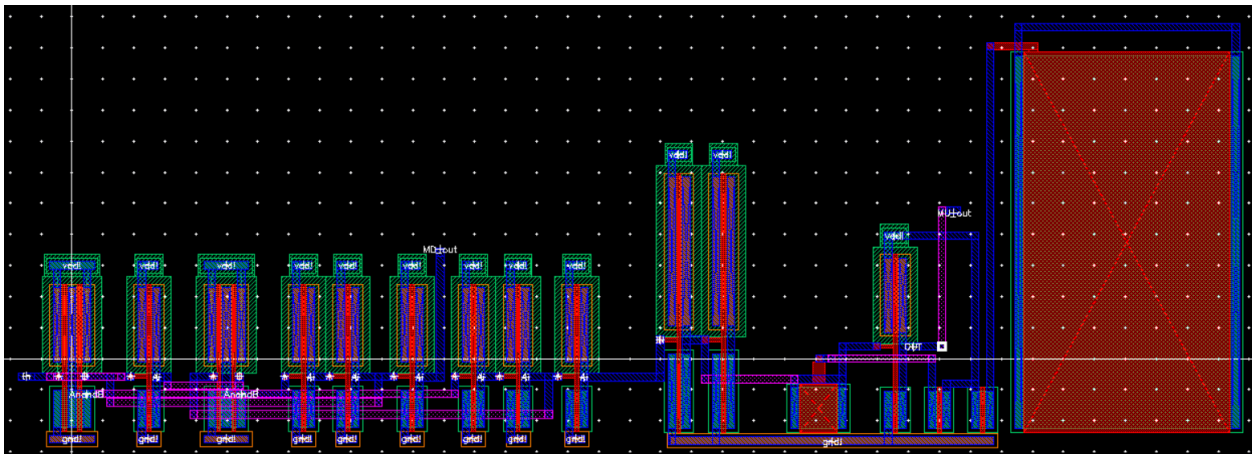
Disclaimer: the sim shown below did not have the decoupling capacitor to smooth out Inp, but in the final schematic it did. However, shown is that the output of the comparator is a smooth and consistent voltage.

4. Latch

Schematic and symbol



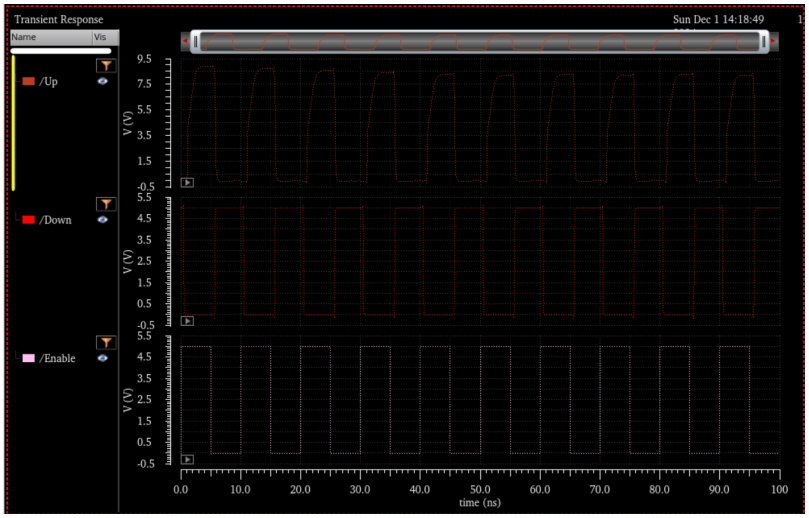
Layout



In digital integrated circuit design, a latch is a fundamental memory element used to store a single bit of data. It is level-sensitive, meaning it can capture and hold data as long as the enable signal is active. Latches are commonly used for temporary data storage, signal synchronization, and maintaining state in digital systems.

Referring back to the provided schematic, the circuit includes feedback loops and interconnected logic gates, which may implement latching behavior. The combination of NAND gates and inverters, along with the feedback paths, suggests that the circuit could temporarily store or stabilize signals. These latches likely help ensure synchronized and stable outputs MU_out and MD_out, which are critical for driving the charge pump module.

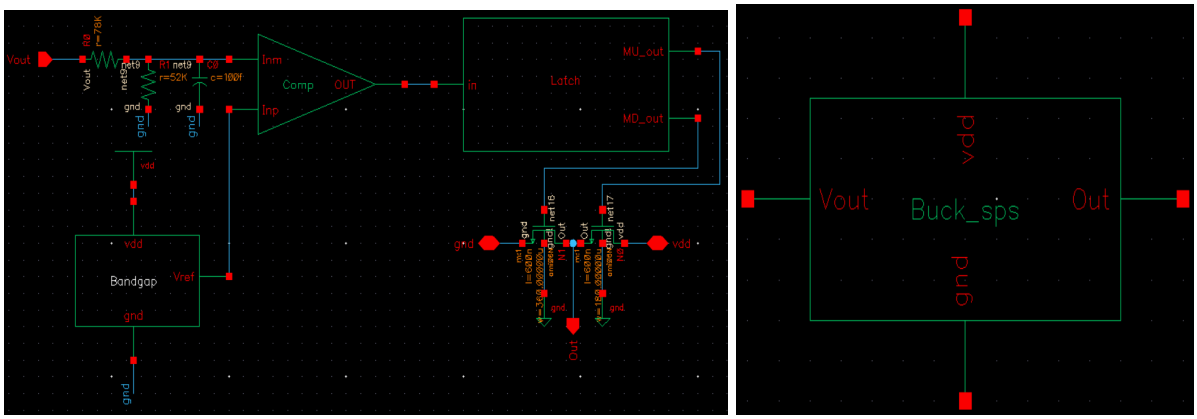
Here the latches serve as intermediate storage elements or as part of the control logic to manage the sequencing of signals. This functionality is essential for systems like charge pumps, oscillators, or state machines, where accurate timing and reliable state retention are crucial for correct operation.



The simulation results show that when the Enable is high, the Up signal is high and the Down signal is low. When the enable signal is high, the NAND gates and cross-coupled feedback ensure complementary operation by driving MU_out high and MD_out low. This behavior occurs because the logic configuration prevents both outputs from being high simultaneously, maintaining proper functionality for downstream components like the charge pump.

5. Buck Converter

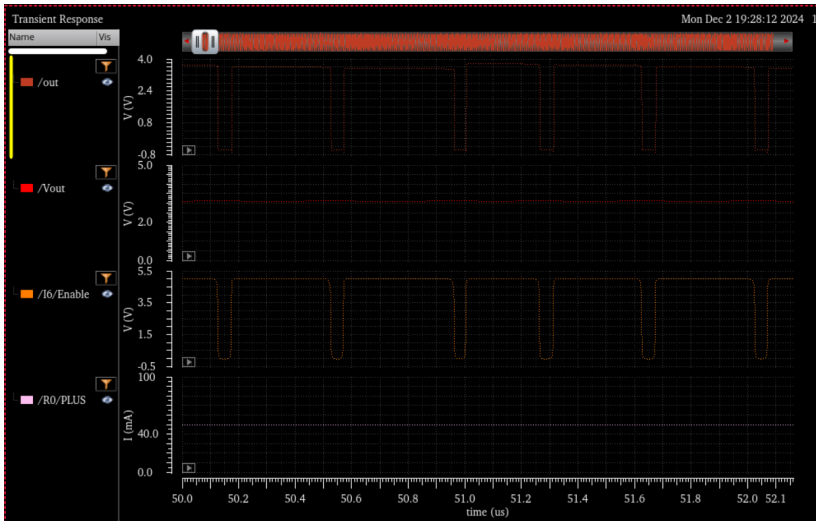
Schematic and symbol



Layout

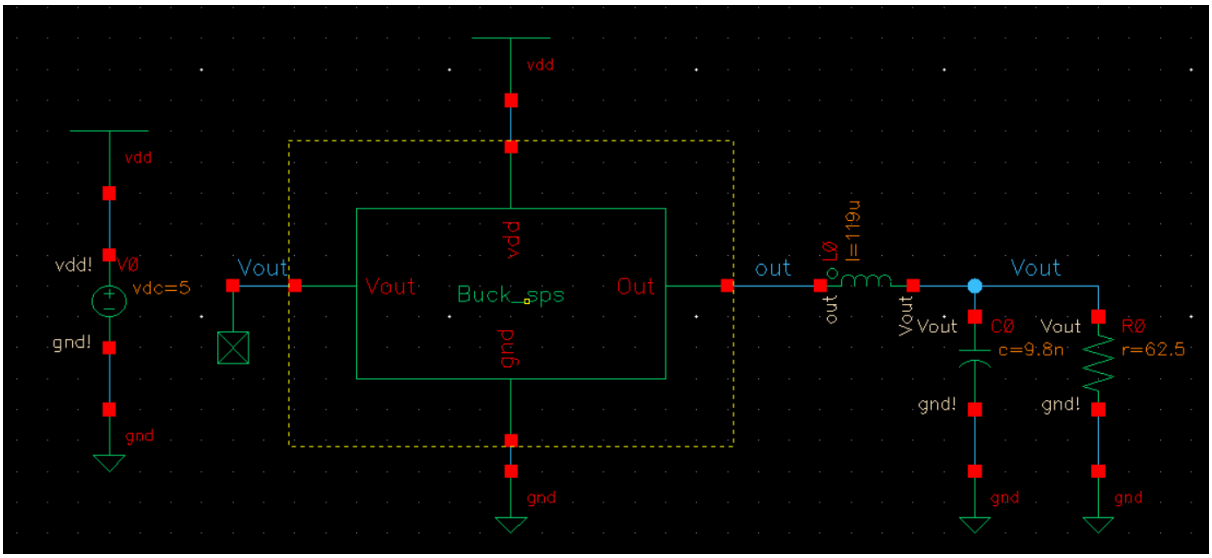
A buck converter is a type of DC-DC switching regulator used in digital integrated circuit design to step down a higher input voltage to a lower output voltage efficiently. It operates by rapidly switching a transistor (typically a MOSFET) on and off at high frequencies, controlling the flow of current through an inductor. During the on phase, energy is stored in the magnetic field of the inductor, and when the switch turns off, the energy is released and delivered to the load. To smooth out the fluctuations in the output voltage caused by the switching action, a capacitor is used at the output. This results in a relatively stable, lower voltage supply with reduced power loss compared to linear regulators, making it ideal for powering digital circuits that require lower voltages from higher-voltage sources. The efficiency of the buck

converter depends on the switching frequency, the inductor, and the quality of the capacitors used, but it can typically achieve efficiencies of 80-90% or higher, making it highly effective for energy-saving applications.



The simulation above shows the working buck converter. The out follows the enable which is the input of the latch/ output of the comparator. Vout is the stepped down voltage that is being regulated and oscillating at around 3.1V to 3.17V. Alongside that, it also shows that there is a constant current output that oscillates between 49.7mA to 50.1mA. This ensures that the buck converter is properly stepping down the input voltage while maintaining a constant, stable current.

Simulation Circuit



The math done to figure out the LRC circuit is as follows:

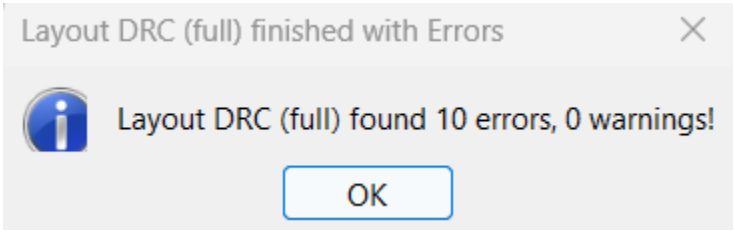
$$V_{OUT} = D * V \qquad D = V_{OUT} / V_S = 3.125V / 5V = 0.625$$

$$L = V_{OUT} * (1 - D) / \Delta i_L * f) = 5V * (1 - 0.625) / (5mA * 2MHz) = 119\ uH$$

$$C = 9.8nF$$

$$R = V_{OUT} / I = 3.125V / 50mA = 62.5\Omega$$

Final DRC



The final DRC came out to only be 10 errors, all having to do with spacing of components.