Lecture 8

8086 CPU Specifications, Operating Modes, Bus Interface

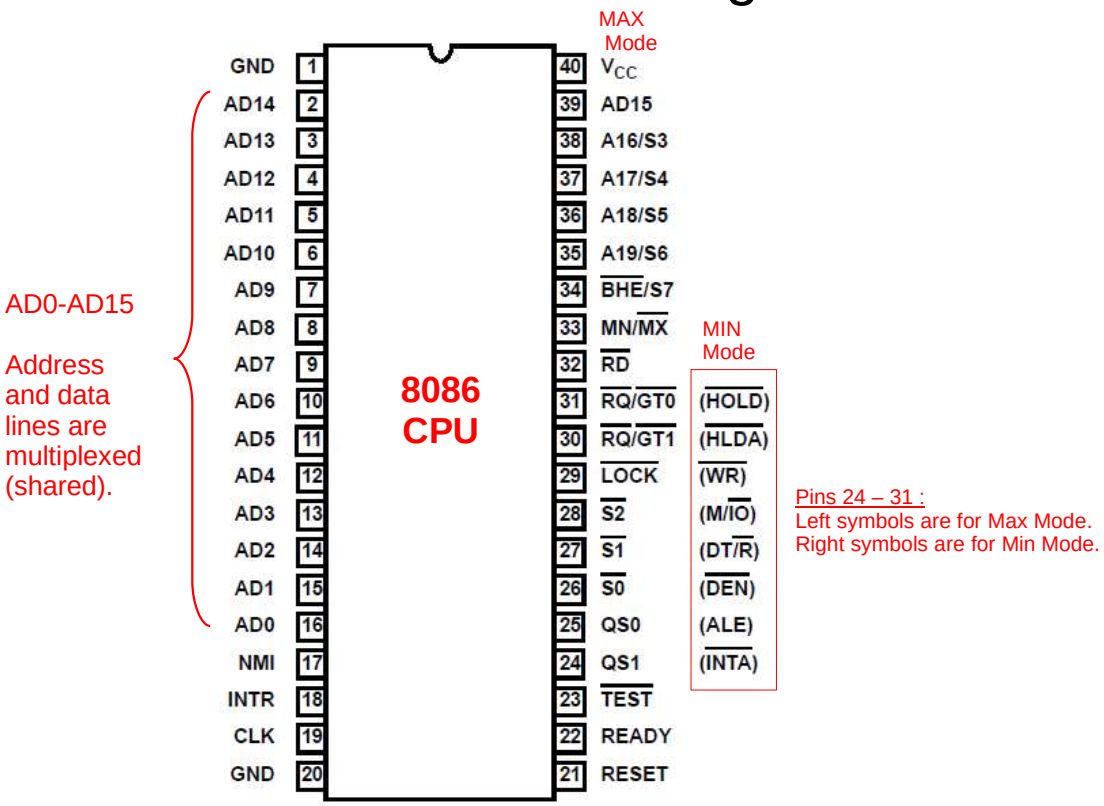
Topics

- 8086 CPU Specifications
- Operating Modes
  - Minimum Mode
  - Maximum Mode
- Bus Interface
  - Demultiplexing of Address/Data Bus
  - Buffering of Data Bus
  - Bus Timing Diagrams

8086 CPU Specifications

Specification	Description
Microprocessor	Intel 80x86
Data Bus Width	16 bit
Address Bus Width	20 bit
Max Memory Size	1 MB (2^{20} bytes)
Clock Speed	5 MHz
CPU Architecture	Von Neumann
Instruction Set Architecture (ISA)	CISC (Complex Instruction Set Computer)
Number of Registers	14 registers
Number of Pins	40-pin DIP (Dual In Package)

8086 CPU Pin Diagram



Descriptions of 8086 Pins

Name	Function	Type
AD15 - AD0	• Address / Data bus • Address bus and data bus lines are multiplexed (shared), in order to reduce the number of pins needed. • Address Lines : A15 – A0 , Data Lines : D15 – D0	Input / Output
A19 / S6 - A16 / S3	• Address / Status • Multiplexed lines in order to reduce number of pins. • Address Lines : A19 – A16 , Status Lines :S6 – S3	Output
MIN / $\overline{\text{MAX}}$	• Minimum / Maximum mode control (CPU operating mode) • If Pin 33 is connected to +5 Volt, CPU operates in MIN mode. • If connected to 0 Volt, CPU operates in MAX mode.	Input
$\overline{\text{RD}}$	• Read control • Used to read data or instructions from memory, or data from input device depending on status of the M / $\overline{\text{IO}}$ signal.	Output
$\overline{\text{WR}}$	• Write control • Used to write data to memory, or to output device depending on status of the M / $\overline{\text{IO}}$ signal.	Output

Descriptions of 8086 Pins

Name	Function	Type
RESET	• System reset • Used to restart the execution. • It causes the processor to immediately terminate its present activity.	Input
CLK	• System clock. • It provides timing to the processor for operations. • Its frequency is different for different 8086 versions (5MHz, 8MHz,10MHz).	Input
V_{CC}	• Voltage Common Collector (+ 5 Volt)	Input
GND	• Ground (0 Volt)	Output

Descriptions of 8086 Pins

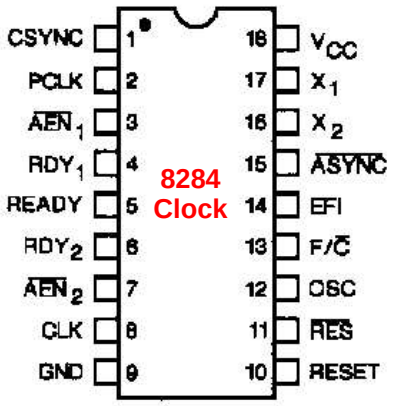
Name	Function	Type
$\overline{\text{TEST}}$	• Wait on Test control • This pin of 8086 is connected with the BUSY pin of 8087 Math Coprocessor chip. • Whenever 8087 is executing an instruction it makes BUSY = 1. • While execution in 8087, 8086 can check 8087 before giving it another instruction.	Input
READY	• Acknowledgement signal from I/O devices that data is transferred. • It is an active high signal. When it is high, it indicates that the device is ready to transfer data. • When it is low, it indicates wait state. • If the memory or I/O device speed is too slow to connect directly to the microprocessor, wait states are inserted into the timing through the use of the READY signal.	Input
NMI	• Non-Maskable Interrupt request • It is an edge triggered input, which causes an interrupt request to the microprocessor.	Input
INTR	• Interrupt request. is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not.	Input
$\overline{\text{INTA}}$	• Interrupt Acknowledge • Given by 8086 CPU, in response to an interrupt on INTR line.	Output
HOLD , HLDA	• Direct Memory Access (DMA) bus request is done using the HOLD and HLDA (Hold Acknowledge) signals.	Input and Output

8284 Clock Generator Chip

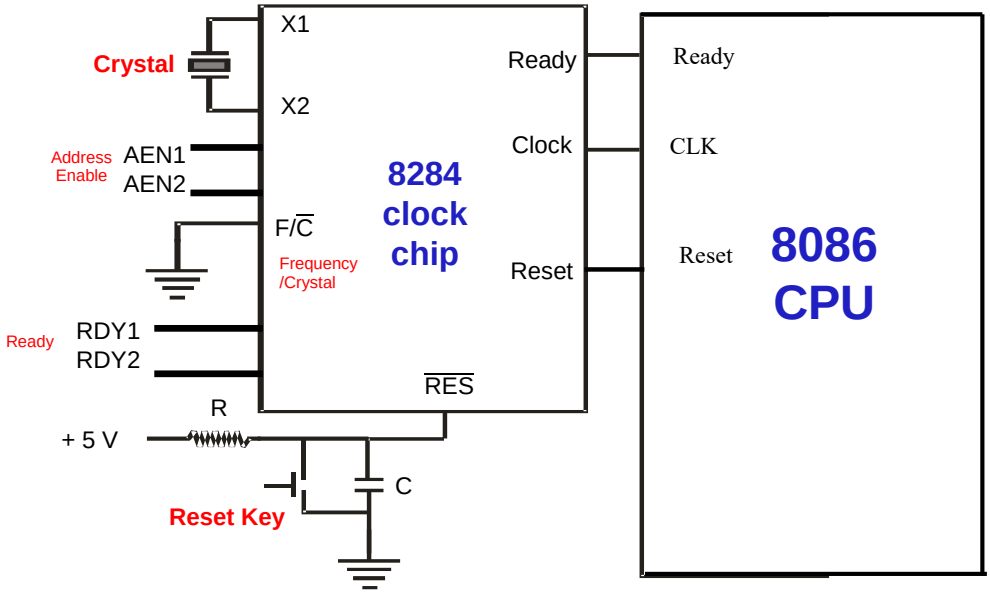
- 8284 Clock Generator chip used with 8086 CPU. (In MIN and MAX modes.)
- CLK pin is used for synchronization of internal and external operations of the CPU.

Clock output pins of 8284 chip:
- CLK = 8086 CPU Clock (5MHz)
- PCLK = Peripheral Clock = ½ x CLK
- OSC = Oscillator Clock = 3 x CLK

Functions of 8284 chip:
- Clocking the CPU and the peripherals
- Reset synchronization
- Ready synchronization



CPU and Clock Connection



Topics

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  - Minimum Mode
  - Maximum Mode
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  - Demultiplexing of Address/Data Bus
  - Buffering of Data Bus
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8086 Operating Modes

- 8086 CPU can operate in two modes : MIN mode and MAX mode.
- The mode is hardwired into the CPU thru the Pin#33, and therefore can not be changed by software.

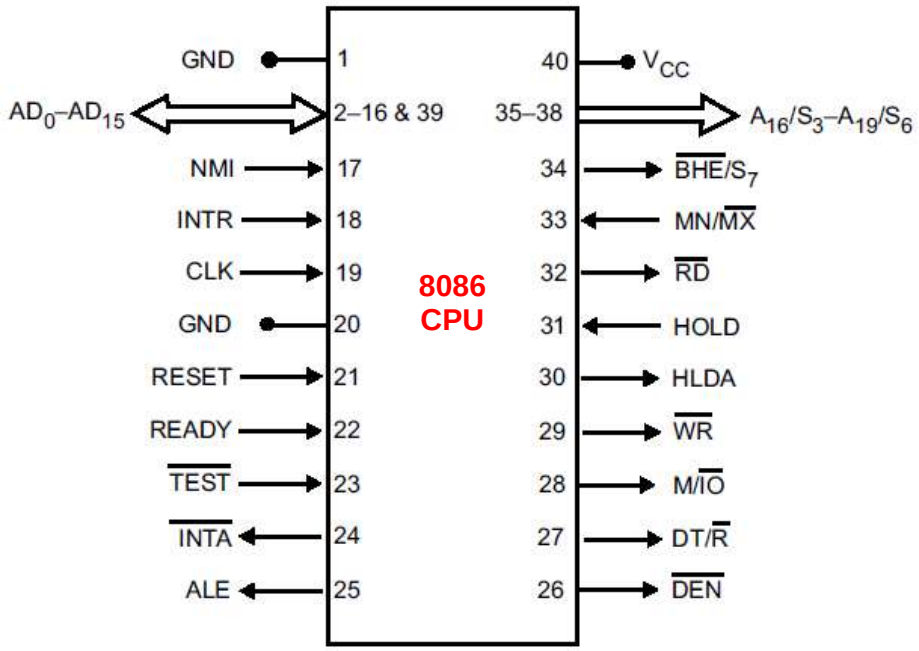
MINIMUM MODE (Single Processor Mode):

- When MN / $\overline{MX}$ input pin is high (logical 1), CPU operates in MIN mode.
- For a small system in which only one 8086 CPU is used, the system operates in MIN mode (Uni processor).
- In MIN mode, the CPU itself issues the control signals required by memory and I/O devices.

MAXIMUM MODE (Multi Processor Mode):

- When MN / $\overline{MX}$ input pin is low (logical 0), CPU operates in MAX mode.
- In MAX mode, a separate Bus Controller chip (8288 chip) is used which generates the control signals.
- Examples of configurations that MAX mode is used:
  - Using more than one 8086 CPU's in a system (Multi processors).
  - Using with an Math Coprocessor such as 8087 chip.

8086 Minimum Mode Pin Directions



Minimum Mode Control Signals

(MIN / $\overline{MAX}$ = V_{CC})

Name	Function	Type
$\overline{WR}$	Write control. It is used to write the data into the memory or the output device depending on the status of M / $\overline{IO}$ signal.	Output
M / $\overline{IO}$	Memory / Input-Output control. It is used to distinguish between memory and I/O operations. When it is high, it indicates I/O operation and when it is low indicates the memory operation.	Output
DT / $\overline{R}$	Data Transmit / Receive. It decides the direction of data flow through The transreceiver. When it is high, data is transmitted out and vice-a-versa.	Output
$\overline{DEN}$	Data Enable. It is used to enable the Data Transceiver Buffer chip. The transreceiver is a device used to separate data from the address/data bus.	Output
$\overline{ALE}$	Address Latch Enable. It is used to enable the Address Latch chip. A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines.	Output
$\overline{BHE}$ / S7	Bus High Enable / Status control signal. It is used to indicate the transfer of data using high data bus D8-D15. (Used as a chip select signal on the higher or lower byte of data bus.) This signal is low during the first clock cycle, thereafter it is active.	Output

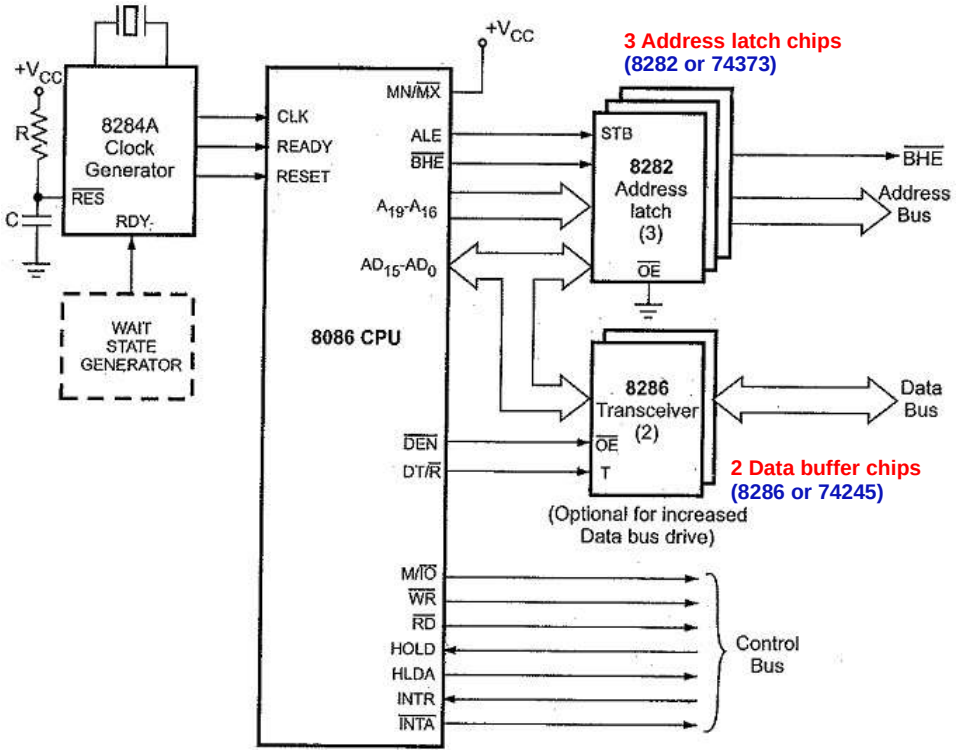
Components for Minimum Mode

- In a minimum mode 8086 system, the 8086 CPU is operated by connecting its MIN / $\overline{MAX}$ input pin to fixed logic 1 (+5 Volt).
- In this mode, all control signals are given out by the CPU chip itself.
- There is a single CPU in the minimum mode system.

- In a 8086 minimum mode system, the components below are required.
  - Bus interface subsystem:
    - Address Bus Latches
    - Data Bus Buffers (Optional)
    - Address Decoder
  - Memory subsytem (ROM and RAM chips)

- Peripheral Input/Output interface chips also can be added if needed.

Minimum Mode Configuration
(Block Diagram)



Minimum Mode Configuration

- Data and address provided by CPU to the memory or I/O port remain on the system bus for a limited amount of time.
- Address must be latched and data must be buffered before they are lost.
- 8086 CPU requires separate address latch chips, and separate tri-state data buffer chips.

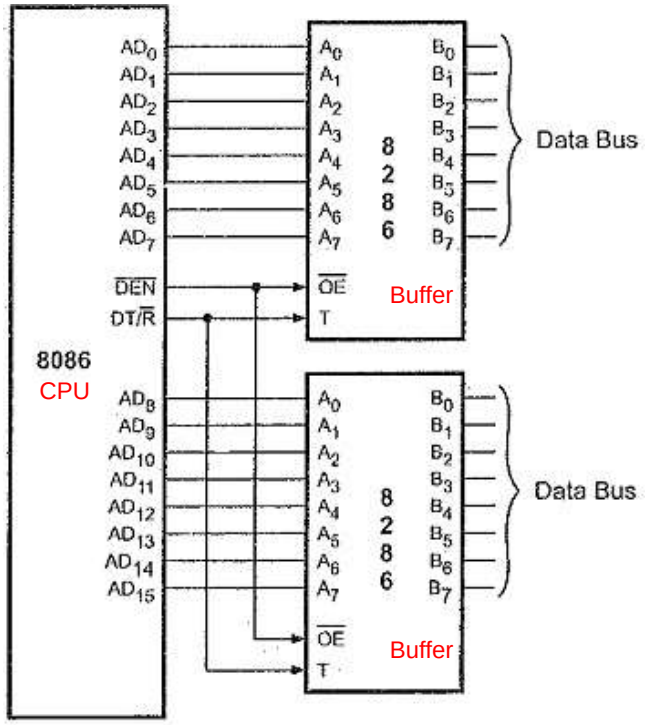
ADDRESS LATCH CHIPS (8282 or 74373):

- Number of Address Latches used are 3.
- Each latch is 8 bit.
- CPU Address Bus is 20 bits.
- Therefore, 20 bit / 8 bit = 3 latches are used.
- With 3 address latches, maximum 1 MB memory can be used.
- If less memory is needed, then number of latches can be reduced.

DATA BUFFER (TRANSCEIVER) CHIPS (8286 or 74245):

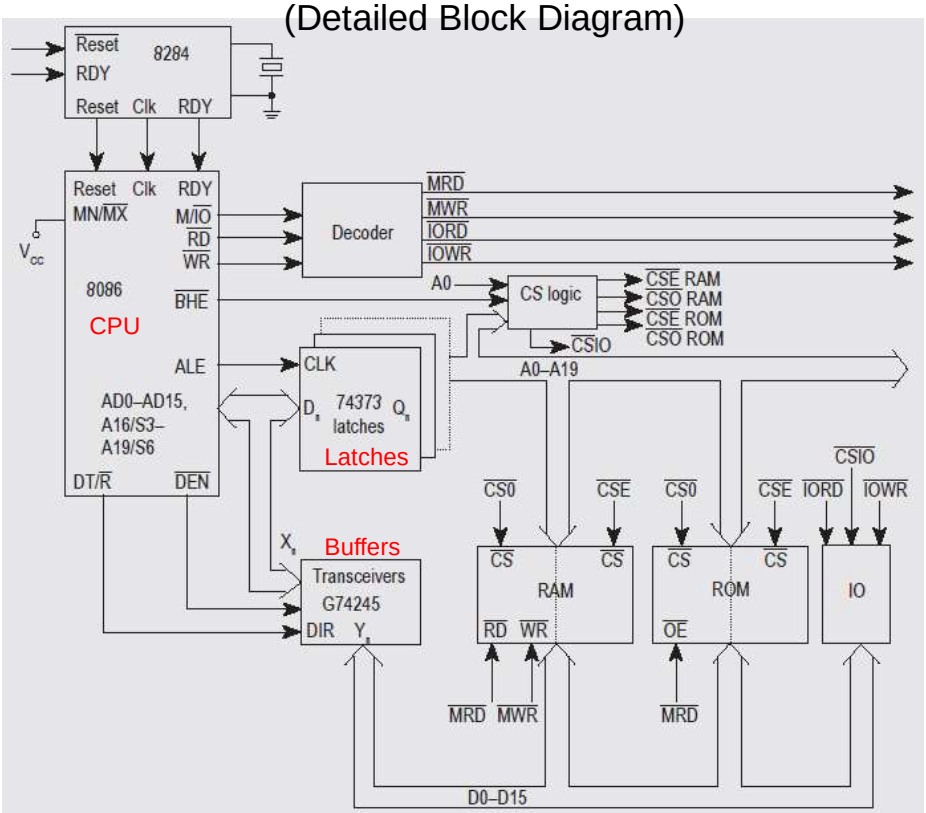
- Transceiver (Transmitter-Receiver) is a kind of tri-state buffer.
- Number of Data Buffers used are 2.
- Each Buffer is 8 bit.
- CPU Data Bus is 16 bits.
- Therefore, 16 bit / 8 bit = 2 buffers used.

Connections of 8086 CPU and Two 8286 Data Buffers (Transceivers)



Minimum Mode Operation of 8086-Based System

(Detailed Block Diagram)



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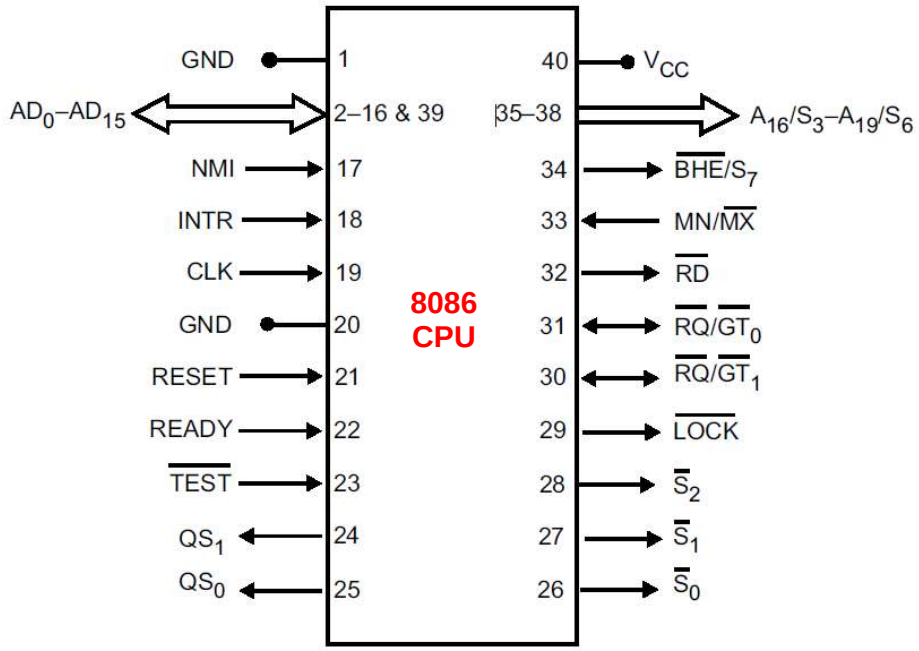
8086 Maximum Mode Pin Directions



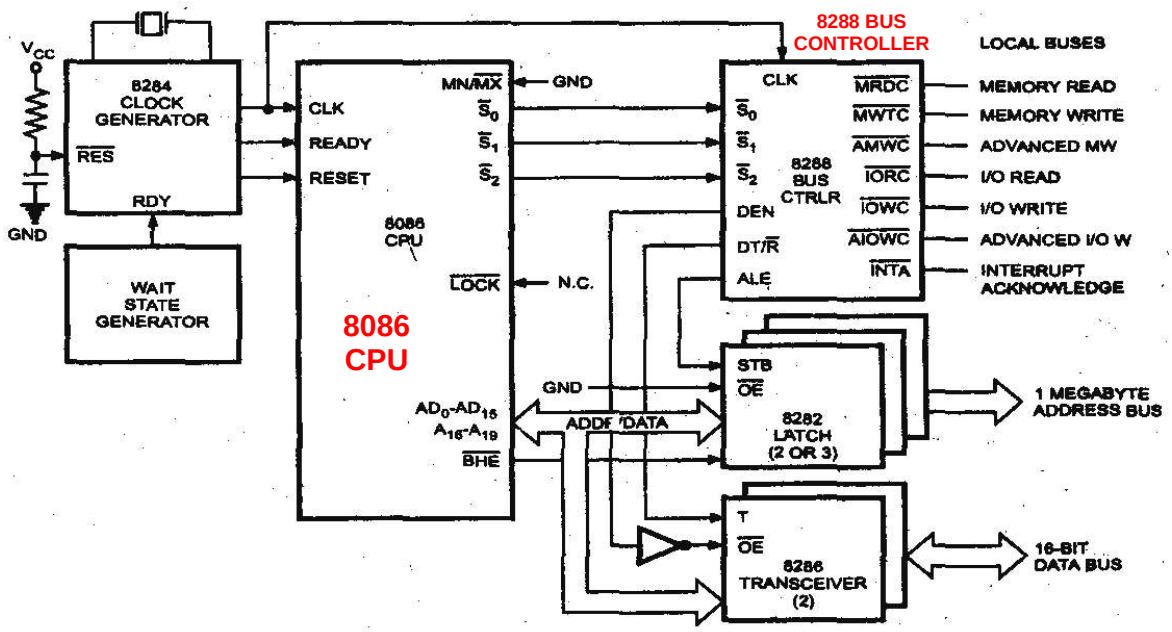
Maximum Mode Control Signals

(MIN / $\overline{\text{MAX}}$ = GND)

Name	Function	Type
RQ / $\overline{\text{GT1}}$ RQ / $\overline{\text{GT0}}$	Request / Grant bus access control. These signals are used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ/GT0 has a higher priority than RQ/GT1.	Input / Output
$\overline{\text{LOCK}}$	Bus priority lock control. When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus. It is activated using the LOCK prefix on any instruction.	Output
$\overline{\text{S2}}$ - $\overline{\text{S0}}$	Bus cycle status. These are the status signals that provide the status of operation, which is used by the **8288 Bus Controller chip** to generate memory & I/O control signals.	Output
$\overline{\text{QS1}}$, $\overline{\text{QS2}}$	Instruction queue status. These are queue status signals. These signals provide the status of instruction queue.	Output

Maximum Mode Configuration

(Block Diagram)



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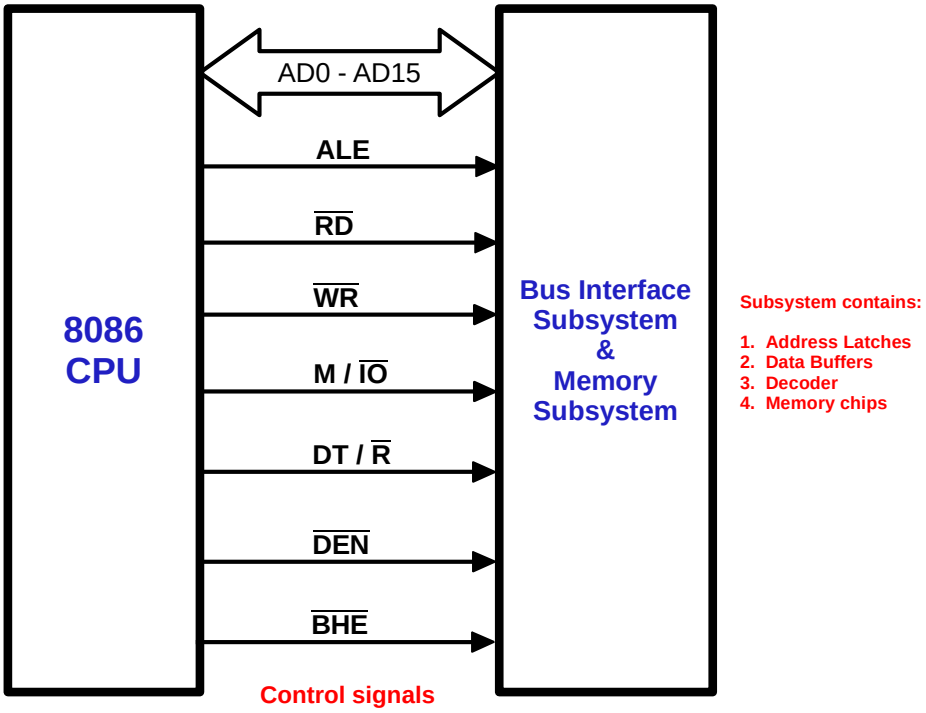
Block Diagram of Bus Interface

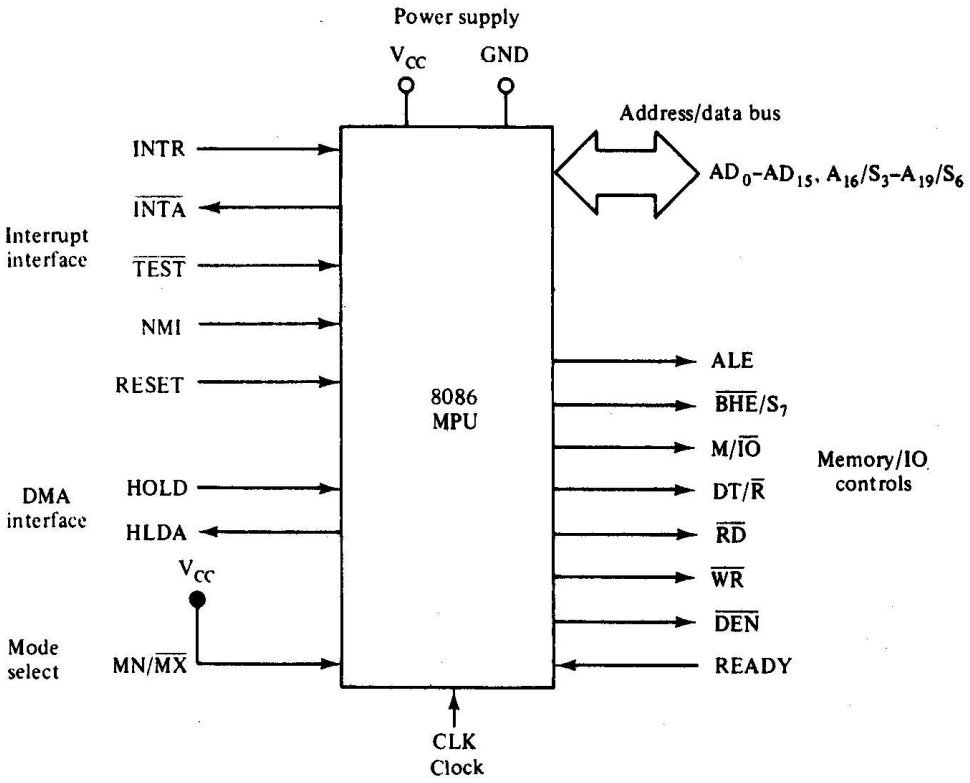


Memory and I/O Control Signals

8086 uses the following control signals to Bus Interface and Memory subsystems.

- Address Latch Enable (ALE) tells external circuitry that a valid address in on the address bus and it should be latched.
- Memory / Input-Output (M / $\overline{IO}$) tells whether a memory transfer or I/O transfer is taking place over the bus. Used to enable/disable memory and/or IO interface.
  M / $\overline{IO}$ = 1 means memory usage, M / $\overline{IO}$ = 0 means Input-Output device usage.
- Data Transmit / Receive (DT / $\overline{R}$) tells external circuitry which direction the data is to be transferred over the data bus (whether CPU will transmit or receive data).
  DT / $\overline{R}$ = 1 means transmit mode is selected (write = output).
  DT / $\overline{R}$ = 0 means read mode is selected (read = input).
- Bank High Enable ($\overline{BHE}$) signal is used as a memory enable signal for the most significant byte half of the data bus, D8 through D15.
- Write ($\overline{WR}$) (active 0) signal tells that a write bus cycle is in progress.
- Read ($\overline{RD}$) (active 0) signal tells that a read bus cycle is in progress.
- Data Enable ($\overline{DEN}$) (active 0) signal enables memory to supply data to CPU.

Bus Interface for Minimum Mode



Bus Interface for Minimum Mode

- Data bus is 16-bit wide D15-D0 lines.
- Multiplexed with A15 through A0 lines.

- Allows 3 types of data transfers:
  - Word data (2 bytes) : Over D15-D0 lines.
  - Low byte data : Over D7-D0
  - High byte data : Over D15-D8

- Memory control signal : BHE (Bank High Enable)
- BHE is used to signal external circuitry, whether or not a byte transfer is taking place over the upper 8 data bus lines (D8-D15).

- A0 line does the same for a byte transfer, over the lower 8 data bus line (D7-D0).

Bus Interface Chips used with 8086 CPU

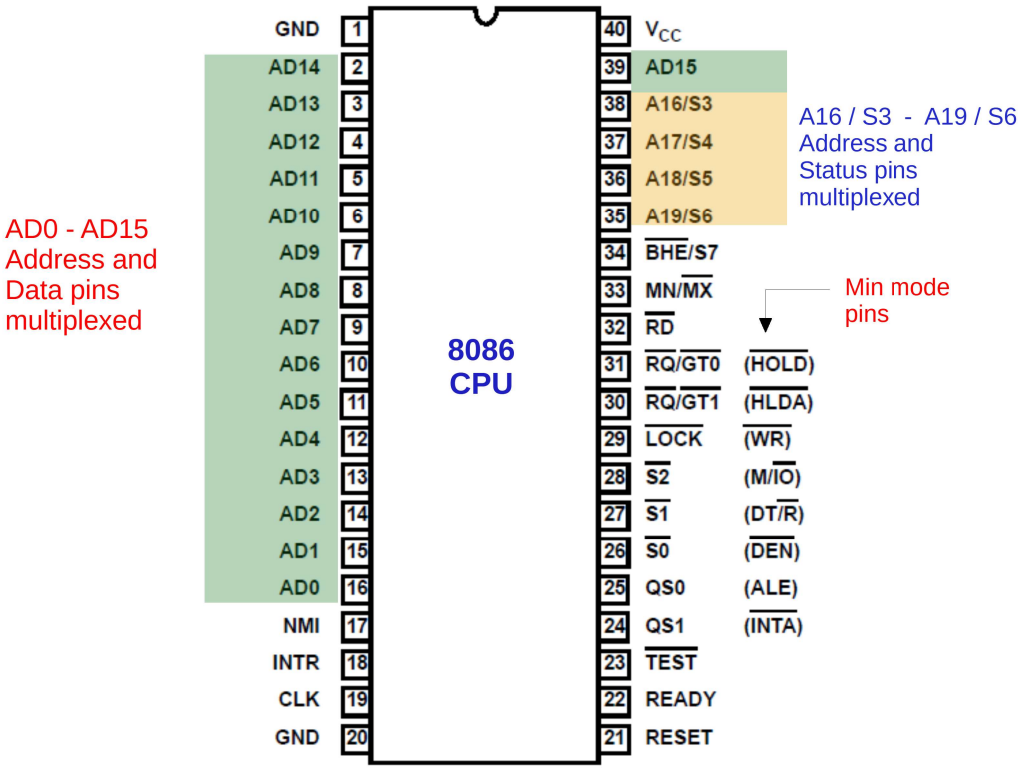
Chip Name	Chip Number	Description
Address Latcher	74373	Octal Transparent Latch With 3-State Outputs
	8282	Octal Latching Bus Driver
Data Buffer (Transceiver)	74245	Octal Bus Transceivers With 3-State Outputs
	8286	Octal Bus Transceiver
Address Decoder	74138	3 to 8 Decoder/Demultiplexer
	74139	2 to 4 Decoder/Demultiplexer

Bus Multiplexing

Multiplexing (Sharing) of Address Bus / Data Bus in 8086 CPU :

- In 8086 CPU design and fabrication, the Address pins , Data pins , and some Status pins were multiplexed (time-shared), in order to reduce total count of chip pins (limited to total 40 pins).
- Address and Data pins multiplexed : AD0 – AD15
- Address and Status pins multiplexed : A16/S3 – A19/S6
- Address bus signals are A0-A19 (20 lines). (Providing 1M byte of addressing space.
- Data bus signals are D0-D15 (16 lines).

Bus Multiplexing

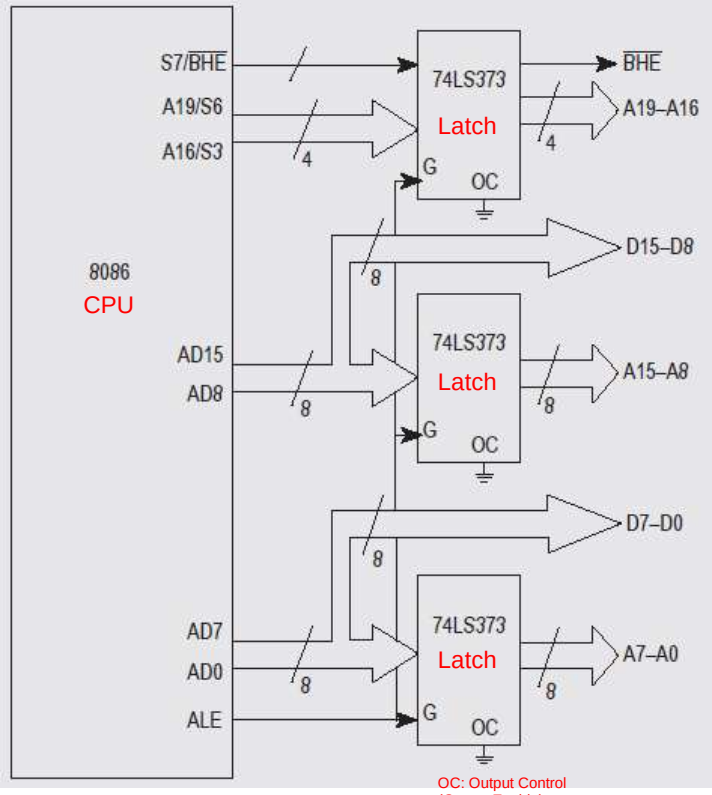


Bus Demultiplexing

Demultiplexing (Separation) of Address Bus / Data Bus:

- The Address/Data (AD0 - AD15) and Address/Status (A16/S3 - A19/S6) pins were multiplexed to reduce the CPU pin count, during fabrication.
- These pins (buses) must be **demultiplexed (separated)** to obtain the signals required for interfacing other circuits (memory chips and I/O interface chips) to the CPU.
- Usually several Address Bus Latches are used for demuxing such as **74373** or **8282** chips.
- The ALE (Address Latch Enable) control signal from the CPU is used to latch the address information (called as Valid Address) that appear briefly on the multiplexed bus.
- It makes the latched address information available for long enough time for correct interfacing to memory.

Bus Demultiplexing: Formation of Separate Address bus (A19–A0) and Data Bus (D15–D0) in 8086



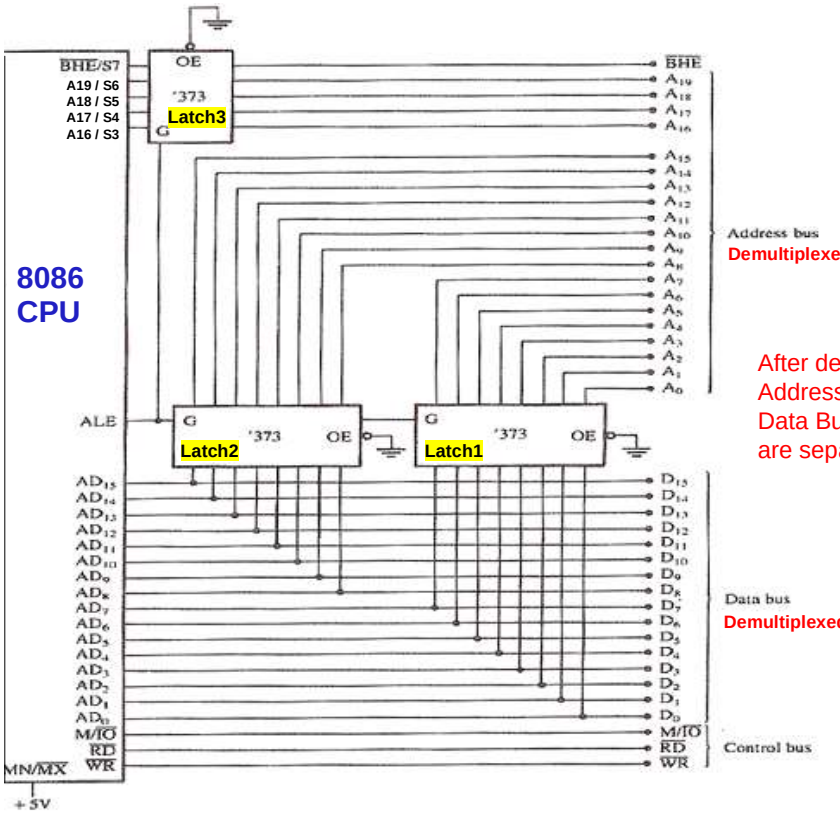
OC: Output Control (Output Enable)

Bus Demultiplexing

- The example above is implemented with 74373 Octal-D-type latches (3 quantities).
- Inputs of latches are AD0-AD15, A16-A19, and BHE from 8086 CPU.
- All latches are permanently enabled by fixing their $\overline{OC}$ inputs at logic 0 (Ground).
- All latches clocked in parallel, with pulse at ALE from CPU.
- Latched and buffered outputs are: A0 - A19, and BHE.
- Outputs of the latches are applied to the address inputs of memory subsystem. (Address decoder, and Read/Write control logic).

Details of Demultiplexed Bus

Three latches (74373 chips) are used for bus demuxing.



After demultiplexing, Address Bus and Data Bus lines are separated.

G: Gate enable
OE: Output Enable

Three Bus Latches (74373 chips) are used for Bus Demultiplexing (Separation).

Latch1 separates AD0 - AD7 shared lines.
New lines :
A0 - A7 and
D0 – D7

Latch2 separates AD8 - AD15 shared lines.
New lines :
A8 - A15 and
D8 – D15

Latch3 separates A16/S3 - A19/S6 shared lines.
New lines :
A16 - A19 and
S3 - S6

Number of direct Address and Data pins of CPU = 20 bits

AD0 - AD15 = 16 bits
A16/S3 - A19/S6 = 4 bits
Total = 16 bits + 4 bits = 20 bits

After Bus Demultiplexing (Bus Separation) :

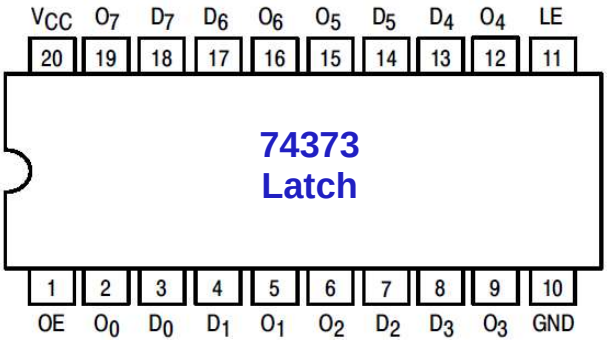
Number of Adress Bus bits = 20 bits
Number of Data Bus bits = 16 bits
Total = 20 bits + 16 bits = 36 bits

- Since 8086 CPU has multiplexed address/data pins, demultiplexing is necessary.
- If another CPU has 36 pins instead of 20 pins for address/data lines, demultiplexing is not necessary.

Address Latch Chips

- A simple latch is a device that can store one bit (a logic 0 or 1) of data.
- Latches are used to de-multiplex (separate) the address/data lines and address/status lines.
- Address Latches are generally implemented as buffered output (one directional) D-type flip-flops.
- Examples of latch chips : 8282, and 74373.
- They are used for separating (demultiplexing) the valid address from the multiplexed (shared) address/data signals.
- Latches are controlled by the ALE (Address Latch Enable) signal generated by 8086 CPU.

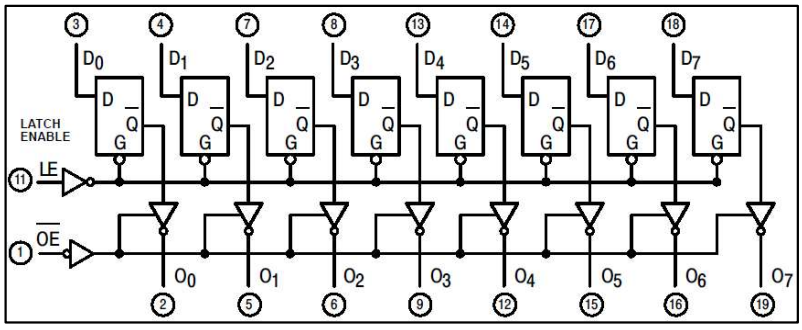
74373 Address Latch chip Pin and Functional Diagrams



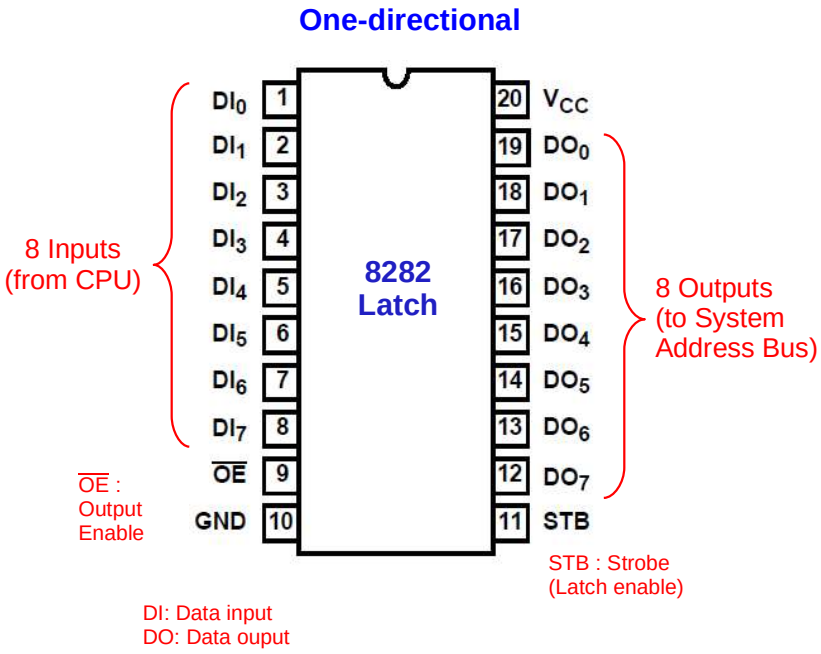
One-directional latches (OUT)

LE : Latch enable

$\overline{OE}$: Output Enable



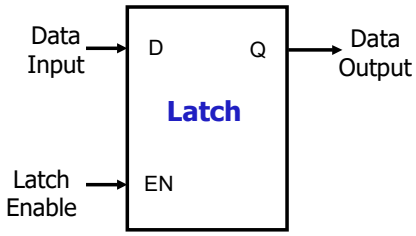
Alternative Address Latch : 8282 chip



Example Latch (1-bit)

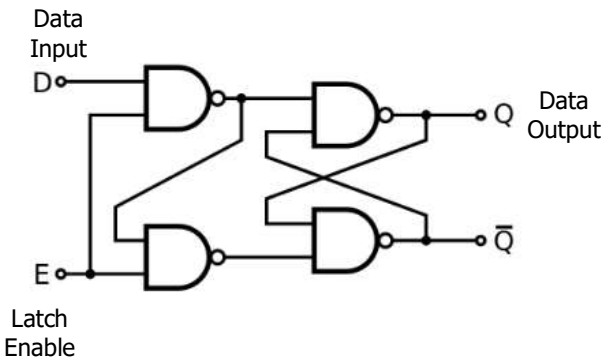
- The following is logic gate equivalent of a 1-bit D-latch (Data latch).
- Latch is a memory device, similar to flip-flop.
- A group of 8 latches (each is 1-bit) represent a 1-byte latch register.

Block diagram (1-bit)



Truth Table

D Input	Q(t+1) Output
0	0
1	1



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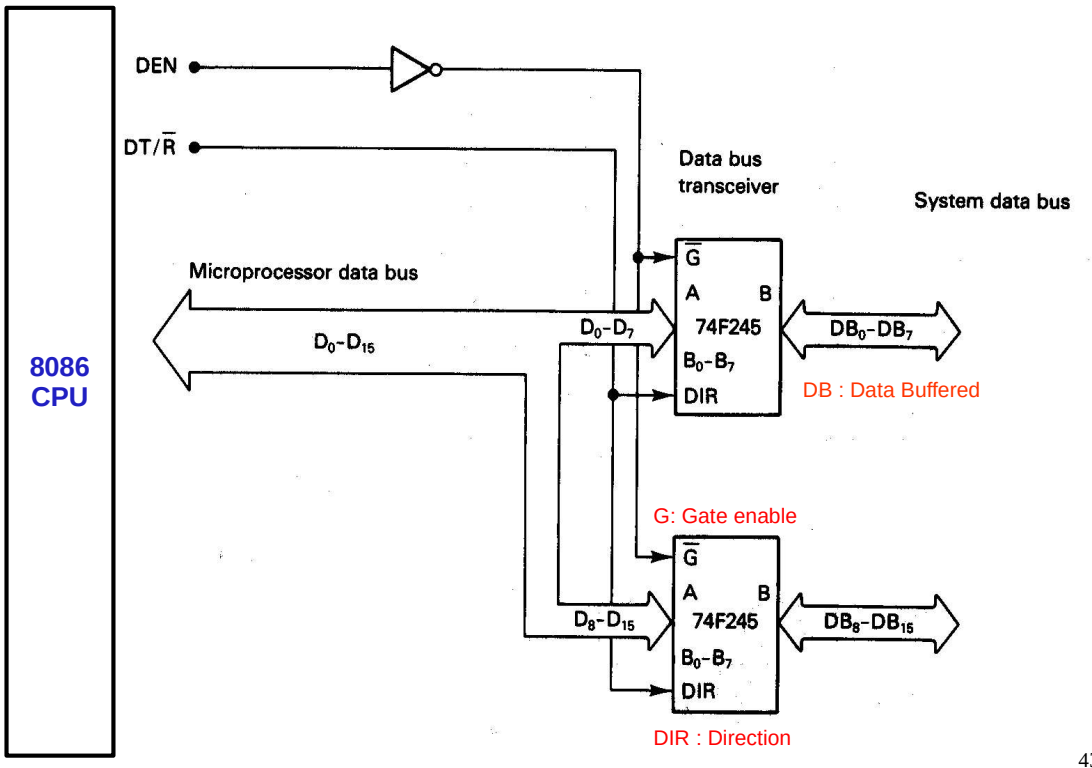
Buffering of Data Bus in 8086 CPU

- Buffering of Data Bus is an optional procedure.
- For small systems with few components, there may be no need for buffering.
- In most cases, the data signals of 8086 CPU should be buffered such as in a computer board.
- Buffering is often needed if more than 10 TTL loads (Transistor-Transistor-Logic) are used as electronic circuit components.
- For example, using too many memory chips and peripheral I/O device interface chips takes too much electrical current from the Data Bus.
- For two-directional data signals (pins used for both input and output), buffering is accomplished with the 74245 (or 8286) two-directional Data Bus buffer chips.
- Data Bus Buffer is also called as Data Transceiver (transmitter / receiver).

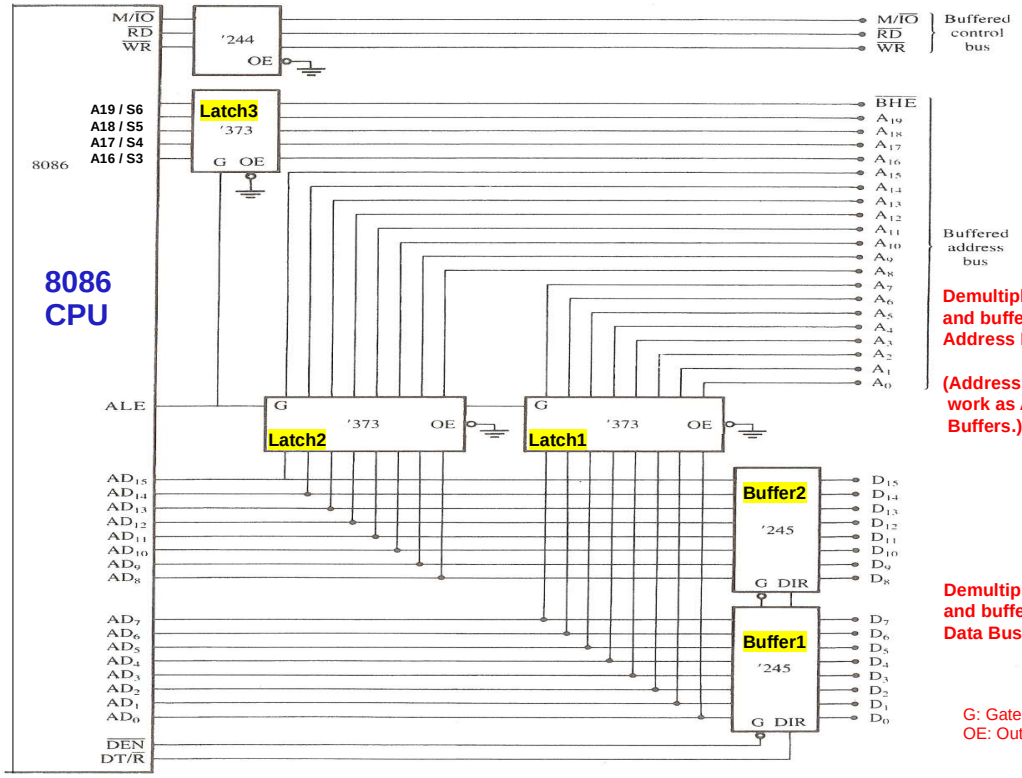
Data Buffer Design



Data Buffer Design

- The example above is implemented with two 74245 Octal two-directional bus transceivers (buffers).
- A inputs/outputs of buffer chips are D0-D15 directly from CPU.
- Direction of both devices set by logic level of DT/R signal.
- Both devices enabled at appropriate time for data transfer by DEN=1
- B inputs/outputs of buffer chips are the buffered data bus lines DB0 through DB15. (DB means Data Buffered).
- Buffered data bus lines applied directly to the memory subsystem.

Demultiplexed and Buffered Bus



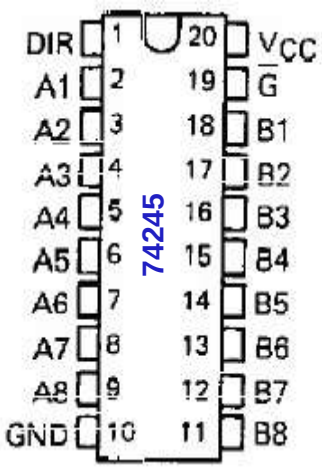
Demultiplexed and Buffered Bus

- In the example above, three Address Latches (74373 chips) are used for bus demuxing.
- Two Data Buffers (74245 chips) are used for Data Bus buffering.
- For non-muxed unidirectional (always output) control bus signals (M / IO, RD, WR), buffering is accomplished with the 74244 chip.

Data Buffer Chips

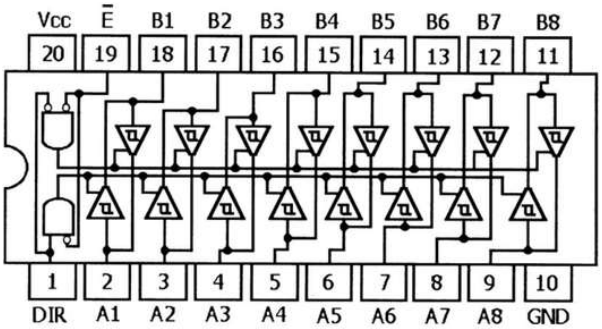
- A data buffer is an 8-bit register, to store the information being provided by the external data bus.
- Buffers are used to drive external loads, and also to isolate a component when disabled.
- **Data Buffers** (Transceiver) are the two-directional Tri-state buffers.
- They are required to separate the valid data from the time multiplexed (shared) address/data signals.
- Examples of Data Buffer chips: 8286, and 74245.
- Data Buffers are controlled by two signals namely, $\overline{DEN}$ (Data Enable) and DT / $\overline{R}$ (Data Transmit / Receive) from CPU.
- $\overline{DEN}$ signal indicates the direction of data, i.e. from or to the CPU.

74245 Data Buffer chip
Pin and Functional Diagrams

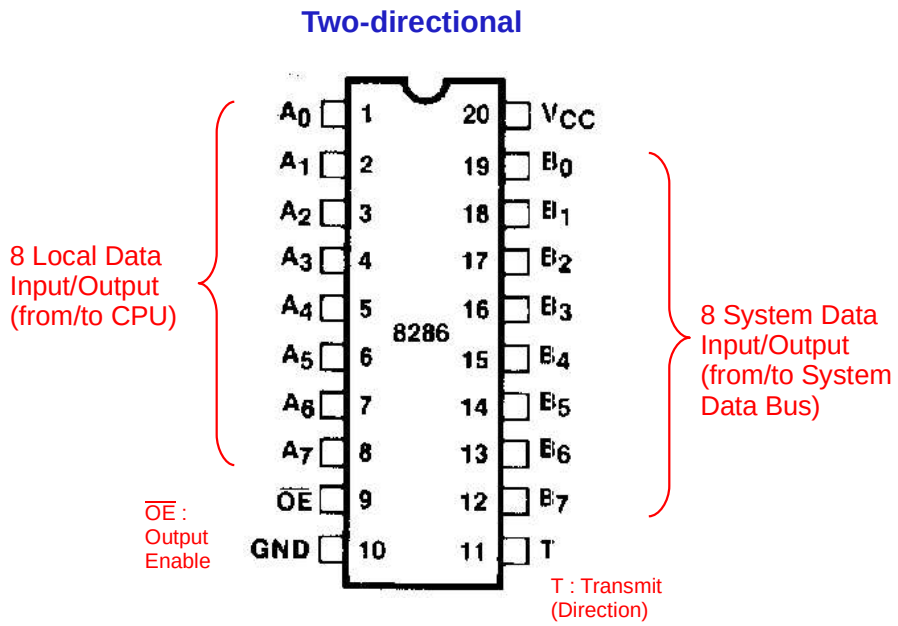


G: Gate enable
DIR : Direction

Two-directional buffers (IN/OUT)



Alternative Data Buffer : 8286 chip



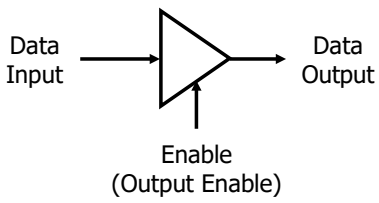
Tri-State Buffer

- A general Buffer provides electrical power amplification of a digital signal.
- Tri-state Buffer is a special buffer circuit, whose output can be electronically disconnected from its output circuitry when required.
- A Tri-state Buffer can be thought of as a controlled switch.
- Its output can be electronically turned ON or OFF by means of an external Control or Enable (EN) signal input.
- Tri-state buffer can be used to isolate devices and circuits from the data bus and one another.
- Tri-state buffers are used as switches to control the direction of data flow in memory access.

Tri-State Buffer

- The following is the circuit symbol of a Tri-State buffer for 1-bit.
- Circuit has two inputs and one output.
  - First input is the normal **data** input for circuit.
  - Second input is an **enable** signal.
    - If enable is set high, output follows the input (1 or 0).
    - If enable is set low, output is disconnected (high impedance state).

Symbol

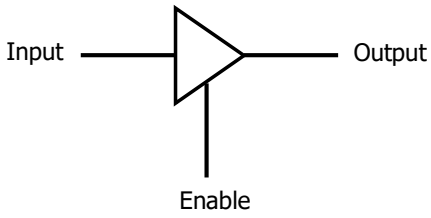


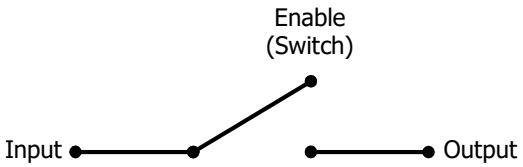
Truth Table

Enable	IN	OUT
0	0	High impendance
0	1	High impendance
1	0	0
1	1	1

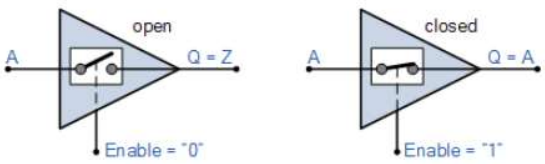
Tri-State Buffer as a Switch

- A tristate buffer can be thought of as a switch.
- If Enable is on, the switch is closed, Input is connected to Output. (Output = Input)
- If Enable is off, the switch is open, Input is disconnected from Output. (Output = Z , means it is in high impedance state)





Switch equivalent:



Topics

- 8086 CPU Specifications
- Operating Modes
  - Minimum Mode
  - Maximum Mode
- Bus Interface
  - Demultiplexing of Address/Data Bus
  - Buffering of Data Bus
  - Bus Timing Diagrams

System Clock and Bus Cycle

- System clock generates **pulses** to synchronize all system events.
- Each fetch-execute instruction cycle is divided into states, which are one clock pulse long.
- Most instructions require multiple steps and several clock pulses to complete.
- Some steps (e.g. memory access) take longer, and may require additional clock pulses to complete.
- The clock speed of a CPU determines how often (frequency) a new instruction is executed.
- It is measured in Mega Hertz (MHz), or Giga Hertz (GHz).
- Example: 1.7 GHz means that the computer executes 1.7x109 clock periods per second.
- Hertz (clock rate) is the unit of frequency measurement.
- It represents number of clock cycles per second.

System Clock and Bus Cycle

- 8086 CPU uses the memory chips and the peripheral Input/Output device interface chips in the periods called as Bus Cycles.
- A data transfer operation to/from the CPU occupies at least one bus cycle.
- Each bus cycle consists of 4 clock cycles (T1, T2, T3, T4 states).

Frequency Units

Frequency Unit	Unit name	Hertz Value
1 KHz	Kilo	10^3
1 MHz	Mega	10^6
1 GHz	Giga	10^9

Time Units

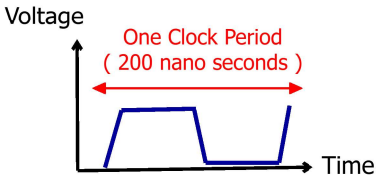
Time Unit	Unit name	Seconds Value
1 ms	Mili	10^{-3}
1 µs	Micro	10^{-6}
1 ns	Nano	10^{-9}

Example : Calculating 8086 CPU Clock Period and Bus Cycle duration

The frequency for 8086 CPU clock is 5 MHz (Mega Hertz).

$$Period(seconds) = \frac{1}{Frequency}$$

Period duration is T = 1 / 5 MHz
= 0.2 micro secons
= 200 nano seconds



Each bus cycle in 8086 consists of 4 clock cycles (T1, T2, T3, T4 states).
Duration for one Bus Cycle = 4 * T
= 4 * 200
= 800 nano seconds (0.8 micro seconds)

Max rate for memory and I/O transactions = 1 / 0.8
= 1.25 Million Instructions Per Seconds (MIPS)

Due to internal instruction queueing (pipe-lining), 8086 CPU can execute 2.5 MIPS

8086 CPU Bus Timing Diagrams

- Bus timing diagrams show the system clocking periods (square wave), CPU control signals, Address Bus, and Data Bus.
  - Horizontal axis represents time (usually in nano seconds).
  - Vertical axis represents the logical levels.
    Upper lines : 1 (+5 volt)
    Lower lines: 0 (0 volt)
    Middle lines : Neither 1 nor 0

Bus Operations for Writing to Memory:

1) CPU outputs the memory address on the address bus.
2) Outputs the data to be written into memory on the data bus.
3) Issues the write ($\overline{WR}$ = 0) and selection (M / $\overline{IO}$ = 1) control signals.

Bus Operations for Reading from Memory:

1) CPU outputs the memory address on the address bus.
2) Issues the read ($\overline{RD}$ = 0) and selection (M / $\overline{IO}$ = 1) control signals.
3) Accepts the data via the data bus.

Diagram of One Bus Cycle for Read Operation

Reading 1-byte from Memory

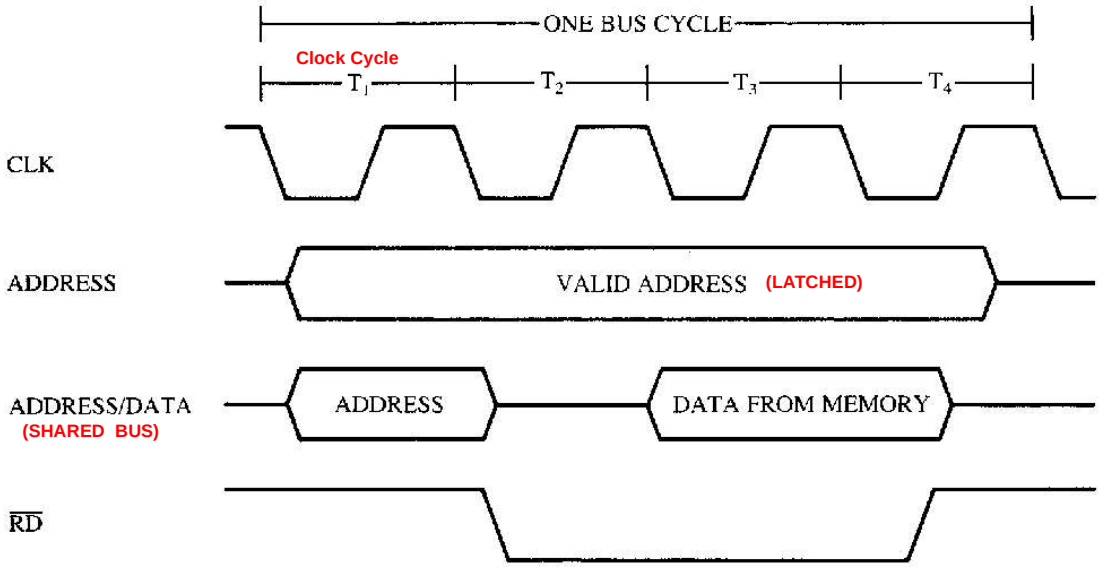
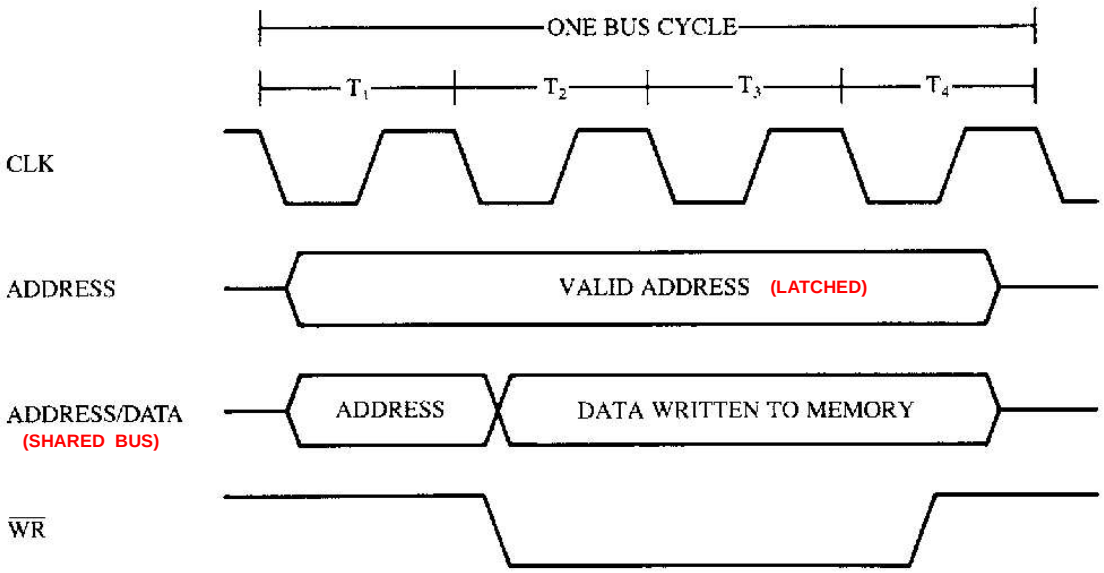


Diagram of One Bus Cycle for Write Operation

Writing 1-byte to Memory



Descriptions of Bus Operations

Clocking Period	Description of Bus Operations
T1	• In T1 , the address of memory or I/O location is sent out via address bus. • The address/data bus is multiplexed and sometimes contains memory-addressing information, sometimes data. • During T1, control signals ALE, $\overline{DT}$ / R , and M / $\overline{IO}$ are also output. • The M / $\overline{IO}$ signal indicates whether the address bus contains a memory address or an I/O device (port) number.
T2	• During T2, CPU issues the $\overline{RD}$ or $\overline{WR}$ signal, and in the case of a write, the data to be written appear on the data bus. • These events cause the memory or I/O device to begin to perform a read or a write operation.
T3	• T3 clocking period is provided to allow the memory time to access data. • If the bus cycle happens to be a read bus cycle, the data bus is sampled at the end of T3.
T4	• In T4, all bus signals are deactivated in preparation for the next bus cycle. • This is also the time when CPU samples the data bus connections for data that are read from memory or I/O.