Prof. Dr. Berna Örs Yalçın **Due Date:** 27.10.2023

EHB205 Introduction to Logic Design

1st Homework

Part 1

1. Convert the hexadecimal number $64CD_{16}$ to binary, to octal and decimal.
2. Convert the decimal number 431 to binary, hexadecimal and octal.
3. Express the following numbers in decimal:
    a. $(10110.0101)_2$
    b. $(16.5)_{16}$
    c. $(26.24)_8$
    d. $(DADA.B)_{16}$
    e. $(1010.1101)_2$
4. Convert the following binary numbers to hexadecimal and to decimal:
    a. 1.10010
    b. 110.010. Explain why the decimal answer in (b) is 4 times that in (a).
5. Draw truth table of the Boolean function f(x,y,z)=x'y+z.

Part 2

1. Get Xilinx ISE 14.7 webpack from https://www.xilinx.com/support/download.html. Install to your computer.
2. Take "OR_gate.vhd" and "OR_gate_tb.vhd" files from ninova.
3. Start "Project Navigator" in "ISE Design Tools" in Xilinx ISE.
4. Build a new project by "New Project" command. Give a name to your project.
5. Add the files mentioned above by "Add Source" command in "Project" tab.
6. When the option is "view" "implementation" and "OR_gate.vhd" is chosen, view your circuits schematic by "view RTL schematic" in "Synthesize" list. Take the picture in order to use in your homework report.
7. Choose "view" "Simulation" option.
8. When "OR_gate_tb.vhd" file is chosen, push "Simulate Behavioral Model" command. You should see a graph with inputs and outputs. Take a picture of this graph between 0 ns – 60 ns for your homework report.
9. Prepare a report which shows that you succesfully completed all the above steps.

Kaynaklar

1) Morris Mano, Micheal Ciletti, Digital Design, Fifth Edition, Pearson.
2) Frank Vahid, Digital design, with RTL design, VHDL, and Verilog, Hoboken, NJ : John Wiley, 2010
3) Peter D Minns, FSM-based digital design using Verilog HDL, Chichester, England : J. Wiley & Sons , c2008
4) Pong P. Chu, FPGA prototyping by Verilog examples Xilinx Spartan -3 version, Hoboken, N.J. : J. Wiley & Sons, c2008