HW4-10093

Sens ERS04

04020034

$100

| x | y | z | A | B | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

## For A

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 |

$A = yz + xy = y(z + x)$

## For B

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |

$B = y'z + xy' + x'yz'$

$= x'y'z + x'yz' + xy'z + xy'z'$

$= x'(y \oplus z) + x(y \oplus z)$

$= y \oplus z$

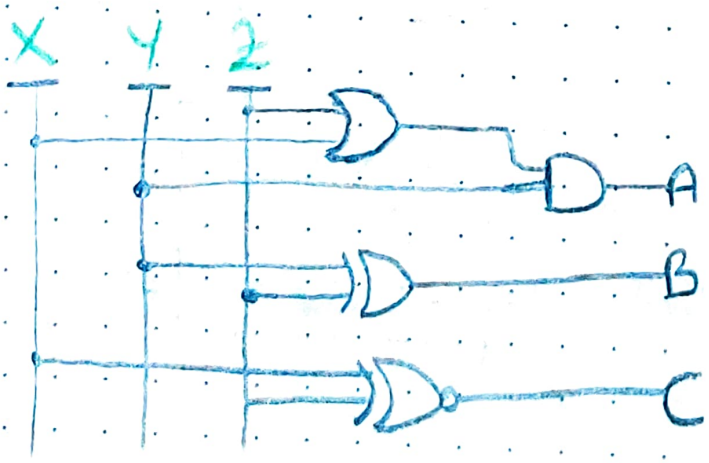
## For C

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |

$C = x'y'z' + xz + x'yz'$

$= x'z' + xz$

$= \overline{x \oplus z}$



$m_0 = 00000 = x'y'z't'w'$
$m_{10} = 01010 = x'yz't w'$
$m_{13} = 01101 = x'yzt'w$
$m_{14} = 01110 = x'yzt w'$
$m_{15} = 01111 = x'yzt w$
$m_{18} = 10001 = xy'z't'w$
$m_{24} = 11000 = xyz't'w'$
$m_{28} = 11100 = xyzt'w'$
$m_{29} = 11101 = xyzt'w$

| | x | y | z | t | w | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ✓ |
| 2 | 0 | 0 | 0 | 1 | 0 | ✓ |
| 16 | 1 | 0 | 0 | 0 | 0 | ✓ |
| 10 | 0 | 1 | 0 | 1 | 0 | ✓ |
| 18 | 1 | 0 | 0 | 1 | 0 | ✓ |
| 24 | 1 | 1 | 0 | 0 | 0 | ✓ |
| 13 | 0 | 1 | 1 | 0 | 1 | ✓ |
| 14 | 0 | 1 | 1 | 1 | 0 | ✓ |
| 28 | 1 | 1 | 1 | 0 | 0 | ✓ |
| 15 | 0 | 1 | 1 | 1 | 1 | ✓ |
| 29 | 1 | 1 | 1 | 0 | 1 | ✓ |
| 31 | 1 | 1 | 1 | 1 | 1 | ✓ |

$m_2 = 00010 = x'y'z't w$
$m_{16} = 10000 = xy'z't w'$
$m_{31} = 11111 = xyzt w$

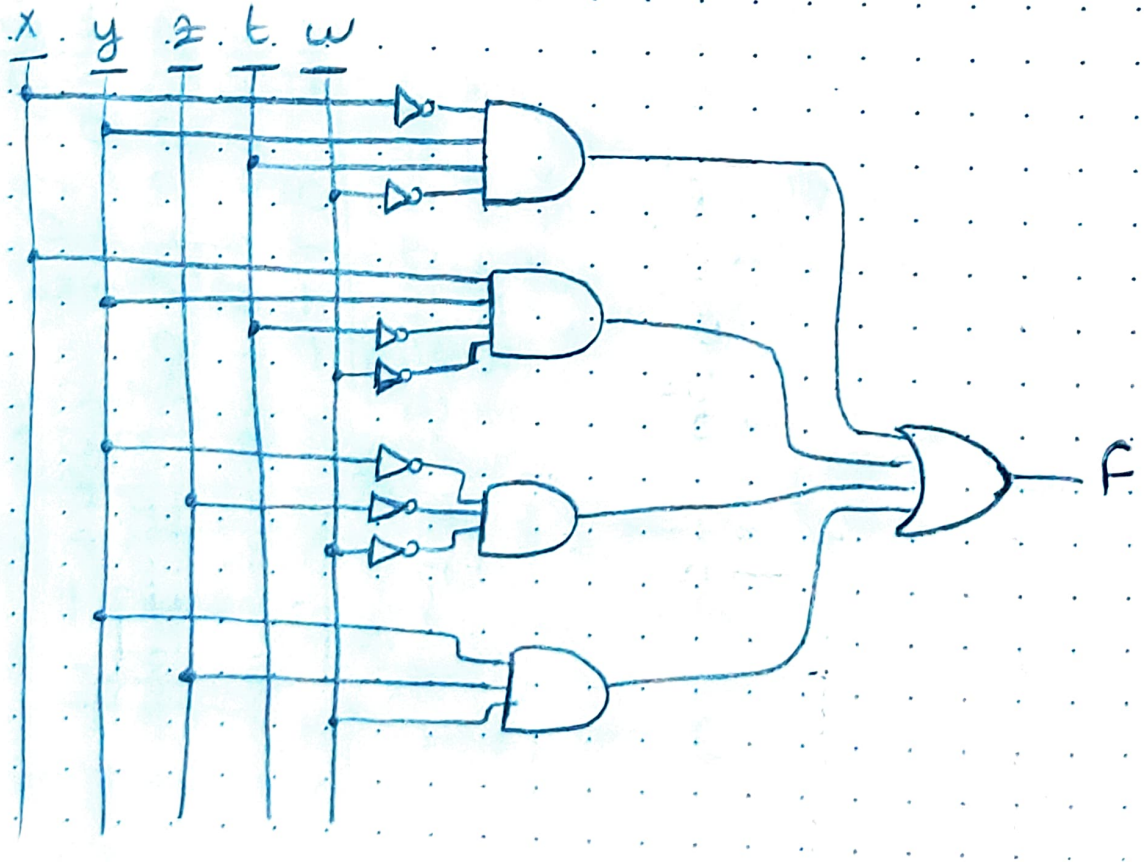
| | | x | y | z | t | w |
|---|---|---|---|---|---|---|
| ✓ | 0, 2 | 0 | 0 | 0 | - | 0 |
| ✓ | 0, 16 | - | 0 | 0 | 0 | 0 |
| A | 2, 10 | 0 | - | 0 | 1 | 0 |
| ✓ | 2, 18 | - | 0 | 0 | 1 | 0 |
| ✓ | 16, 18 | 1 | 0 | 0 | - | 0 |
| F | 16, 24 | 1 | - | 0 | 0 | 0 |
| C | 10, 14 | 0 | 1 | - | 1 | 0 |
| D | 24, 28 | 1 | 1 | - | 0 | 0 |
| ✓ | 13, 15 | 0 | 1 | 1 | - | 1 |
| E | 14, 15 | 0 | 1 | 1 | 1 | - |
| ✓ | 13, 29 | - | 1 | 1 | 0 | 1 |
| F | 28, 29 | 1 | 1 | 1 | 0 | - |
| ✓ | 15, 31 | - | 1 | 1 | 1 | 1 |
| ✓ | 29, 31 | 1 | 1 | 1 | - | 1 |

| | x y z t w |
|---|---|
| G 0,2,16,18 | - 0 0 - 0 |
| 0,16,2,18 | - 0 0 - 0 |
| H 13,15,29,31 | - 1 1 - 1 |
| 13,29,15,31 | - 1 1 - 1 |

$$F = C + D + G + H$$

$$= x'yt'w' + xyt'w' + y'z'w + yzw$$

| | 0 | 10 | 13 | 14 | 15 | 18 | 24 | 28 | 29 |
|---|---|---|---|---|---|---|---|---|---|
| A | | X | | | | | | | |
| B | | | | | | | X | | |
| C | | X | | (X) | | | | | |
| D | | | | | | | X | X | |
| E | | | | X | X | | | | |
| F | | | | | | | | X | X |
| G | X | X | | | | (X) | | | |
| H | | | (X) | | X | | | | X |



| BCD input | | | | Decimal output |
|---|---|---|---|---|
| A | B | C | D | |
| 0 | 0 | 0 | 0 | $0 \rightarrow D_0$ |
| 0 | 0 | 0 | 1 | $1 \rightarrow D_1$ |
| 0 | 0 | 1 | 0 | $2 \rightarrow D_2$ |
| 0 | 0 | 1 | 1 | $3 \rightarrow D_3$ |
| 0 | 1 | 0 | 0 | $4 \rightarrow D_4$ |
| 0 | 1 | 0 | 1 | $5 \rightarrow D_5$ |
| 0 | 1 | 1 | 0 | $6 \rightarrow D_6$ |
| 0 | 1 | 1 | 1 | $7 \rightarrow D_7$ |
| 1 | 0 | 0 | 0 | $8 \rightarrow D_8$ |
| 1 | 0 | 0 | 1 | $9 \rightarrow D_9$ |
| 1 | 0 | 1 | 0 | X |
| 1 | 0 | 1 | 1 | X |
| 1 | 1 | 0 | 0 | X |
| 1 | 1 | 0 | 1 | X |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | X |

(3)

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | $D_0$ | $D_1$ | $D_3$ | $D_2$ |
| 01 | $D_4$ | $D_5$ | $D_7$ | $D_6$ |
| 11 | X | X | X | X |
| 10 | $D_8$ | $D_9$ | X | X |

$D_0 = A'B'C'D'$

$D_1 = A'B'C'D$

$D_2 = B'CD'$

$D_3 = B'CD$

$D_4 = BC'D'$

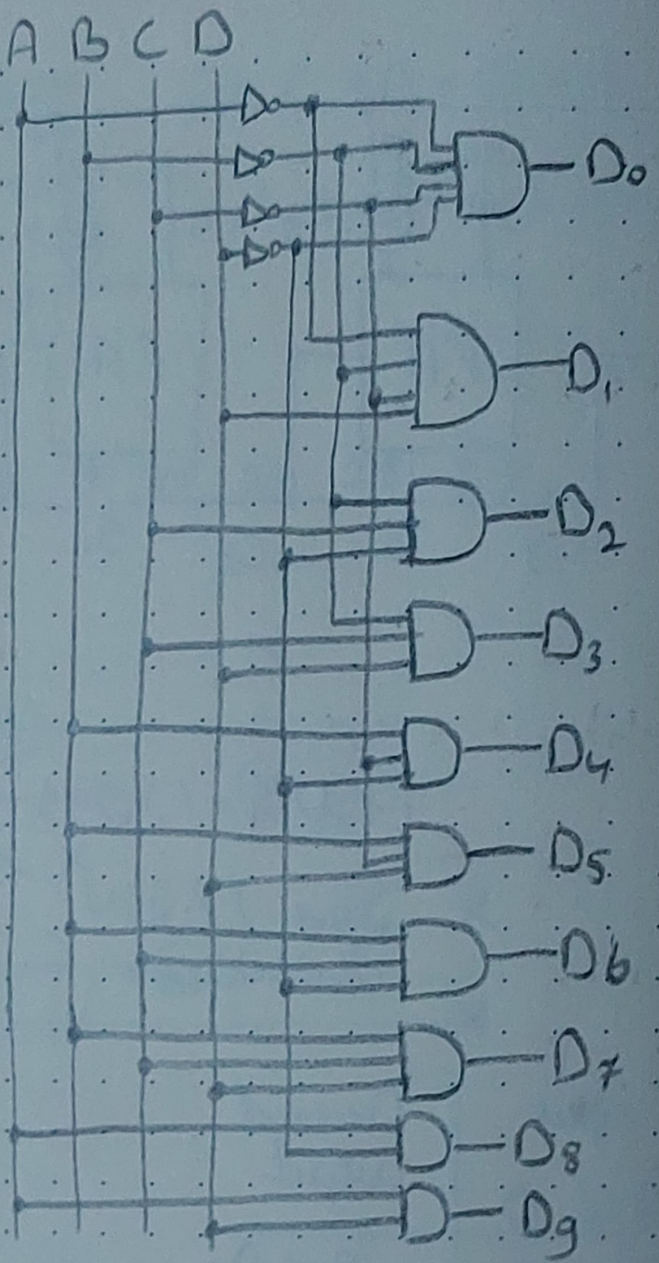
$D_5 = BC'D$

$D_6 = BCD'$

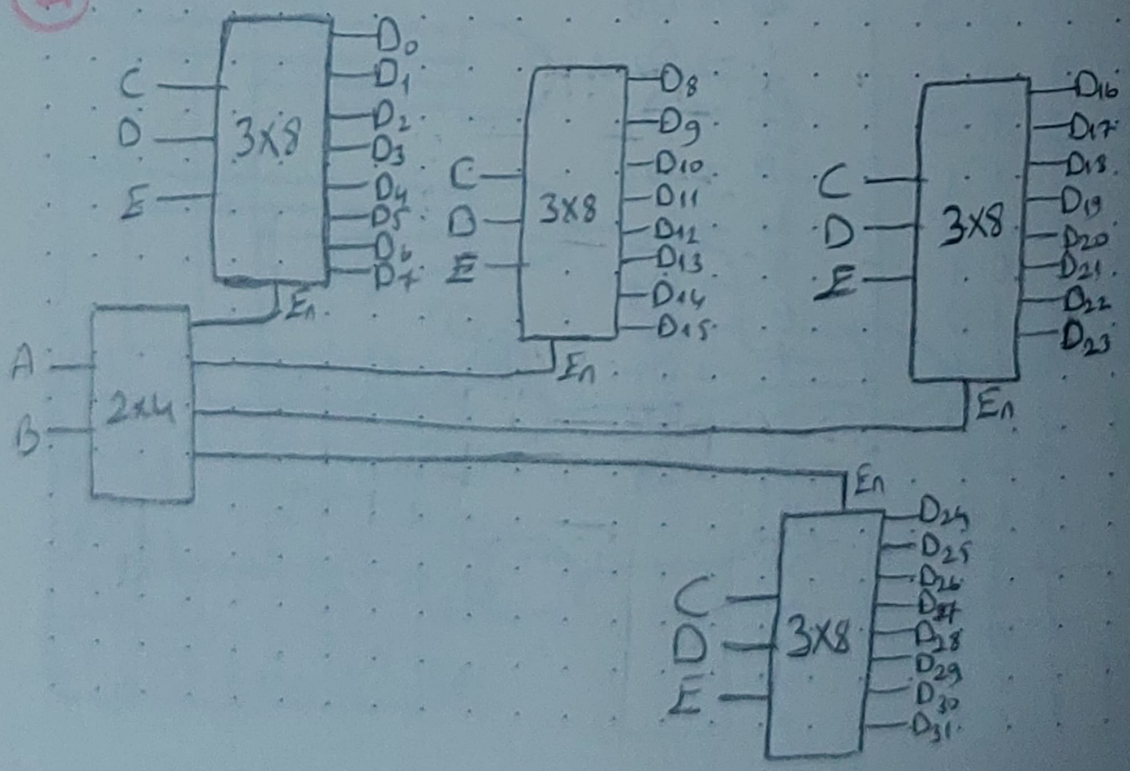
$D_7 = BCD$

$D_8 = AD'$

$D_9 = AD$




(4)



(5)

$f_1 = x'yz' + xz$

$= x'yz' + xyz + xy'z$

0 1 0 | 1 1 1 | 1 0 1

$m_2$ $m_7$ $m_5$

$f_3 = xy'z' + x'y$

1 0 0 | 0 1 1 | 0 1 0

$= xy'z' + x'yz + x'yz'$

$m_4$ $m_3$ $m_2$

$f_5 = x'y'z' + xy$

$= x'y'z' + xyz + xyz'$

0 0 0 | 1 1 1 | 1 1 0

$m_0$ $m_7$ $m_6$

$f_2 = (y' + x)z$

$= y'z + xz = xy'z + x'y'z +$

$xyz + \cancel{xy'z}$

$= xy'z + x'y'z + xyz$

$m_5$ 1 0 1 $m_1$ 0 0 1 1 1 1 $m_7$

$f_4 = y'z' + x'y + yz'$

$= xy'z' + x'y'z' + x'yz + x'yz'$

$+ xyz' + \cancel{x'yz'}$

$= xy'z' + x'y'z' + x'yz + x'yz' + xyz'$

1 0 0 | 0 0 0 | 0 1 1 | 0 1 0 | 1 1 0

$m_4$ $m_0$ $m_3$ $m_2$ $m_6$

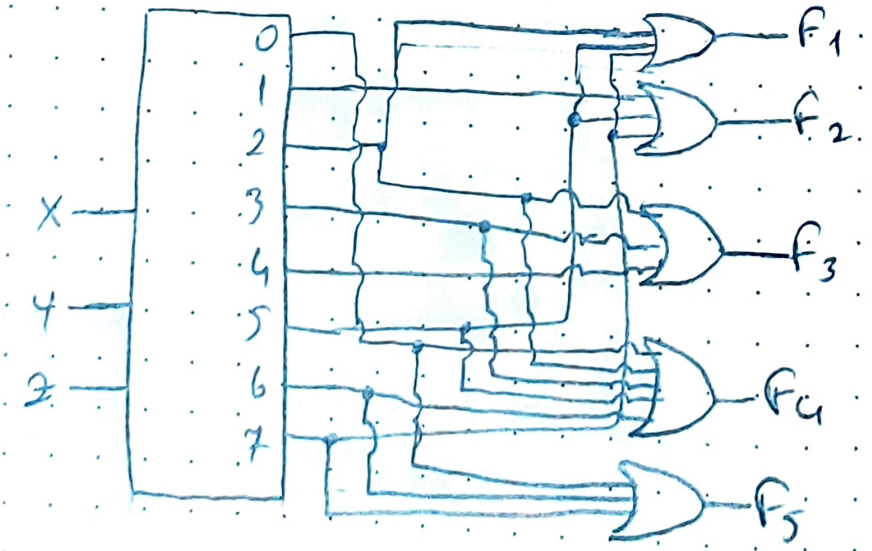
$f_1 = \sum(m_2, m_5, m_7)$

$f_2 = \sum(m_1, m_5, m_7)$

$f_3 = \sum(m_2, m_3, m_4)$

$f_4 = \sum(m_0, m_2, m_3, m_4, m_6)$

$f_5 = \sum(m_0, m_6, m_7)$




Sara ERSOY
04020043

a and b are 1-bit positive integers

$a_3a_2a_1a_0$ $b_3b_2b_1b_0$

$t_0 = (a_0'b_0 + a_0b_0')'$ $t_1 = (a_1'b_1 + a_1b_1')'$

$t_2 = (a_2'b_2 + a_2b_2')'$ $t_3 = (a_3'b_3 + a_3b_3')'$

$x = (a>b) = a_3b_3' + t_3a_2b_2' + t_3t_2a_1b_1' + t_3t_2t_1a_0b_0'$

$z = (a<b) = a_3'b_3 + t_3a_2'b_2 + t_3t_2a_1'b_1 + t_3t_2t_1a_0'b_0$

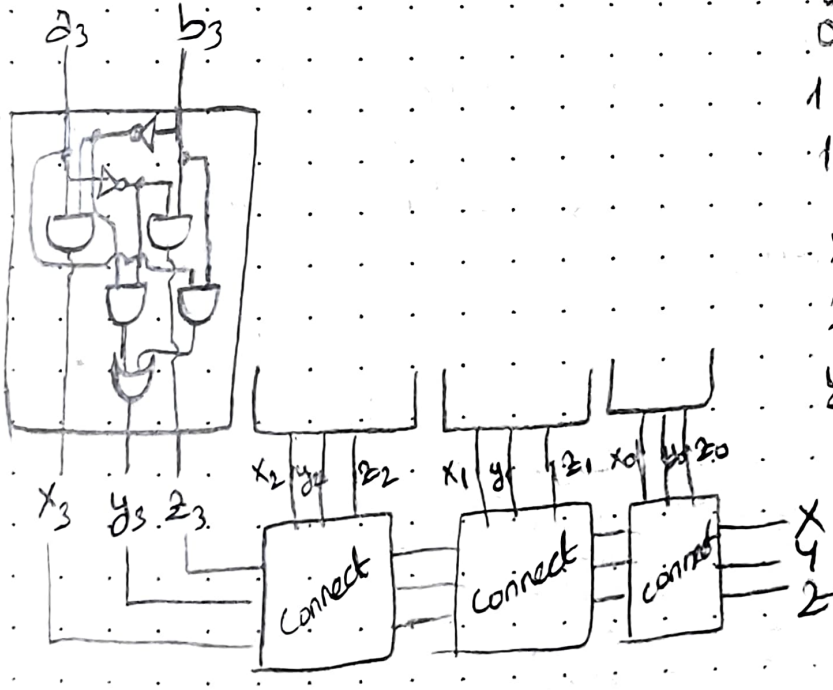
$y = (a=b) = t_3t_2t_1t_0$

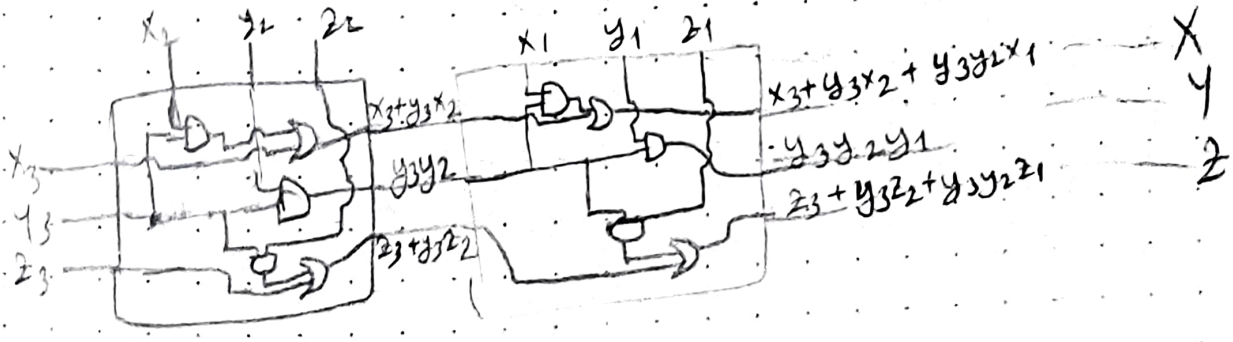
| a | b | x | y | z |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |

$x = ab'$

$z = a'b$

$y = a'b' + ab$



ISE Project Navigator (P.20131013) - /home/ise/Documents/HW4/HW4.xise - [POZ_COMPARE.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- HW4
- xc3s400-4pq208
  - POZ_COMPARE - Behavioral (POZ_C
    - M1 - COMP_1_bit - Behavioral (COM
    - M2 - CON_COMP_1_bit - Behaviora
    - M3 - CON_COMP_1_bit - Behaviora
    - M4 - CON_COMP_1_bit - Behaviora

No Processes Running

Processes: POZ_COMPARE - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simula...
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

Start Design Files Libraries

```
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity POZ_COMPARE is
33      Port ( a3,a2,a1,a0,b3,b2,b1,b0 : in  STD_LOGIC;
34             X,Y,Z : out  STD_LOGIC);
35  end POZ_COMPARE;
36
37  architecture Behavioral of POZ_COMPARE is
38
39  Component COMP_1_bit is
40      Port ( a,b : in  STD_LOGIC;
41             x,y,z : out  STD_LOGIC);
42  end Component;
43
44  Component CON_COMP_1_bit is
45      Port ( ai,bi,xi,yi,zi : in  STD_LOGIC;
46             O4,O5,O6 : out  STD_LOGIC);
47  end Component;
48
49  Signal s1,s2,s3,s4,s5,s6,s7,s8,s9: std_logic;
50
51  begin
52
53  M1: COMP_1_bit port map (a3, b3, s1, s2, s3);
54  M2: CON_COMP_1_bit port map (a2, b2, s1, s2, s3, s4,s5,s6);
55  M3: CON_COMP_1_bit port map (a1, b1, s4, s5, s6, s7,s8,s9);
56  M4: CON_COMP_1_bit port map (a0, b0, s7, s8, s9, X,Y,Z);
57
58  end Behavioral;
59
60
```

CON_COMP_1_bit.vhd | POZ_COMPARE.vhd | POZ_COMPARE (RTL2) | POZ_COMPARE_tb.vhd | COMP_1_bit_tb.vhd

Ln 54 Col 32 VHDL

ISE Project Navigator (P.20131013) - /home/ise/Documents/HW4/HW4.xise - [CON_COMP_1_bit.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- HW4
- xc3s400-4pq208
  - POZ_COMPARE - Behavioral (POZ_C
    - M1 - COMP_1_bit - Behavioral (CON
    - M2 - CON_COMP_1_bit - Behaviora
    - M3 - CON_COMP_1_bit - Behaviora
    - M4 - CON_COMP_1_bit - Behaviora

No Processes Running

Processes: M2 - CON_COMP_1_bit - Behavioral

- Design Utilities
- Check Syntax

```
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity CON_COMP_1_bit is
33      Port ( ai,bi,xi,yi,zi : in  STD_LOGIC;
34             O4,O5,O6 : out  STD_LOGIC);
35  end CON_COMP_1_bit;
36
37  architecture Behavioral of CON_COMP_1_bit is
38
39  Component COMP_1_bit is
40      Port ( a,b : in  STD_LOGIC;
41             x,y,z : out  STD_LOGIC);
42  end Component;
43
44  Component CONNECT is
45      Port ( ix3,ix2,iy3,iy2,iz3,iz2 : in  STD_LOGIC;
46             O1,O2,O3 : out  STD_LOGIC);
47  end Component;
48
49  Signal s1,s2,s3: std_logic;
50
51  begin
52
53  M1: COMP_1_bit port map (ai, bi, s1, s2, s3);
54  M2: CONNECT port map (xi, s1, yi, s2, zi, s3, O4,O5,O6);
55
56  end Behavioral;
57
58
```

Start Design Files Libraries

CON_COMP_1_bit.vhd | POZ_COMPARE.vhd | POZ_COMPARE (RTL2) | POZ_COMPARE_tb.vhd | COMP_1_bit_tb.vhd | COMP_1_bit.

Ln 37 Col 1 VHDL

ISE_14.7_VIRTUAL_MACHINE [Çalışıyor] - Oracle VM VirtualBox

Dosya Makine Görünüm Giriş Aygıtlar Yardım

Applications Places System — Fri Oct 27, 2:11 AM

ISE Project Navigator (P.20131013) - /home/ise/Documents/HW4/HW4.xise - [POZ_COMPARE (RTL2)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Behavioral

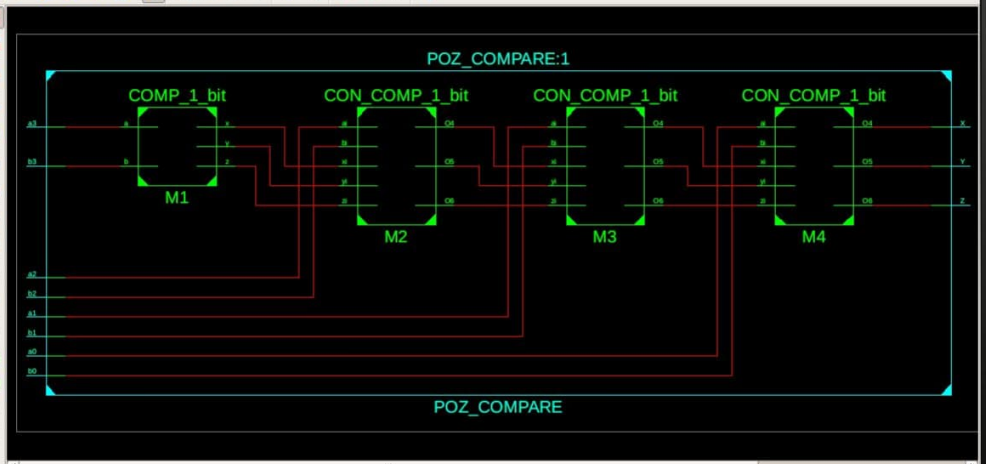
Hierarchy

- HW4
- xc3s400-4pq208
- COMP_1_bit_tb - behavior (COMP_1_b
- POZ_COMPARE_tb - behavior (POZ_C

No Processes Running

Processes: POZ_COMPARE_tb - behavior

- ISim Simulator
  - Behavioral Check Syntax
  - Simulate Behavioral Model




Start Design Files Libraries

CON_COMP_1_bit.vhd | POZ_COMPARE.vhd | POZ_COMPARE (RTL2) | POZ_COMPARE_tb.vhd | COMP_1_bit_tb.vhd

View by Category

**Design Objects of Top Level Block**

Instances: POZ_COMPARE

Pins: POZ_COMPARE

Signals: POZ_COMPARE, a0, a1

**Properties of Instance: POZ_COMPARE**

| Name | Value |
|---|---|
| Type | POZ_COMPARE:1 |
| Part | xc3s400-4pq208 |
| OriginalSymbol | POZ_COMPARE |

Console Errors Warnings Find in Files Results View by Category

[2732,1296]

[Terminal] | [ISE Project Navigator (...] | [Terminal] | [ISE Project Navigator (...] | [Terminal] | [ISE Project Navigator (...] | [Documents - File Brow...]

Right Control

ISE_14.7_VIRTUAL_MACHINE [Çalışıyor] - Oracle VM VirtualBox

Dosya Makine Görünüm Giriş Aygıtlar Yardım

Applications Places System

Fri Oct 27, 2:12 AM

ISE Project Navigator (P.20131013) - /home/ise/Documents/HW4/HW4.xise - [POZ_COMPARE (RTL2)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

HW4

xc3s400-4pq208

POZ_COMPARE - Behavioral (POZ_C

M1 - COMP_1_bit - Behavioral (CON

M2 - CON_COMP_1_bit - Behaviora

M3 - CON_COMP_1_bit - Behaviora

M4 - CON_COMP_1_bit - Behaviora

No Processes Running

Processes: POZ_COMPARE - Behavioral

Design Summary/Reports

Design Utilities

User Constraints

Synthesize - XST

View RTL Schematic

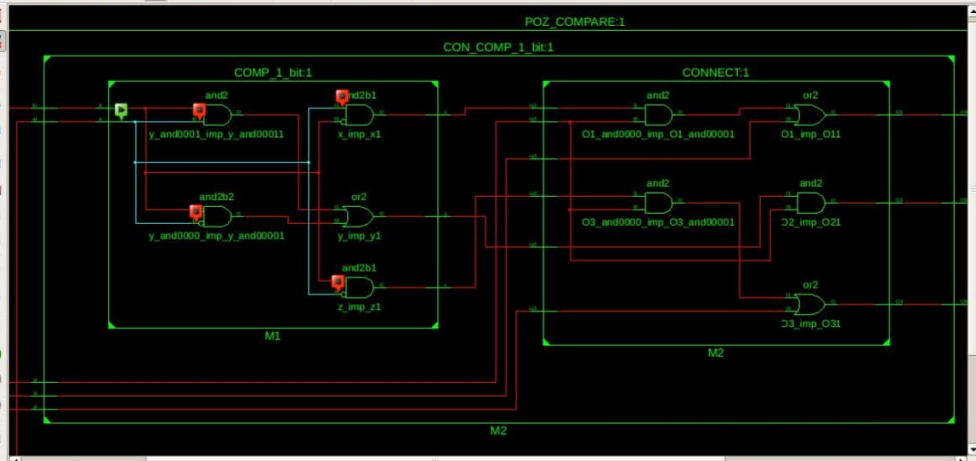
View Technology Schematic

Check Syntax

Generate Post-Synthesis Simu...

Implement Design

Generate Programming File




Start Design Files Libraries

CON_COMP_1_bit.vhd POZ_COMPARE.vhd POZ_COMPARE (RTL2) POZ_COMPARE_tb.vhd COMP_1_bit_tb.vhd

View by Category

Design Objects of Top Level Block

Instances: M2, M1, M2

Pins: bi, M1, M2

Signals: M1, a, b

Properties of Signal: a

| Name | Value |
|---|---|
| PortPolarity | Input |
| PortName | a |
| Name | a |

Console Errors Warnings Find in Files Results View by Category

[2076,2128]

[Terminal] [ISE Project Navigator (... [Terminal] [ISE Project Navigator (... [Terminal] [ISE Project Navigator (... [Documents - File Brow...

Right Control

ISE_14.7_VIRTUAL_MACHINE [Çalışıyor] - Oracle VM VirtualBox

Dosya Makine Görünüm Giriş Aygıtlar Yardım

Applications Places System Fri Oct 27, 2:10 AM

ISim (P.20131013) - [Default.wcfg]

File Edit View Simulation Window Layout Help

Re-launch

Instances and Processes

| Instance and Process Name | Design Unit | Block Type |
|---|---|---|
| poz_compare_tb | poz_compa... | VHDL Entity |
| std_logic_1164 | std_logic_1... | VHDL Package |

| Name | Value |
|---|---|
| a3 | 0 |
| a2 | 0 |
| a1 | 0 |
| a0 | 0 |
| b3 | 0 |
| b2 | 1 |
| b1 | 0 |
| b0 | 0 |
| x | 0 |
| y | 0 |
| z | 1 |

57.005 ns

0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns

X1: 57.005 ns

Instances and Processes | Source Files

Default.wcfg

Console

```
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

Console | Compilation Log | Breakpoints | Find in Files Results | Search Results

Sim Time: 1,000,000 ps

[Terminal] | [ISE Project Navigator (...] | [Terminal] | ISE Project Navigator (... | [Terminal] | ISE Project Navigator (... | Documents - File Brow... | ISim (P.20131013) - [D...

Right Control