Prof. Dr. Berna Örs Yalçın   **Due Date: 11.11.2023**

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EHB205 Introduction to Logic Design
2nd Homework

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Part 1

1) Demonstrate the validity of the following identities by means of truth tables:
   a. $((x + y + z)\, x\, y)' = x'\, y'\, z' + x + y$
   b. $x(x' + y + z) = xy + xz$

2) Simplify the following Boolean expressions to a minimum number of literals:
   a. $ABC + A'B + ABC'$
   b. $(x + y)'\, (x' + y')$
   c. $xy + x\, (wz + wz')$
   d. $(a' + c')\, (a + b' + c')$

3) Boolean functions for the outputs $c_2(a_1,a_0,b_1,b_0)$, $c_1(a_1,a_0,b_1,b_0)$ and $c_0(a_1,a_0,b_1,b_0)$ shown by the below truth table will be implemented in Part 2.
   a. Find sum of product (SOP) representations of the Boolean functions $c_2(a_1,a_0,b_1,b_0)$, $c_1(a_1,a_0,b_1,b_0)$ and $c_0(a_1,a_0,b_1,b_0)$ defined by the below truth table.
   b. Simplify the $c_2(a_1,a_0,b_1,b_0)$, $c_1(a_1,a_0,b_1,b_0)$ and $c_0(a_1,a_0,b_1,b_0)$ Boolean functions.

a_1	a_0	b_1	b_0	c_2	c_1	c_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

Part2

1) Create a new project as explained in your first homework.
2) Take "OR_gate.vhd" and "OR_gate_tb.vhd" files from Ninova. You will design your circuit by changing these files.
3) "Save As" "OR_gate.vhd" file by giving name "Boolean_Function_Case_Statement.vhd" that will be used to define one of your designs.
4) Add your "Boolean_Function_Case_Statement.vhd" file by "Add Sources", "Add or create design sources" to your project.
5) Change the names and the number of inputs and outputs according to the truth table given above. You have four inputs, a_1, a_0, b_1, b_0 and three outputs, c_2, c_1 and c_0.

6) Change the data types of inputs and outputs according to the examples given in the following web pages

- http://www.csit-sun.pub.ro/courses/Masterat/Materiale_Suplimentare/Xilinx%20Synthesis%20Technology/toolbox.xilinx.com/docsan/xilinx4/data/docs/xst/vhdl3.html
- https://startingelectronics.org/software/VHDL-CPLD-course/tut13-VHDL-data-types-and-operators/
- http://www.brunel.ac.uk/~eestmba/hdl/dtypevhdl1.html
- https://en.wikibooks.org/wiki/Programmable_Logic/VHDL_Data_Types
- https://web.engr.oregonstate.edu/~sllu/vhdl/lec2e.html

7) Describe the functionality of your circuit under "architecture begin" by using "case statement" as given in the following web pages

- https://www.ics.uci.edu/~jmoorkan/vhdlref/cases.html
- https://www.nandland.com/vhdl/examples/example-case-statement.html
- https://www.allaboutcircuits.com/technical-articles/sequential-vhdl-if-and-case-statements/
- http://vhdl.renerta.com/mobile/source/vhd00014.htm
- https://insights.sigasi.com/tech/signal-assignments-vhdl-withselect-whenelse-and-case/

8) Make sure that "Boolean_Function_Case_Statement.vhd" is your top module. You can change top module by right click to the module that you would like to implement and choose "Set as Top" from the list. Produce the RTL schematic of your design.

9) "Save As" "OR_gate_tb.vhd" file by giving name "Boolean_Function_Case_Statement_tb.vhd" that will be used to describe your testbench for simulation of your design represented in Part 2.3.

10) Add your "Boolean_Function_Case_Statement_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.

11) Write the test bench file to test your design by using "Boolean_Function_Case_Statement_tb.vhd". You can find examples to write testbenches in VHDL in the following web pages. Simulate your design, produce wave form for your report.

- https://vhdlguide.readthedocs.io/en/latest/vhdl/testbench.html
- https://www.fpgatutorial.com/how-to-write-a-basic-testbench-using-vhdl/
- https://allaboutfpga.com/vhdl-testbench-tutorial/
- https://technobyte.org/testbench-vhdl-types-examples-steps/

12) "Save As" "Boolean_Function_Case_Statement.vhd" file by giving name "Boolean_Function_Data_Flow.vhd" that will be used to describe your second design.

13) Add your "Boolean_Function_Data_Flow.vhd" file by "Add Sources", "Add or create design sources" to your project.

14) Add your "Boolean_Function_Data_Flow.vhd" file to your project.

15) Describe the functionality of your circuit under "architecture begin" by using "data flow modelling" as given in the following web pages

- https://vhdlguide.readthedocs.io/en/latest/vhdl/dataflow.html

- https://www.oreilly.com/library/view/vhdl/9788131732113/xhtml/chapter005.xhtml
- https://buzztech.in/vhdl-modelling-styles-behavioral-dataflow-structural/
- https://www.technobyte.org/vhdl-code-for-an-encoder-dataflow/

16) Make sure that your "Boolean_Function_Data_Flow.vhd" is your top module. Produce the RTL schematic of your design.

17) "Save As" "Boolean_Function_Case_Statement_tb.vhd" file by giving name "Boolean_Function_Data_Flow_tb.vhd" that will represent your testbench for simulation of your second design represented in Part 2.15.

18) Add your "Boolean_Function_Data_Flow_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.

19) Write the test bench file to test your design by using "Boolean_Function_Data_Flow_tb.vhd". Simulate your design.

References

1) Morris Mano, Micheal Ciletti, **Digital Design**, Fifth Edition, Pearson.
2) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010
3) Peter D Minns, **FSM-based digital design using Verilog HDL,** Chichester, England : J. Wiley & Sons , c2008
4) Pong P. Chu, **FPGA prototyping by Verilog examples Xilinx Spartan -3 version**, Hoboken, N.J. : J. Wiley & Sons, c2008