HW3 - 10093

Sens. ERS04

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①

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

For A

x \ yz	00	01	11	10
0	0	0	1	0
1	0	0	1	1

$A = yz + xy = y(z + x)$

For B

x \ yz	00	01	11	10
0	0	1	0	1
1	1	1	0	0

$B = y'z + xy' + x'yz'$

$= x'y'z + x'yz' + xy'z + xy'z'$

$= x'(y \oplus z) + x(y \oplus z)$

$= y \oplus z$

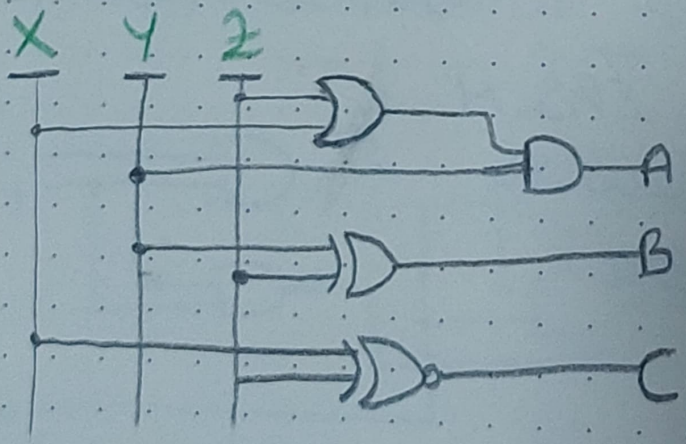
For C

x \ yz	00	01	11	10
0	1	0	0	1
1	0	1	1	0

$C = x'y'z' + xz + x'yz'$

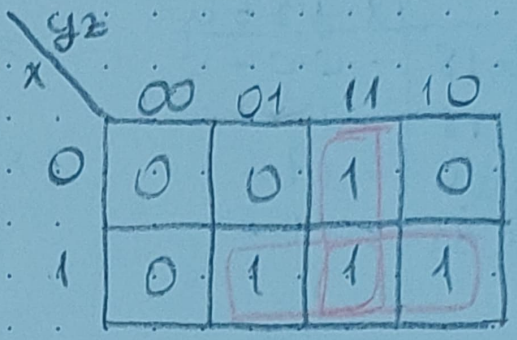
$= x'z' + xz$

$= \overline{x \oplus z}$

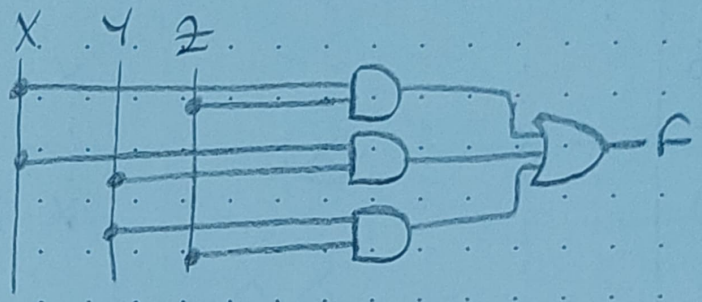


2)

x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



$F = xz + xy + yz$



3)

$m_0 = 00000 = x'y'z't'w'$
$m_2 = 00010 = x'y'z't w'$
$m_{10} = 01010 = x'y z' t w'$
$m_{16} = 10000 = x y' z' t' w'$
$m_{13} = 01101 = x'y z t' w$
$m_{31} = 11111 = x y z t w$
$m_{14} = 01110 = x'y z t w'$
$m_{15} = 01111 = x'y z t w$
$m_{17} = 10001 = x y' z' t' w$
$m_{24} = 11000 = x y z' t' w'$
$m_{28} = 11100 = x y z t' w'$
$m_{29} = 11101 = x y z t' w$

	x y z t w
0	0 0 0 0 0 ✓
2	0 0 0 1 0 ✓
16	1 0 0 0 0 ✓
10	0 1 0 1 0 ✓
18	1 0 0 1 0 ✓
24	1 1 0 0 0 ✓
13	0 1 1 0 1 ✓
14	0 1 1 1 0 ✓
28	1 1 1 0 0 ✓
15	0 1 1 1 1 ✓
29	1 1 1 0 1 ✓
31	1 1 1 1 1 ✓

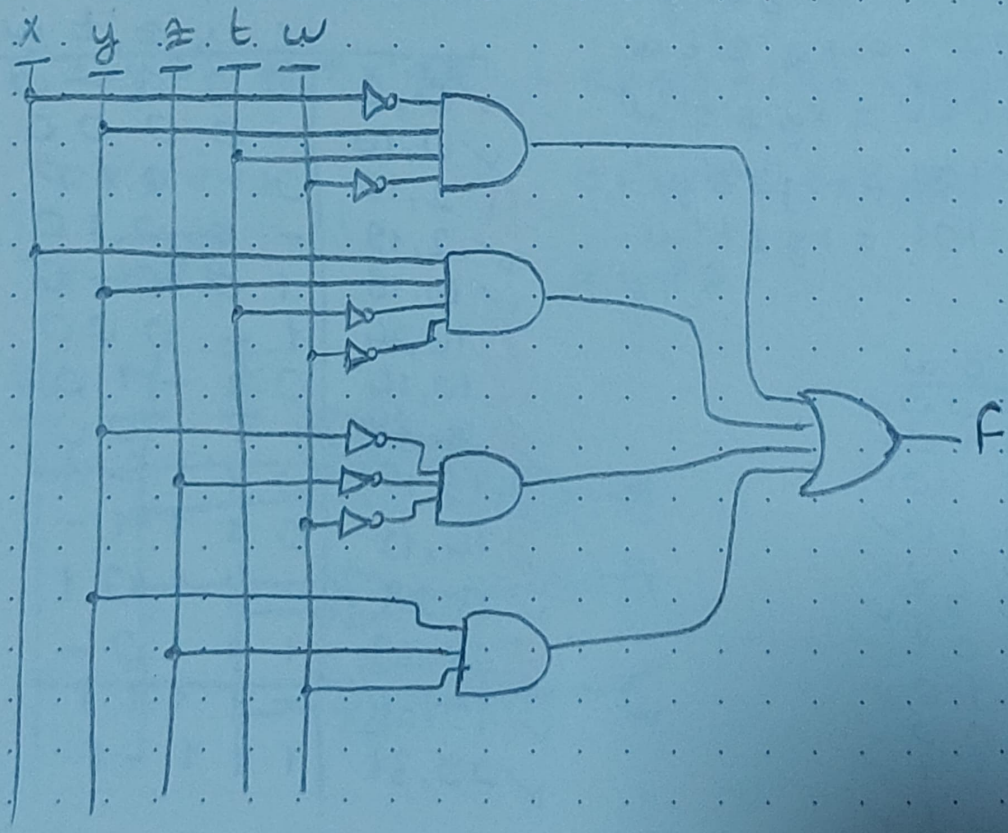
	x y z t w
✓ 0,2	0 0 0 - 0
✓ 0,16	- 0 0 0 0
A 2,10	0 - 0 1 0
✓ 2,18	- 0 0 1 0
✓ 16,18	1 0 0 - 0
B 16,24	1 - 0 0 0
C 10,14	0 1 - 1 0
D 24,28	1 1 - 0 0
✓ 13,15	0 1 1 - 1
E 14,15	0 1 1 1 -
✓ 13,29	- 1 1 0 1
F 28,29	1 1 1 0 -
✓ 15,31	- 1 1 1 1
✓ 29,31	1 1 1 - 1

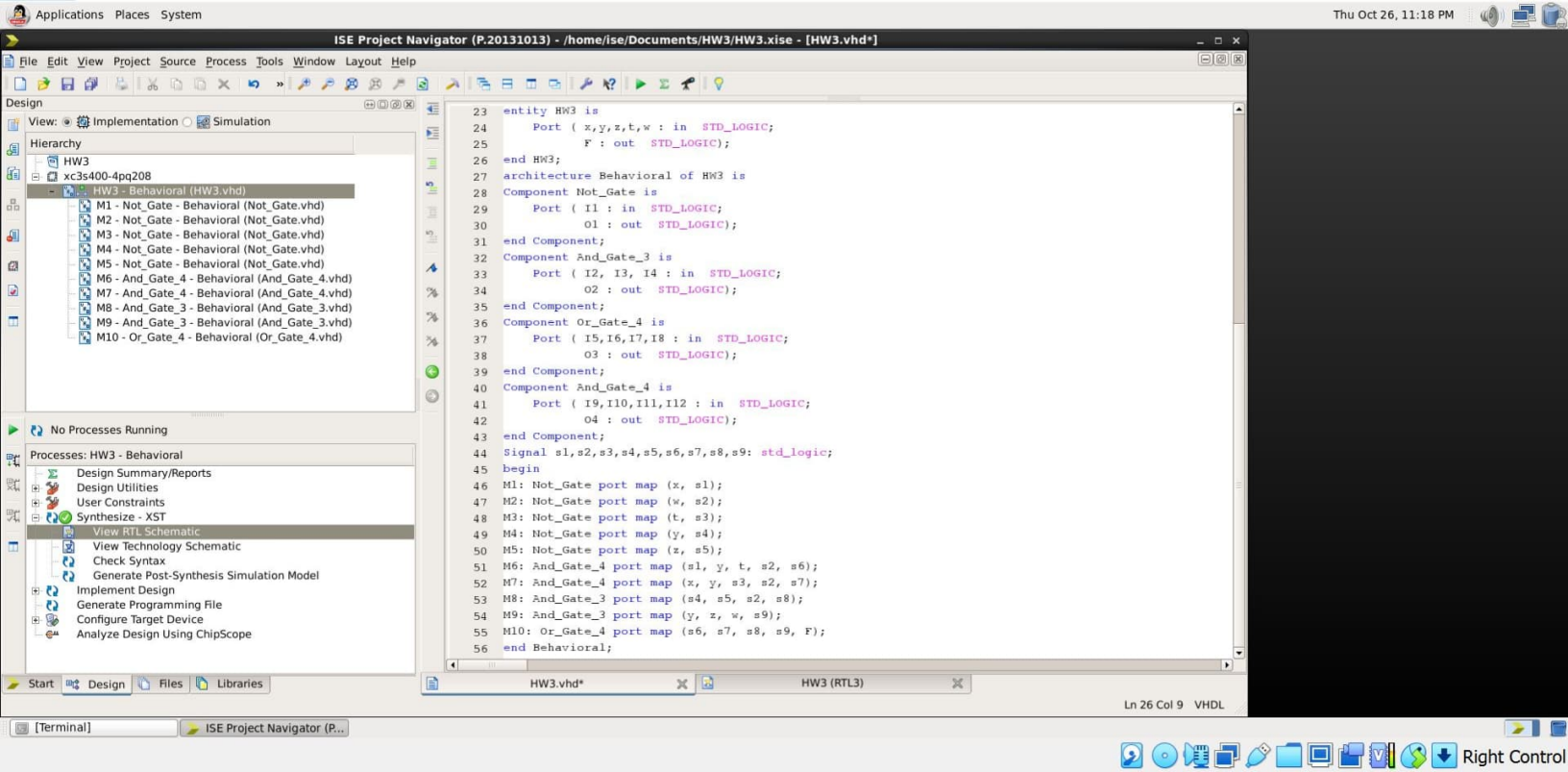
	x y z t w
G 0, 2, 16, 18	- 0 0 - 0
0, 16, 2, 18	- 0 0 - 0
H 13, 15, 29, 31	- 1 1 - 1
~~13, 29, 15, 31~~	- 1 1 - 1

$f = C + D + G + H$

$= x'yt w' + xyt'w' + y'z'w + yzw$

	0	10	13	14	15	18	24	28	29
A		X							
B							X		
C		X		(X)					
D							X	X	
E				X	X				
F								X	X
G	X	X				(X)			
H			(X)		X				X




Applications Places System
Thu Oct 26, 11:18 PM
ISE Project Navigator (P.20131013) - /home/ise/Documents/HW3/HW3.xise - [HW3.vhd*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
HW3
xc3s400-4pq208
HW3 - Behavioral (HW3.vhd)
M1 - Not_Gate - Behavioral (Not_Gate.vhd)
M2 - Not_Gate - Behavioral (Not_Gate.vhd)
M3 - Not_Gate - Behavioral (Not_Gate.vhd)
M4 - Not_Gate - Behavioral (Not_Gate.vhd)
M5 - Not_Gate - Behavioral (Not_Gate.vhd)
M6 - And_Gate_4 - Behavioral (And_Gate_4.vhd)
M7 - And_Gate_4 - Behavioral (And_Gate_4.vhd)
M8 - And_Gate_3 - Behavioral (And_Gate_3.vhd)
M9 - And_Gate_3 - Behavioral (And_Gate_3.vhd)
M10 - Or_Gate_4 - Behavioral (Or_Gate_4.vhd)
No Processes Running
Processes: HW3 - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start Design Files Libraries
23 entity HW3 is
24 Port (x,y,z,t,w : in STD_LOGIC;
25 F : out STD_LOGIC);
26 end HW3;
27 architecture Behavioral of HW3 is
28 Component Not_Gate is
29 Port (I1 : in STD_LOGIC;
30 O1 : out STD_LOGIC);
31 end Component;
32 Component And_Gate_3 is
33 Port (I2, I3, I4 : in STD_LOGIC;
34 O2 : out STD_LOGIC);
35 end Component;
36 Component Or_Gate_4 is
37 Port (I5,I6,I7,I8 : in STD_LOGIC;
38 O3 : out STD_LOGIC);
39 end Component;
40 Component And_Gate_4 is
41 Port (I9,I10,I11,I12 : in STD_LOGIC;
42 O4 : out STD_LOGIC);
43 end Component;
44 Signal s1,s2,s3,s4,s5,s6,s7,s8,s9: std_logic;
45 begin
46 M1: Not_Gate port map (x, s1);
47 M2: Not_Gate port map (w, s2);
48 M3: Not_Gate port map (t, s3);
49 M4: Not_Gate port map (y, s4);
50 M5: Not_Gate port map (z, s5);
51 M6: And_Gate_4 port map (s1, y, t, s2, s6);
52 M7: And_Gate_4 port map (x, y, s3, s2, s7);
53 M8: And_Gate_3 port map (s4, s5, s2, s8);
54 M9: And_Gate_3 port map (y, z, w, s9);
55 M10: Or_Gate_4 port map (s6, s7, s8, s9, F);
56 end Behavioral;
HW3.vhd*
HW3 (RTL3)
Ln 26 Col 9 VHDL
[Terminal]
ISE Project Navigator (P...
Right Control

ISim (P.20131013) - [Default.wcfg]

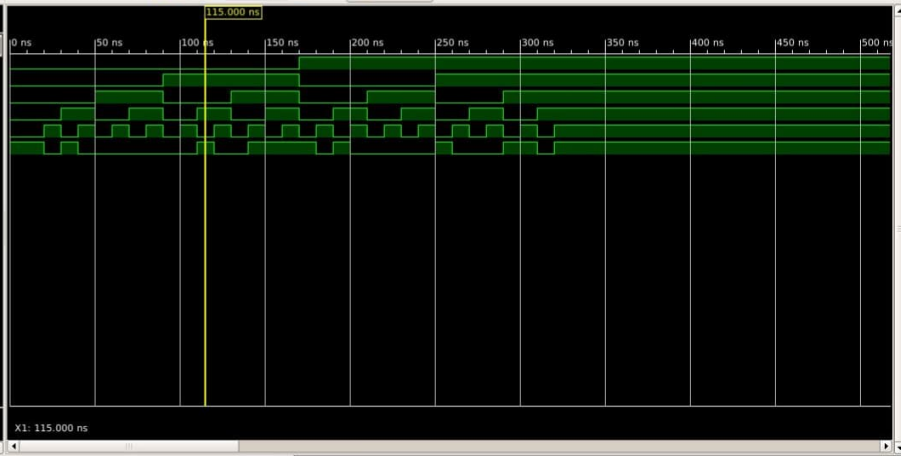
File Edit View Simulation Window Layout Help

Re-launch

Instances and Processes

Instance and Process Name	Design Unit	Block Type
hw3_tb	hw3_tb(beh...	VHDL Entity
std_logic_1164	std_logic_1...	VHDL Package

Name	Value
x	0
y	1
z	0
t	1
w	0
f	1



Instances and Processes | Source Files

Default.wcfg

Console

```
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

Console | Compilation Log | Breakpoints | Find in Files Results | Search Results

Sim Time: 1,000,000 ps

[Terminal] | ISE Project Navigator (... | ISim (P.20131013) - [D...

Right Control

Dosya Makine Görünüm Giriş Aygıtlar Yardım

Applications Places System Thu Oct 26, 11:15 PM

ISE Project Navigator (P.20131013) - /home/ise/Documents/HW3/HW3.xise - [HW3 (RTL3)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

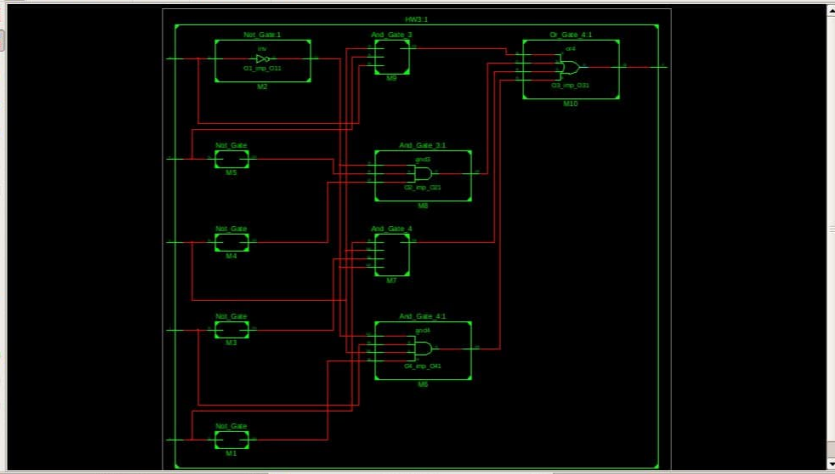
- HW3
- xc3s400-4pq208
- HW3 - Behavioral (HW3.vhd)
  - M1 - Not_Gate - Behavioral (Not_Gate.vhd)
  - M2 - Not_Gate - Behavioral (Not_Gate.vhd)
  - M3 - Not_Gate - Behavioral (Not_Gate.vhd)
  - M4 - Not_Gate - Behavioral (Not_Gate.vhd)
  - M5 - Not_Gate - Behavioral (Not_Gate.vhd)
  - M6 - And_Gate_4 - Behavioral (And_Gate_4.vhd)
  - M7 - And_Gate_4 - Behavioral (And_Gate_4.vhd)
  - M8 - And_Gate_3 - Behavioral (And_Gate_3.vhd)
  - M9 - And_Gate_3 - Behavioral (And_Gate_3.vhd)
  - M10 - Or_Gate_4 - Behavioral (Or_Gate_4.vhd)

No Processes Running

Processes: HW3 - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File

Start Design Files Libraries



HW3.vhd HW3 (RTL3)

View by Category

Design Objects of Top Level Block

Instances: M9, M10

Pins: M8, M10

Signals: M8, M10, s1

Properties: (No Selection)

Name Value

Console Errors Warnings Find in Files Results View by Category

[1400,3488]

[Terminal] ISE Project Navigator (P...)

Right Control