VIJITH P V

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Carrier Objective

Seeking a responsible and career-oriented opportunity in an organization that could utilize my knowledge and ability in a competitive environment, where as a part of team, I can dynamically work towards growth of organization and gain satisfaction thereof.

Personal Profile

- **VLSI Professional** with **more than two years** of experience in **VLSI Front end design** and **FPGA implementation**.
- Good understanding of the **ASIC** and **FPGA** design flow.
- Knowledge of HDLs **VERILOG,VHDL.**
- Works on various industry standard tools **Xilinx Design Suite 14.2**,Altera **Quartus**, Mentor Graphics **Modelsim 10.2d**.
- Works on Xilinx **Spartan 3 SERIES** and Altera **Cyclone** FPGA kits.
- Works on Communication Protocols **UART, I2C, SPI.**
- Works on Image Processing Algorithms like **MEDIAN FILTER,GABOR FILTER,STEGNOGRAPHY**.
- Works on various encoding and decoding modules **VITTERBI ,GOLAY CODEC,REED SOLOMON.**
- Works on various Encryption and Decryption standards **AES,DES,TRIPLE DES,RC5,RC6.**

Technical Skills

- **HDL : VERILOG,VHDL**
- **EDA Tools**
  - Mentor Graphics Tool Suite (ModelSim)
  - Xilinx Design suite 14.2
  - Altera Quartus

- **FPGA kits** : Spartan 3,Spartan 3E
- **Other Languages :** C, Embedded C, Assembly Language (8085, 8051 and PIC)
- **Operating System :** Linux, Windows

Professional Experience

VLSI Design Engineer

Company Name: Focuz Innovations(P) Ltd

Location: Cochin
Period: Jun 2012 – Feb 2014

Design Manager

Company Name: Aspire Technologies

Location: Cochin
Period: May 2011 - Jun 2012

Education

- **Master of science in Electronics** at St.Thomas college Thrissur, Calicut University, Kerala, India in 2008-2010.
- Division Attained – **First Class** (**70.83**%)

Academic Activities	**Project Name**	**Description**
Main project	"Touch screen controlled data collection robot"	It is a data collection robot which is controlled by touch screen keypad.The robot is collected data wherever it moves and the collected data is sent back to control station using zigbee.
Seminar	"Brain Machine Interface"	This uses brain activity to command,control,actuate and communicate with the world directly through brain integration with peripheral devices and systems.
Core Subjects	Advance digital signal processing,Telematics,Embedded system Artifical intelligence,VLSI design, tool & technology.	

- **Bachelor of Science in Electronics** at Prajyoti Nikethan College pudukad, Calicut University, Kerala, India in 2005-2008.
- Division Attained – **First class**(**80.70**%)

Works	Project Name	Description
Main project	**“** Wireless power distribution control system ” **.**	Different power sections are controlled wirelessly by master station using RF module.
Core subjects	Control System and Biomedical equipments,Microwave and Television Engineering, Digital Signal Processing and Semiconductor Fabrication Technology,C++ and Network theory.	
Lab Experiments	Electronic Circuits, Digital Circuits, Analog Circuits, Microprocessor 8085, Communication (Analog and Digital).	

- **Intermediate** (Twelfth Standard) St.Antonys H.S.S, Pudukad, Thrissur, Board of Higher Secondary Education, Kerala, India in 2003-2005
  Percentage of marks:78%

- **High School** (Tenth Standard) Deepthi High School Thalore, Board of Public Education, Kerala, India in 2003
  Percentage of marks:80.83%

Projects

- Median Filter
  - HDL:VHDL
  - Tool: Xilinx ISE 14.2,Spartan 3E kit
  - Median filter mechanism use to remove the salt and pepper noise interfere in image and to reconstruct clarity of image
  - It comprises of three modules
    - Window Selection
    - Sorting
    - Threshold
    - Window Append

- Qpsk Modem
  - HDL:Verilog
  - Tool: Xilinx ISE 14.2,Spartan 3E kit
  - Qpsk modem is used mainly for long distance communications especially satellite communications.
  - It has mainly two modules
    - Modulator
      - Carrier wave generator

- PN generator
- Qpsk mapping
- Demodulator

- PID Controller for DC Motor Speed Control System

  - HDL:Verilog
  - Tool: Xilinx ISE 14.2,Spartan 3E kit
  - The project contains PWM generation, motor control, feedback mechanism
  - The Fpga part reads the values form sensor module connected externally ,according with this value desired counts are generated from PID top module part and with this control signal different pwm waves are generating and thus vary the speed of motor.

- Serial Communication Interface with Error Detection Scheme

  - HDL:Verilog
  - Tool: Xilinx ISE 14.2,Spartan 3E kit
  - The project consists of four modules hamming encoder and decoder for error detection and correction and uses UART transmitter and Detector

References

Rajeev C R

Job Title	**:**	Technical Manager
Company	**:**	Aspire Technologies
Email	**:**	aspire.rajeev@gmail.com
Telephone	**:**	9447122922
Type	**:**	Professional

Declaration

I here by declare that the above information given by me is true to the best of my Knowledge.

Place: **VIJITH PV**

Date: