

Realtek Ameba1 DEV01 User Manual

This document define pin out of Ameba DEV.

Version 1.8



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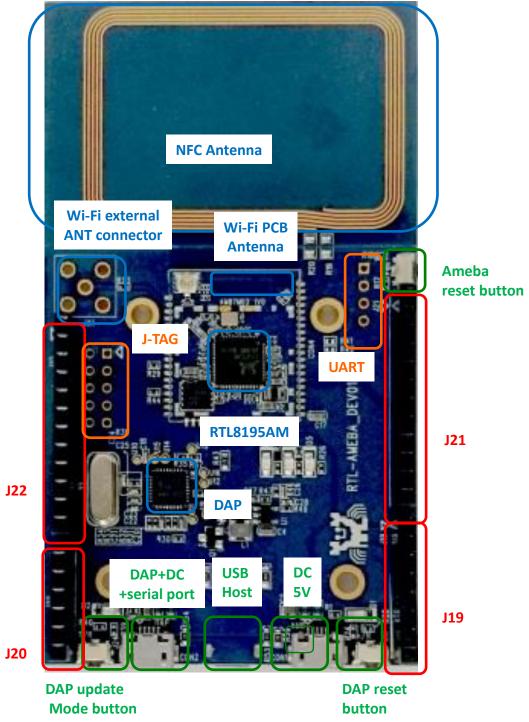


1 Hardware block diagram

• IC: RTL8195AM

Module HDK version: HDK-AM95A03_1V0

DEV HDK version: RTL-AMEBA_DEV01_1v1





2 System requirements

- Windows PC (XP, Vista, 7)
- USB type A to Micro-B USB cable x 1
- RS-232 to UART board(debug) x 1, JTAG cable x1 (option)

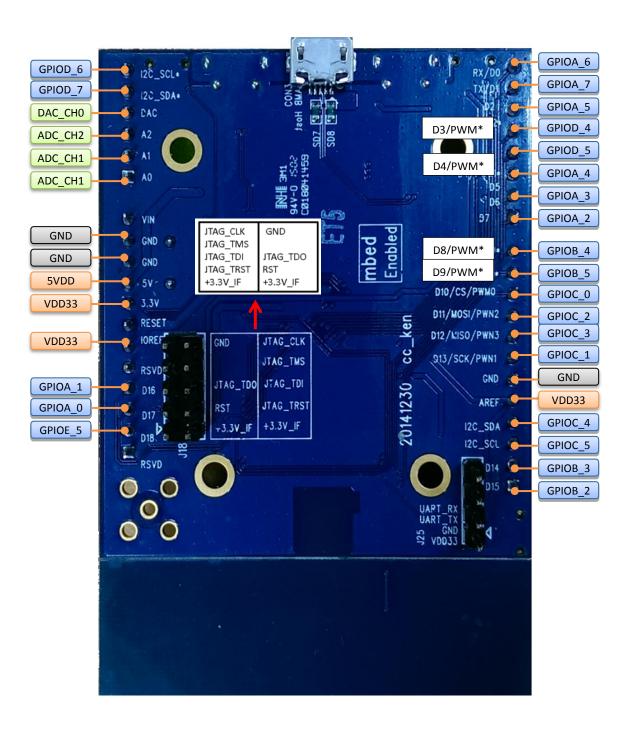
3 Pin out reference

3.1 Pin out table

Con	DEV name	Pin	Net name	Con	DEV name	Pin	Net name
	I2C_SCL	6	GPIOD_6		RX/D0	8	GPIOA_6
	I2C_SDA	5	GPIOD_7		TX/D1	7	GPIOA_7
	DAC	4	DAC_CH0		D2	6	GPIOA_5
120	A2	3	ADC_CH2	110	D3/PWM*	5	GPIOD_4
J20	A1	2	ADC_CH1	J19	D4/PWM*	4	GPIOD_5
	A0	1	ADC_CH1		D5	3	GPIOA_4
					D6	2	GPIOA_3
					D7	1	GPIOA_2
Con	DEV name	Pin	Net name	Con	DEV name	Pin	Net name
	VIN	12	NC		D8/PWM*	12	GPIOB_4
	GND	11	GROUND		D9/PWM*	11	GPIOB_5
	GND	10	GROUND		D10/CS/PWM0	10	GPIOC_0
	5V	9	5VDD		D11/MOSI/PWM2	9	GPIOC_2
	3.3V	8	VDD33		D12/MISO/PWM3	8	GPIOC_3
sJ22	RESET	7	NC	J21	D13/SCK/PWM1	7	GPIOC_1
SJ 2.2	IOREF	6	VDD33	$\int J \mathcal{L} 1$	GND	6	GND
	RSVD	5	NC		AREF	5	VDD33
	D16	4	GPIOA_1		I2C_SDA*	4	GPIOC_4
	D17	3	GPIOA_0		I2C_SCL*	3	GPIOC_5
	D18	2	GPIOE_5		D14	2	GPIOB_3
	RSVD	1	NC		D15	1	GPIOB_2

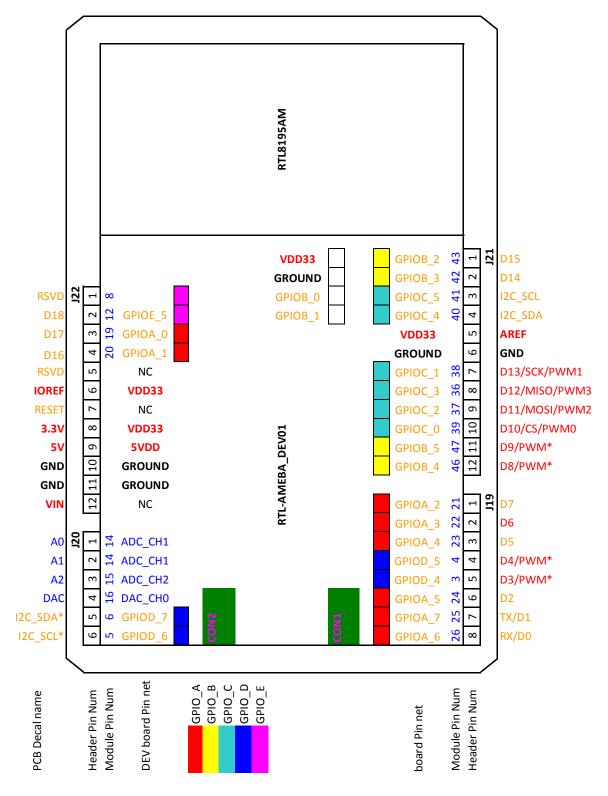


3.2 Pin out reference





3.3 Pin connection table



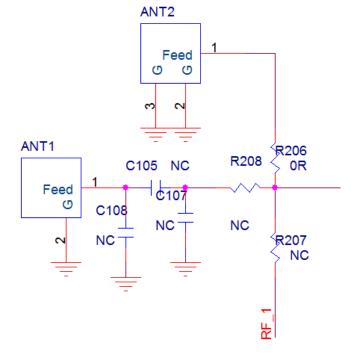


4 Antenna hardware setup

■ I-PEX/U.FL connector: R206

External antenna: R207

■ PCB antenna: R208







5 Peripherals support

• Debug UART: GPIOB_[0..1]

• JTAG: GPIOE_[0..4]

5.1 Pin function table setup

• Multiple functions are supported by group setup.

- For example: GPIOA_6(Rx), GPIOA_7(Tx), GPIOA_3(RTS) and GPIOA_5(CTS) are used if UART0 function. GPIOA_3(RTS) and GPIOA_5(CTS) can not be used as other functions.
- For example: GPIOC_0, GPIOC_1, GPIOC_2, GPIOC_2, GPIOC_3 are used if PWM is occupied. GPIOC_1(PWM1) and GPIOC_2(PWM2) can not be used as other functions.

PIN name	JTAG	SDD	SDH	МП	UART Group	I2C Group	CDT Group	I2S Group	PCM Group	WL_LED	PWM	ETE	WKDT	GPIO INT	Default State	SCHMT
GPIOA_0		SD_D2	SD_D2	MII_RX_CK	UART2_IN		SPI1_MISO							GPIO_INT	PH	0
GPIOA_1		SD_D3	SD_D3	MII_RXD0	UART2_CTS		SPI1_MOSI							GPIO_INT	Н	
GPIOA_2		SD_CMD	SD_CMD	MII_RXD1	LIART2_RTS		SPI1_CLK								PH	0
GPIOA_3		SD_CLK	SD_CLK	MII_RXD2	UARTO_RTS			SPL							PH	0
GPIOA_4		SD_D0	SD_D0	MII_RXD3	UART2_OUT	لحممنا	SPI1_CS								PH	
GPIOA_5		SD_D1	SD_D1	MII_RXDV	UARTO_CTS	UAKT							D_SBY0		PH	
GPIOA_6		SD_INT	SD_CD	MII_RXERR	UARTO_IN										PH	
GPIOA_7			SD WP	MII_COL	UARTÓ OUT										Н	
GPIOB_0					UART_LOG_OUT							ETE0	D_SLP0		Н	
GPIOB_1		SD	IIO	_ <	UART_LÓG_IN					WL_LED0		ETE1			PH	
GPIOB_2				•		12C3_SCL						ETE2			Н	0
GPIOB_3		Debu	g con	sole		12C3 SDA						ETE3		GPIO_INT	PH	
GPIOB_4			0			inc				WL_LED0	PWM0			GPIO_INT	PH	
GPIOB_5						120				WL_LEDO	DM/M1				PH	0
GPIOC_0				MII_TXD2	UARTO_IN	SPI	SPIO_CSO	12S1_WS	PCM1_SYNC		PWM0	ETE0			Н	
GPIOC_1				MII_TXD1	UARTO_CTS	SPI	SPIO_CLK	I2S1_CLK	PCM1_CLK		PWM1	ETE1		GPIO_INT	Н	0
GPIOC_2				MII_TXD0	UARTO_RTS	7	SPI0_MOSI	I2S1_SD_TX	PCM1_OUT		PWM2				Н	
GPIOC_3				MII_TX_CK	UARTO_OUT		SPI0_MISO	I2S1_MCK	PCM1_IN		PWM3			GPIO_INT	Н	0
GPIOC_4				MII_TXD3	12C 1	_	SPIO_CS1	I2S1_SD_RX	1 128	•		PV	VM	GPIO_INT	ΗI	
GPIOC_5				MII_TXEN		I2C1_SCL	SPIO_CS2							GPIO_INT	ΗI	0
GPIOD_4				MII_MDC		I2CO_SDA	SPI1_CS		PCM1_SYNC		PWM0	ETE0		GPIO_INT	PH	0
GPIOD_5	JTAG			MII_MDIO	UART2_CTS	12CO_SCL	SPI1_CLK		PCM1_CLK		PWM1	_	D_SBY2	GPIO_INT	PH	0
GPIOD_6					UART2_RTS	I2C1_SCL	SPI1_MOSI	12S0_SD_RX	PCM1_OUT		PWM2	ETE2		GPIO_INT	PH	0
GPIOD_7	_				UART2_OUT	I2C1_SDA	SPI1_MISO		PCM1_IN		PWM3	ETE3		GPIO_INT	PH	0
	JTAG_TRST				UARTO_OUT	I2C2_SCL	SPIO_CSO	12S0_WS	PCM0_SYNC		PWM0				PH	0
	JTAG_TDI				UARTO_RTS	I2C2_SDA	SPIO_CLK	12SO_CLK	PCM0_CLK		PWM1			GPIO_INT	PH	0
	JTAG_TDÓ				UARTO_CTS	I2C3_SCL	SPI0_MOSI	I2SO_SD_TX	PCM0_OUT		PWM2			GPIO_INT	PH	0
	JTAG_TMS				UARTO_IN			I2SO_MCK	PCM0_IN		PWM3		D_SBY3	GPIO_INT	PH	0
GPIOE_4	JTAG_CLK					I2C3_SCL	SPIO_CS1								PH	0



5.2 Peripheral Descriptions

		Baud rate				
	UART_LOG	38400 Hz				
UART	UART0	4 MHz				
	UART2	4 MHz				
		Clock rate				
	SPI0_Master	20.8 MHz				
SPI	SPI0_Slave_TRx	4.1 MHz				
J SFI	SPI1_Master	41.6 MHz				
	SPI1_Slave_TRx					
		Clock rate				
	Standard mode	0~100 kb/s				
I2C	Fast mode	<400 kb/s				
	High-speed mode	<3.4Mb/s				

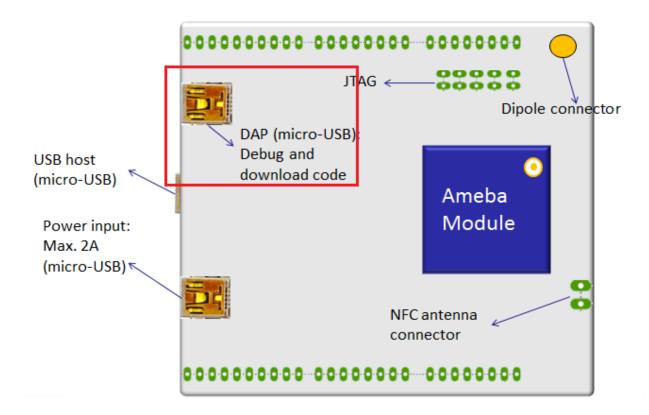


6 Hardware configuration

6.1 CMSIS-DAP

RTL-AMEBA_DEV01 supports CMSIS-DAP debugger. It requires installing "serial to USB driver"at first. Serial to USB driver can be found in tools\serial_to_usb\mbedWinSerial_16466.

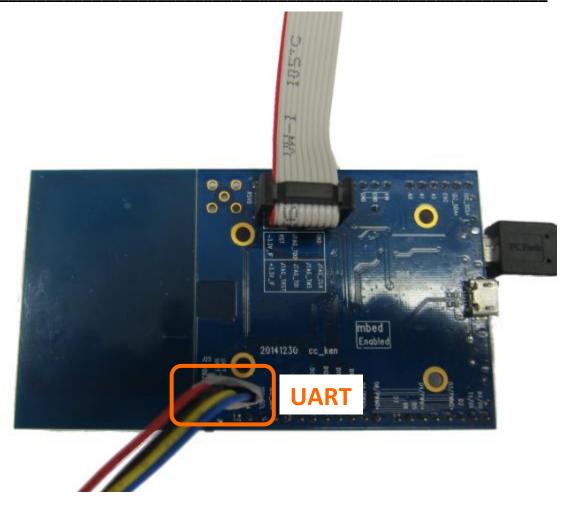
Connect board to the PC with micro-USB cable.



6.2 J-Link/JTAG

Weld JTAG and log UART connectors to HDK board and connect with pitch 2.54mm 2x5pins connector. It is recommended to weld the connector on the bottom side. Users can connect extension boards from top side.





Dupont Line or 2.54mm 2x5 pins connector.

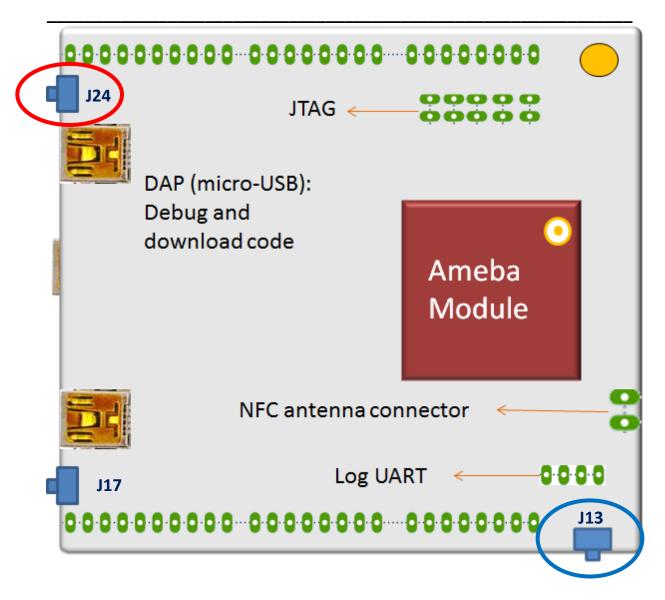




<u>Power On(Disable DAP mode)</u>

Holding TGT_NRESET button (J24, red-circled) then press Pdn button (J13, blur-circled). Release the button after power on.



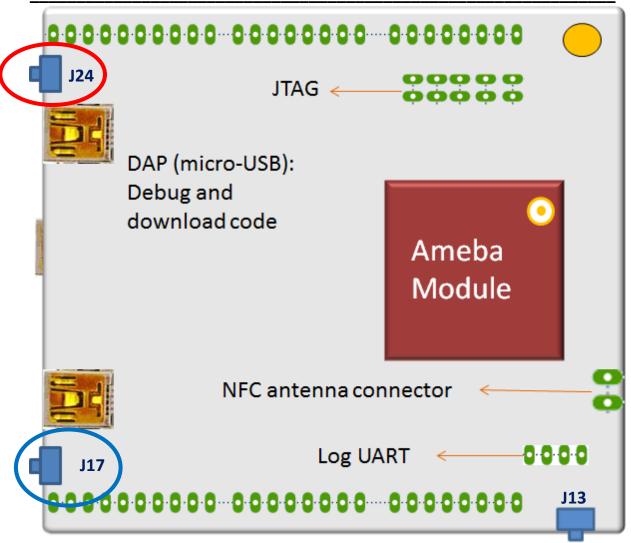


6.3 DAP mode

In DAP mode, the DAP firmware can be updated.

Holding TGT_NRESET button (J24, red-circled) then press nRESET button (J17, blur-circled). Then the DAP mode window will show up.



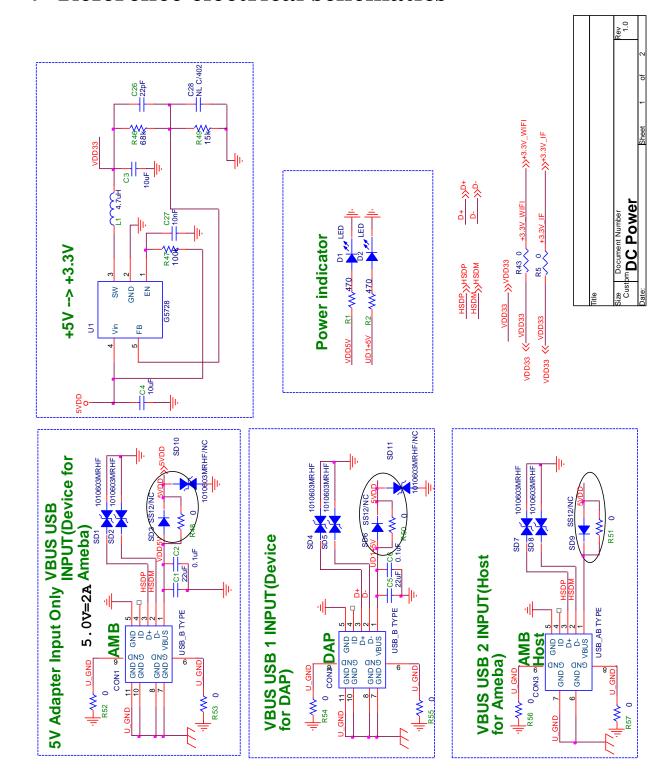


DAP window will show up when entering DAP mode.

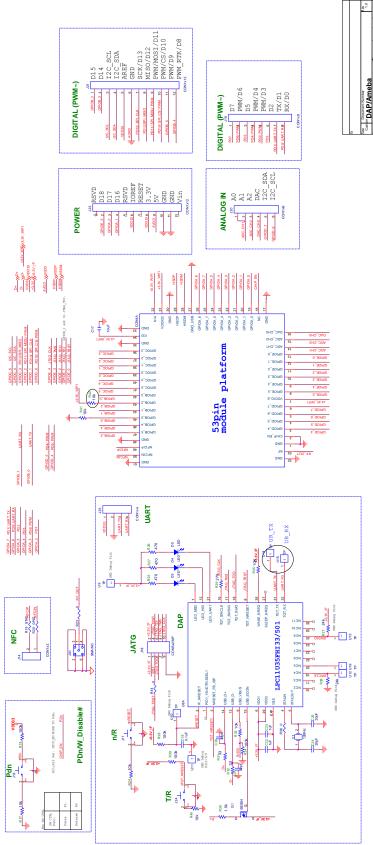




7 Reference electrical schematics

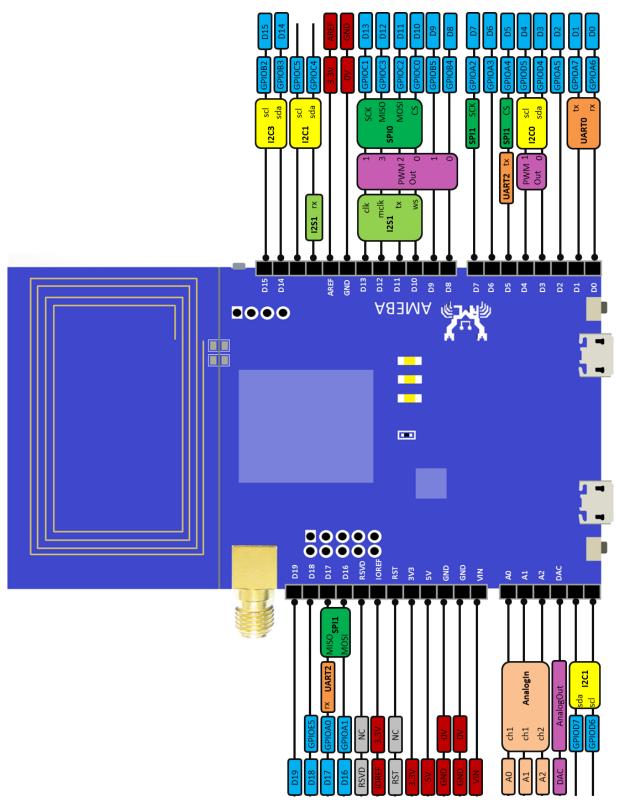








8 Ameba1 DEV01 pin out





9 Sensor board

• Extension board: RTL-AMEBA_EXT B2_2V0

