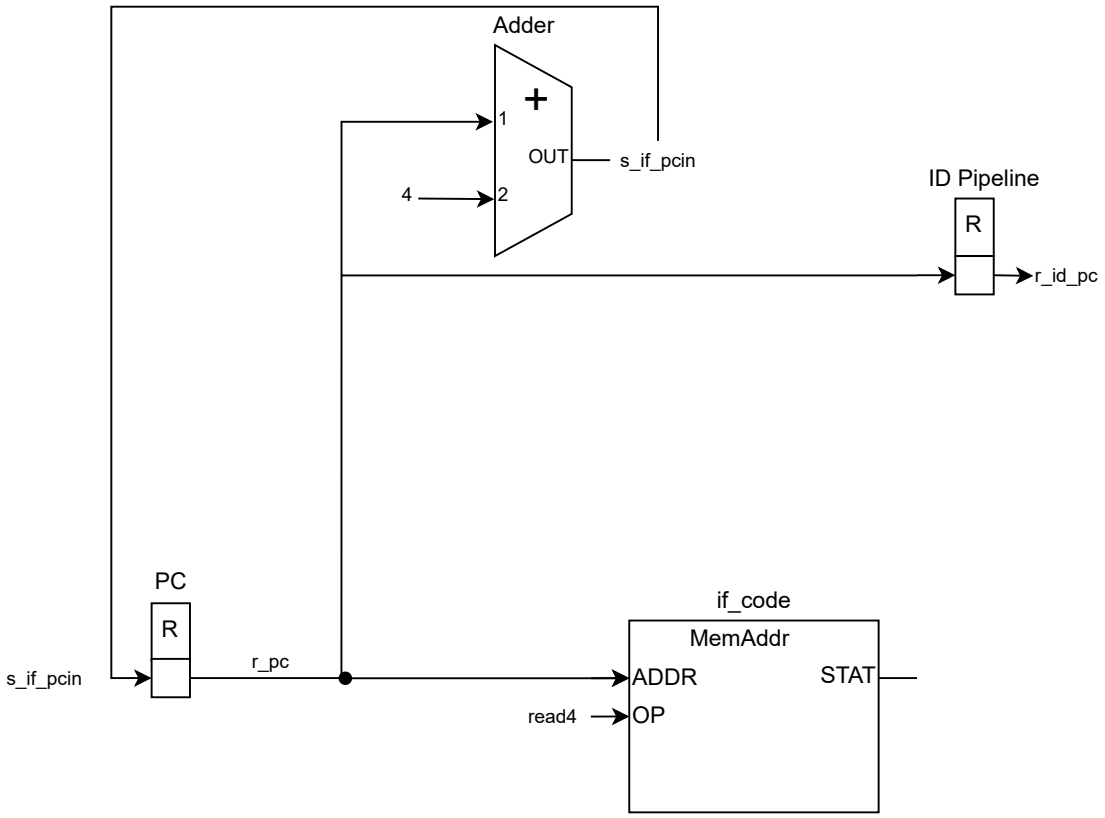
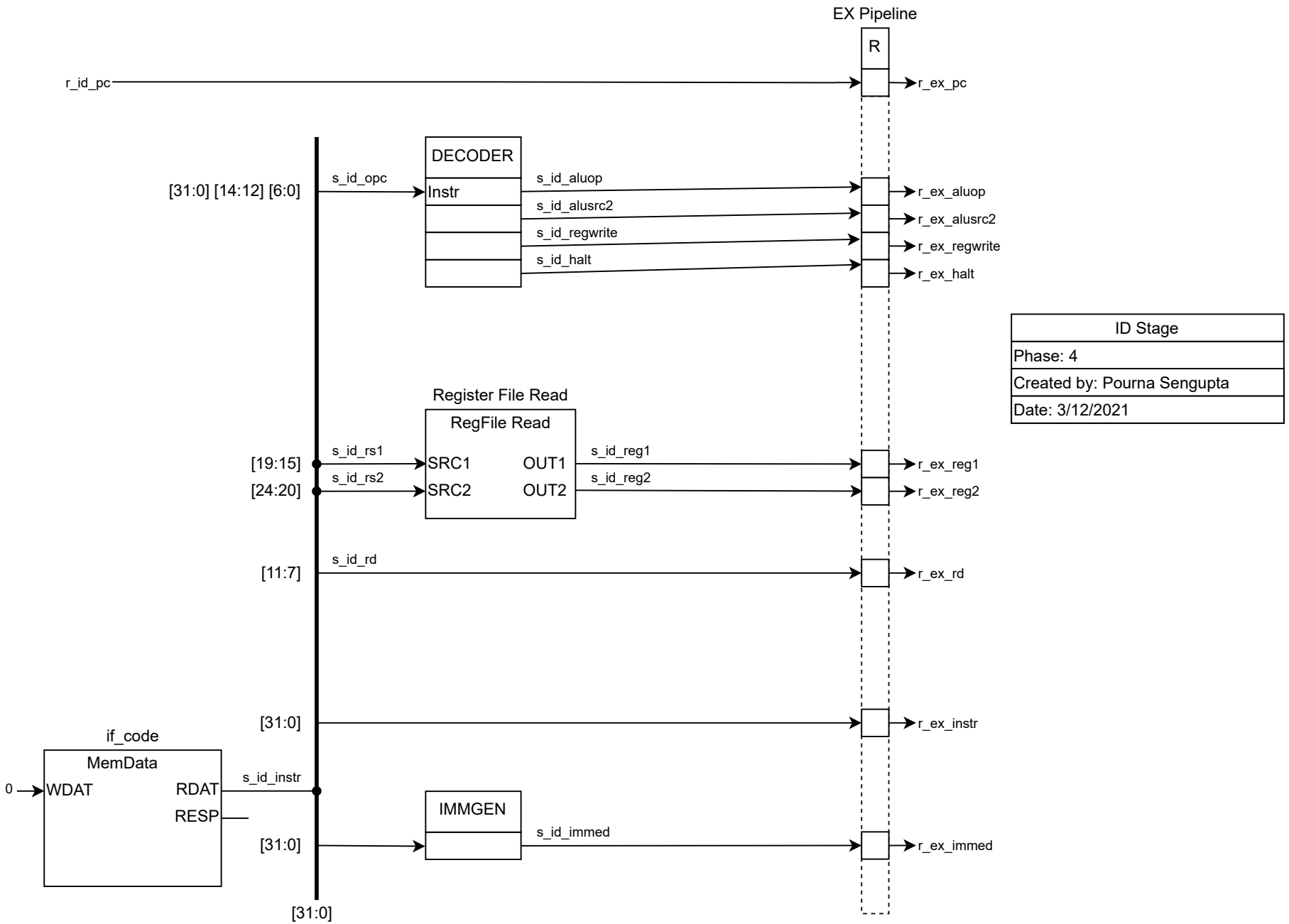
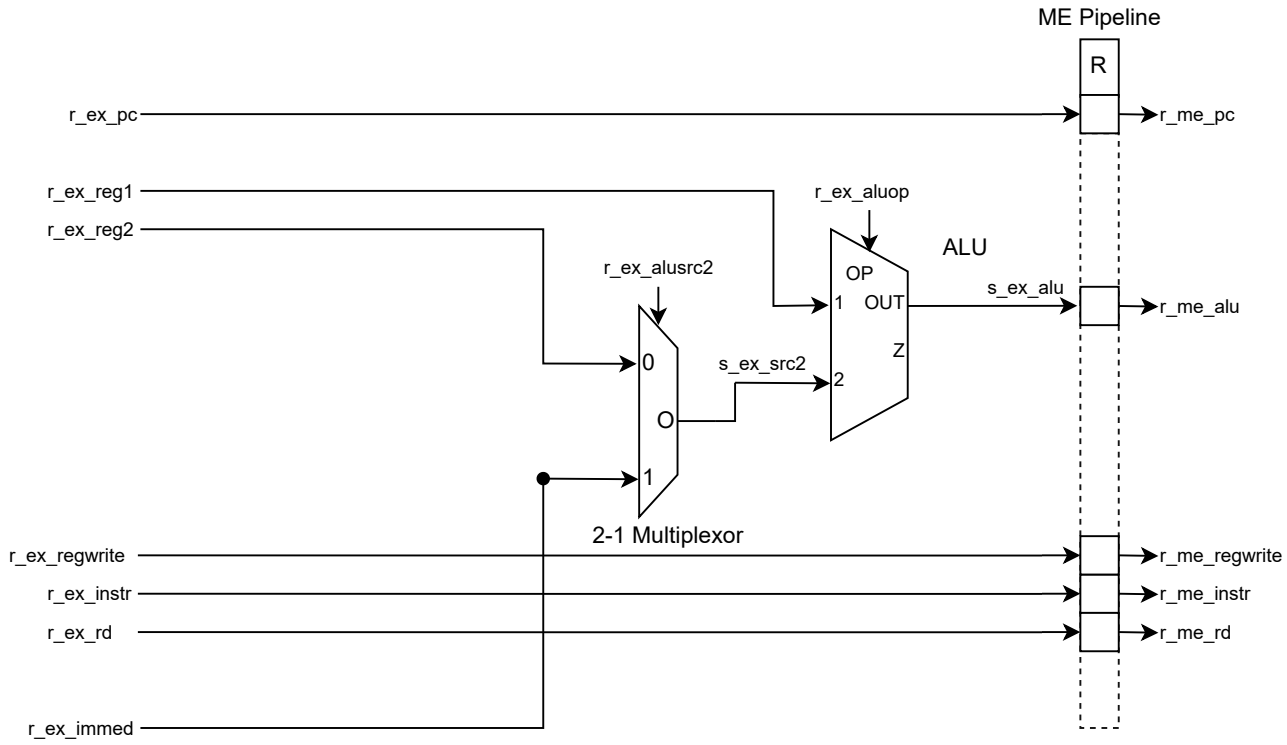
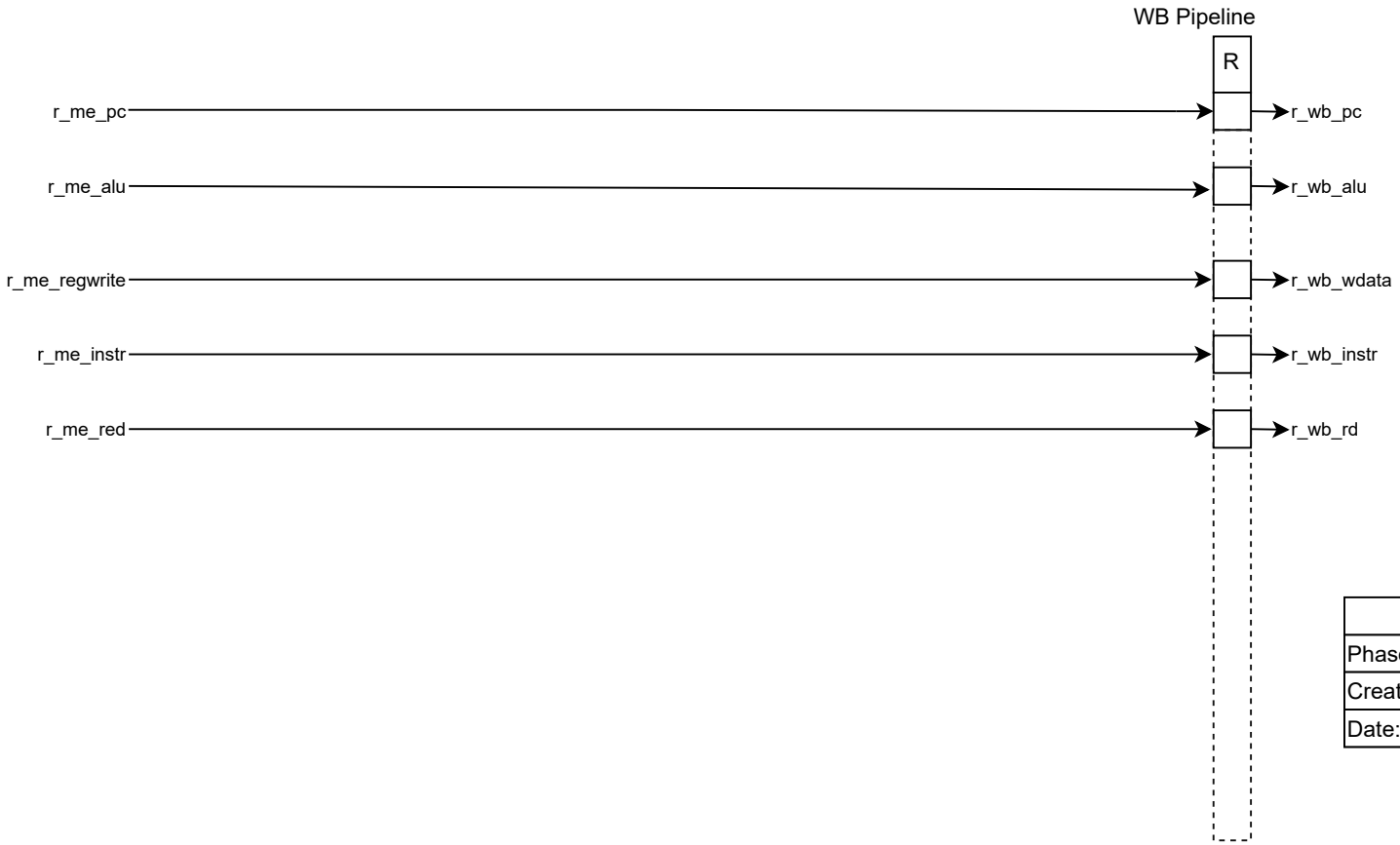
IF Stage
Phase: 4
Created by: Pourna Sengupta
Date: 3/12/2021




EX Pipeline
R
r_id_pc
r_ex_pc
DECODER
[31:0] [14:12] [6:0]
s_id_opc
Instr
s_id_aluop
s_id_alusrc2
s_id_regwrite
s_id_halt
r_ex_aluop
r_ex_alusrc2
r_ex_regwrite
r_ex_halt
ID Stage
Phase: 4
Created by: Pourna Sengupta
Date: 3/12/2021
Register File Read
RegFile Read
[19:15]
[24:20]
s_id_rs1
s_id_rs2
SRC1
SRC2
OUT1
OUT2
s_id_reg1
s_id_reg2
r_ex_reg1
r_ex_reg2
[11:7]
s_id_rd
r_ex_rd
[31:0]
r_ex_instr
if_code
MemData
0
WDAT
RDAT
RESP
s_id_instr
IMMGEN
[31:0]
s_id_immed
r_ex_immed
[31:0]

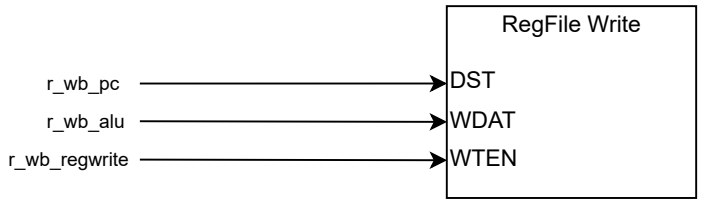


EX Stage
Phase: 4
Created by: Pourna Sengupta
Date: 3/12/2021



ME Stage
Phase: 4
Created by: Pourna Sengupta
Date: 3/12/2021

Register File Write

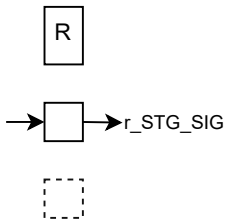


WB Stage
Phase: 4
Created by: Pourna Sengupta
Date: 3/12/2021

Signal Labels

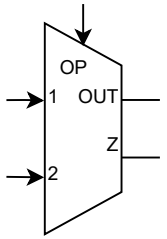
Signals In	Signals Out	Signals Internal
r_STG_SIG	s_STG_SIG	s_STG_SIG
s_STG_SIG		

Register

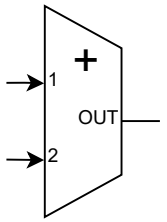


Arithmetic

ALU

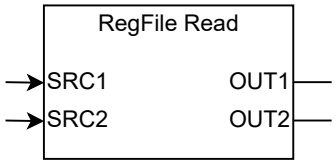


Adder

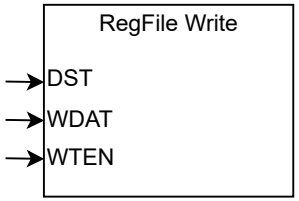


Register File

Register File Read

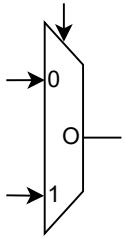


Register File Write

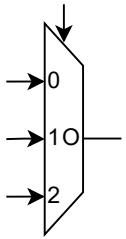


Multiplexors

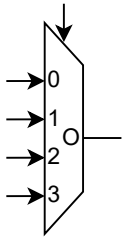
2-1 Multiplexor



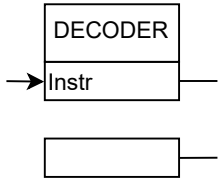
3-1 Multiplexor



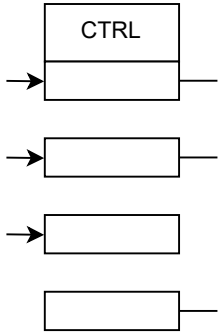
4-1 Multiplexor



Decoder

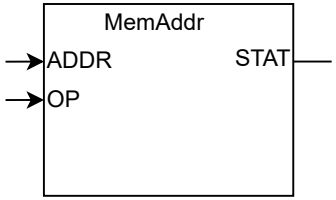


Control

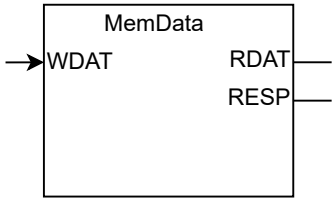


Memories

Memory Address



Memory Data



Shape Library
Phase: ALL
Created by: Steve Sheafor
Date: 5/28/2018