Improve Transition Fault Diagnosability Via Observation Point Insertion

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Abstract - In this work, a design for diagnosability (DFD) method based on observation point (OP) insertion is proposed to improve the diagnosis resolution of transition faults in a circuit. The main objective is to minimize the number of observation points since this number will directly affect the area overhead of the circuit. We develop a novel algorithm to generate a set of OP candidates and then select a minimal number of OPs from this set which can distinguish all targeted fault pairs. An observation point insertion logic is also proposed that can efficiently reuse the output pins in the original circuit so as to reduce the number of extra output pins. In addition, a novel structural distance calculation method for synthesized circuits is proposed that considers the mixed structure of primitive gates and complicated gates, including AOI or OAI gates. Experimental results show that after applying the OP insertion method, all aborted fault pairs can be distinguished and the number of required observation points is quite small. We also use the observation points to distinguish those indistinguished far-away fault pairs. Experimental results show that all targeted fault pairs can be distinguished with a few observation points and a set of diagnosis patterns for ISCAS89 and ITC99 circuits.

Index Terms—Fault diagnosis, distinguishing multiple types of faults, stuck-at-faults, bridging faults.

I. INTRODUCTION

Observation point (OP) insertion is commonly used to increase the observability of a circuit and improve its testability. This technique can also be utilized to enhance the diagnosability of circuits in a new manufacturing process so as to ramp the yield of the process quickly. Figure 1 shows a diagnosis flow with an extra observation point insertion step. The input is the original circuit. A set of test patterns (TP) is first generated by using a commercial ATPG tool. For the fault pairs that cannot be distinguished by the TP, a set of diagnosis patterns (DP) is further generated. After that, for the still indistinguished fault pairs (INDISFP), including equivalentfault pairs and aborted pairs, we perform the observation point insertion method and get a modified circuit with some observation points. Then when the chips containing the modified circuit are manufactured, the test patterns (TP) and additional diagnosis patterns (DP) are applied to the chips via automatic test equipment (ATE) to produce a failure log (FL), i.e., the output responses of failing patterns. The FL is then analyzed by a diagnosis analysis tool to derive a list of candidates (CD) for the physical failure analysis (PFA) process. Since all fault pairs can be distinguished with the observation points added, the diagnosability of circuit can be enhanced significantly, which can efficiently narrow down the candidates and quickly reach actual defect locations to ascertain the causes of the defects.

In general, a good OP insertion based design for diagnosis should achieve three objectives: 1) high distinguishability to distinguish most, if not all, indistinguished faults, 2) only a small number of observation points required, and 3) small area overhead induced by each OP.

In this paper, we propose an efficient observation point insertion procedure that mainly contains two methods. First, a

novel observation point generation and selection algorithm is developed which can generate a set of valid observation points and select a minimal number of observation points to distinguish all targeted fault pairs. Second, a widely used observation point insertion logic is adopted that can share the output pins of the original circuit using some multiplexers. The insertion logic can effectively reduce the extra output pins for observation points. Experimental results show that all aborted fault pairs during diagnosis pattern generation can be distinguished by adding a small number of observation points.

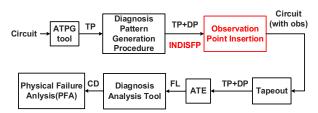


Fig. 1. A diagnosis flow with an extra observation point insertion step

We also apply our method to the in-distinguished far-away fault pairs, including equivalent-fault pairs. Experimental results show that when the distance of the two faults in a fault pair is set to 4 or more gates away, we only need 9 and 14 observation points to distinguish all transition-fault pairs of ISCAS89 and ITC99 circuits, respectively. To the best of our knowledge, this is the first work to apply OP insertion to the transition fault diagnosis problem. Compared to the recent results in OP insertion for stuck-at faults [2], our work requires much less numbers of observation points.

The rest of the paper is organized as follows. Section II illustrates the proposed observation point insertion, which mainly contains two parts: 1) the observation point selection algorithm, and 2) the observation point insertion architecture. Section III describes a novel structural distance calculation method. The experimental results are given in Section IV. Finally Section V concludes this paper.

II. OBSERVATION POINT INSERTION ALGORITHM AND LOGIC

We start with a fault pair list that cannot be distinguished by the diagnosis algorithm presented in [4], which is so far the most effective one in terms of diagnosis resolution, where diagnosis resolution is defined as the fraction of fault pairs that can be identified as containing two equivalent faults or containing two faults that can be distinguished by the algorithm. This list contains two types of fault pairs:

- 1) Aborted fault pairs: the two faults in a pair cannot be distinguished by a diagnosis pattern generation tool due to the backtracking limitation of the ATPG tool. These fault pairs need to be distinguished in order to reach 100% diagnosis resolution.
- 2) *Indistinguished far-away fault pairs*: the two faults in a pair cannot be distinguished by test or diagnosis patterns; they may or may not be equivalent, and their distance in

the circuit is large. The two faults may be reported as defect candidates simultaneously. This will impose difficulty on the later PFA process since it may be impossible to observe the actual manufactured results on both sites with the destructive PFA process.

We next describe an *observation point generation and* selection algorithm that can identify a set of observation points efficiently to help distinguish the targeted pairs, followed by the description of the *observation point insertion architecture*.

A. Observation Point Generation and Selection Algorithm

The observation point generation and selection algorithm is shown in Figure 2. The input to this algorithm is the fault pair set mentioned above and the output is a set of observation points to be inserted and the additional diagnosis patterns required. The algorithm consists of two parts: OP generation and OP selection. For OP generation, two steps are used to find a set of valid observation points (VOP) for each fault pair, where a VOP is defined as an OP that can capture the fault effect of only one but not both faults of the fault pair using diagnosis patterns generated in the following second step. Clearly the targeted fault pair can be distinguished if a VOP is inserted into the circuit.

- 1) For a pair of two faults, we first put the gates in the fanout-cones of two faults into two sets called FA1 and FA2, respectively. Then we put the output pins of all gates in the union of FA1 and FA2 into a set of observation point candidates (OBS-Cand). We then pick up the OPs in OBS-Cand that are not in the intersection of FA1 and FA2 and perform fault simulation by using TP and DP generated from the previous diagnosis pattern generation procedure. If there are some OPs that can capture the fault effect of only one fault, we add these OPs into VOP. This step is quite efficient in selecting valid OPs since these OPs are located in the fanout-cone of only one fault.
- 2) All OPs in OBS-Cand are temporarily inserted to circuit, and a diagnosis test pattern generation process [4] with n-detection limit is used to generate patterns to distinguish the targeted fault pair. The n-detection limit helps us identify more OP candidates that can be added to the VOP set. After this process, we perform fault simulation with the newly-generated patterns and select the OPs that can capture the fault effect from only one fault of a fault pair into the VOP set.

Figure 3 shows an example of VOP generation, the target fault pair contains two faults F1 (N0: slow-to-rise) and F2 (N3: slow-to-rise). The fanout-cone of F1 contains five gates G1, G3, G4, G5 and G6 and the fanout-cone of F2 contains four gates G3, G4, G5 and G6. In the first step, we put the output pins (N1, N3, N4, N5, and N6) of the gates (G1, G3, G4, G5, G6) into OBS-Cand. Since only N1 is not in both fanout cone, we perform fault simulation with the previously generated TP and DP and examine whether N1 can capture the fault effect of only one fault or not. We find that the output N1 can capture the faulty response from F1 but not F2, hence the output pin N1 is added into the VOP set of this fault pair.

In the second step, we insert all OPs (N1, N3, N4, N5, and N6) into the circuit and generate diagnosis patterns with

n-detection limit to distinguish this fault pair. We can find that N3, N5, and N6 can also capture the faulty response from F2 but not F1, and thus these outputs are added into the VOP set.

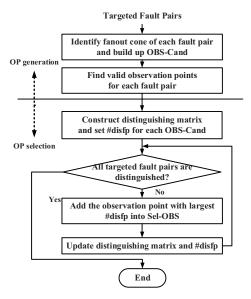


Fig. 2. Flow of observation point generation and selection

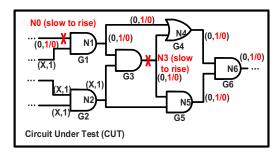


Fig. 3. Flow of observation point generation and selection

After generating the VOP sets for all fault pairs, the OP selection procedure is executed, which is basically a set covering problem. A greedy algorithm is used to select a minimal number OPs in VOP to distinguish all targeted fault pairs. Finally, the selected OPs is added to a selected observation point set (Sel-OBS). Figure 4 shows an example. We have six OPs (N1-N6) in the VOP sets of four fault pairs. We build a distinguishing matrix shown in Figure 4(a), where a value "1" in an entry means that the fault effect of the corresponding fault pair can be captured by the corresponding OP. The last row (#disfp) shows the number of distinguished fault pairs for each OP. We will select the OP with the maximum #disfp and add it to Sel-OBS. Then we remove the selected OP and update the distinguishing matrix. We iterate the above steps until all targeted fault pairs are distinguished. Figure 4(a) and (b) show that two OPs (N3 and N4) are enough to cover all fault pairs.

B. The Observation Point Insertion Logic

The control logic for observation point insertion includes a set of multiplexers and a control input pin, where all multiplexers are controlled by the control pin. For each observation point, a multiplexer is inserted into a circuit with the 1-input connected to a line driving a primary or pseudo

primary output of the original circuit, the 0-input connected to the OP, and the output connected to the original primary or pseudo primary output. All multiplexers are controlled by a control pin. When the input is 0, the output of multiplexer will capture the signal from OP, otherwise the output will capture the signal from the original output. The major advantage of this architecture is that we do not need additional output pins when the number of OPs in Sel-OBS is smaller than the total number of (pseudo) primary outputs. We only need one additional input to control the inserted multiplexers for all OPs when applying the newly-generated diagnosis patterns. This "output sharing" technique is commonly used for a design with limited output pins.

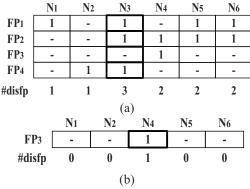


Fig. 4. Set covering problem

III. STRUCTURAL DISTANCE CALCULATION

In this work, we also study the problem of inserting OP for fault pairs that contain equivalent but far-away faults. These fault pairs also needed to be distinguished for a new process technology since determining the exact locations of defects are highly desired. We first employ a structural distance calculation method to calculate the distance between two faults in a fault pair. Different from [2] that deals with only primary gates (NAND, NOR, XOR, etc.), our method also deal with AND-OR-Inverter (AOI) and OR-AND-Inverter (OAI) gates. We define the distance between two lines in a circuit as the smallest number of gates traversed when tracing the circuit from one line to the other. Figure 5 shows an example with four faults in the circuit (Fo to F3). For pair (F0, F1), since they are located in the same fan-out stem and branch, the distance of this fault pair is 0. For pair (F0, F2), the distance is 2 since the path from F₀ to F₂ includes an AND gate and an AOI gate. For pair (F₀, F₃), the distance is 3 since the path includes the path from F₀ to F₂ and the path from F₂ to F₃.

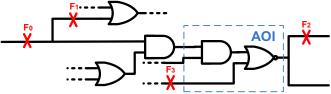


Fig. 5. An example of structural distance calculation

IV. EXPERIMENTAL RESULTS

We implement the Observation Point Insertion method by using C++ program together with the ATPG tool from the Mentor Graphic Company (Mentor Tessent FastScan v9.3). All experiments are done on a DELL R710 3.47GHz with 4G RAM. We apply the method to ISCAS'89 and ITC'99 benchmark circuits and the results are described next.

A. Results of OP Insertion for Aborted Fault Pairs

In Table I, we show the results of observation point insertion for aborted fault pairs only. Since only s15850, b15, b17 and b20 have aborted fault pairs after applying the diagnosis pattern generation proposed in [4], we only show the results of these 4 circuits. Columns 1 and 2 show the circuit name and the number of aborted pairs, respectively. Under column "OBS Insertion", we give the numbers of distinguished fault pairs (#DIS) and the selected observation points (#OBS), and the area-overhead due to the observation point insertion. We can find that all 255 aborted fault pairs can be distinguished by using 111 observation point. The area-overhead are only 0.08%, 0.61%, 0.77% and 0.04% of the original circuits.

Table I: The results of Observation Point Insertion for aborted pairs

CUT	#AB	OBS Insertion						
CUI		#DIS	#OBS	Area-Overhead (%)				
s15850	6	6	2	0.08				
b15	89	89	22	0.61				
b17	154	154	85	0.77				
b20	3	3	2	0.04				
Total	255	255	111					

B. Results of Observation Point Insertion for Fault Pairs with Large Distance

The diagnostic pattern generation presented in [4] can report a set of indistinguished fault pairs which includes equivalent-fault pairs as well as aborted fault pairs. In this paper we calculate the structural distance between two faults in each indistinguished fault pair. The results are shown in Table II. The distances of indistinguished pairs range from 0 to 5. The last row shows the total number of each column and the number in parentheses shows the percentage of each distance. We can find that only 0.76% of the indistinguished fault pairs have a distance equal to or larger than 4 and most fault pairs (84.75%) have a distance of 0 or 1, meaning that most indistinguished fault pairs are located at the same net or at the I/O of the same gate.

Table II: Distance Distribution of Indistinguished Pairs

CUT	#INDIS-		Pair Distance							
CUI	FP	0	1	2	3	4	5			
s1196	122	19	70	27	6	0	0			
s1423	196	23	150	22	1	0	0			
s5378	141	71	61	8	1	0	0			
s9234	83	18	47	17	1	0	0			
s13207	528	76	357	83	6	6	0			
s15850	1144	125	672	154	81	86	6			
s38417	439	27	342	64	6	0	0			
s38584	2858	329	2089	413	25	2	0			
ISCAS89	5511	688	3808	788	127	94	6			
b14	495	24	406	62	2	1	0			
b15	1171	187	748	212	21	1	0			
b17	2772	365	2069	291	43	4	0			
b20	1131	75	913	127	16	0	0			
b21	1240	72	1035	125	8	0	0			
b22	1686	109	1379	188	10	0	0			
ITC99	8495	833	6550	1050	101	6	0			
Total	14006	1521 (10.8)	10358 (73.95)	1838 (13.1)	228 (1.6)	100 (0.72)	6 (0.04)			

We add OP for the indistinguished-fault pairs with the distance larger than 3 (0.76%) and 1 (15.25%) respectively. The results on these fault pairs are shown in Table III. Columns 1 and 2 show the circuit name and the number of indistinguished fault pairs under test patterns, respectively. Under column "DPG", we give the number of distinguished pairs and indistinguished pairs. Under column "OBS (dist>=4)" and "OBS (dist>=2)", we show the results for the fault pairs whose distances are larger than 3 and 1, respectively, and give the numbers of distinguished pairs (#DIS), indistinguished pairs (#Indis), diagnosis patterns (#DP) and observation points (#OBS). Using s15850 as an example, there are 1458 indistinguished fault pairs by using test patters (TP) only. After DPG, we can distinguish 314 fault pairs and 1144 remains indistinguished. For the fault pairs with the distance larger than 3, we can distinguish more 240 fault pairs by adding 92 diagnosis patterns and 6 observation points. Note that many (240-92 = 148) fault pairs with a distance less than 4 are also distinguished. For the fault pairs with the distance larger than 1, we can further distinguish 702 fault pairs by adding 327 diagnosis patterns and 71 observation points. In the last row, we give the average number of each column for all ISCAS'89 and ITC'99 circuits.

We further compare the results with [2] which deals with the observation point insertion for stuck-at faults. This work also generates diagnosis patterns to distinguish fault pairs first. Then a structural distance calculation method is performed for the indistinguished pairs. We compare our work with [2] for dealing with fault pairs with distance larger than 3 and show the results in Table IV. We show the numbers of indistinguished pairs after diagnosis pattern generation, the selected OPs, the distinguished pairs by using OPs and the average number of fault pairs that can be distinguished for each OP insertion. Note that the OPs is selected to deal the fault pairs with distance larger than 3. The numbers of fault pairs with distances larger than 3 are only 8 and 240 in our method among totally 528 and 1144 indistinguished fault pairs, while they are 608 and 1182 in [2]. This implies that our DPG can perform better than that of [2] and thus the numbers of OPs needed using our method will be less than those of [2]. However the large differences between these two methods, i.e., (1 for s13207 and 6 for s15850) vs (152 for s13207 and 194 for s15850), still demonstrate the high efficiency of our method. In fact, when comparing the average number of fault pairs that can be distinguished by each OB insertion, 4 and 6.09 pairs per OP for s13207 and s15850 are reported in [2] while our method can achieve 8 and 40 pairs per OP insertion, which clearly shows the much better efficiency of our method.

Table IV: The comparison results with [2] for the faults (Pair Distance >=4)

CUT		[2			Ours				
	#INDIS -FP	OPS	DIS- FP	DIS-FP/ OPS	#INDIS- FP	OPS	DIS- FP	DIS-FP/ OPS	
s13207	2043	152	608	4	528	1	8	8	
s15850	2820	194	1182	6.09	1144	6	240	40	

Table III: The results of Observation Point Insertion for ISCAS'89 and ITC'99 circuits

CUT	#Indis	DPG [4]		<i>OBS (dist >= 4)</i>				<i>OBS (dist >= 2)</i>			
	(TP)	#DIS	#Indis	#DIS	#Indis	#DP	#OBS	#DIS	#Indis	#DP	#OBS
s1196	145	23	122	23	122	-	-	71	74	33	8
s1423	278	82	196	82	196	-	-	116	162	23	21
s5378	475	334	141	334	141	-	-	348	127	9	3
s9234	284	201	83	201	83	-	-	222	62	18	18
s13207	1107	579	528	587	520	6	1	705	402	95	62
s15850	1458	314	1144	554	904	92	6	702	756	327	71
s38417	1607	1168	439	1168	439	-	-	1245	362	70	56
s38584	3971	1113	2858	1154	2817	2	2	1919	2052	440	312
ISCAS89	9325	3814	5511	4103	5222	100	9	5328	3997	1015	551
b14	2132	1637	495	1641	491	1	1	1761	371	65	63
b15	2243	1072	1171	1079	1164	1	1	1492	751	235	184
b17	5905	3133	2772	3148	2757	4	3	3765	2140	338	227
b20	3190	2059	1131	2059	1131	-	-	2323	867	143	134
b21	3241	2001	1240	2001	1240	-	-	2250	991	133	123
b22	4721	3035	1686	3035	1686	-	-	3409	1312	198	186
ITC99	21432	12937	8495	12963	8469	6	5	15000	6432	1112	917
Total	30757	16751	14006	17066	13691	106	14	20328	10429	2127	1468

V. CONCLUSIONS

In this paper, we propose an efficient procedure to insert observation points to distinguish fault pairs that cannot be distinguished by a state-of-the-art diagnosis pattern generation tool. A novel observation point generation and selection algorithm is presented. A greedy approach is used to select a minimal number OPs to distinguish all targeted fault pairs. After OP selection, an observation point insertion logic is used to share the output pins in the original circuit for OPs. Experimental results show that only 111 OPs are needed to distinguish 255 aborted fault pairs with the overhead less than 0.77% for all circuits. If only the fault pairs with large distance (>=4) are considered, which only account for 0.76% of all indistinguished pairs, our procedure only needs 14 OPs for all ISCAS'89 and ITC'99 circuits.

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