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On Acceleration of Test Points Selection for Scan-Based BIST

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SUMMARY This paper presents an acceleration of test points selection for circuits designed by a full-scan based BIST scheme. In order to accelerate the test points selection based on cost minimization, and reflecting random pattern testability, we introduce three techniques, the simultaneous selection of plural test points, the simplified selection of test points by the cost reduction factor, and the reduction of the number of test point candidates. We implement a program based on the proposed techniques and evaluate its efficiency experimentally using large scale circuits (26 k–420 k gates).

key words: *test points, BIST, optimization, testability*

1. Introduction

Increasing gate counts of logic LSIs are causing many difficulties in getting good quality test pattern generation. The increase of test data size (or test pattern length) is one difficulty which is becoming a big problem from the viewpoint of test cost, i.e. tester memory size and testing time. The Built-In Self-Test (BIST) [1], which is composed of a pseudo-random pattern generator, the circuit under test and a signature analyzer, can solve this problem. However, BIST requires many patterns for high fault coverage due to the nature of the pseudo-random pattern test. In order to solve the problem raised by poor random pattern testability, the built-in weighted random test method [2] and test points insertion (TPI) method [3]–[10] have been proposed. In particular, the TPI method improves random pattern testability efficiently, by inserting control points which improve controllability and observation points which improve observability.

The TPI method should select the most effective test points possible for testability because test points require an additional circuit area and cause additional path delay. However, the problem of optimal test points insertion in circuits with reconvergent fanout has been proven to be NP-complete [3]. Three different approaches to select test points have been proposed recently, a method using fault simulation [4], a method using the random testability measure [5], [6], and a method based on path tracing [7]. Especially for the second type, the test points selection based on cost minimization, and reflecting random pattern testability, results in high fault coverage for a reasonable pattern length [6]. This cost minimization approach has been enhanced to reduce the performance degradation by the inserted test points [8] and to reduce computational complexity [9]. Also, a method to enhance fault coverage by changing available test points in phases has been reported [10].

In designing large scale circuits based on the TPI method, one problem is the turn around time for test points selection, which must be executed between logic synthesis and layout design in the design flow. In order to ensure design term is not increased, an acceleration of test points selection is required.

This paper proposes acceleration techniques of test points selection based on the cost minimization, and reflecting random pattern testability, for circuits designed by a full-scan based BIST scheme. Section 2 outlines the TPI method and considers the procedure time for test points selection. Section 3 describes techniques for accelerating test points selection. A program is implemented based on the proposed techniques and its efficiency is evaluated experimentally using large scale circuits (26 k–420 k gates) in Sect. 4.

2. Test Points Selection Based on Cost Minimization

2.1 TPI Method

The TPI method is a technique that improves testability for a circuit under test by inserting test points. Examples of circuit inserting test points are shown in Fig. 1. Figure 1 (a) shows the control-1 point which improves 1-controllability for signals j and k, Fig. 1 (b) shows the control-0 point which improves 0-controllability for signals j and k, and Fig. 1 (c) shows the observation point

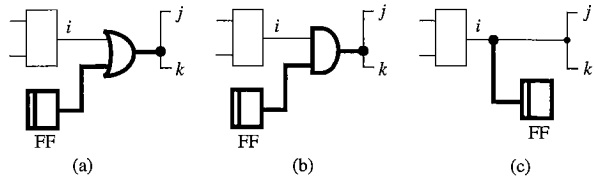

Fig. 1 Example of test points.

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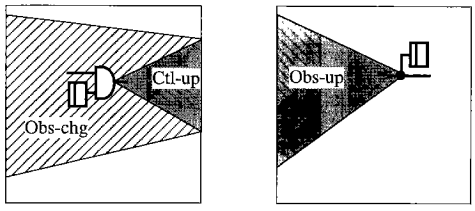

(a) Control point (b) Observation point

Fig. 2 TPI-effective region and TPI-influence region of a test point.

which improves observability for signal i. In the case of control points, the signal from the scannable flip-flop to the OR/AND-gate has to be set to the non-controlling value, that is 0 for Fig. 1 (a) and 1 for Fig. 1 (b) in the normal operation mode.

Figure 2 illustrates the region of the circuit where a test point influences the testability of signals. As shown in Fig. 2 (a), a control point improves the controllability of the region where the inserted signal propagates toward outputs (Ctl-up), and changes the observability of the region where the signals changing controllability propagate toward inputs (Obs-chg). As shown in Fig. 2 (b), an observation point improves the observability of the region where the inserted signal propagates toward inputs (Obs-up). We define the TPI-effective region as the region in which controllability is improved in the case of control points (Ctl-up in Fig. 2 (a)), and the region in which observability is improved in the case of observation points (Obs-up in Fig. 2 (b)). And we define the TPI-influence region as the region that controllability or observability change (both Ctl-up and Obs-chg in Fig. 2 (a), Obs-up in Fig. 2 (b)).

2.2 COP Testability Measure and Cost Function

Like the approach of [6], our approach is based on the well-known probabilistic random pattern testability measure called COP (Controllability Observability Procedure) [11]. C_i represents 1-controllability for signal i, that is the probability for which signal i has a logic value 1. O_i represents observability for signal i, that is the probability for which a logic value at signal i can be observed in at least one of the primary outputs or the scannable flip-flops. $P_{i/s}$ represents the probability detecting the stuck-at-s fault at signal i by a random pattern, and it is defined as $P_{i/s} = C_i(s) \cdot O_i$, where $C_i(0) = C_i$, $C_i(1) = 1 - C_i$. Then the cost function U in [12] is defined as

$$U = \frac{1}{|F|} \sum_{i/s \in F} \frac{1}{P_{i/s}}$$

where F represents the set of target faults. The cost function U can be viewed as the average expected pattern length of all the faults in F for random pattern tests because $\frac{1}{P_{i/s}}$ is the expected test length for the stuck-at-s fault at signal i. So it is regarded as the cost reflecting the testability in the whole circuit under test.

2.3 Test Points Selection

A test points selection problem is formalized as follows: given the number of test points, select the set of test points such that they minimize the cost U. In [6], an algorithm to calculate the approximate solution for this problem was proposed, and it was reported that the test points selected by this algorithm improve the fault coverage for random pattern tests. The acceleration techniques explained later basically uses this algorithm, so it is described below. In brief, selection of the test point is repeated such that the cost U after insertion is a minimum until the given number of test points is achieved. Since calculation of the cost U after inserting test point candidates for every test point selection wastes CPU time, the CRF (Cost Reduction Factor) was introduced in [6] to approximate the reduction of U due to insertion of a test point candidate. The test point candidate with the large CRF value is regarded as one of good candidates in terms of the cost reduction. The CRFs at signal i for a control-1 point in Fig. 1 (a), a control-0 point in Fig. 1 (b) and an observation point in Fig. 1 (c) are represented by CRF_i^{OR}, CRF_i^{AND} and CRF_i^{OBS} and are defined below:

$$CRF_i^{OR} = \frac{C_i - 1}{C_i + 1} \cdot C_i \cdot \frac{\partial U}{\partial C_i} - \frac{2}{C_i \cdot (1 - C_i) \cdot O_i}$$

$$CRF_i^{AND} = \frac{1 - C_i}{2 - C_i} \cdot C_i \cdot \frac{\partial U}{\partial C_i} - \frac{2}{C_i \cdot (1 - C_i) \cdot O_i}$$

$$CRF_i^{OBS} = (O_i - 1) \cdot O_i \cdot \frac{\partial U}{\partial O_i}$$

if i is a fanout stem

$$CRF_i^{OBS} = (O_i - 1) \cdot O_i \cdot \frac{\partial U}{\partial O_i} - \left(\frac{1}{C_i} + \frac{1}{1 - C_i} \right)$$

otherwise

where $\frac{\partial U}{\partial C_i}$ and $\frac{\partial U}{\partial O_i}$ represent gradients of the cost U for 1-controllability and observability at signal i respectively. The gradients of all signals can be computed in linear time [12]. The selection procedure of a test point using the CRFs is described as follows. First the COP testability measure, the cost U, and the gradients are computed. Next the CRFs at all signals are computed and the set of test point candidates is determined according to the CRF values. For every candidate, the cost U when it is inserted is computed, and the candidate which has the minimum cost after insertion is selected as the new test point.

2.4 Consideration of Time for Test Points Selection

The time for test points selection based on the above algorithm is considered. Given the number of test points N_{tp} and the number of test point candidates N_{cand},

N_{cand} is assumed constant during test points selection for a circuit. T_{cop} represents the calculation time of the COP testability measure and the cost U, and T_{crf} represents the calculation time of the gradients and the CRFs. Then the total time of test points selection T is given as:

$$T = (T_{cop} + T_{crf} + T_{cop} \cdot N_{cand}) \cdot N_{tp}. \quad (1)$$

The gate count of the circuit under test is represented by g in the following. N_{tp} is assumed to be proportional to g to keep high fault coverage, and N_{cand} is also proportional to g to keep the quality of the solution. T_{crf} is found to be proportional to g [12]. T_{cop} is proportional to g in the worst case, though T_{cop} may be less than linear order of g by using a event-driven method, that is, the COP testability measure is updated for the only signals in the TPI-influence region when a test point is inserted. Then T is proportional to $O(g^3)$ in the worst case, since the calculation of the COP testability measure and the cost for candidates is a bottleneck. This is a problem, considering that this algorithm is applied to large scale circuits. As described above, the key to accelerate test points selection is reducing the iteration number of the outermost loop in which a test point is selected, i.e. N_{tp}, and reducing the number of test point candidates, i.e. N_{cand}.

3. Acceleration Techniques for Test Points Selection

This paper proposes acceleration techniques for test point selection algorithm described in Sect. 2.3 in the following.

3.1 Simultaneous Selection Technique

In the simultaneous selection technique, plural test point candidates are selected as new test points simultaneously when they not interfere each other. We can define the relations between two test points using Fig. 3.

As shown in Fig. 3 (a), a strong relationship is defined if the TPI-effective region of one test point overlaps with the TPI-influence region of the other test point. If and only if two control points have a strong relationship, the TPI-influence region of one test point includes the other test point, as shown in Fig. 3 (a-1). In the case of two test points including at least one observation point, if the TPI-influence region of one test point includes the other test point, they have a strong relationship. But the contrary is not true. There are cases of two test points with a strong relationship, such as the TPI-influence region of one test point does not include the other, as shown in Figs. 3 (a-2), (a-3).

Next, as shown in Fig. 3 (b), a weak relationship is defined if the TPI-effective regions of two control points do not overlap, but their TPI-influence regions do. A weak relationship is not defined if two test points have at least one observation point. Finally, as shown in Fig. 3 (c), we define the relationship independent if the TPI-influence regions of two test points are distinct from each other.

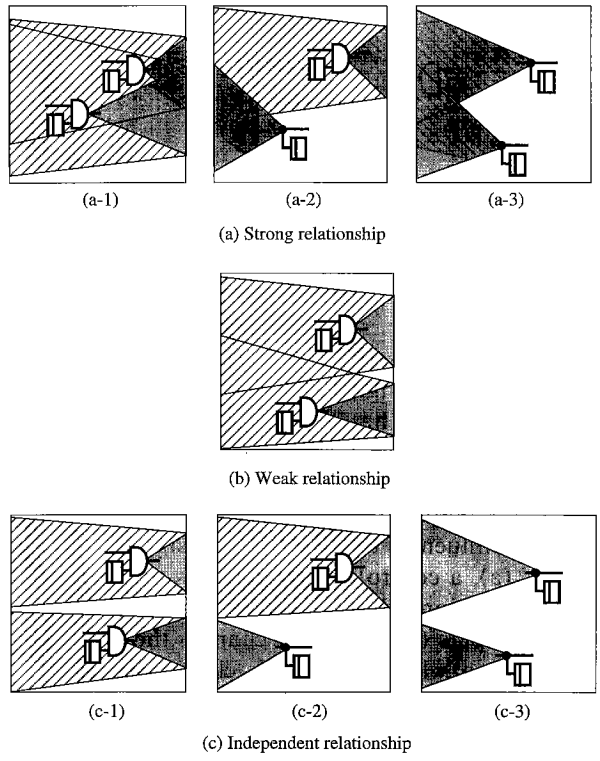

Fig. 3 Relationships between two test points.

Using the relationships defined above, we select new plural test points from candidates by a simultaneous selection as follows. First, like the algorithm described in Sect. 2.3, the COP testability measure, the cost U, the gradients and the CRFs are computed, and the set of test point candidates is determined according to the CRF values. For every candidate, the cost U when it is inserted is computed, and the candidate which has the minimum cost after insertion is selected as the first test point. Next, the TPI-influence regions of the selected test point and every candidate are calculated, and the candidates which have a strong relationship with the test point are removed from the set of candidates. The candidate which has the minimum cost in the updated set is selected as the second test point. This procdure is repeated until the set of candidates is empty. As a result, the plural selected test points are those of weak or independent relationship.

This simultaneous selection reduces the iteration number of the outermost loop, that is N_{tp} in the Eq. (1). In order to keep the ability to minimize the cost, we restrict the test points selected simultaneously using the following condition for the ratio of cost reduction:

$$1 - \frac{U_i}{U} > P_{sim} \cdot \left(1 - \frac{\min Ui}{U}\right) \quad (2)$$

where U_i represents the cost of inserting the test point candidate i, U represents the cost for the current circuit, and P_{sim} is a given threshold.

3.2 Simple Selection Technique

The simple selection technique uses the CRFs which approximate the reduction of U due to insertion of a test point candidate as the only guide in the test point selection process. So it omits the cost calculation for test point candidates by selecting the candidate whose CRF value is the maximum, that is, N_{cand} in the Eq. (1) equals to 0. In order to keep the ability to minimize the cost, we use this technique in the selection process after n test points have been inserted if the condition for the ratio of cost reduction is satisfied as below:

$$1 - \frac{U[n]}{U[n-1]} > P_{smp} \tag{3}$$

where $U[n]$ and $U[n-1]$ represent the costs for the circuit after n and $n-1$ test points have been inserted, and P_{smp} is a given threshold.

3.3 Candidates Reduction Technique

In the candidates reduction technique, the process to calculate the cost U for candidates is terminated if a candidate turns out to reduce the cost sufficiently of the circuit in which it is inserted. So this technique reduces the number of test point candidates, that is N_{cand} in the Eq. (1). We adopt the condition for a candidate to reduce the cost sufficiently as:

$$1 - \frac{U_i}{U[n]} > P_{abs}$$
$$\text{or} \quad 1 - \frac{U_i}{U[n]} > P_{rel} \cdot \left(1 - \frac{U[n]}{U[n-1]}\right) \tag{4}$$

where $U[n]$ and $U[n-1]$ represent the costs for the circuit after n and $n-1$ test points have been inserted, U_i represents the cost of inserting the test point candidate i. P_{abs} and P_{rel} are given thresholds for the absolute condition and relative condition respectively.

3.4 Using Acceleration Techniques Together

Each of acceleration techniques described above does not give enough speed-up because of the trade-off between the effect of speed-up and the optimization ability. We can achieve enough speed-up without degrading the quality of solution by using the three techniques together.

Figure 4 shows the procedure for test points selection with the three techniques as a C-language program. The number of test points (N_{tp}), the maximum number of test point candidates (N_{cand}), and the parameters in the acceleration techniques (P_{sim}, P_{smp}, P_{abs}, P_{rel}

```
Test_Points_Selection (N_tp, N_cand) {
  /* S : Set of test points */
  /* n : Number of test points (= #S) */
  /* U[n] : Cost after n test points insertion */
  /* U_i : Cost for test point candidate i */
  S = φ;
  n = 0;
  while (n < N_tp) {
    Compute the cost U[n];
    Compute gradients and CRFs for each signal;
    if (n > 0 and 1 - U[n]/U[n-1] > P_smp) {                    ... (a)
      Select test point i with the largest CRF;
      Insert selected test point i;
      continue;
    }
    Determine the set of candidates S_1, where
    S_1 = {candidate i | i has the largest N_cand CRF }
    S_2 = φ;
    while (S_1 ≠ φ) {
      Select i ∈ S_1 with the largest CRF;
      Compute the cost U_i;
      Move i ∈ S_1 to S_2;
      if (1 - U_i/U[n] > P_abs
        or (n > 0 and 1 - U_i/U[n] > P_rel · (1 - U[n]/U[n-1])))   ... (b)
        break;
    }
    S_3 = Simultaneous_Selection (S_2, {U_i | i ∈ S_2});        ... (c)
    Insert the test points in S_3;
    S = S ∪ S_3;
    n = n + #S_3;
  }
  return S;
} /* Test_Points_Selection */
Simultaneous_Selection (S_2, {U_i | i ∈ S_2}) {
  for (i ∈ S_2) {
    if (1 - U_i/U[n] > P_sim · (1 - min{U_k|k∈S_2}/U[n]))
      Delete i from S_2;
  }
  S_3 = φ;
  while (S_2 ≠ φ) {
    Move i ∈ S_2 such that U_i = min{U_k|k ∈ S_2} to S_3;
    for (j ∈ S_2) {
      if ( i and j have a strong relationship )
        Delete j from S_2 ;
    }
  }
  return S_3;
} /* Simultaneous_Selection */
```

Fig. 4 Procedure of test points selection with acceleration techniques.

in Eqs. (2)–(4)) are given. In Fig. 4, the part of (a), (b) and (c) shows the procedure of the simple selection technique, the candidates reduction technique and the simultaneous selection technique respectively.

4. Experimental Results

We have implemented the program based on the proposed techniques and conducted experiments using one of the ISCAS'89 benchmark circuits [13] and several industrial circuits (92 k–420 k gates), where all circuits are designed full-scan. Table 1 shows their characteristics, where #Gate, #In, #Out, #Bid and #FF mean the number of primitive gates in our tools, primary inputs, primary outputs, bidirectional edges and flip-flops.

Table 2 shows experimental results for the original circuit (Original Circuit), test points selection without using the acceleration techniques (Without Acceleration), the simultaneous selection technique (Simultaneous Sel.), the simple selection technique (Simple Sel.), the candidates reduction technique (Reduc. Candidates), and the case of using three acceleration techniques together (All Tech.) are shown. Each acceleration technique was executed with two parameter cases. In each cell of the table, the cost (Cost), the fault efficiency by random pattern tests (Ef), CPU-time for test points selection on HITACHI9000V/VR260-EG (T), and the ratio of speed-up to CPU-time without using the acceleration techniques (SU) are shown. The number of test points and the maximum number of test point candidates are given as 0.1% and 0.02% of the number of gates shown in Table 1, respectively. As concerns fault efficiency, we ran the fault simulations with 32 k random patterns for s38584 and 512 k random patterns for the other circuits, and identified the redundant faults by ATPG for the undetected faults.

Table 1 Characteristics of circuits.

Circuit	#Gate	#In	#Out	#Bid	#FF
s38584	26 k	12	278	0	1452
A	92 k	50	45	85	3481
B	177 k	162	170	14	8451
C	181 k	252	231	14	7323
D	223 k	176	184	149	13227
E	420 k	184	39	89	24987

4.1 Simultaneous Selection Technique

The results for the simultaneous selection technique are shown in columns 5–6 of Table 2. In order to show that the proposed condition in selecting test points simultaneously is adequate, two conditions are considered: the first is only for test points with weak and independent relationships as described in Sect. 3.1 (Proposed Condition), and the second is for test points which are not included in the TPI-influence regions of the others (Loose Condition). In the loose condition, there is an instance that test points with a strong relationship are selected simultaneously, such as Figs. 3 (a-2), (a-3), though the calculations of the TPI-influence regions for each test

Table 2 Experimental results.

Circuit	Item	Orignal Circuit	Without Acceleration	Simultaneous Sel.		Simple Sel.		Reduc. Candidates		All Tech.
				Proposed Condition	Loose Condition	*Psmp*=0.1	*Psmp*=0.0	*Pabs*=0.08 *Prel*=0.95	*Pabs*=0.05 *Prel*=0.90	
s38584	Cost	5.0E+16	7.3E+6	7.6E+6	8.6E+6	6.0E+6	6.1E+6	7.8E+6	8.0E+6	8.1E+6
	Ef(%)	98.59	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00
	T(s)		20	14	11	17	15	17	16	12
	SU		-	1.4	1.7	1.1	1.3	1.2	1.2	1.6
A	Cost	1.3E+42	3.1E+8	4.4E+8	6.8E+8	2.8E+8	3.0E+8	2.9E+8	3.0E+8	3.3E+8
	Ef(%)	87.16	98.91	98.83	98.62	99.01	98.94	98.90	98.91	98.97
	T(s)		298	155	138	213	137	196	163	147
	SU		-	1.9	2.2	1.4	2.2	1.5	1.8	2.0
B	Cost	5.1E+26	1.1E+9	2.5E+9	8.8E+9	1.1E+9	1.5E+9	1.3E+9	1.5E+9	1.6E+9
	Ef(%)	94.87	99.00	98.89	98.05	99.09	98.84	98.99	98.93	98.95
	T(s)		1284	439	369	1066	472	744	651	347
	SU		-	2.9	3.5	1.2	2.7	1.7	2.0	3.7
C	Cost	7.9E+43	5.0E+8	6.7E+8	1.1E+9	5.1E+8	6.5E+8	5.2E+8	4.9E+8	5.9E+8
	Ef(%)	96.00	99.24	99.10	99.10	99.27	99.21	99.23	99.17	99.21
	T(s)		1806	785	565	1502	543	992	893	492
	SU		-	2.3	3.2	1.2	3.3	1.8	2.0	3.7
D	Cost	1.3E+37	4.7E+8	4.8E+8	2.7E+9	3.7E+8	3.7E+8	4.2E+8	4.6E+8	4.2E+8
	Ef(%)	95.25	99.41	99.35	99.08	99.46	99.45	99.47	99.40	99.37
	T(s)		2204	744	597	1987	712	1345	942	568
	SU		-	3.0	3.7	1.1	3.1	1.6	2.3	3.9
E	Cost	1.6E+164	4.3E+9	6.1E+9	2.2E+10	4.6E+9	1.6E+10	5.6E+9	5.8E+9	6.1E+9
	Ef(%)	94.23	98.15	97.84	97.53	98.14	97.51	97.91	97.92	98.00
	T(s)		12511	4624	4298	11207	2378	5090	3958	2687
	SU		-	2.7	2.9	1.1	5.3	2.5	3.2	4.7

Table 3 N_{sim} in simultaneous selection technique.

Circuit	Average	Maximum
s38584	1.6	3
A	2.2	6
B	4.1	12
C	2.8	13
D	3.8	8
E	3.0	15

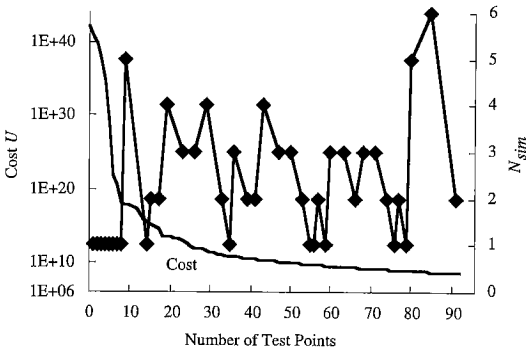

Fig. 5 Change of N_{sim} in simultaneous selection technique (Circuit A).

point candidate are omitted. The threshold P_{sim} is both set to 0.1. The ability of optimization with or without this technique is kept for the proposed condition, but it is clearly degraded for the loose condition. So the proposed condition that selects only test points with weak and independent relationship is proper from the viewpoint of optimization.

By increasing the gate count of the circuit, the effect of speed-up using this acceleration technique increases. The number of test points selected simultaneously N_{sim}, which is closely related to the effect of speed-up, is shown in Table 3. It is tend to increase as the gate count of circuit increases, though there are some differences among circuits. This is because the rate of increase in the gate count of the TPI-influence regions for candidates is smaller than that in the gate count of circuits, so that the regions which have an independent relationship are increasing in number. Consequently, this acceleration technique is better suited to large scale circuits.

Figure 5 shows the change of N_{sim} and the cost U in the test point selection process for circuit A. N_{sim} is 1 for less than 10 test points when the change rate of the cost is large. This is because there is a part of circuit with extremely poor testability, so test points gather around there to improve it. On the other hand, this technique works after many test points have been inserted because they uniform testability and the parts of circuit with poor testability are widely distributed.

4.2 Simple Selection Technique

The results for two parameter cases in applying the simple selection technique are shown in columns 7–8 of

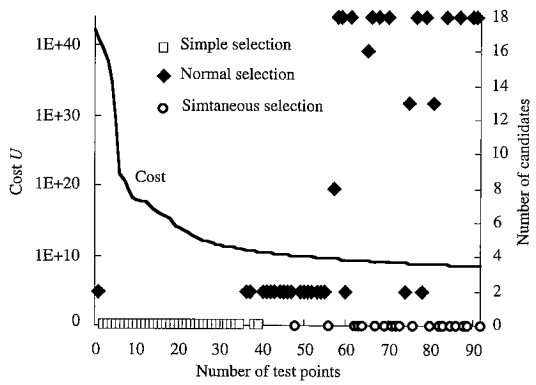

Fig. 6 Acceleration techniques and change of cost U (Circuit A).

Table 2: in the first, the ratio of cost reduction is sufficiently large ($P_{smp} = 0.1$), and in the second all ratios are included ($P_{smp} = 0.0$). The optimization ability with or without this technique is kept in the first case, but it is degraded in the second. The reason is as follows. If the change rate of U is large, the CRFs are good guidelines for test points selection. However, if the change rate of U is small, the CRFs are slightly loose since the parts of the circuit with poor testability are widely distributed and there are many candidates with CRFs whose value is near the maximum CRF.

4.3 Candidates Reduction Technique

The results for two parameter cases in applying the candidates reduction technique are shown in columns 9–10 of Table 2. The number of calculations for the cost of inserting candidates is more in the first case ($P_{abs} = 0.08$, $P_{rel} = 0.95$) than the second case ($P_{abs} = 0.05$, $P_{rel} = 0.90$). The speed-up is larger but the ability of optimization is smaller when the number of calculation for the cost of candidates is smaller. This is natural, considering the trade-off between the effect of speed-up and the ability of optimization.

4.4 Using Acceleration Techniques Together

The results when using the three techniques together are shown in column 11 of Table 2. We have achieved 1.6–4.7 speed-up while retaining almost all the effect of improved fault coverage.

Figure 6 shows results using the acceleration techniques and the number of candidates for calculating the cost in selecting each test point for circuit A. The candidates reduction technique works if the number of candidates for calculating the cost is less than 18 (0.02% of 92 k) in the case of normal selection. The change of the cost U is also shown in Fig. 6. The simple selection technique works just after the beginning of the process since the change rate of U is large. On the other hand, the simultaneous selection technique begins to work when

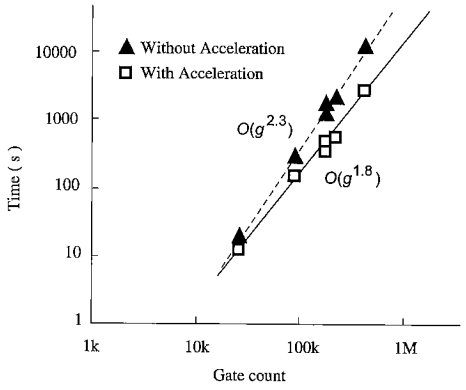

Fig. 7 Comparison of CPU-time for test points selection with acceleration and without it.

the change rate of U is small. Consequently each acceleration technique works for a suitable case, so that more effective speed-up can be achieve by using them together.

Figure 7 shows the relation between the gate count and the CPU-time for test points selection. In the case with the acceleration and without it, test points selection procedures run almost $O(g^{1.8})$ and $O(g^{2.3})$ respectively, where g is the gate count. For example, if we check a circuit with 2M gates using the same machine, the procedure time is expected to about 12 hours when using the acceleration techniques, though it is expected to about 120 hours without them. Consequently, the proposed techniques is more available for large scale circuits.

5. Conclusion

This paper presented an acceleration of test points selection based on the cost minimization, and reflecting random pattern testability for circuits designed by a full-scan based BIST scheme. We proposed three acceleration techniques, the simultaneous selection of plural test points, the simplified selection of test points by the cost reduction factor, and the reduction of the number of test point candidates. We implemented a program based on the proposed techniques and evaluated its efficiency experimentally using large scale circuits (26 k–420 k gates). The simultaneous selection technique was judged very good for large scale circuits.

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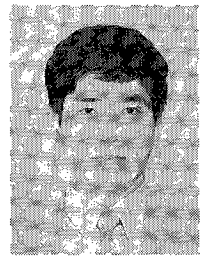

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