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REVIEW ON LFSR FOR LOW POWER BIST

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***Abstract*—While testing an integrated circuit, large chip size, and excess power dissipation are the major issues. As compared to its working mode, the testing mode power dissipation is very high. In addition to this, the inefficiency of ATE and its time-consuming nature makes the external testing much more difficult. LFSR is used for testing ASIC chips. The pseudo-random variable generated by the LFSR is used for the testing process. The pseudo-random variable testing has some advantages such that it uses simple hardware for the on-chip test generating process. BIST is one of the most efficient low power testing methods. LFSR is used in the BIST for the generation of test patterns. This paper compares the various architecture of the LFSR for BIST and its associated power dissipation**

Keywords-ATE, LFSR, ASIC, BIST, Power dissipation MCML, Transmission gate, GDI, Pass transistor.

I. INTRODUCTION

For the VLSI design, the use of transistors is inevitable. In the case of complex circuits, large no of transistors are used in a single chip. This may lead to increased power dissipation which results in heat dissipation and finally damage of the circuit. Decreasing the supply voltage, transistor capacitance, and switching frequency can solve this problem to a certain extent [1]. So that the chip area power dissipation and transistor count are a major concern.

Power dissipation is a crucial factor in testing. Higher power dissipation during the testing raises the temperature of the chip and more current will be drawn from the circuit, which results in damage of the circuit. So reducing the power dissipation in the design is given primary importance in VLSI. Introduction of BIST (Built-In Self-Test) is an assured solution to this problem. LFSR is used in BIST [2] for pattern generation.

BIST (Built-in self-Test) is a DFT technique which allows the self-testing of the circuit. The advantage of BIST as compared to other techniques its improved area testability and normal speed. And it is more economical than other testing methods because of its reduced use of ATE (Automatic Test Equipment) [3].

Fig. 1 is the schematic representation of BIST architecture. LFSR is used as the test pattern generator. The pattern generated by the LFSR is given to the Circuit which is needed to be tested (CUT) and the output obtained is analysed by the Test Response Analyser (TRA). A MISR is used as the TRA and all these units are controlled by BIST controller [4]

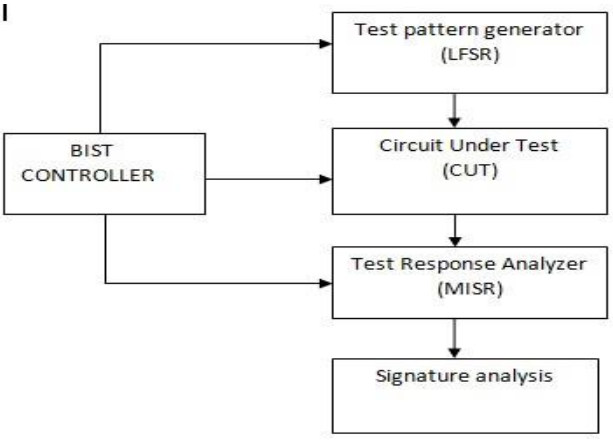

Fig. 1. BIST architecture

II. LFSR

Fig. 2 is the schematic representation of 4 bit Linear Feedback Shift Register It contains shift registers and a feedback connection. Master-slave D flip flops are used for shift registers and XOR gate is used for feedback connection. The flip flops are connected in series and output of the 1st flip flop is connected to the input of the 2nd and so on and XOR gate is used for the feedback connection. Initially, a seed value is given to the LFSR through the PRESET pin, which consists of zeros and ones. Selection of seed value requires more attention due to its dependence on power dissipation during testing. The current state of the register determines the values of its output sequences.

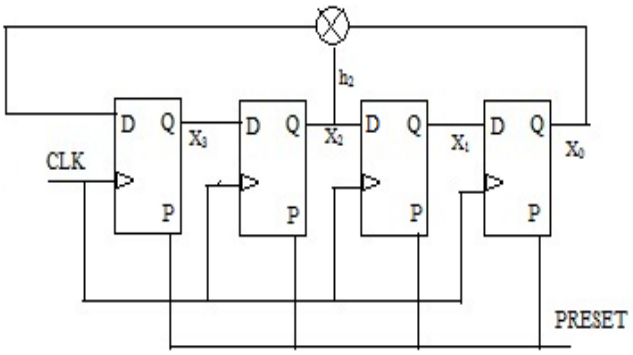

Fig. 2 Linear Feedback Shift Register

III. DESIGN ASPECTS OF LFSR

LFSR consist of both D flip flop and XOR gate. Considering design aspects of D flip flop and XOR gate, introducing modifications in the circuit designs we can improve the overall efficiency of LFSR.

A. Conventional CMOS LFSR

Fig. 3 is the schematic representation of NAND gate D Flip Flop. It contains 8 NAND gates. The seed value of the LFSR is given through the Preset pin

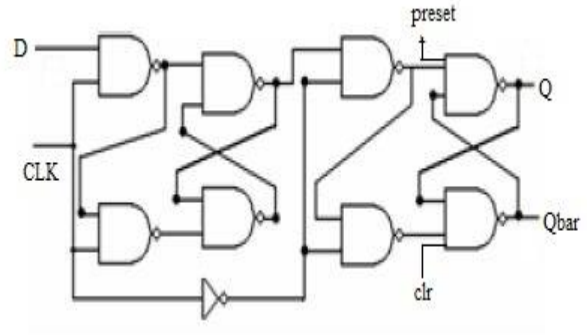

Fig. 3. NAND gate D flip flop

Fig. 4 shows the conventional XOR gate using CMOS technology

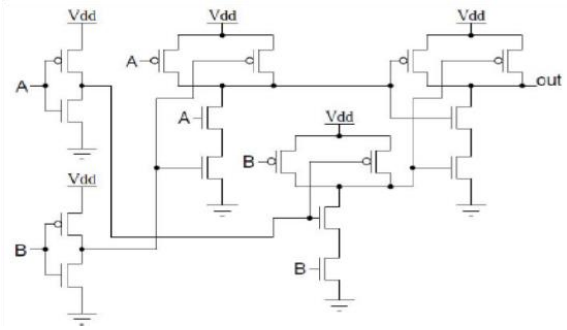

Fig. 4. Conventional XOR gate

B. MCML LFSR

Schematic representation of MCML D Flip Flop is depicted in Fig. 5 This circuit has a sample stage and hold stage. The bias voltage is applied through the transistor M_1. M_4 and M_5 are the transistors of the sample stage, which are used for detecting and tracking the input voltage. M_6 and M_7 are transistors of hold stage they are cross-coupled transistors and stores the data's sampled by the circuit. The current I_{SS} passes the sample stage when the CLK signal is high, otherwise, the clock signal flows through the hold stage [5-9]

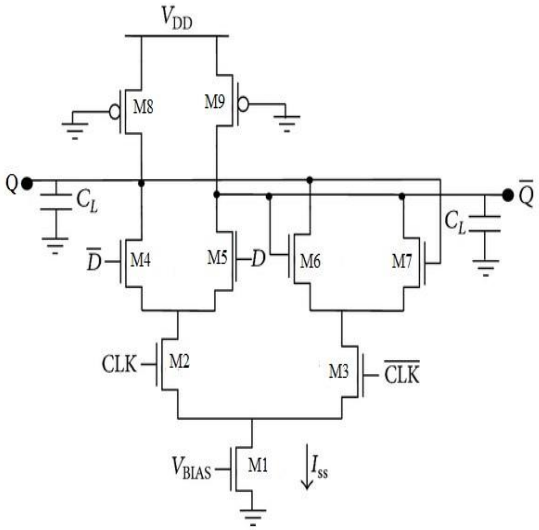

Fig. 5. MCML D Flip Flop

Fig. 6 Shows the MCML XOR gate. Bias voltage V_{BAIS} is applied to the gate terminal transistor M1, act as a constant current source. Source couple transistors are arranged in two levels

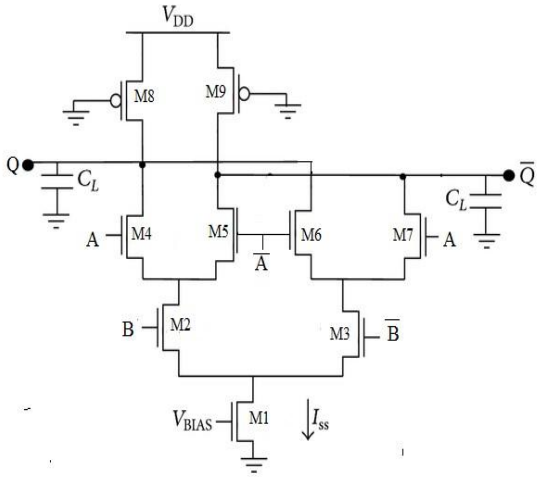

Fig. 6. MCML XOR gate

C. TRANSMISSION GATE LFSR design

Schematic representation of Transmission gate D Flip Flop is depicted in Fig. 7 When the clock is at the negative edge. The transistors T_1 and T_4 will be in active state and transistor T_2 and T_3 will be in OFF state, which forms a loop between the inverters I_3, I_4 and the transistor T_4. So slave stores the last triggered value of input Din and at the same time master latches the upcoming state but it doesn't enter into the slave since T_3 is in the off state

When the clock is at the positive edge the transistor T_2 and T_3 will be an active state, which allows the latched state to enters into the slave section i.e. a loop is formed between inverters I_1, I_2, and transistor T_2 [10]

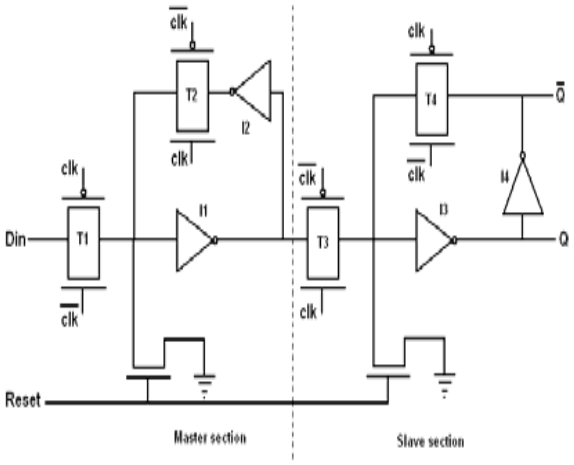

Fig. 7 Transmission gate D Flip Flop

Fig.8 shows the XOR gate using Transmission gate. It consists of an inverter and transmission gate output of the inverter is connected to the Transmission gate input

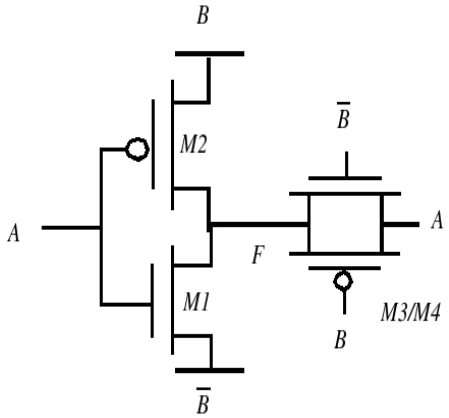

Fig. 8. XOR gate using Transmission gate.

D. GDI based LFSR design

Schematic of GDI LFSR is shown in Fig. 9. The basic cell of GDI consists of 2 transistors which are complementary in nature. Using this cell various functions like AND, OR, NOT and Multiplexing can be implemented.

The main advantage this technique is its less transistor count which is associated with least power dissipation so it is a better option for low power circuits. The Circuit consists of GDI MUX and inverters. [11]

- Body gates: It is a GDI MUX. Clock signals are connected to its gates so they are responsible for determining circuit state. Based on the clock signal it acts as either a transparent state or holding state
- Inverters (x): used for inverting the outputs of MUX and swing restoration process
- Preset input: used for inputting seed values

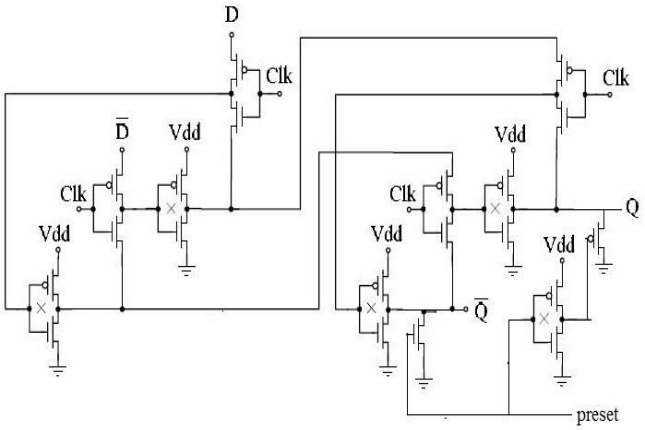

Fig. 9. GDI D Flip Flop

Fig. 10 is schematic representation of XOR gate using GDI technology. It consists of an inverter and basic GDI cell

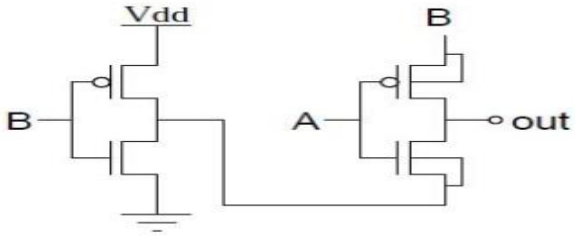

Fig. 10. GDI XOR gate

E. PASS TRANSISTOR LFSR design

Schematic representation of Pass transistor D Flip Flop [12] is depicted in Fig. 11. When clock = 0, the PMOS transistors which are connected to the clock signal will be in an active state. And the NMOS transistors which are connected to the clock signal will be an off state. So the

inverters present in the master section act as a memory state and the inverters present in the slave section responds the opposite way

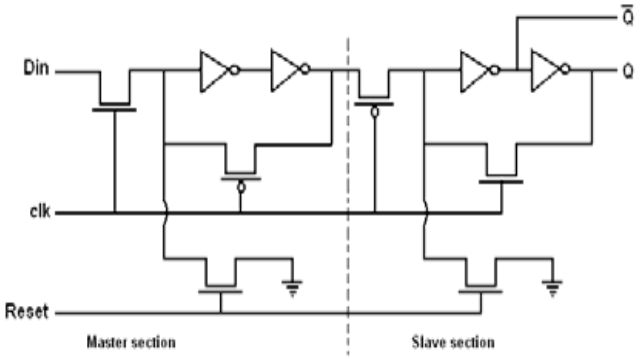

Fig.11. Pass transistor D Flip Flop

Fig. 12. Schematic of the XOR gate using pass transistors is depicted in Fig.12. It is a simple XOR gate. It consists of only two transistors so less power dissipation compared to others

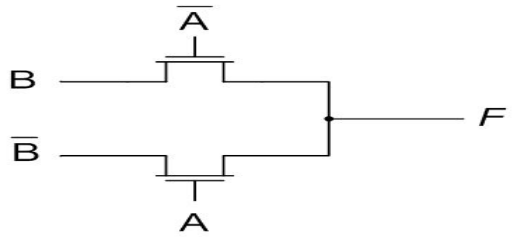

Fig. 12. Pass transistors XOR gate

IV. COMPARATIVE ANALYSIS

TABLE 1. COMPARISON TABLE OF LFSR

LFSR	Technology (nm)	Max Frequency (GHz)	Power (µW)	Delay (ns)
Conventional	90	1.8	106	9.73
Using Transmission Gate	90	1.7	99.6	8.29
Using GDI	90	1.9	34.72	6.81
Using Pass Transistor	90	1.4	28.188	7.14

LFSR using various designs are compared in Table.1. Here we can see that the LFSR using GDI has high speed and LFSR using Pass Transistor has less power dissipation

V. CONCLUSION

Various LFSR designs for the implementation of BIST are analyzed in this paper. It is found that LFSR design using pass transistor has the lowest power dissipation and least transistor count. So LFSR design using pass transistor is a suitable choice to design and implement low power and area efficient BIST. For the high-speed applications, we should go for GDI

As the next step other techniques which yield low power consumption are to be considered and using the better LFSR a BIST circuit is to be implemented

REFERENCES

[1] A circuits & systems perspective "CMOS VLSI design" by Neil Weste, Harris& Banerjee

[2] "Basic CMOS Cell Design" by Etienne Sicard&SoniaDelmasBendhia.

[3] N. Ahmed, M. H. Tehranipour, M. Nourani, "Low Power Pattern Generation for BIST Architecture", Center for Integrated Circuits & Systems, The Univ.of Texas at Dallas Richardson, TX 75083

[4] E. RaghuveeraK Hari Kishore, ShaikShoukat Vali and G.SiriVennela"VERILOG IMPLEMENTATION OF UART WITH BIST TECHNIQUE FOR TPG"*International Journal of Pure and Applied Mathematics 2017*

[5] G. Caruso and A. Macchiarella, "A methodology for the design of MOS current-mode logic circuits," *IEICE Transactions on Electronics, vol. 93, issue. 2, 2010, pp. 172–181.*

[6] V. Srinivasan, D.S. Ha, and J.B. Sulistyo, "Gigahertz-range MCML multiplier architectures," *IEEE International Symposium on Circuits and Systems, vol. II, pp. 785-788, May 2004*

[7] S. Bruma, "Impact of on-chip process variations on MCMLperformance," Proceedings of the IEEE International Systems on- ChipConference, pp. 135–140, September 2003..

[8] Radhika, N. Pandey, K. Gupta, and M. Gupta, "A novel high-speed MCML square root carry select adder for mixed-signal applications, "International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT), 2013

[9] Samiksha Agarwal1, Neeta Pandey, Bharat Choudhary "Design of MCML-based LFSR for low power and mixed signal applications", IEEE 2015

[10] Doshi N. A., Dhobale S. B., and Kakade S. R. "LFSR Counter Implementation in CMOS VLSI"World Academy of Science, Engineering and Technology International Journal of Computer and Information Engineering Vol:2, No:12, 2008

[11] Radhika Sharma, Balwinder Singh, "Design and Analysis of Linear Feedback Shift Register(LFSR) Using Gate Diffusion Input(GDI) Technique" IEEE 2016

[12] Kazuo Yano," A 3.8 CMOS 16 * 16 –b multiplier using complementary pass-transistor Logic" *IEEE Journal of solid-state circuits, vol-25, No-2, April 1990*