Digital Combination Lock

*This folder only provides the Verilog code but not files of the set up in the Quartus Prime

Introduction

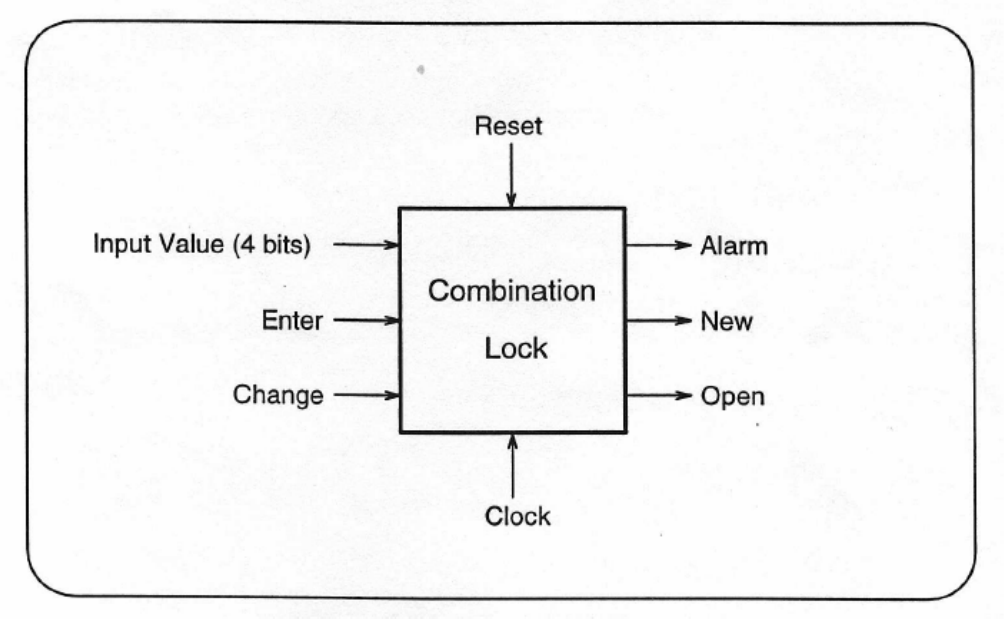

Figure : Combination Lock

This program compute a combination lock with the following algorithm:

Set the 4 input bits (X = x3x2x1x0) to the desired value and “press” Enter (set Enter input HIGH).

If X matches the stored 4-bit combination, then the door will open (output Open goes HIGH). The door should stay open until Enter is “pressed” again. If two incorrect combinations are entered in a row, the alarm goes off (output Alarm goes HIGH). The alarm can only be cancelled by resetting the system (set Reset input HIGH). When the system is reset, the stored combination should be set to ’0110’. To change the combination, set the input to the old combination and “press” Change (set Change input HIGH). If this is done correctly, output New goes HIGH to signal user to enter new combination. Set the 4 input bits to the new combination and “press” either Change or Enter to store the new value. Two incorrect values will set off the alarm as above. To provide output for your circuit,

use seven-segment display HEX5. If all outputs are LOW, then display ‘-’. If Alarm active, then display ‘A’. If New active, display ‘n’. Finally, if Open active display ‘O’.

Demonstration

Demonstrate the circuit by compiling it for the Cyclone V FPGA (5CSEMA5F31C6) device and downloading it to the DE1-SoC board. (Using other boards is fine)

Use toggle switches SW[9], SW[8], SW[7], SW[6] for inputs x3, x2, x1, x0 respectively. Connect Enter to KEY[0], Change to KEY[1], and connect the Reset signal to KEY[2]. Use one 50 MHz free running clock on the Altera board for your Clock input.