Sfwr Eng 2GA3 Assignment 4

Due: 13:40 Thursday April 2, 2020.

All assignments are to be done individually, and handed in at the start of class. Please make sure multiple sheets are stapled together.

Note: Please make sure you put your name, student number, and **tutorial section** on the first page of your assignment. Marked assignments will be returned in your tutorial section.

Note 2: As the assignment may not be returned before the final exam, it is recommended that you keep a copy of your assignment so you can check it against the posted solutions.

Written Exercises

Complete the following questions from "Computer Organization and Design: The Hardware Software Interface: ARM Edition":

Chapter 4:

1) Using Figure 4.13 of textbook (Truth table for the 4 ALU control bits, called Operation), derive a boolean expression for bit 0 (rightmost bit) of the 4 bit output, labelled "Operation." You do not need to use Boolean logic or kmaps to minimize the expression, but you should try to use the minimal number of input signals in your expression as possible. (Hint: focus on bits that differ between the items)

2) Using Figure 4.22 of textbook (Truth table for main control unit), derive a boolean expression for output "memWrite." You do not need to use Boolean logic or kmaps to minimize the expression, but you should try to use the minimal number of input signals in your expression as possible. (Hint: focus on bits that differ between the items)

3) Consider the instruction below and Figure 4.17 of the textbook (The simple datapath with the control unit) and answer the following questions:

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LDUR X2, [X1, #23]
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a) What values should the control unit assign to all of its control outputs (blue lines leaving the Oval labelled as "Control") once this instruction has been fetched and decoded?

b) What will the 5 bit inputs to the register file be for Read Register 1, and Write Register?

c) What will the 64 bit output of the sign extender unit be? Specify as a a 64 bit hex number.

d) Which resources (blocks that are labelled, i.e. "Registers") provide a useful function for this instruction?

e) Which resources (if any) produce no output for this instruction? Which resources (if any) produce an output that is not used? Assume that Data memory produces no output if MemRead = 0.

f) What is the address of the instruction to execute next?

4) 4.4 (All parts. Only consider the instructions that are implemented by our datapath).

5) 4.12, parts 4.12.1-4.12.4. Hint: this needs to be done in the same clock cycle.

6) 4.16 (all parts)

7) 4.20. Note: NOP instruction does nothing, just adds a 1 cycle delay to pipeline before next instruction is fetched.