# Analog front end for multichannel data acquisition

## Objective:

To identify and test an Integrated circuit for performing the task of an analog front end for the low speed analog multichannel data acquisition card (DAQ card).

## Requirements:

- Small size
- 8 channel input,
- Programmable gain,
- Differential input to limit transmission noise,
- High pass filter to limit high frequency noise.

## Purpose of AFE:

Most electronically controlled devices consist of sensing devices that are connected to one or more microcontroller units (MCUs) that are at the heart of embedded systems. The MCU processes that incoming signal and executes control functions according to some programmed instruction.

The sensor performs the task of detecting or measuring the some physical parameter, while the purpose of the MCU is to execute control in accordance with the incoming information. These components together constitute what is called a "detect and control" function.

Current Detect and Control systems include more than just sensors and MCUs. In particular, they usually employ analog circuitry to convert the analog signals produced by the sensors into digital signals that MCU can use. This circuitry in particular is called an analog front end forms an essential building block that connects the sensor's output to the MCU's input. The sensor signal may be too weak or its type may differ from the one required by the MCU.

MCUs usually have in-built analog-to-digital converter functions (ADCs or A/Ds) for translating analog sensor signals into a digital format. ADCs generally employ a limit to range of input voltages. If the sensor output voltage is too low, the MCU cannot accept it and an external AFE is necessary to amplify the low-level sensor signal to make it suitable for use.
Amplifying the input signal in turn amplifies the noise and hence the AFE is also required to perform the task of removing the noise. Signal from a sensor is inherently too noisy; that is, the output contains too many unwanted frequencies. This noise must be removed before the analog signal is converted to digital. The AFE solution employs low-pass filter circuitry to block out high-frequency noise and/or high-pass filter circuits to remove lower-frequency noise (motion artifacts).

Typically, sensors output a voltage, but some output a current. MCU ADC circuits do not accept current inputs, so such currents have to be converted to voltages before going to the MCU. This current-to-voltage conversion is performed by special external AFE circuit, called a trans-impedance (I/V) circuit, which also amplifies the resulting voltage to levels usable by the MCU.

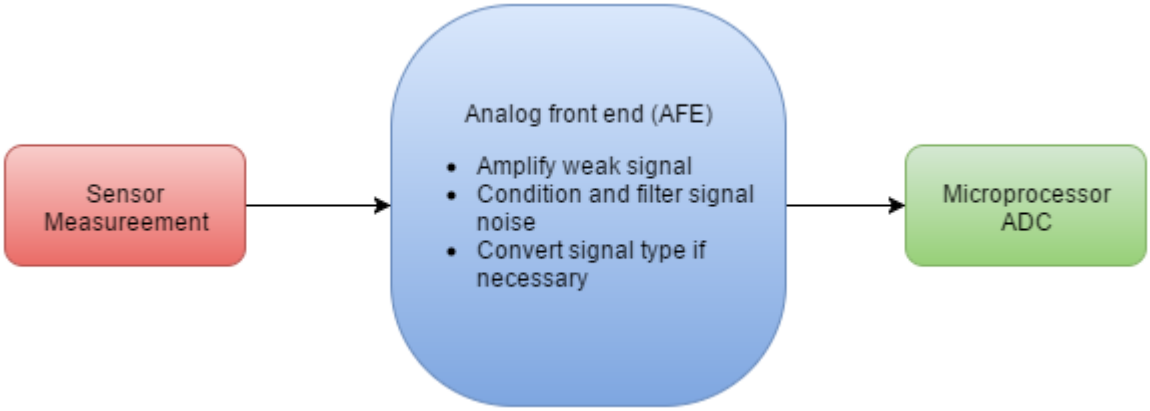


**Figure 1: Block Diagram of a Detect and Control System**

## Commercially Available AFE's:

1. **VCA 5807**
2. **PGA 5807**
3. **ADS 1198**

**TABLE 1: COMPARISION OF IC's PERFORMANCE**

| Features | VCA 5807 | PGA 5807 | ADS 1198 |
|---|---|---|---|
| Input Channels | 8 | 8 | 8 |
| Noise density | 0.9 nV/√Hz | 2.1 nV/√Hz | 12$\mu V_{PP}$ (150Hz BW, G = 6) |
| ADC | Na | na | 16-bit |
| Features | LNA<br>PGA<br>LCAT<br>LPF<br>CW Mixer | LNA<br>PGA<br>LPF | PGA<br>Delta-Sigma ADC<br>Oscillator |

The IC being evaluated currently is the VCA 5807, it was considered better than the other choices due to the following reasons:

- Since we plan to use an microcontroller for the purpose of ADC we are not considering ADS 1198 as it has inbuilt ADC
- VCA 5807 provides better noise performance compared to PGA 5807
- VCA 5807 provided larger choices of value for gain due to the presence of an inbuilt attenuator
- It can also double up as a CW mixer for Ultrasound applications.

# VGA 5807 - Specification

## Block Diagram:

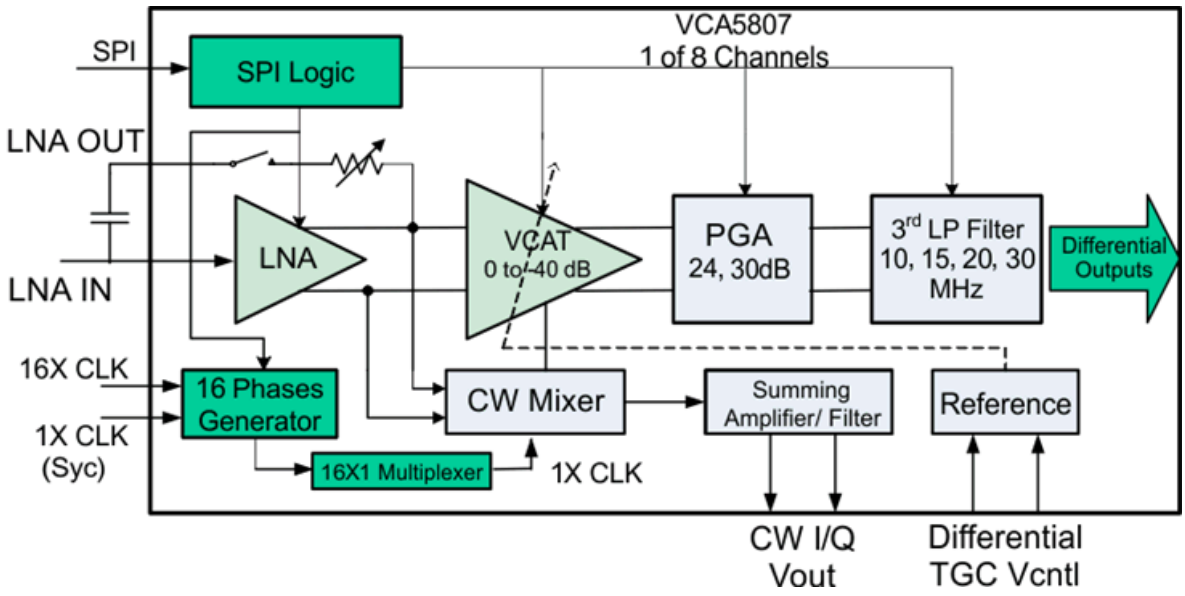


**Figure 2: Block Diagram VCA 5807**

## Pin Diagram:

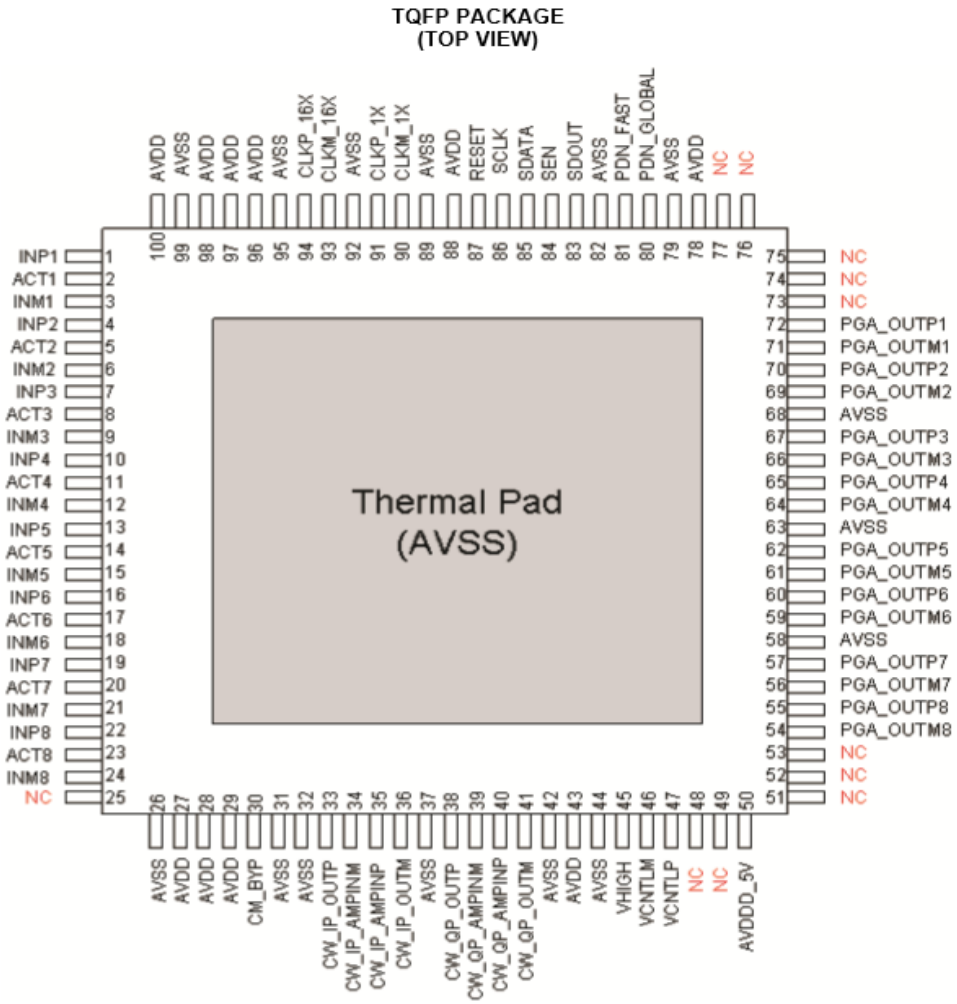


**Figure 3: Pin Diagram**

### TABLE 2: PIN DESCRIPTION

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 2, 5, 8, 11, 14, 17, 20, 23 | ACT1 to ACT8 | Active termination input pins for Channel 1 to 8. 1 µF capacitors are recommended. |
| 3, 6, 9, 12, 15, 18, 21, 24 | INM1…INM8 | CH1~8 complimentary analog inputs. Bypass to ground with ≥ 0.015µF capacitors. The HPF response of the LNA depends on the capacitors. Please see LOW-NOISE AMPLIFIER (LNA). |
| 1, 4, 7, 10, 13, 16, 19, 22 | INP1...INP8 | CH1~8 analog inputs. AC couple to inputs with ≥ 0.1µF capacitors. |
| 27, 28, 29, 43, 78, 88, 96, 97, 98, 100 | AVDD 3.3V | Analog supply for LNA, VCAT, PGA, LPF and CWD blocks. |

## Typical Connection Diagram:

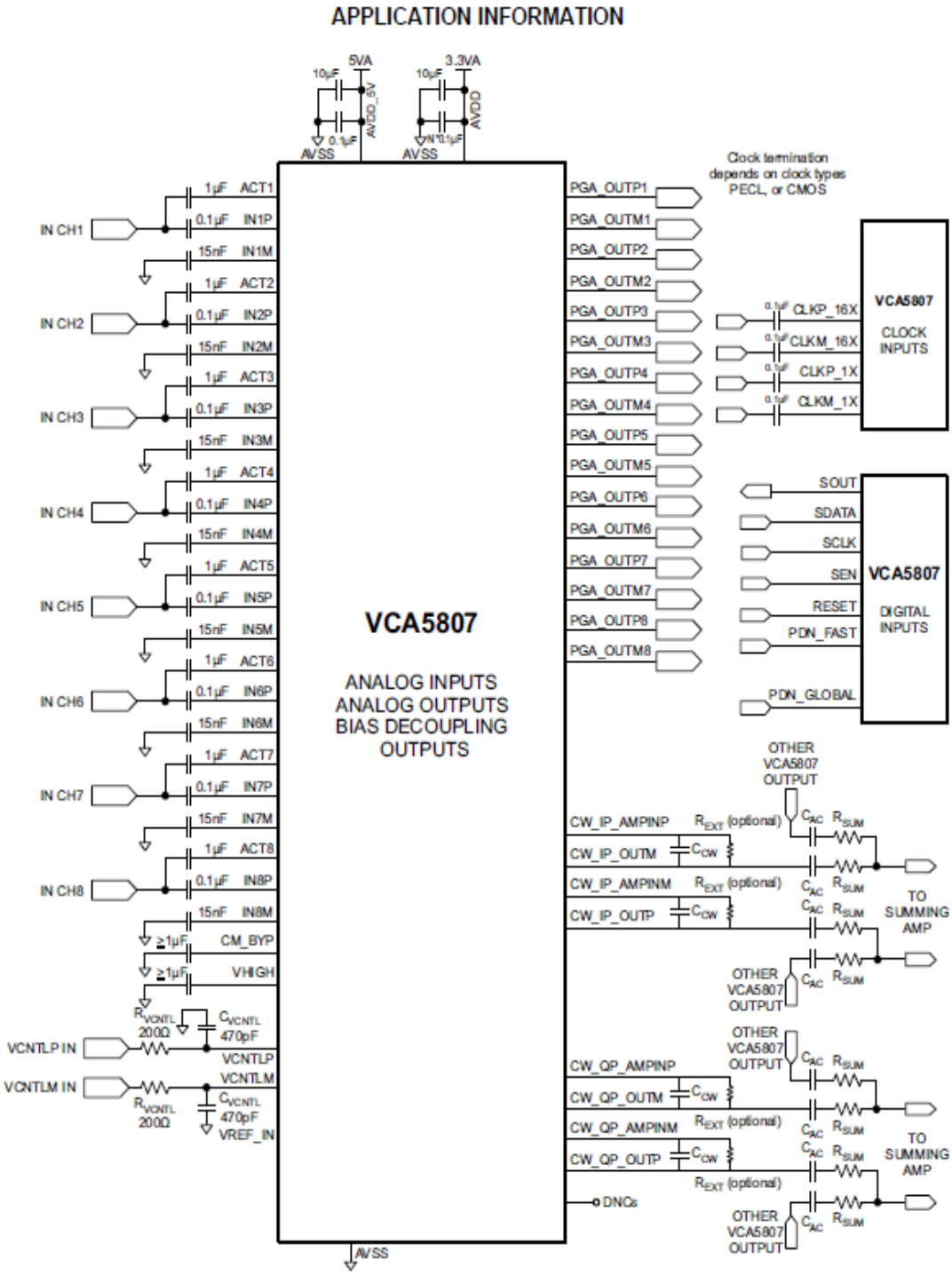


**Figure 4: Connection Diagram**

# Theory of Operation – VCA 5807 Overview

## Low Noise Amplifier (LNA):

The LNA is configurable for a programmable gain of 12/18/24 dB. To achieve low DC offset drift, the VCA5807 incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a high-pass filter. The high pass cut-off frequency can be set using the CBYPASS. The cut-off varies more or less linearly with the value of CBYPASS.

**TABLE 3: CBYPASS vs HIGH PASS FREQUENCY**

| CBYPASS | CUT-OFF FREQUENCY |
|---|---|
| 15nF | 100 kHz |
| 47nF | 33 kHz |
| 1uF | < 2 kHz |

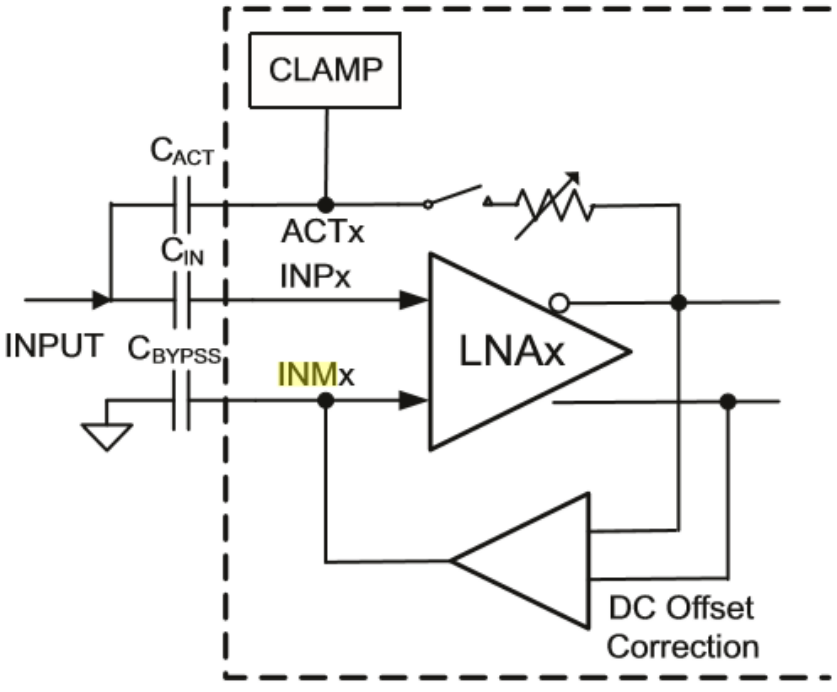


**Figure 5: Input Pin Configuration**

## Programmable Gain Amplifier (PGA):

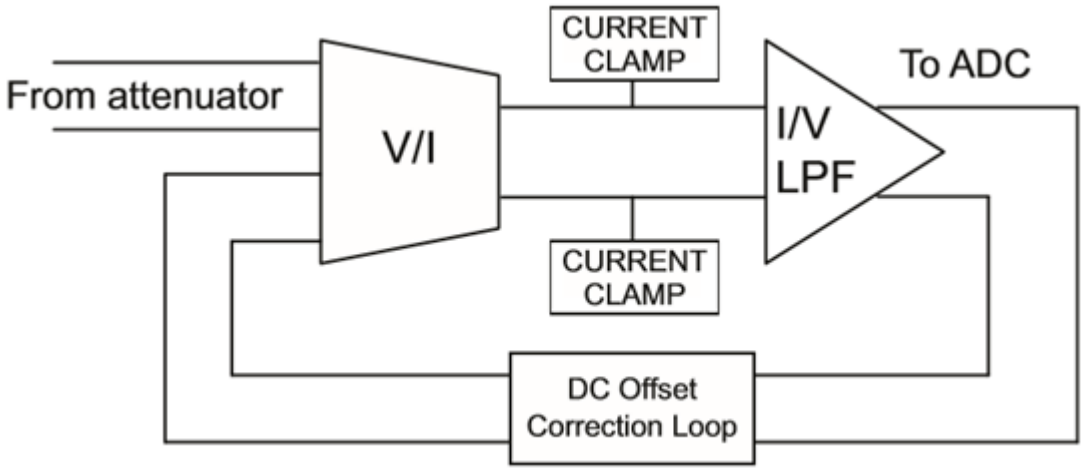


**Figure 6: Simplified Block Diagram of PGA**

The PGA can be configured for a gain of 24/30 dB. The DC offset correction loop also has a high pass response with a cut-off of 80 kHz. Since our application deal with signals in the range of 1-10 kHz the offset correction loop is disabled using register 0X33[4].To improve the overload recovery performance of the PGA the clamping circuit can be enabled.

To maximize the output dynamic range the clamp circuit is enabled

## SPI Operation:

The different modes of the IC can be programmed using serial interface. The interface supports interface clock frequency from few Hz to 20 MHz. The data is divided into register address (8 bit) and data (16 bit).

The serial interface is setup through the pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET.

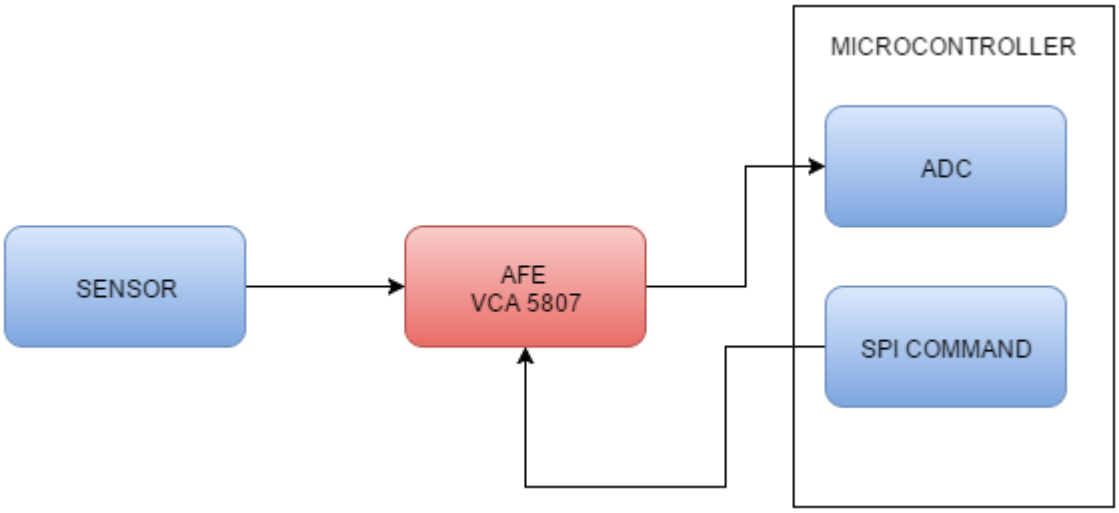


**Figure 7: Simple AFE Setup**

**TABLE 4: REGISTERS AND THEIR FUNCTION**

| ADDRESS (DEC) | ADDRESS (HEX) | DEFAUT VALUE | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| 52[12] | 0x34[12] | 0 | LNA_INTEGRATOR_DISABLE | 0: Enable<br>1: Disable offset integrator for LNA. Please see the explanation for this function in the following section |
| 52[14:13] | 0x34[14:13] | 0 | LNA_GAIN | 00: 18dB<br>01: 24dB<br>10: 12dB<br>11: Reserved |
| 59[3:2] | 0x3B[3:2] | 0 | HPF_CUT-OFF | 00: 100KHz<br>01: 50KHz<br>10: 200KHz<br>11: 150KHz |
| 51[13] | 0x33[13] | 0 | PGA_GAIN_CONTROL | 0:24dB<br>1:30dB |

# VCA 5807 EVM EVALUATION:

## VCA 5807 EVM Connection Setup:

The evaluation board has 3 input supply pins for +5, Gnd, -5 V. When the power supply to the board is supplied to the NI work station DC power supply, care must be taken to ensure that the default current limit is changed from 0.1 A to 1 A, because the evaluation board draws a current of around 0.7 A from the +5 Power supply and 0.2 A from -5 power supply. The input signal is provided in the INP 1 (J1) and output is measured from OUT 1 (J33).

In the software the required gain is set using a drop down menu. The LNA_OFFSET_INTEGRATOR and the PGA_INTEGRATOR are disabled for frequencies lower than 100 kHz.

The practical gain for input signal of 10mV and frequency 1 MHz and 1 kHz are tabulated in the following page.(The LNA_OFFSET_INTEGRATOR and PGA_INTEGRATOR were disabled for both 1 MHz and 1 kHz signal)

## Input signal of 1 MHz frequency (Sine Wave, CBypass = 15nF):

(*We obtained the same results for 10 kHz frequency)

| Serial No | LNA Gain (dB) | PGA Gain (dB) | Input Voltage (mV) | Output(V) Peak V (p-pV) | Gain (Ratio) | |
|---|---|---|---|---|---|---|
| | | | | | Theoretical | Practical |
| 1 | 12 | 24 | 10(20) | 0.6602(1.3) | 63.1 | 66 |
| 2 | 12 | 30 | 10(20) | 1.3(2.6) | 125.9 | 130 |
| 3 | 18 | 24 | 5(10) | 0.6305(1.3) | 125.9 | 126 |
| 4 | 18 | 30 | 5(10) | 1.2(2.5) | 251.2 | 240 |
| 5 | 24 | 24 | 5(10) | 1.2(2.5) | 251.2 | 240 |
| 6 | 24 | 30 | 5(10) | Distortion | 501.2 | - |

## Input signal of 1 kHz frequency (Sine Wave, CBypass = 15nF):

| Serial No | LNA Gain (dB) | PGA Gain (dB) | Input Voltage (mV) | Output | Gain | |
|---|---|---|---|---|---|---|
| | | | | | Theoretical | Practical |
| 1 | 12 | 24 | 10(20) | 180.4(359.06) | 63.1 | 18.04 |
| 2 | 12 | 30 | 10(20) | 365.2(732.03) | 125.9 | 36.52 |
| 3 | 18 | 24 | 5(10) | 211(420.29) | 125.9 | 42.03 |
| 4 | 18 | 30 | 5(10) | 422.6(848.94) | 251.2 | 84.89 |
| 5 | 24 | 24 | 5(10) | 394.7(784.92) | 251.2 | 78.49 |
| 6 | 24 | 30 | 5(10) | Distortion | 501.2 | - |

## OBSERVATION:

- It is observed that even with the LNA_OFFSET_INTEGRATOR is disable the AFE provides linear performances only for the range between 10 kHz to 10 MHz. Though it produces output for lower frequencies <10 kHz it does not produce the required gain.

- When the LNA offset integrator is disabled the input supply voltage reduces to half automatically for LNA gain 18 dB and above.

- The output signal ranges in amplitude from -1.7 to +1.7 volts. When the output theoretically exceeds this range the practical output signal gets clipped off. With the PGA_CLAMP enabled the output ranges from – 2.2 to +2.2 volts but the signal gets distorted from the expected sine wave appearance.

- We experimented by changing the CBypass from 15nF to 1uF to reduce the cut-off below 2 kHz (as mentioned in the data sheet). The values are tabulated below.

## Input signal of 1 kHz frequency (Sine Wave, CBypass = 1uF)

| Serial No | LNA Gain (dB) | PGA Gain (dB) | Input Voltage (mV) | Output | Gain | |
|---|---|---|---|---|---|---|
| | | | | | Theoretical | Practical |
| 1 | 12 | 24 | 10(20) | 180.4(359.06) | 63.1 | 18.04 |
| 2 | 12 | 30 | 10(20) | 175.9(342.36) | 125.9 | 17.59 |
| 3 | 18 | 24 | 10(20) | 175.9(340.6) | 125.9 | 17.59 |
| 4 | 18 | 30 | 10(20) | 370.7(742.5) | 251.2 | 37.07 |
| 5 | 24 | 24 | 10(20) | 354(701.4) | 251.2 | 35.4 |
| 6 | 24 | 30 | 10(20) | Distortion | 501.2 | - |

- It can be seen that even now there exists some cut-off, as the board is not giving the required gain. It was observed that when the input frequency was increased from 1 kHz to 10 kHz the gain attained the desired value at around 8kHz just as in the case where CBypass = 15nF was used.