# **OPERATING SYSTEM**

UNIT 2

P3 P2P,

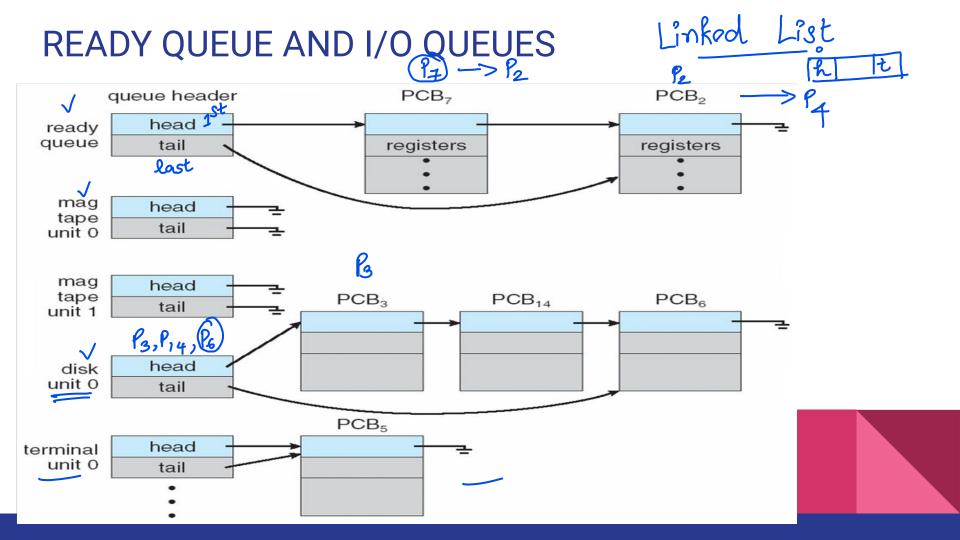




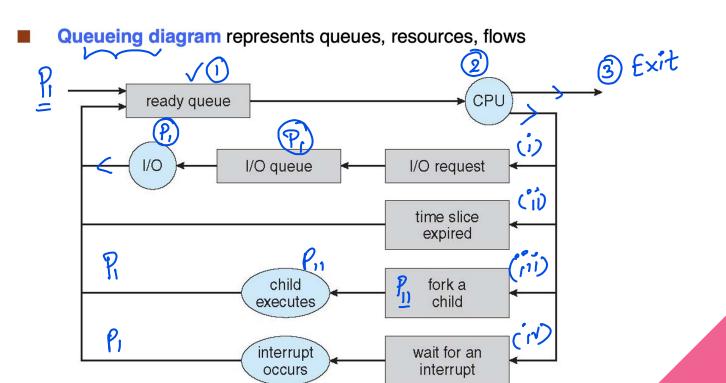
#### PROCESS SCHEDULING

- Maximize CPU use, quickly switch processes onto CPU for time sharing
- Process scheduler selects among available processes for next execution on CPU
- Maintains scheduling queues of processes
- Job queue set of all processes in the system
- Ready queue set of all processes residing in main memory, ready and waiting to execute
- Device queues set of processes waiting for an I/O device
  - Processes migrate among the various queues

Key > P, Pe P4



#### REPRESENTATION OF PROCESS SCHEDULING



## **Schedulers** $\Rightarrow$

- Ready quene -> P, P2 P4 P5 P8
- Short-term scheduler (or CPU scheduler) selects which process should be executed next and allocates CPU



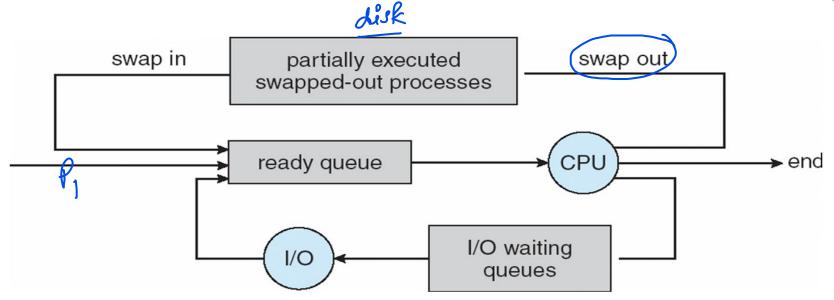
- Short-term scheduler is invoked frequently (milliseconds) ⇒ (must be fast)
- Long-term scheduler (or job scheduler) selects which processes should be brought into the ready queue
  - Long-term scheduler is invoked infrequently (seconds, minutes) ⇒
    (may be slow)√
  - The long-term scheduler controls the degree of multiprogramming
- Processes can be described as either:
  - I/O-bound process spends more time doing I/O than computations, many short CPU bursts
  - CPU-bound process spends more time doing computations; few very long CPU bursts
- Long-term scheduler strives for good process mix

### MEDIUM TERM SCHEDULER ✓

Ready

- Medium-term scheduler can be added if degree of multiple programming needs to decrease
  - Remove process from memory, store on disk, bring back in from disk to continue execution: swapping

CPU=sdisk





Proces switching

When CPU switches to another process, the system must save the state of the old process and load the saved state for the new process via a context switch



- Context of a process represented in the PCB ✓
- Context-switch time is overhead; the system does no useful work while switching
  - The more complex the OS and the PCB → the longer the context switch
- Time dependent on hardware support
  - Some hardware provides multiple sets of registers per CPU
    → multiple contexts loaded at once ✓