DESIGN OF D FLIP FLOP USING CMOS LOGIC

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Abstract

Flip Flops are the fundamental construction elements for sequential circuits, including registers, counters and memory elements. This work had implemented a low-power, high-speed D flip-flop using open-source library components from the eSim EDA tool. The objective of the D Flip Flop design is going to employ CMOS logic gates using PMOS and NMOS transistors with controlled area and channel width to length area to achieve switching speed while optimisation and minimising static and dynamic power consumption. Simulations are carried out in Ngspice through eSim for validation of functionality, propagation delay, and power dissipation. The results demonstrate that this D flip-flop Design provides reliable edge-triggered performance with reduced power overhead and improved operational speed, making it suitable for VLSI circuits in low-power applications.

Circuit Details

The D flip-flop is designed with CMOS technology employing NMOS and PMOS transistors from e sim device library and a supply voltage of maximum upto 5V. The kicad schematic implementation is given in the circuit diagram in figure 1 as implemented in e sim schematic builder.

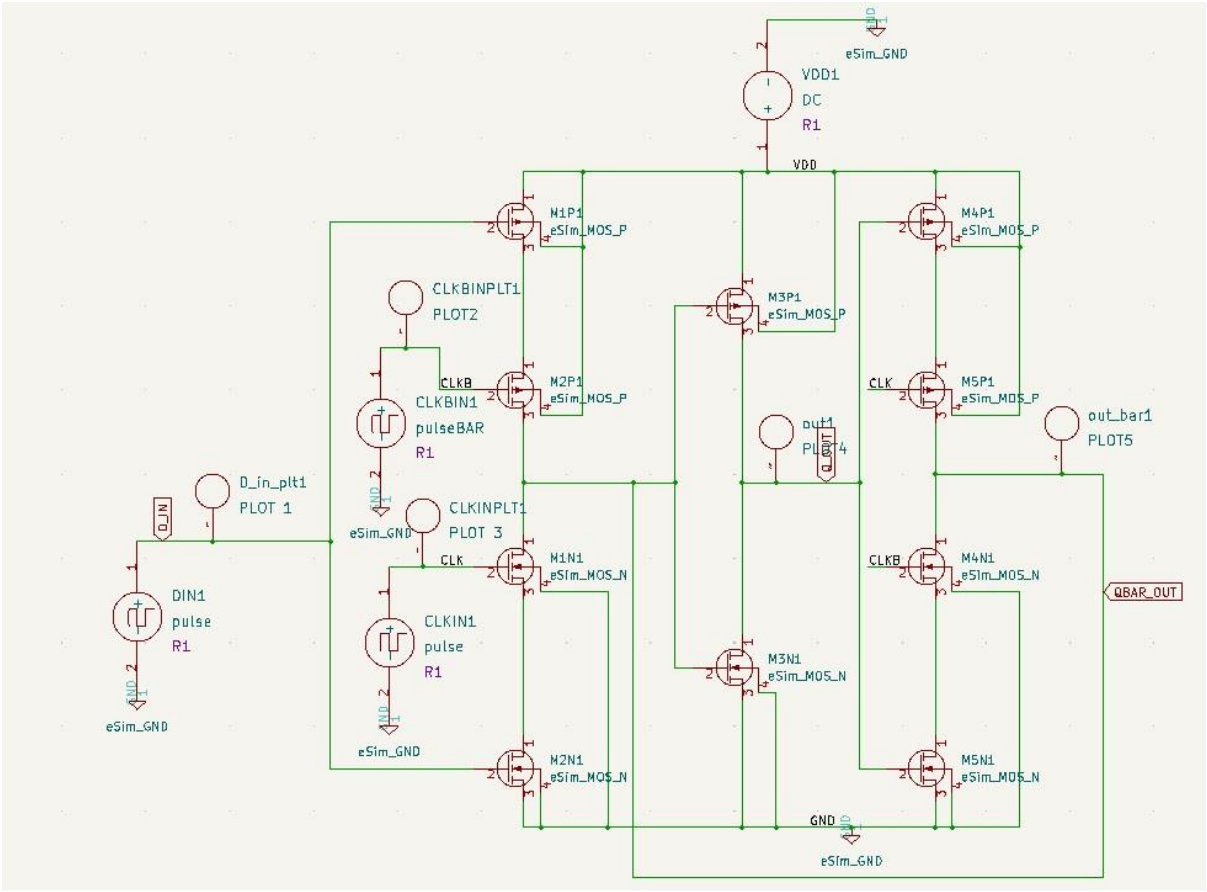

Figure 1: KiCAD Schematic Circuit Diagram of D Flip Flop implementation in esim

D Flip Flop logic stores the value at the Data in put Din and passes it to the output OUT at the rising edge of the clock that is when the clock transits from 0 to 1. D flip flop is thus an edge triggered device i.e. the output changes only when the clock transits from 0 to 1.

Output waveform

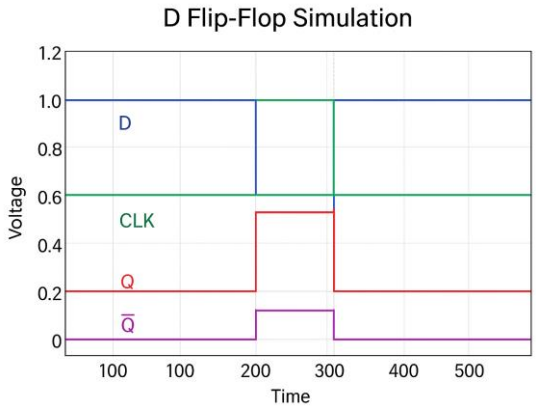

Figure 2: Output Waveform

Conclusion: This project has implemented the D Flip Flop through e sim CMOS logic using both e sim NMOS and e sim PMOS transistor with Data and clock input. The output of the implementation can be realized at OUT and OUT BAR pins. The circuit is activated through DC Power supply of 5v while the clock and clock bar are provided from e sim pulse source. The data input is given through e sim pulse source with a longer time interval when compared to e sim clock pulses for realizing data inputs. The input and output signals are plotted using e sim voltage plot tools.

References

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