

# Circuit Board Guidelines for aQFN<sup>™</sup> Package nAN-40

**Application Note**

v1.1

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# Revision history

Date	Version	Description
April 2018	1.1	Corrected the measurement size of the blind vias
March 2018	1.0	First release

# 1 Introduction

This application note provides information about the aQFN73™ package found on Nordic Semiconductor's nRF52840-QIAA system on chip (SoC). Here you will find how to create the device PCB footprint, the PCB land pattern design, and guidelines for circuit board assembly.

## 2 Package information

Advanced Quad Flat No-lead (aQFN™) is a leadless, multi-row, fine pitch lead frame packaging solution. With a low profile and small footprint, aQFN is a light weight, free-form I/O design which lends itself to enhanced thermal and electrical performance. The aQFN package has a significant cost benefit due to its economical materials and simpler packaging process.

The following mechanical specifications show the dimensions of the aQFN73 7 x 7 mm package in millimeters:

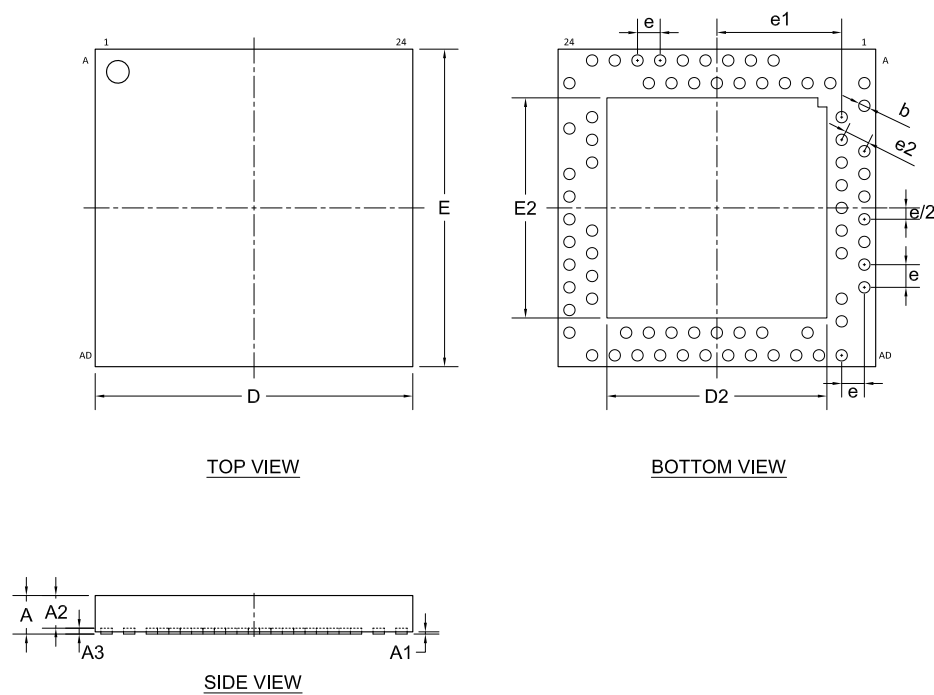


Figure 1: aQFN73 7 x 7 mm package

	A	A1	A2	A3	b	D, E	D2, E2	e	e1	e2
Min.		0.02			0.20		4.75			
Nom.		0.05	0.675	0.13	0.25	7.00	4.85	0.5	2.75	0.559
Max.	0.85	0.08			0.30		4.95			

Table 1: aQFN73 dimensions in millimeters

# 3 PCB land pad design

This chapter shows the recommended dimensions for the component's footprint. To ensure a good electrical connection and solderability of the aQFN73 package, use the included land pattern design. The following figure illustrates the PCB land pad design and dimensions in millimeters:

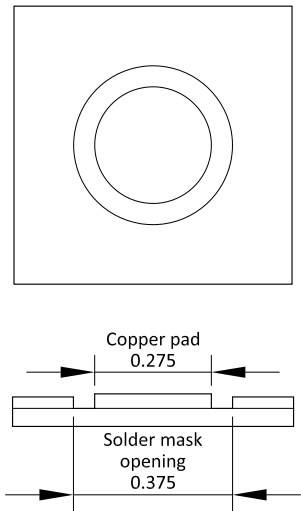


Figure 2: PCB land pad design

The following figure illustrates the PCB thermal pad design and dimensions in millimeters:

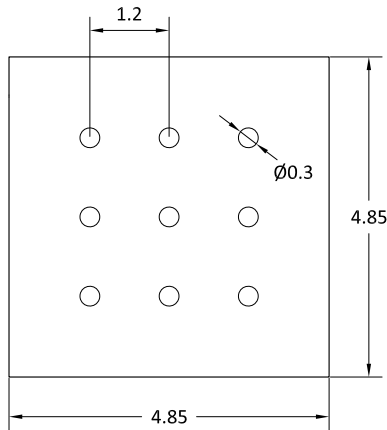


Figure 3: PCB thermal pad design

The following table includes the dimensions of the PCB land pad design:

PCB land pad design	Dimension (mm)
Copper pad diameter	0.275
Solder mask	0.375
Paste mask opening	0.3
Stencil thickness	0.1
Exposed die pad size	4.85
Exposed die pad via diameter	0.3
Exposed die pad via pitch	1.2

Table 2: PCB land pad design

The following figure shows the top view of the aQFN73 footprint with the pads organized in a 250µm grid. The figure illustrates the copper pads (red), solder mask (purple), paste mask (grey), exposed die pad via holes (gray and brown), and package outline (black).

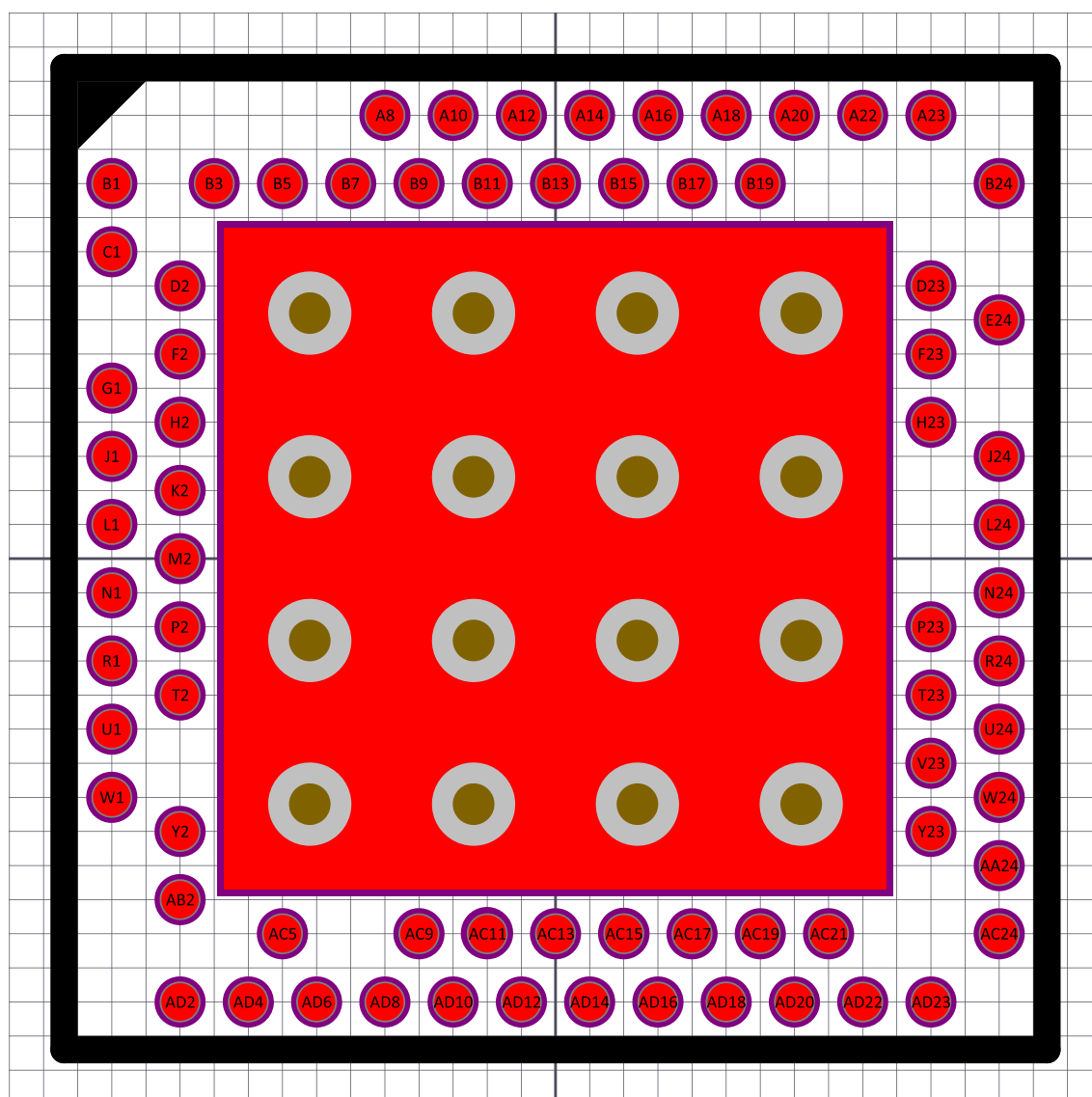


Figure 4: aQFN73 footprint with 250 µm grid

# 4 PCB land pattern design

This chapter contains a recommended PCB land pattern for the aQFN73 package.

The layout in the following figures illustrates the use of a four-layer board with micro vias:

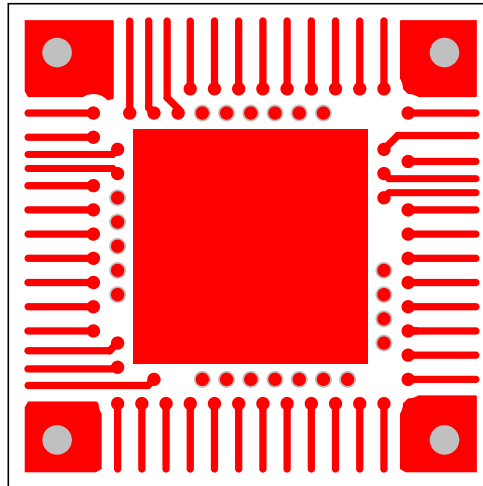


Figure 5: Top layer

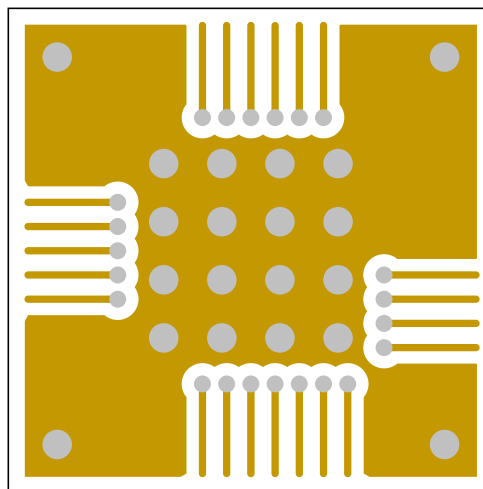


Figure 6: Mid layer 1



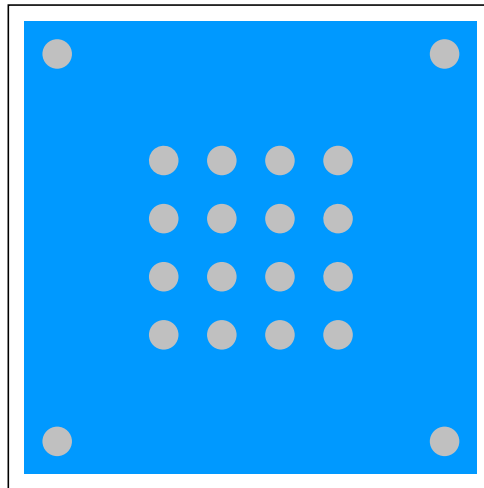


Figure 7: Mid layer 2

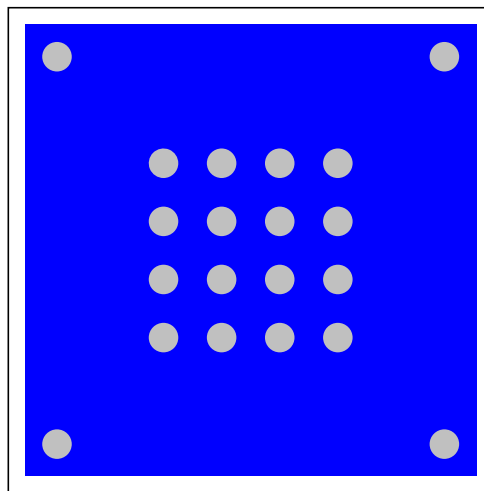


Figure 8: Bottom layer

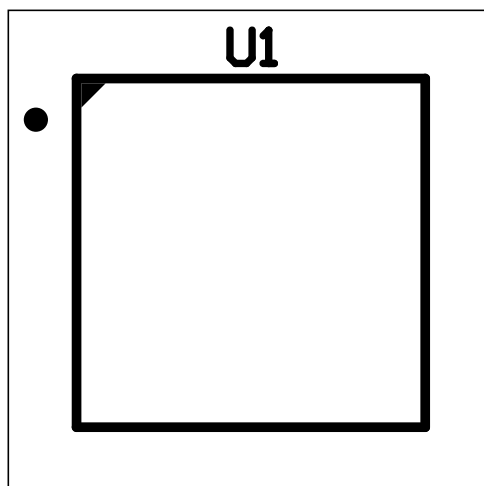


Figure 9: Top silkscreen overlay

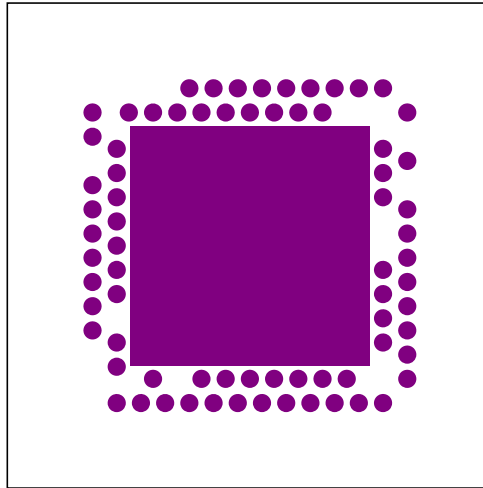


Figure 10: Top solder mask

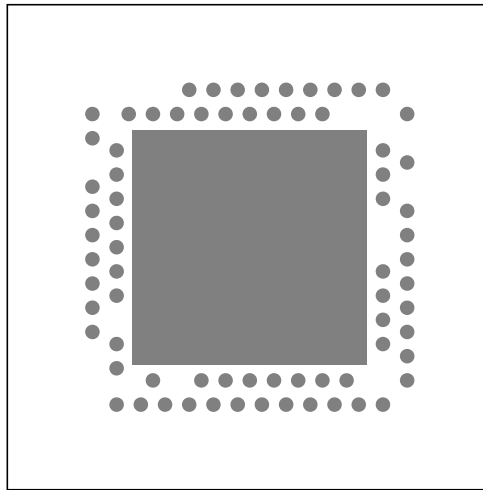


Figure 11: Top paste mask

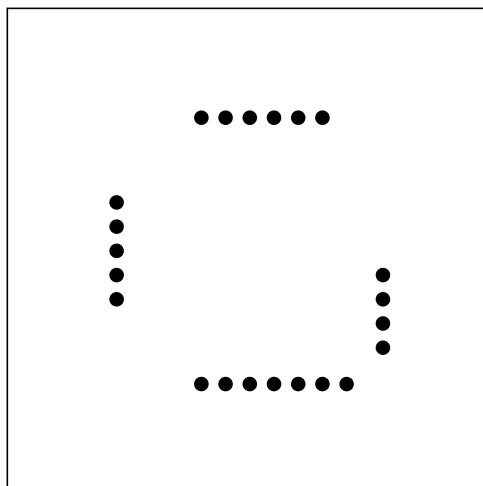


Figure 12: Via capping

Due to the 0.5 mm pitch of the pads in the aQFN package, using via-in-pad technology for routing inner pads is required. Using IPC-4761 Type VII: Filled and capped vias is recommended to ensure good soldering.

Parameter	Design rule (mm)
Minimum trace width	0.145
Minimum clearance	0.145
Hole size blind via	0.15
Hole size through hole via	0.305
Via pad blind via	0.35
Via pad through hole via	0.61

*Table 3: Used design rules*

As the copper pad diameter is small, to ensure an even surface with good solderability, using Electroless Nickel Immersion Gold (ENIG) or similar surface finish on the circuit board is recommended.

For more information on the PCB land pattern design, see the reference layout files at [www.nordicsemi.com](http://www.nordicsemi.com).

# 5 Reflow

This chapter contains information about the recommended reflow profile and solder paste for circuit board assembly using aQFN73.

Type 4 solder paste (25 to 45 micron particle size range) or finer should be used for solder printing. Senju M705-S101-S4 is a recommended solder paste. The following diagram shows the reflow profile for SAC305 solder paste, which is commonly used:

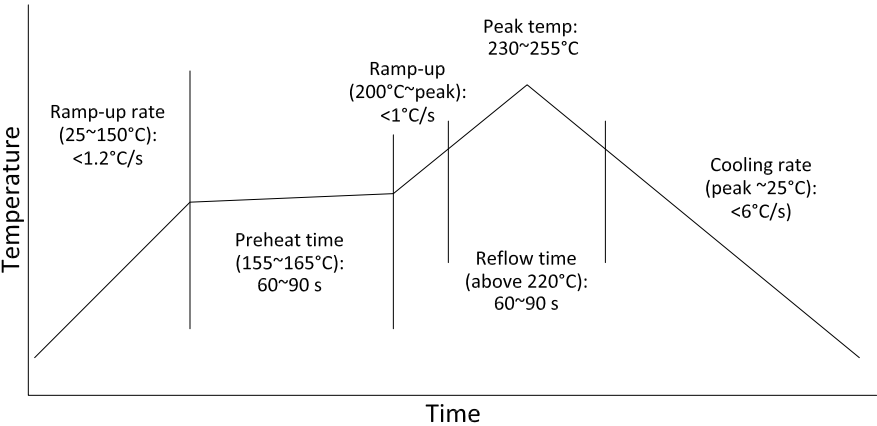


Figure 13: Reflow profile

The following table shows typical temperatures and ramp-up rates for the aQFN package's reflow soldering profile:

Profile feature	Specification	Temperature °C
Ramp-up rate	<1.2°C/s	25~150
Preheat time	60~90 s	155~165
Ramp-up	<1°C/s	200~ peak
Reflow time	60~90 s	Above 220
Peak	-	230~255
Cooling rate	<6°C/s	25~ peak

Table 4: Reflow profile

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