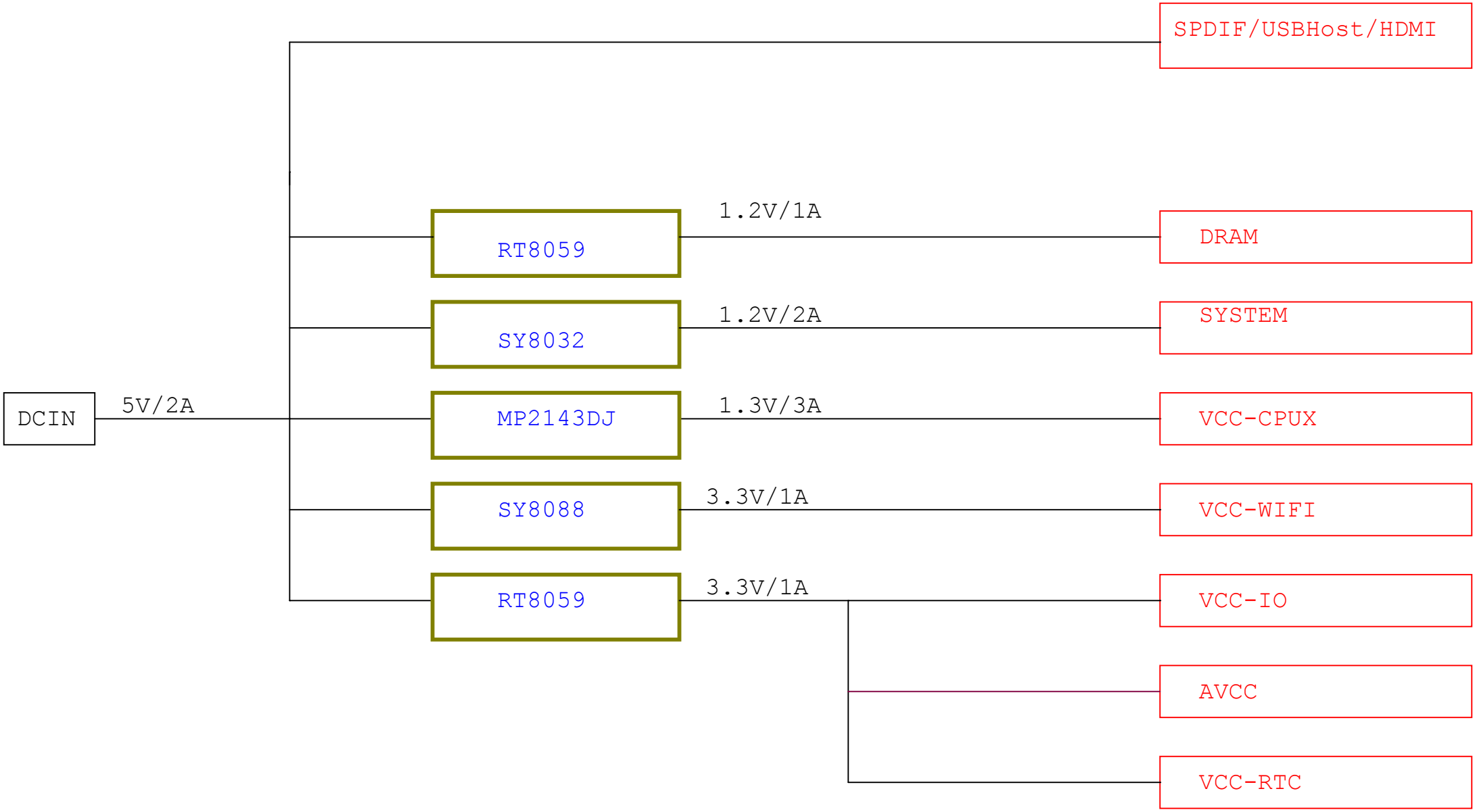
REVISION HISTORY

Schematics Index:

01 REVISION HISTORY
02 POWER TREE
03 GPIO ASSIGNMENT
04 DDR3 16X1
05 CPU
06 POWER
07 eMMC
08 CONNECT

ShengZhen RerVision Technology GO., LTD	
Design Name	H3_CoreBorad
Size: A4	Page Name: REVISION HISTORY
Rev: <RevCode>	
Date: Wednesday, February 07, 2018	Sheet 1 of 8

POWER TREE



ShengZhen RerVision Technology GO., LTD		
Design Name: H3_CoreBorad		
Size: A4	Page Name: POWER TREE	Rev: <RevCode>
Date: Wednesday, February 07, 2018	Sheet 2 of 8	

GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	TMS/DRVVBUS0	3/1	JTAG /USB
PA1	TCK/DRVVBUS1	3/1	
PA2	TDO/WPS	3/1	
PA3	TDI	3	
PA4	UART-TX	3	UART
PA5	UART-RX	3	
PA6	SIM-PWREN	7	SMART CARD
PA7	SIM-CLK	7	
PA8	SIM-DAT	7	
PA9	SIM-RST	7	
PA10	SIM-DET	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	USBID	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	CARD0
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

PIN	Define	CFG	Function
PC0	NWE	2/3	NAND /eMMC /NOR
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	
PC5	NRE	2/3	
PC6	NRB0	2/3	
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PG0	WL-SDIO-CLK	7	WIFI
PG1	WL-SDIO-CMD	7	
PG2	WL-SDIO-D0	7	
PG3	WL-SDIO-D1	7	
PG4	WL-SDIO-D2	7	
PG5	WL-SDIO-D3	7	
PG6	BT-UART-TX	7	BT
PG7	BT-UART-RX	7	
PG8	BT-UART-RTS	7	
PG9	BT-UART-CTS	7	
PG10	WL-WAKE-AP	7	WIFI&BT GPIO
PG11	BT-WAKE-AP	7	
PG12	BT-RST-N	7	
PG13	NC	7	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

PIN	Define	CFG	Function
PL0	TWI	2	TWI
PL1	TWI	2	
PL2	USB0-DRVVBUS	1	USB
PL3	USB1-DRVVBUS	1	
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	CPUX-VSET	7	CPUX-VSET
PL7	WIFI-EN	7	WIFI-EN
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

PIN	Define	CFG	Function
PE0	TS-CLK	7	
PE1	TS-ERR	7	
PE2	TS-SYNC	7	
PE3	TS-DVLD	7	
PE4	TS-D0	7	
PE5	TS-D1	7	
PE6	TS-D2	7	
PE7	TS-D3	7	
PE8	TS-D4	7	
PE9	TS-D5	7	
PE10	TS-D6	7	
PE11	TS-D7	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

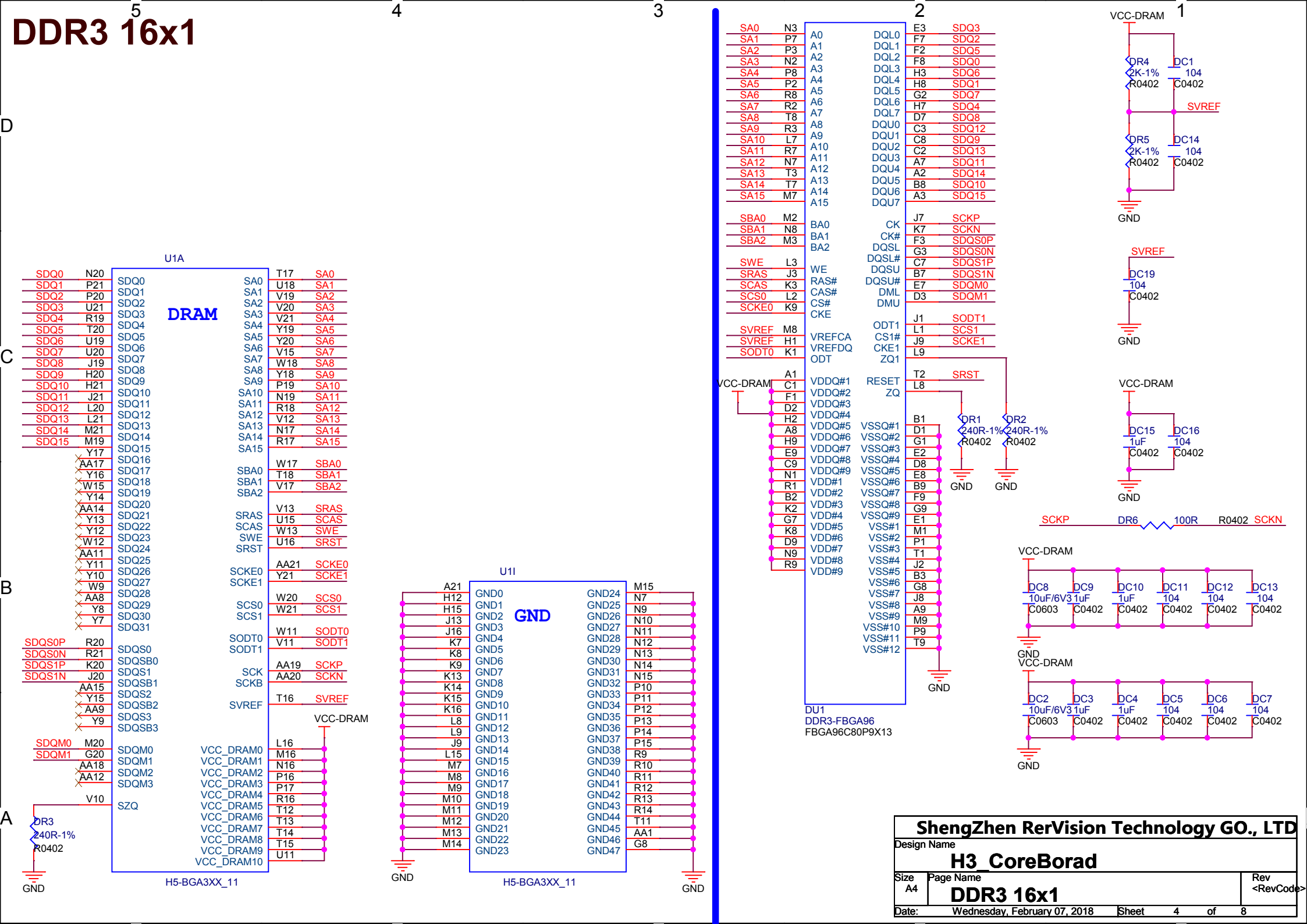
ShengZhen RerVision Technology GO., LTD

Design Name: H3_CoreBorad

Size: A4 | Page Name: GPIO ASSIGNMENT | Rev: <RevCode>

Date: Wednesday, February 07, 2018 | Sheet 3 of 8

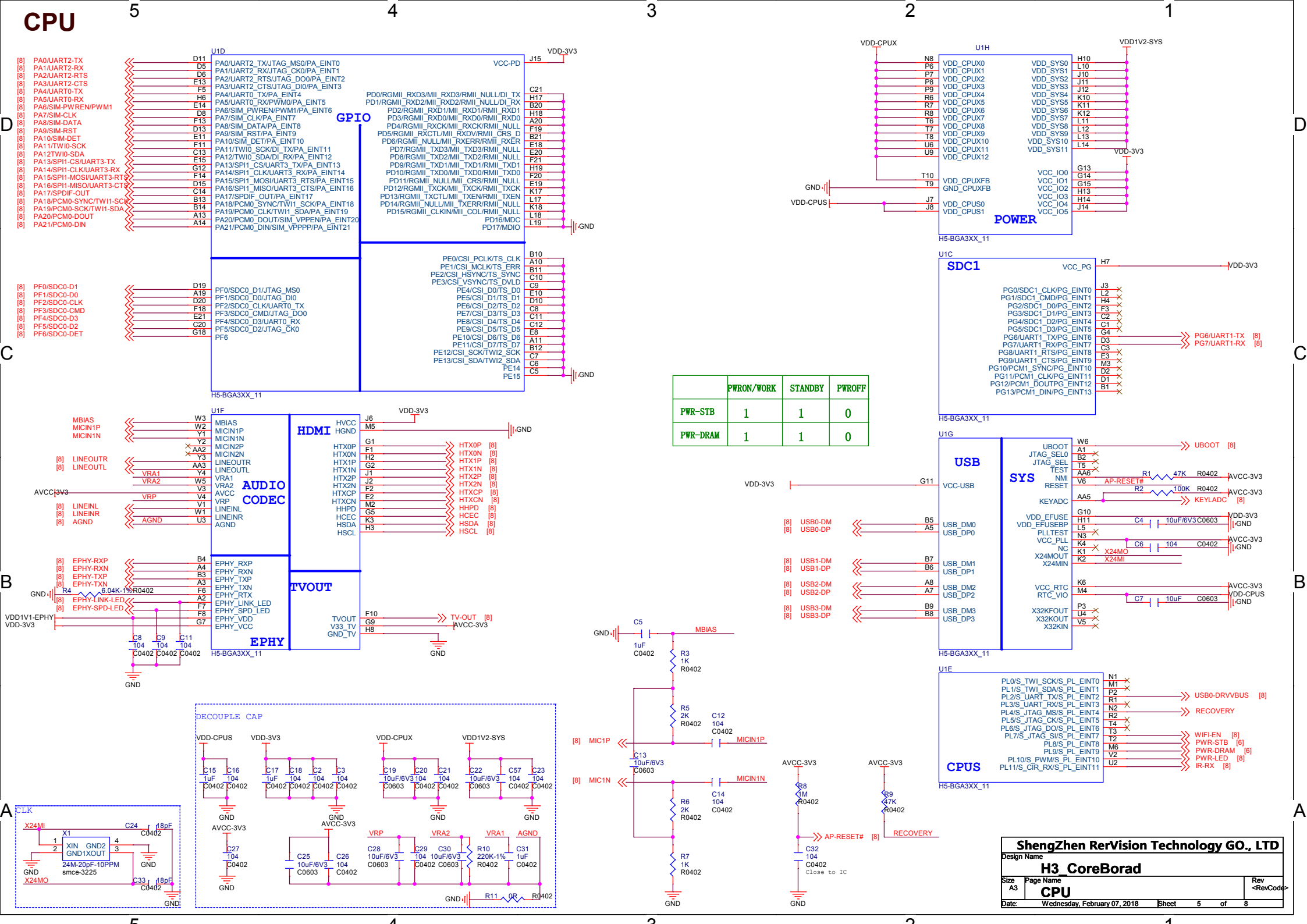
DDR3 16x1



Design Name	H3_CoreBorad
Size	A4
Page Name	DDR3 16x1
Rev	<RevCode>
Date:	Wednesday, February 07, 2018
Sheet	4 of 8

ShengZhen RerVision Technology GO., LTD

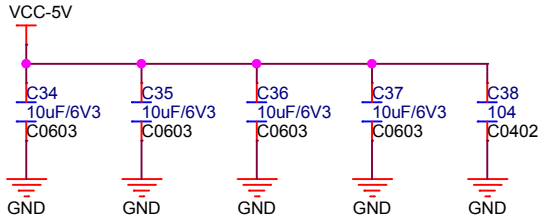
CPU



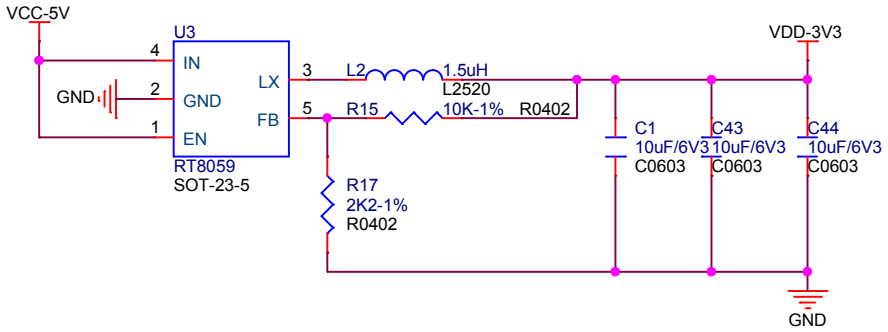
	PWRON/WORK	STANDBY	PWROFF
PWR-STB	1	1	0
PWR-DRAM	1	1	0

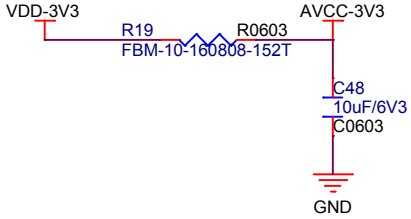
POWER

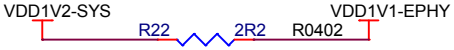
DCIN



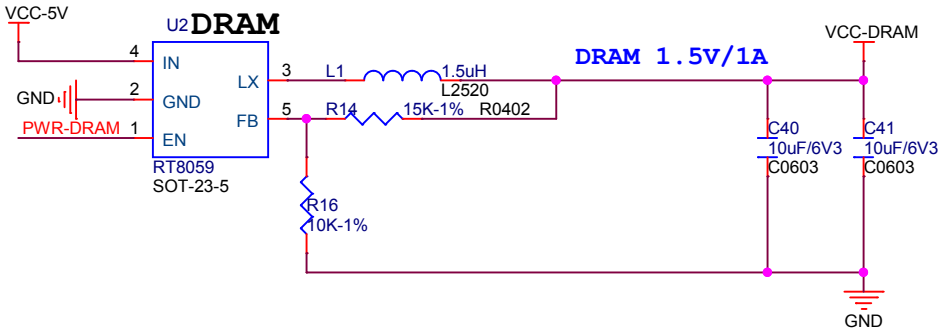
VDD3V3



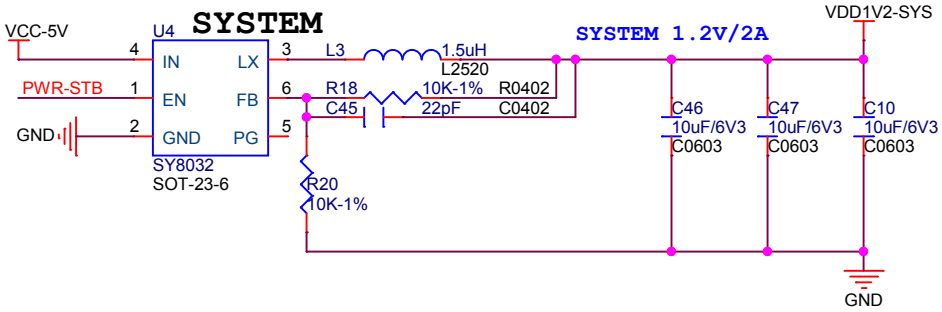




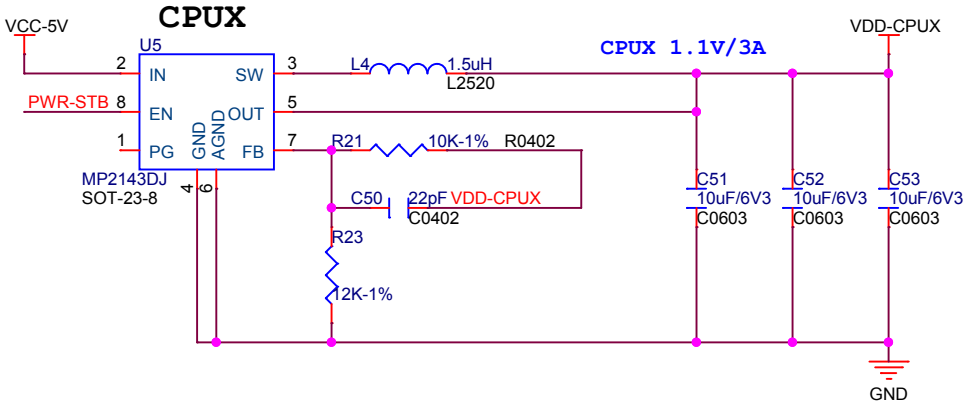
DRAM



SYSTEM



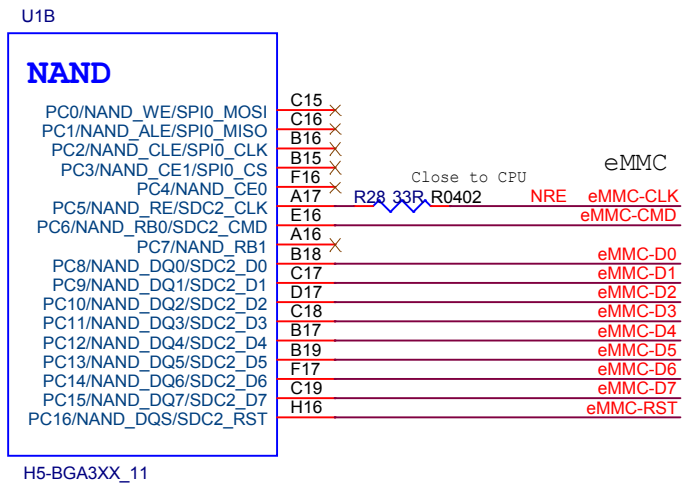
CPUX

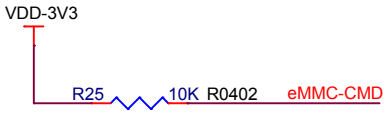


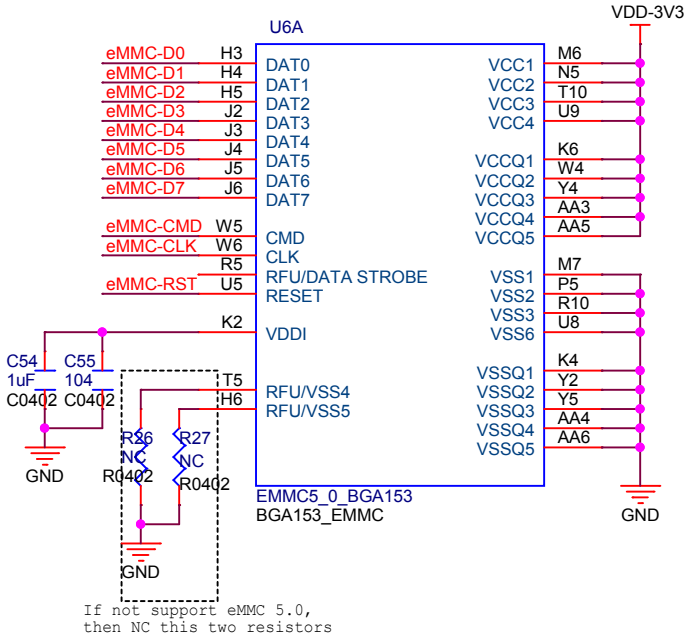
注：VDD-CPUFB 远端 反馈 走线 防 干 扰，请包地。

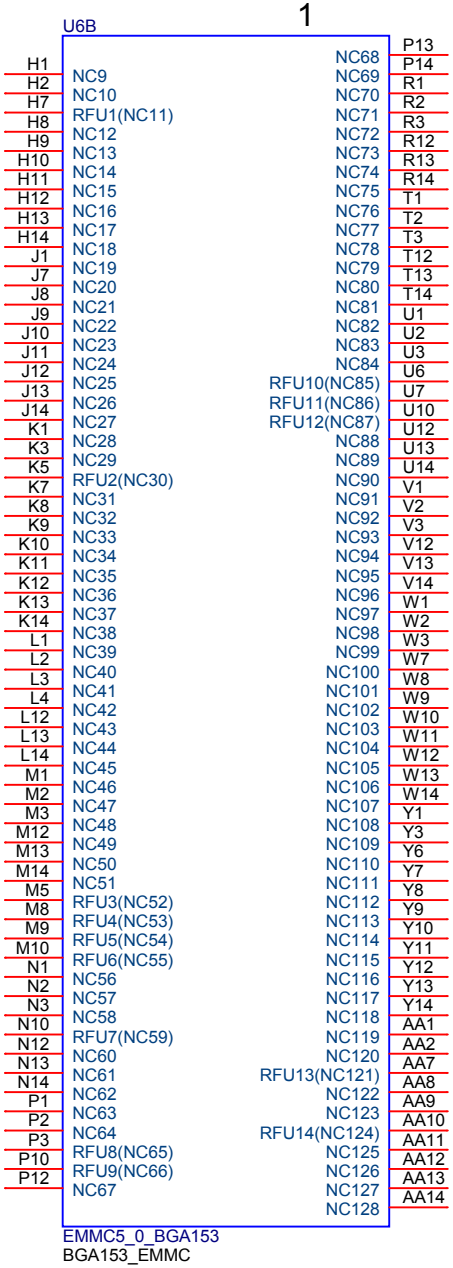
ShengZhen RerVision Technology GO., LTD		
Design Name: H3_CoreBorad		
Size: A4	Page Name: POWER	Rev: <RevCode>
Date: Wednesday, February 07, 2018	Sheet 6 of 8	

eMMC



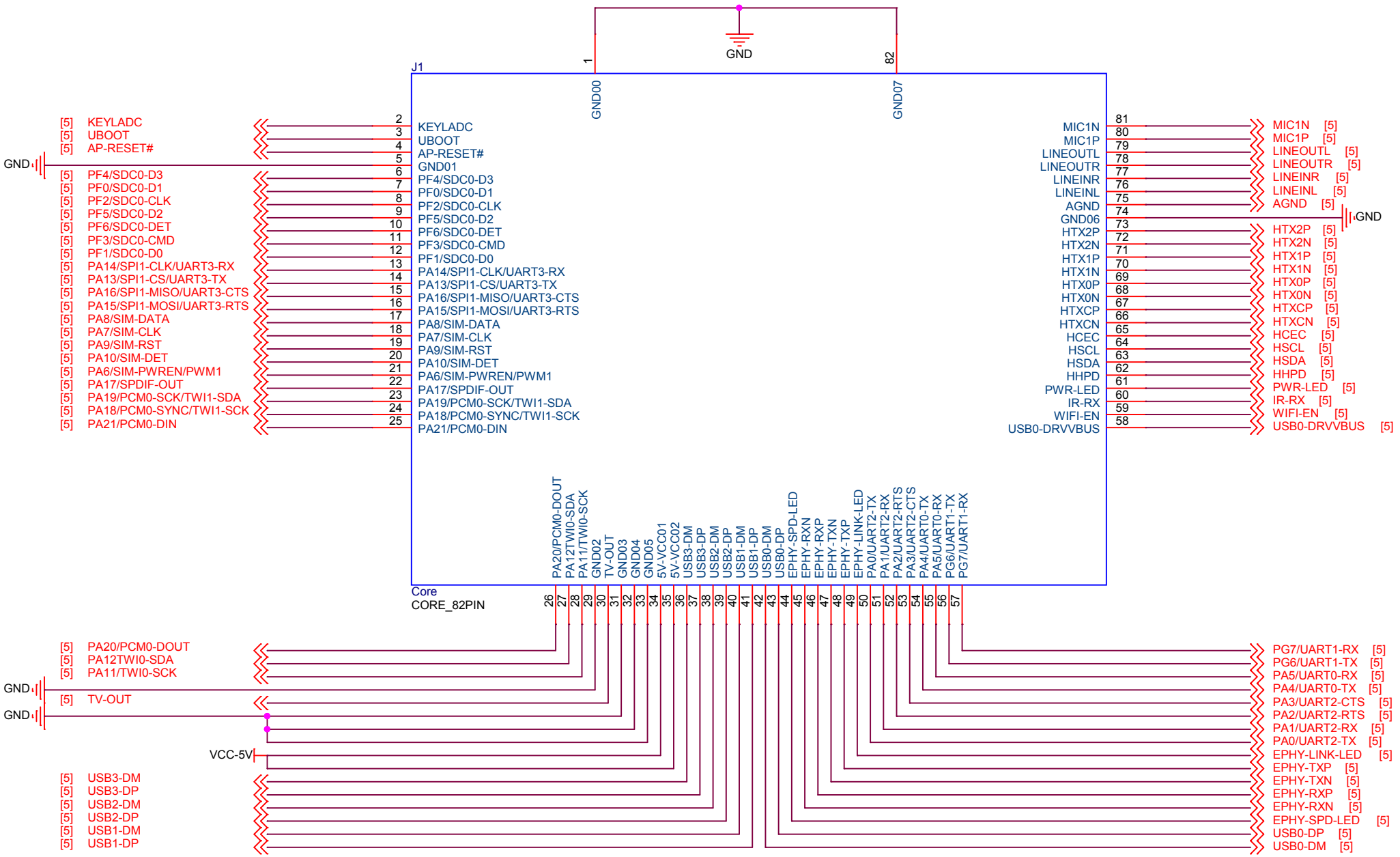






ShengZhen RerVision Technology GO., LTD			
Design Name: H3_CoreBorad			
Size: A4	Page Name: eMMC		Rev: <RevCode>
Date: Wednesday, February 07, 2018		Sheet 7 of 8	

CONNECT



Design Name	H3_CoreBorad
Size	A4
Page Name	CONNECT
Rev	<RevCode>
Date:	Wednesday, February 07, 2018
Sheet	8 of 8

ShengZhen RerVision Technology GO., LTD