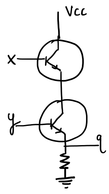
CS M51A Homework 3

Thursday, October 15, 2020 10:32 PM

I completed this assignment entirely on my own except for discussion with Janice Tsai

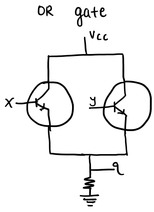
1. NPN bipolar transistors

AND gate



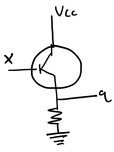
x	y	q
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



x	y	q
0	0	0
0	1	1
1	0	1
1	1	1

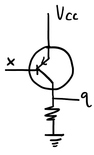
buffer gate



x	q
0	0
1	1

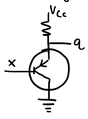
2. PNP bipolar transistors

Inverter gate



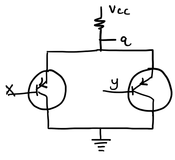
x	q
0	1
1	0

buffer gate



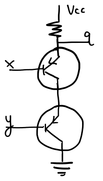
x	q
0	0
1	1

AND gate



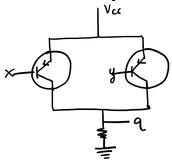
x	y	q
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



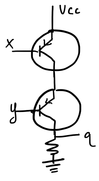
x	y	q
0	0	0
0	1	1
1	0	1
1	1	1

NAND gate



x	y	q
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate



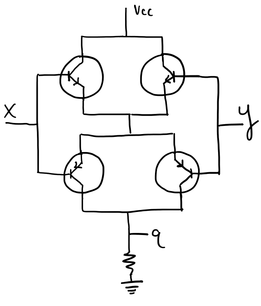
x	y	q
0	0	1
0	1	0
1	0	0
1	1	0

3. exclusive-OR gate

$(x' \cdot y) + (x \cdot y')$, ← 5 operations

$(x + y) \cdot (x \cdot y)'$ ← 4 operations

OR NPN, AND NPN, NAND PNP

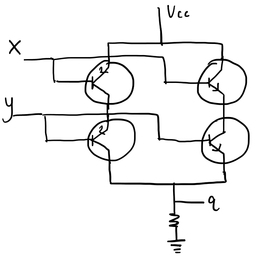


x	y	q
0	0	0
0	1	1
1	0	1
1	1	0

equivalence gate

$(x' \cdot y') + (x \cdot y)$

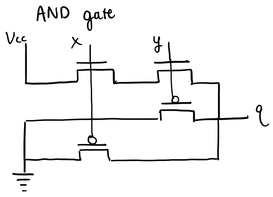
PNP inverter & NPN NPN



x	y	q
0	0	1
0	1	0
1	0	0
1	1	1

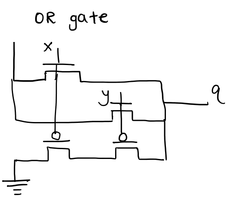
4. CMOS gates - Nmos + Pmos, 2 transistors per input

AND gate



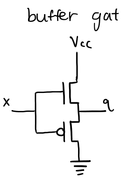
x	y	q
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



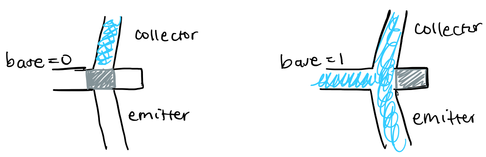
x	y	q
0	0	0
0	1	1
1	0	1
1	1	1

buffer gate



x	q
0	0
1	1

5. Water-pipe "transistor"



In my water-pipe transistor, there is a plug/block that blocks the water from the collector pipe from travelling to the emitter. this is the initial state (when the base = 0).

When the base input is 1, there is water travelling and its pressure pushes the block out of the way to allow the water to travel between the collector and emitter.