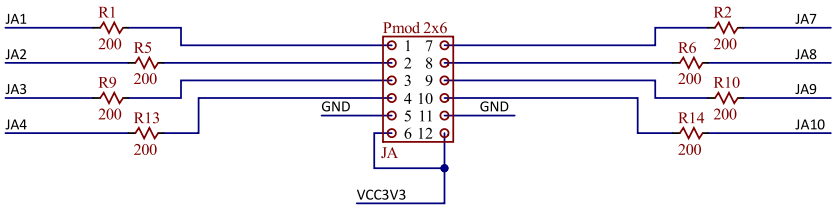

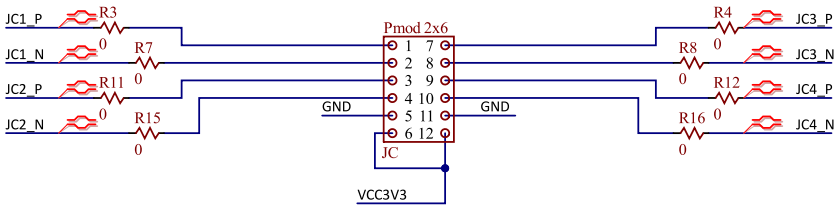

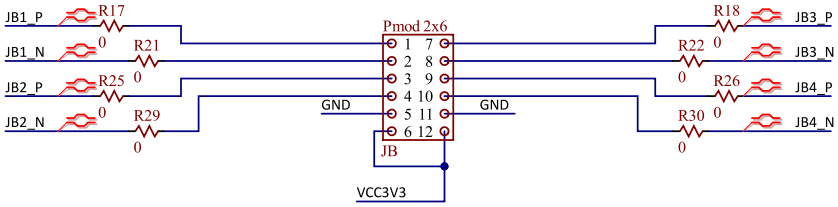

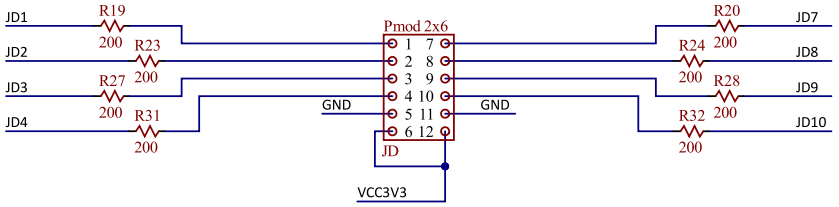

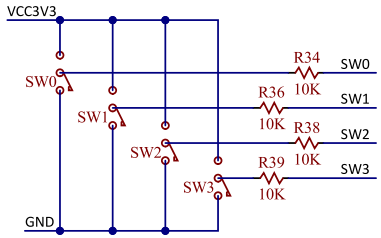

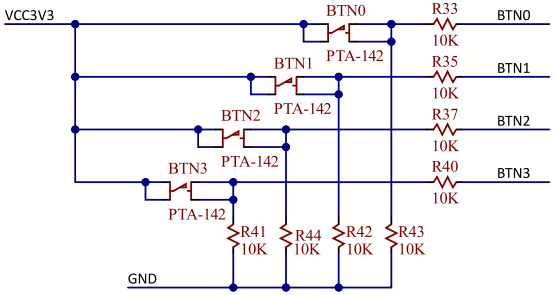

Foot F1
Foot F2
Foot F3
Foot F4

Avnet | Xilinx | Digilent Inc. | CE | ROHS | Chinese ROHS | Arty A7

Title	Arty A7
Rev	E.2
Circuit	PMOD, BTN, SWTs
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	1 out of 12

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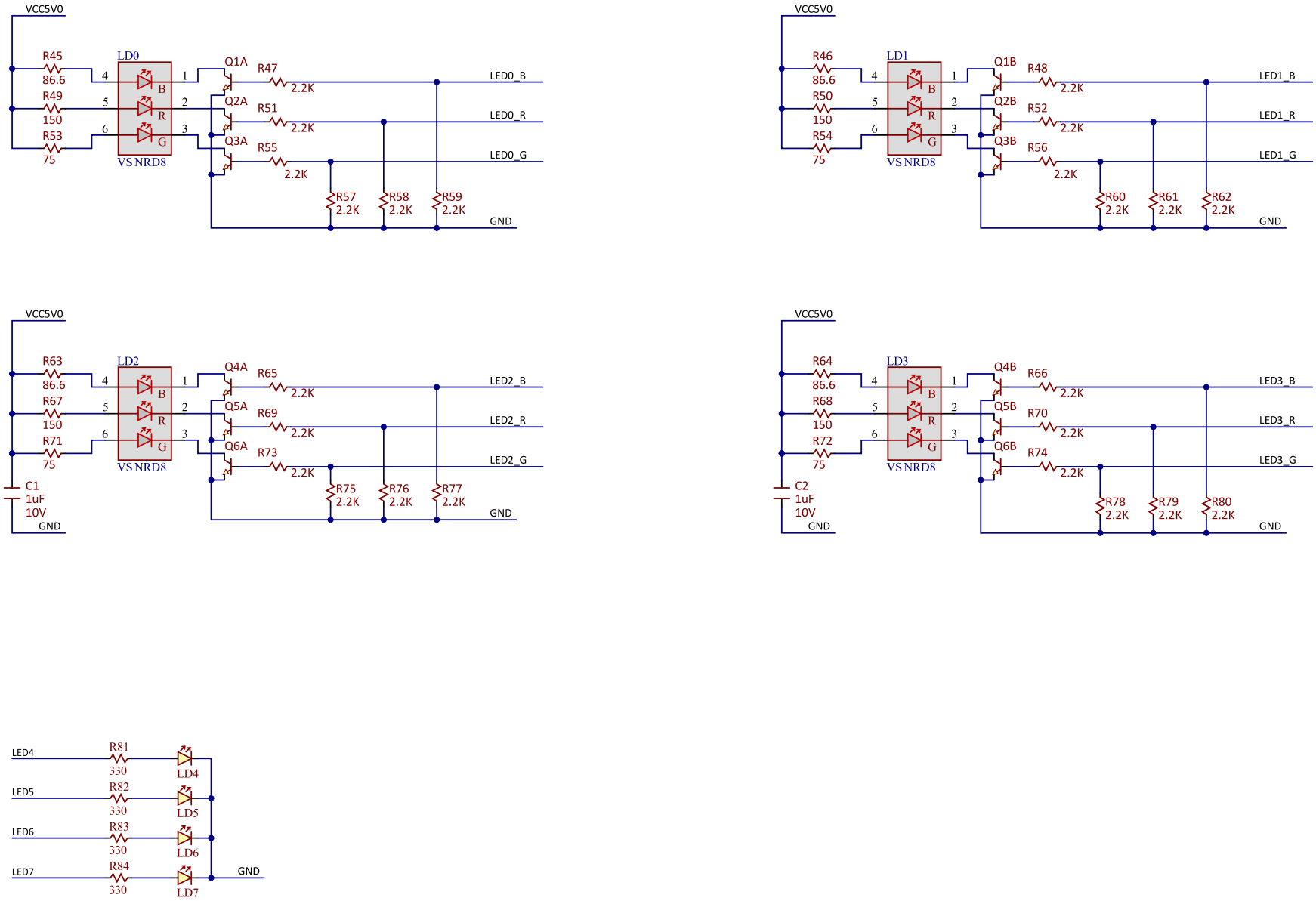
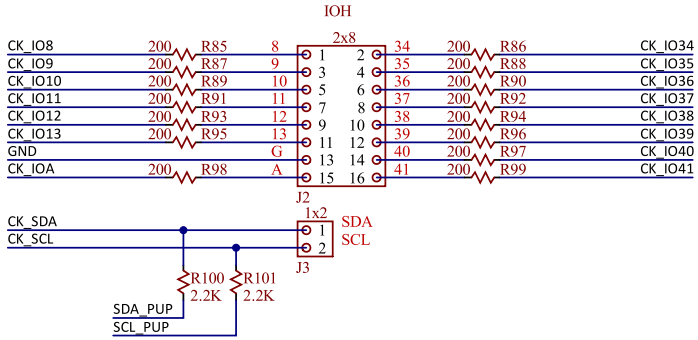
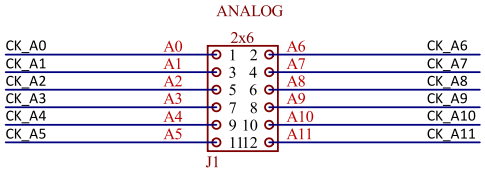
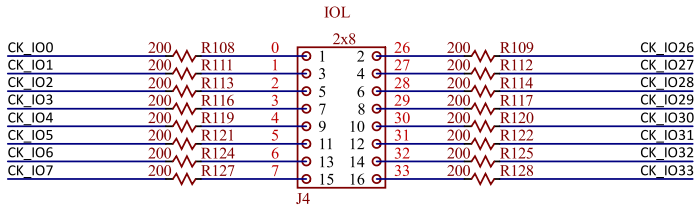
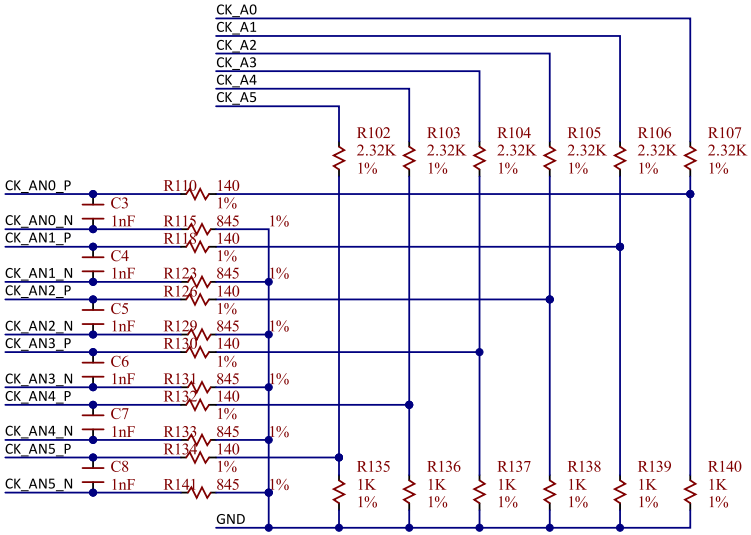


Title	Arty A7
Rev	E.2
Circuit	LEDs
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	2 out of 12

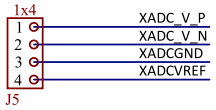


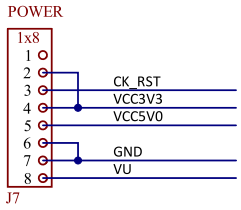


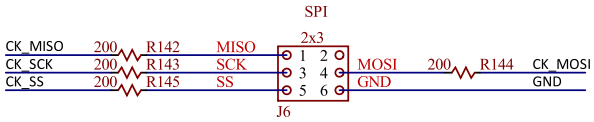




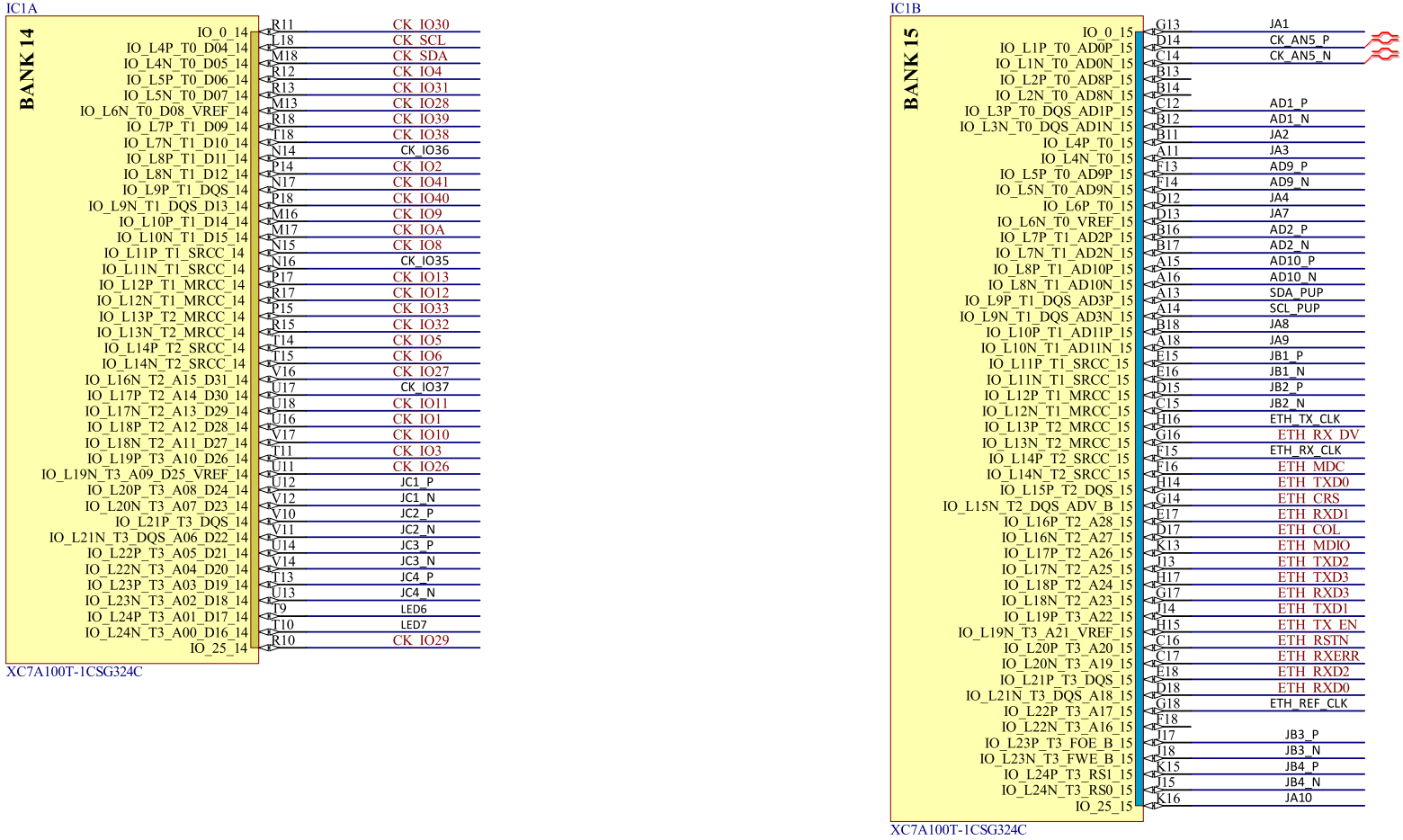
Note: Terminate N signals next to Analog Header







Title	Arty A7
Rev	E.2
Circuit	CHipKIT IO
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	3 out of 12


IC1A
BANK 14
IO_0_14 R11 CK_IO30
IO_L4P_T0_D04_14 T8 CK_SCL
IO_L4N_T0_D05_14 M18 CK_SDA
IO_L5P_T0_D06_14 R12 CK_IO4
IO_L5N_T0_D07_14 R13 CK_IO31
IO_L6N_T0_D08_VREF_14 M13 CK_IO28
IO_L7P_T1_D09_14 R18 CK_IO39
IO_L7N_T1_D10_14 T18 CK_IO38
IO_L8P_T1_D11_14 N14 CK_IO36
IO_L8N_T1_D12_14 P14 CK_IO2
IO_L9P_T1_DQS_14 N17 CK_IO41
IO_L9N_T1_DQS_D13_14 P18 CK_IO40
IO_L10P_T1_D14_14 M16 CK_IO9
IO_L10N_T1_D15_14 M17 CK_IOA
IO_L11P_T1_SRCC_14 N15 CK_IO8
IO_L11N_T1_SRCC_14 N16 CK_IO35
IO_L12P_T1_MRCC_14 P17 CK_IO13
IO_L12N_T1_MRCC_14 R17 CK_IO12
IO_L13P_T2_MRCC_14 P15 CK_IO33
IO_L13N_T2_MRCC_14 R15 CK_IO32
IO_L14P_T2_SRCC_14 T14 CK_IO5
IO_L14N_T2_SRCC_14 T15 CK_IO6
IO_L16N_T2_A15_D31_14 V16 CK_IO27
IO_L17P_T2_A14_D30_14 U17 CK_IO37
IO_L17N_T2_A13_D29_14 U18 CK_IO11
IO_L18P_T2_A12_D28_14 U16 CK_IO1
IO_L18N_T2_A11_D27_14 V17 CK_IO10
IO_L19P_T3_A10_D26_14 T11 CK_IO3
IO_L19N_T3_A09_D25_VREF_14 U11 CK_IO26
IO_L20P_T3_A08_D24_14 U12 JC1_P
IO_L20N_T3_A07_D23_14 V12 JC1_N
IO_L21P_T3_DQS_14 V10 JC2_P
IO_L21N_T3_DQS_A06_D22_14 V11 JC2_N
IO_L22P_T3_A05_D21_14 U14 JC3_P
IO_L22N_T3_A04_D20_14 V14 JC3_N
IO_L23P_T3_A03_D19_14 T13 JC4_P
IO_L23N_T3_A02_D18_14 U13 JC4_N
IO_L24P_T3_A01_D17_14 T9 LED6
IO_L24N_T3_A00_D16_14 T10 LED7
IO_25_14 R10 CK_IO29
XC7A100T-1CSG324C
IC1B
BANK 15
IO_0_15 G13 JA1
IO_L1P_T0_AD0P_15 D14 CK_AN5_P
IO_L1N_T0_AD0N_15 C14 CK_AN5_N
IO_L2P_T0_AD8P_15 B13
IO_L2N_T0_AD8N_15 B14
IO_L3P_T0_DQS_AD1P_15 C12 AD1_P
IO_L3N_T0_DQS_AD1N_15 B12 AD1_N
IO_L4P_T0_15 B11 JA2
IO_L4N_T0_15 A11 JA3
IO_L5P_T0_AD9P_15 F13 AD9_P
IO_L5N_T0_AD9N_15 F14 AD9_N
IO_L6P_T0_15 D12 JA4
IO_L6N_T0_VREF_15 D13 JA7
IO_L7P_T1_AD2P_15 B16 AD2_P
IO_L7N_T1_AD2N_15 B17 AD2_N
IO_L8P_T1_AD10P_15 A15 AD10_P
IO_L8N_T1_AD10N_15 A16 AD10_N
IO_L9P_T1_DQS_AD3P_15 A13 SDA_PUP
IO_L9N_T1_DQS_AD3N_15 A14 SCL_PUP
IO_L10P_T1_AD11P_15 B18 JA8
IO_L10N_T1_AD11N_15 A18 JA9
IO_L11P_T1_SRCC_15 E15 JB1_P
IO_L11N_T1_SRCC_15 E16 JB1_N
IO_L12P_T1_MRCC_15 D15 JB2_P
IO_L12N_T1_MRCC_15 C15 JB2_N
IO_L13P_T2_MRCC_15 H16 ETH_TX_CLK
IO_L13N_T2_MRCC_15 G16 ETH_RX_DV
IO_L14P_T2_SRCC_15 F15 ETH_RX_CLK
IO_L14N_T2_SRCC_15 F16 ETH_MDC
IO_L15P_T2_DQS_15 H14 ETH_TXD0
IO_L15N_T2_DQS_ADV_B_15 G14 ETH_CRS
IO_L16P_T2_A28_15 E17 ETH_RXD1
IO_L16N_T2_A27_15 D17 ETH_COL
IO_L17P_T2_A26_15 K13 ETH_MDIO
IO_L17N_T2_A25_15 J13 ETH_TXD2
IO_L18P_T2_A24_15 H17 ETH_TXD3
IO_L18N_T2_A23_15 G17 ETH_RXD3
IO_L19P_T3_A22_15 J14 ETH_TXD1
IO_L19N_T3_A21_VREF_15 H15 ETH_TX_EN
IO_L20P_T3_A20_15 C16 ETH_RSTN
IO_L20N_T3_A19_15 C17 ETH_RXERR
IO_L21P_T3_DQS_15 E18 ETH_RXD2
IO_L21N_T3_DQS_A18_15 D18 ETH_RXD0
IO_L22P_T3_A17_15 G18 ETH_REF_CLK
IO_L22N_T3_A16_15 F18
IO_L23P_T3_FOE_B_15 J17 JB3_P
IO_L23N_T3_FWE_B_15 J18 JB3_N
IO_L24P_T3_RS1_15 K15 JB4_P
IO_L24N_T3_RS0_15 J15 JB4_N
IO_25_15 K16 JA10
XC7A100T-1CSG324C
IC1C
BANK 16
IO_L6N_T0_VREF_16 D9 BTN0
IO_L11P_T1_SRCC_16 C9 BTN1
IO_L11N_T1_SRCC_16 B9 BTN2
IO_L12P_T1_MRCC_16 B8 BTN3
IO_L12N_T1_MRCC_16 A8 SW0
IO_L13P_T2_MRCC_16 C11 SW1
IO_L13N_T2_MRCC_16 C10 SW2
IO_L14P_T2_SRCC_16 A10 SW3
IO_L14N_T2_SRCC_16 A9 UART_TXD_IN
IO_L19N_T3_VREF_16 D10 UART_RXD_OUT
XC7A100T-1CSG324C
VSNS5V0_P R146 100 1% AD1_P
VSNS5V0_N R147 100 1% C9 910pF AD1_N
SNS5V0_P R148 845 1% AD9_P
SNS5V0_N R149 845 1% C10 1nF AD9_N
VSNSVU_P R150 100 1% AD2_P
VSNSVU_N R151 100 1% C11 820pF AD2_N
SNSVCCINT_P R152 845 1% AD10_P
SNSVCCINT_N R153 845 1% C12 1nF AD10_N
Title
Arty A7
Rev
E.2
Circuit
FPGA Banks
Doc# 500-319
Engineer MTA
Author GMA
Date 1/25/2022
Sheet# 4 out of 12
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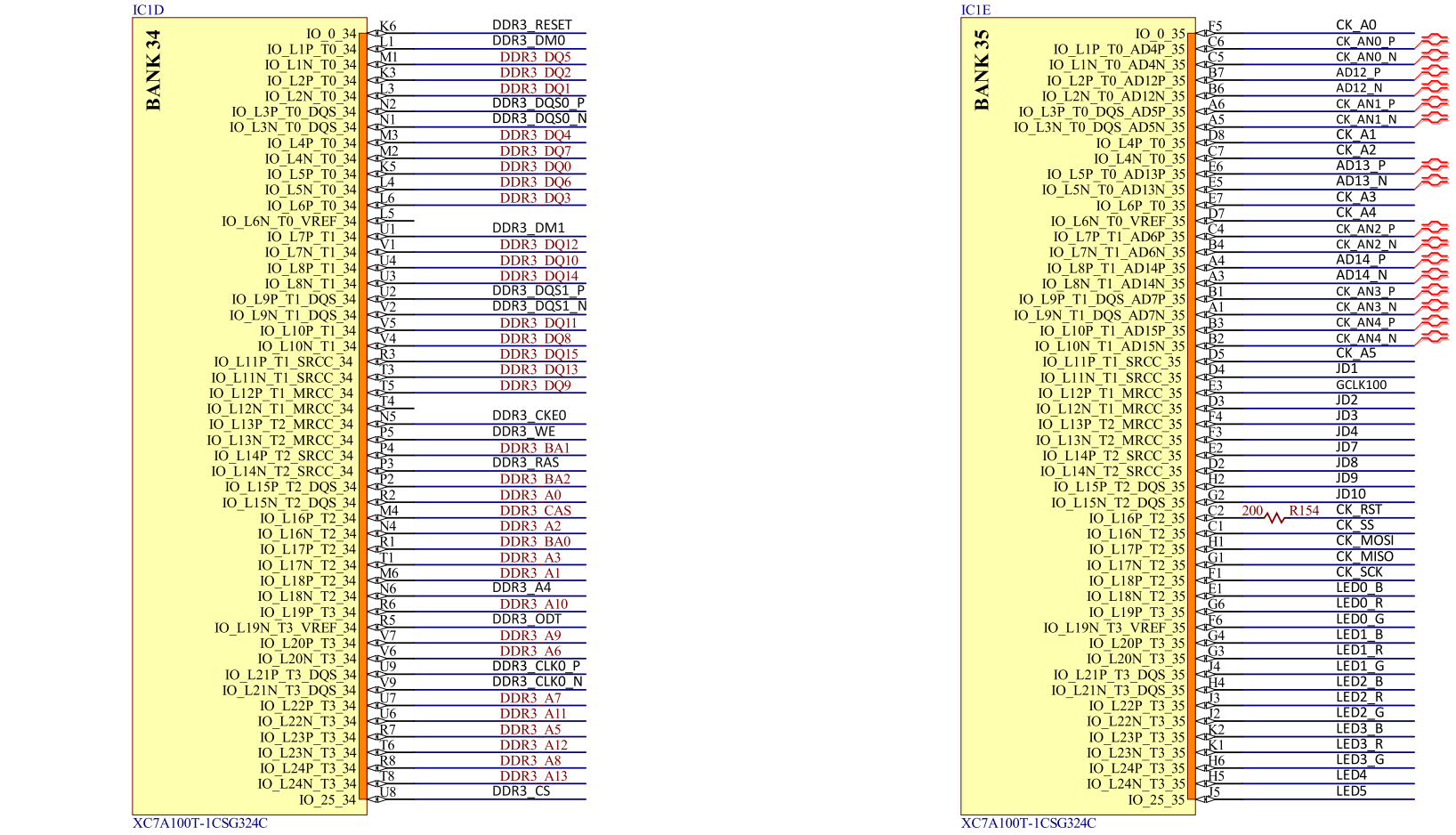
IC1D
BANK 34
IO_0_34 K6 DDR3_RESET
IO_L1P_T0_34 J1 DDR3_DM0
IO_L1N_T0_34 M1 DDR3_DQ5
IO_L2P_T0_34 K3 DDR3_DQ2
IO_L2N_T0_34 L3 DDR3_DQ1
IO_L3P_T0_DQS_34 N2 DDR3_DQS0_P
IO_L3N_T0_DQS_34 N1 DDR3_DQS0_N
IO_L4P_T0_34 M3 DDR3_DQ4
IO_L4N_T0_34 M2 DDR3_DQ7
IO_L5P_T0_34 K5 DDR3_DQ0
IO_L5N_T0_34 L4 DDR3_DQ6
IO_L6P_T0_34 L6 DDR3_DQ3
IO_L6N_T0_VREF_34 J5
IO_L7P_T1_34 U1 DDR3_DM1
IO_L7N_T1_34 V1 DDR3_DQ12
IO_L8P_T1_34 U4 DDR3_DQ10
IO_L8N_T1_34 U3 DDR3_DQ14
IO_L9P_T1_DQS_34 U2 DDR3_DQS1_P
IO_L9N_T1_DQS_34 V2 DDR3_DQS1_N
IO_L10P_T1_34 V5 DDR3_DQ11
IO_L10N_T1_34 V4 DDR3_DQ8
IO_L11P_T1_SRCC_34 R3 DDR3_DQ15
IO_L11N_T1_SRCC_34 T3 DDR3_DQ13
IO_L12P_T1_MRCC_34 T5 DDR3_DQ9
IO_L12N_T1_MRCC_34 T4
IO_L13P_T2_MRCC_34 N5 DDR3_CKE0
IO_L13N_T2_MRCC_34 P5 DDR3_WE
IO_L14P_T2_SRCC_34 P4 DDR3_BA1
IO_L14N_T2_SRCC_34 P3 DDR3_RAS
IO_L15P_T2_DQS_34 P2 DDR3_BA2
IO_L15N_T2_DQS_34 R2 DDR3_A0
IO_L16P_T2_34 M4 DDR3_CAS
IO_L16N_T2_34 N4 DDR3_A2
IO_L17P_T2_34 R1 DDR3_BA0
IO_L17N_T2_34 T1 DDR3_A3
IO_L18P_T2_34 M6 DDR3_A1
IO_L18N_T2_34 N6 DDR3_A4
IO_L19P_T3_34 R6 DDR3_A10
IO_L19N_T3_VREF_34 R5 DDR3_ODT
IO_L20P_T3_34 V7 DDR3_A9
IO_L20N_T3_34 V6 DDR3_A6
IO_L21P_T3_DQS_34 U9 DDR3_CLK0_P
IO_L21N_T3_DQS_34 V9 DDR3_CLK0_N
IO_L22P_T3_34 U7 DDR3_A7
IO_L22N_T3_34 U6 DDR3_A11
IO_L23P_T3_34 R7 DDR3_A5
IO_L23N_T3_34 T6 DDR3_A12
IO_L24P_T3_34 R8 DDR3_A8
IO_L24N_T3_34 T8 DDR3_A13
IO_25_34 U8 DDR3_CS
XC7A100T-1CSG324C
IC1E
BANK 35
IO_0_35 F5 CK_A0
IO_L1P_T0_AD4P_35 C6 CK_AN0_P
IO_L1N_T0_AD4N_35 C5 CK_AN0_N
IO_L2P_T0_AD12P_35 B7 AD12_P
IO_L2N_T0_AD12N_35 B6 AD12_N
IO_L3P_T0_DQS_AD5P_35 A6 CK_AN1_P
IO_L3N_T0_DQS_AD5N_35 A5 CK_AN1_N
IO_L4P_T0_35 D8 CK_A1
IO_L4N_T0_35 C7 CK_A2
IO_L5P_T0_AD13P_35 E6 AD13_P
IO_L5N_T0_AD13N_35 E5 AD13_N
IO_L6P_T0_35 E7 CK_A3
IO_L6N_T0_VREF_35 D7 CK_A4
IO_L7P_T1_AD6P_35 C4 CK_AN2_P
IO_L7N_T1_AD6N_35 B4 CK_AN2_N
IO_L8P_T1_AD14P_35 A4 AD14_P
IO_L8N_T1_AD14N_35 A3 AD14_N
IO_L9P_T1_DQS_AD7P_35 B1 CK_AN3_P
IO_L9N_T1_DQS_AD7N_35 A1 CK_AN3_N
IO_L10P_T1_AD15P_35 B3 CK_AN4_P
IO_L10N_T1_AD15N_35 B2 CK_AN4_N
IO_L11P_T1_SRCC_35 D5 CK_A5
IO_L11N_T1_SRCC_35 D4 JD1
IO_L12P_T1_MRCC_35 E3 GCLK100
IO_L12N_T1_MRCC_35 D3 JD2
IO_L13P_T2_MRCC_35 F4 JD3
IO_L13N_T2_MRCC_35 F3 JD4
IO_L14P_T2_SRCC_35 E2 JD7
IO_L14N_T2_SRCC_35 D2 JD8
IO_L15P_T2_DQS_35 H2 JD9
IO_L15N_T2_DQS_35 G2 JD10
IO_L16P_T2_35 C2 200 R154 CK_RST
IO_L16N_T2_35 C1 CK_SS
IO_L17P_T2_35 H1 CK_MOSI
IO_L17N_T2_35 G1 CK_MISO
IO_L18P_T2_35 F1 CK_SCK
IO_L18N_T2_35 E1 LED0_B
IO_L19P_T3_35 G6 LED0_R
IO_L19N_T3_VREF_35 F6 LED0_G
IO_L20P_T3_35 G4 LED1_B
IO_L20N_T3_35 G3 LED1_R
IO_L21P_T3_DQS_35 J4 LED1_G
IO_L21N_T3_DQS_35 H4 LED2_B
IO_L22P_T3_35 J3 LED2_R
IO_L22N_T3_35 J2 LED2_G
IO_L23P_T3_35 K2 LED3_B
IO_L23N_T3_35 K1 LED3_R
IO_L24P_T3_35 H6 LED3_G
IO_L24N_T3_35 H5 LED4
IO_25_35 J5 LED5
XC7A100T-1CSG324C
VCC3V3
C14
100nF
GND
IC2
VDD
STBY
OUT
GND
GCLK100
GND
ASEM1-100.000MHZ-LC-T
VCC3V3
R155
10K
CK_RST
R158
200
BTNR
PTA-142 Red Knob
GND
CK_A6 R156 140 C13 AD12_P
CK_A7 R157 140 1nF No Load AD12_N
CK_A8 R159 140 C15 AD13_P
CK_A9 R160 140 1nF No Load AD13_N
CK_A10 R161 140 C16 AD14_P
CK_A11 R162 140 1nF No Load AD14_N
Title
Arty A7
Rev
E.2
Circuit
FPGA Banks
Doc# 500-319
Engineer MTA
Author GMA
Date 1/25/2022
Sheet# 5 out of 12
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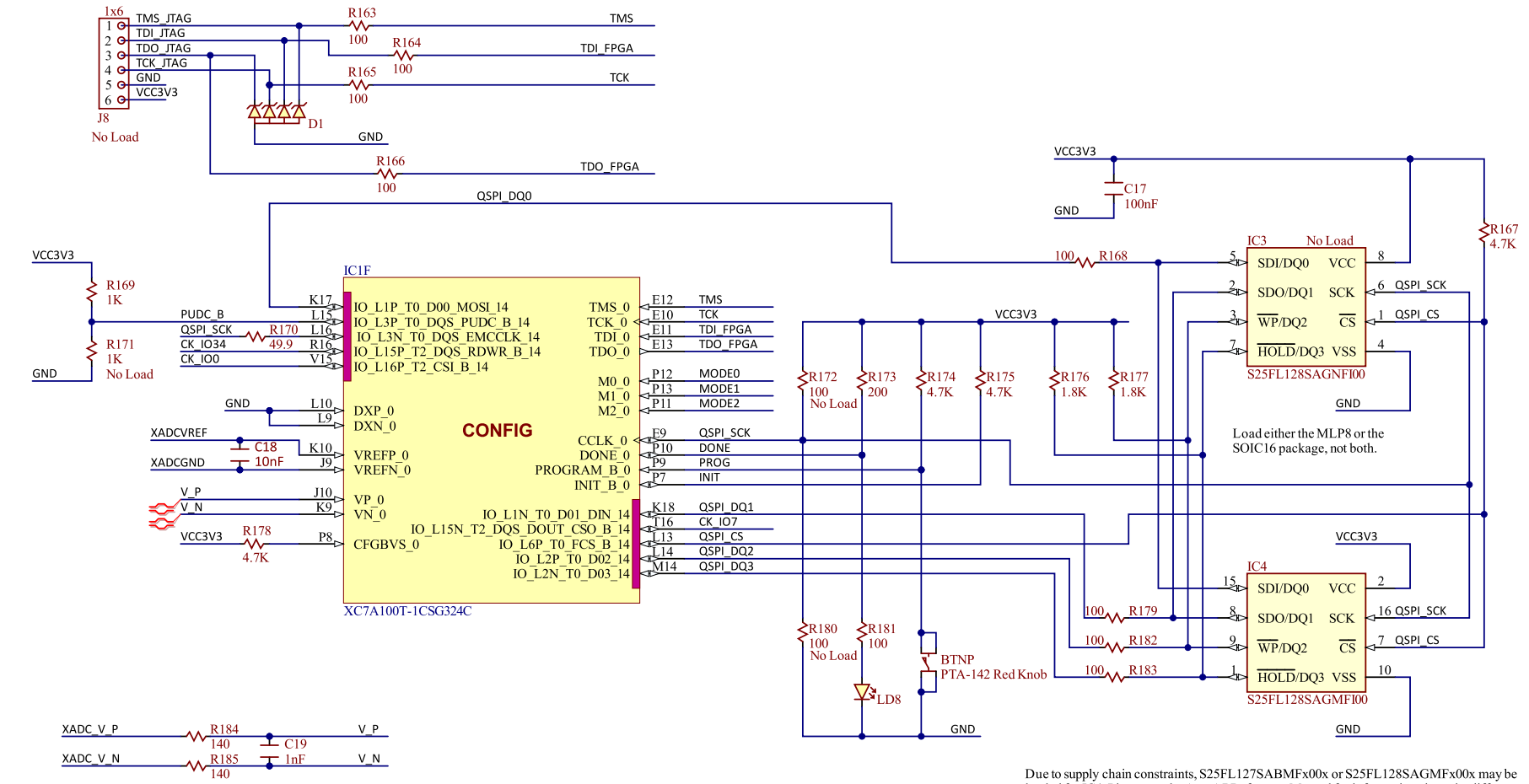
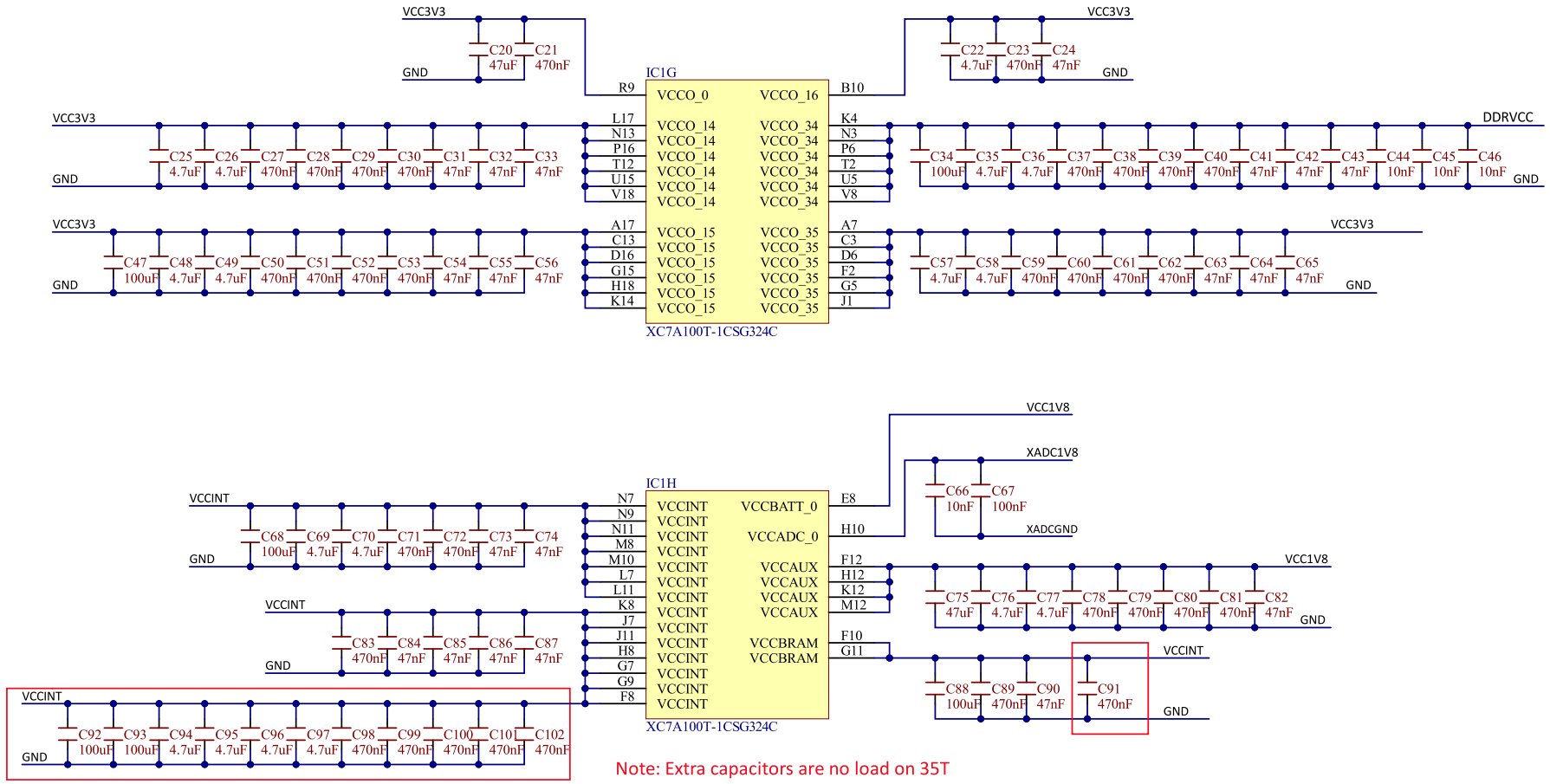
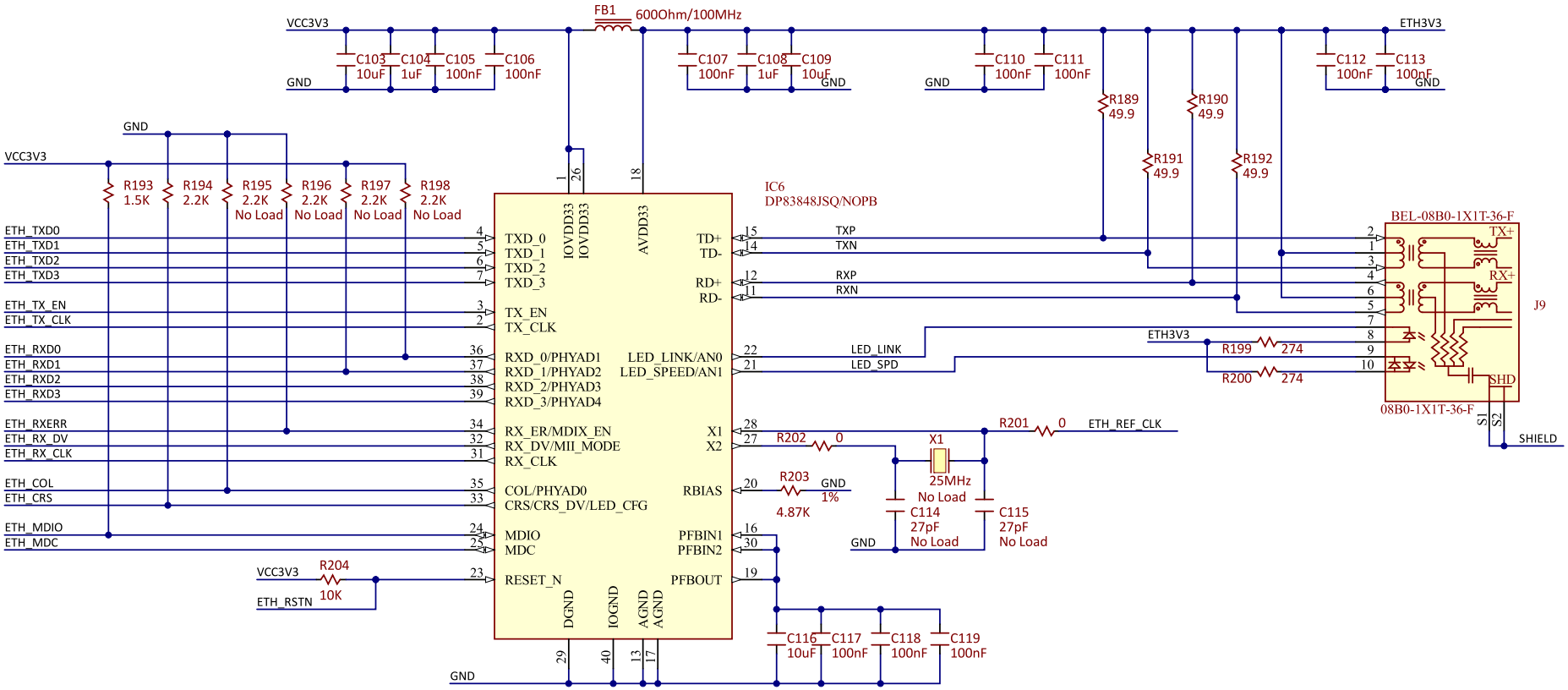


Due to supply chain constraints, S25FL127SABMFx00x or S25FL128SAGMFx00x may be loaded for IC4. Please see the Arty A7 Reference Manual for information about the differences between these Quad-SPI Flash Memories and how to identify which memory is installed on your board.

Title	Arty A7
Rev	E.2
Circuit	CONFIG, SPI FLASH
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	6 out of 12



Title	Arty A7
Rev	E.2
Circuit	FPGA Power
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	7 out of 12



NOTE: REF_CLK In Mode (ETH_REF_CLK = 25MHz)

NOTE: PHY MDIO Address = 00001

Title	Arty A7
Rev	E.2
Circuit	ETHERNET
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
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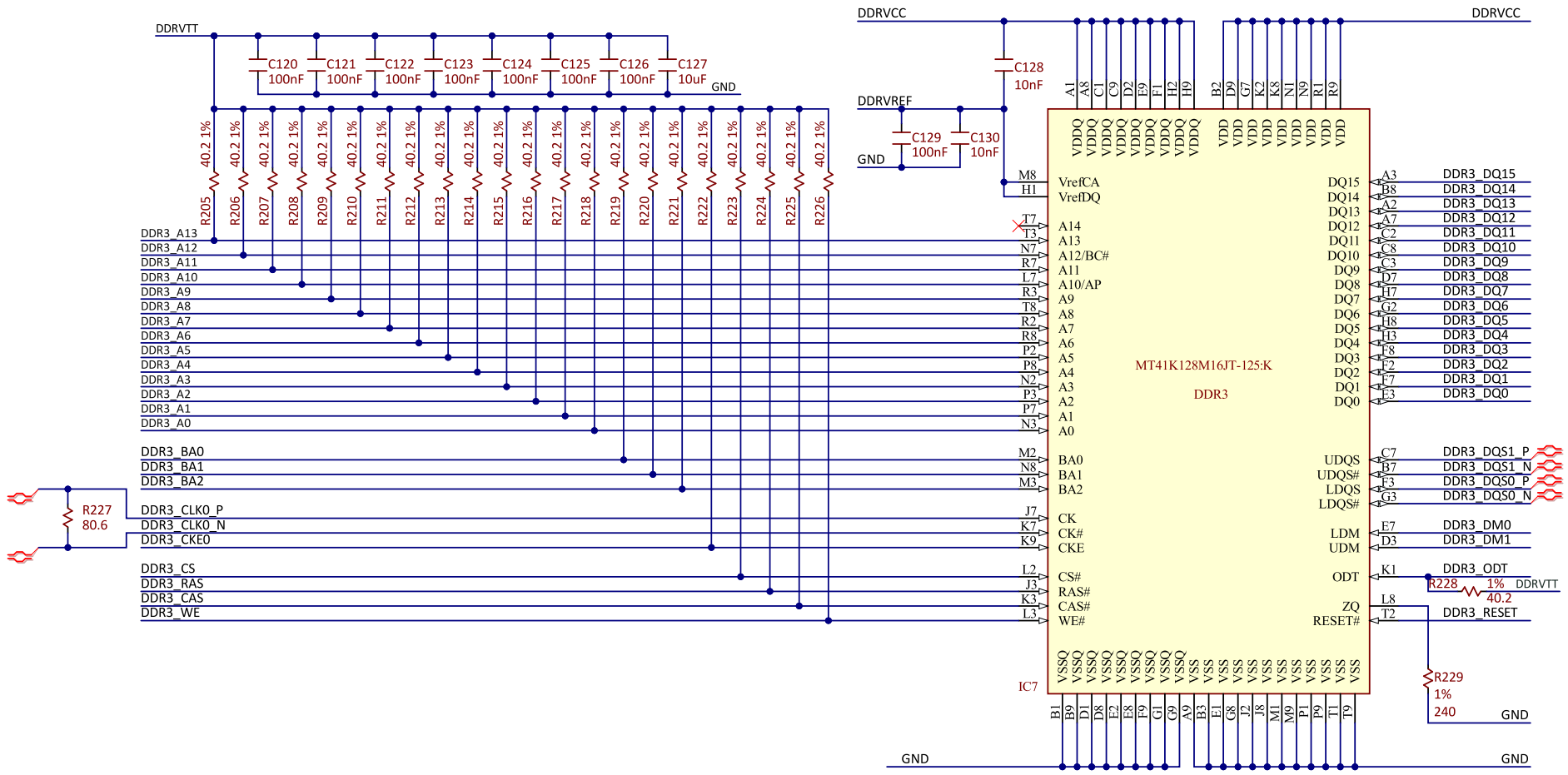

Title	Arty A7
Rev	E.2
Circuit	DDR3
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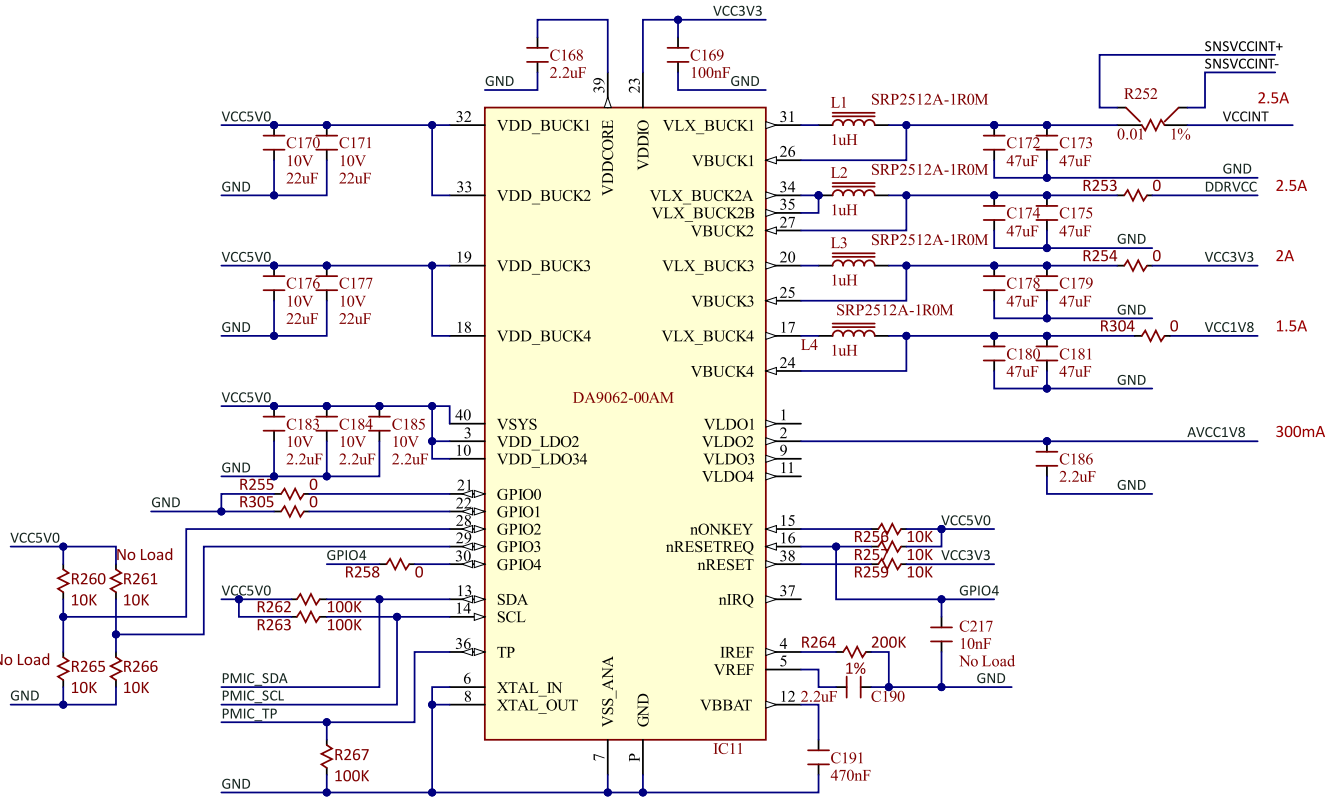
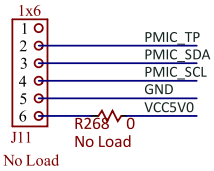


VCCINT Voltage Configuration

R260	R265	VCCINT
Load	No Load	1.0V
No Load	Load	0.95V

DDR Voltage Configuration

R261	R266	DDRVCC	DDRVTT
Load	No Load	1.5V	0.75V
No Load	Load	1.35V	0.675V



Title	Arty A7
Rev	E.2
Circuit	Power Regulation
Doc#	500-319
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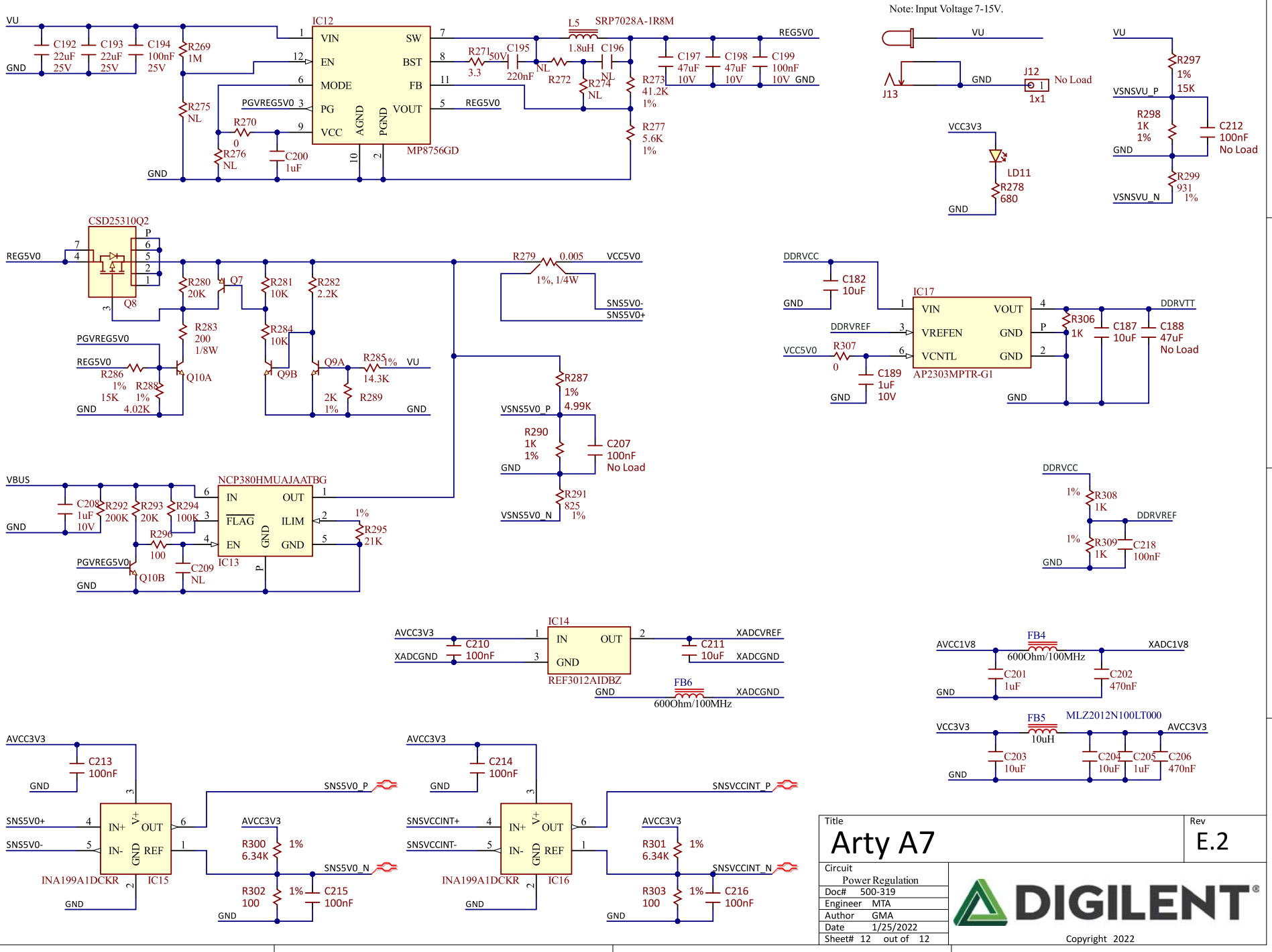
Note: Input Voltage 7-15V.
IC12
MP8756GD
L5 SRP7028A-1R8M
REG5V0
VU
GND
PGVREG5V0
VCC3V3
LD11
R278 680
J12 No Load
J13
VSNSVU_P
VSNSVU_N
C212 100nF No Load
CSD25310Q2
Q7
Q8
Q9A
Q9B
Q10A
R279 0.005 1%, 1/4W
VCC5V0
SNS5V0-
SNS5V0+
VSNS5V0_P
VSNS5V0_N
C207 100nF No Load
DDRVCC
IC17
AP2303MPTR-G1
DDRVTT
DDRVREF
C182 10uF
C187 10uF
C188 47uF No Load
VBUS
NCP380HMUAJAATBG
IC13
Q10B
C218 100nF
IC14
REF3012AIDBZ
AVCC3V3
XADCVREF
XADCGND
FB6 600Ohm/100MHz
AVCC1V8
XADC1V8
FB4 600Ohm/100MHz
FB5 MLZ2012N100LT000 10uH
IC15
IC16
INA199A1DCKR
SNS5V0_P
SNS5V0_N
SNSVCCINT_P
SNSVCCINT_N
Title
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Circuit
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Author GMA
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