



# FPGA Example\_2\_PWM

2022. 07. 06.

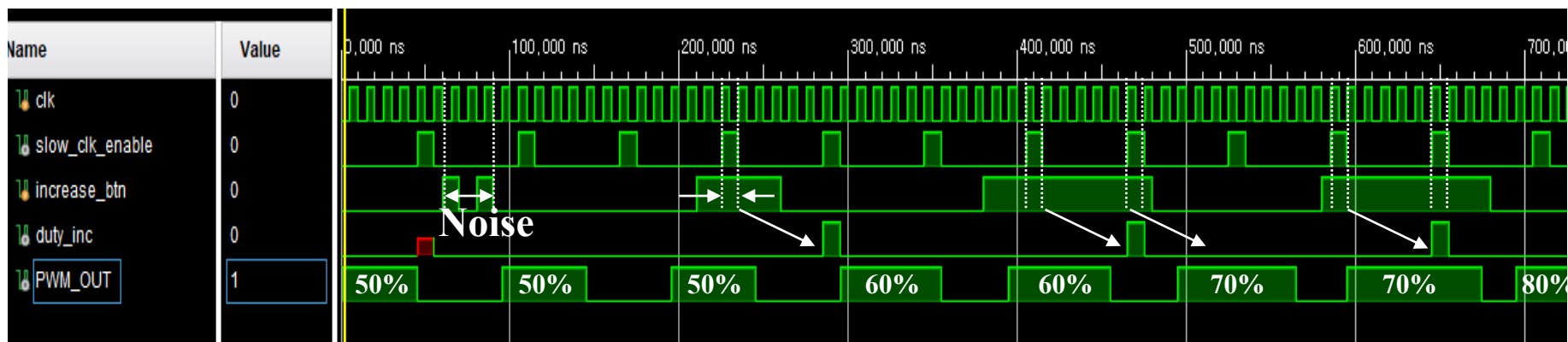
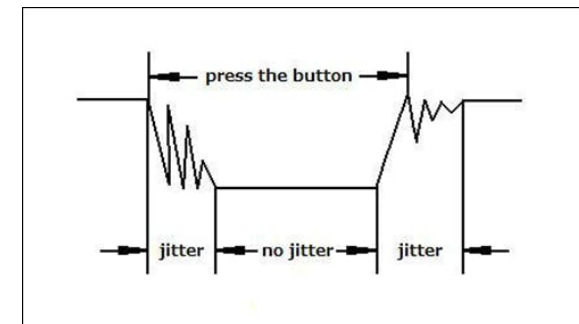
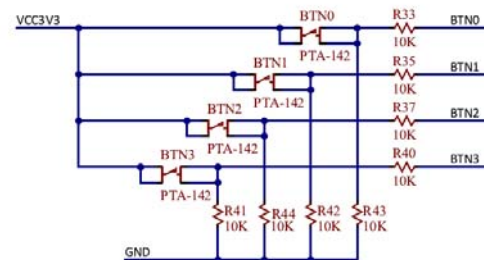
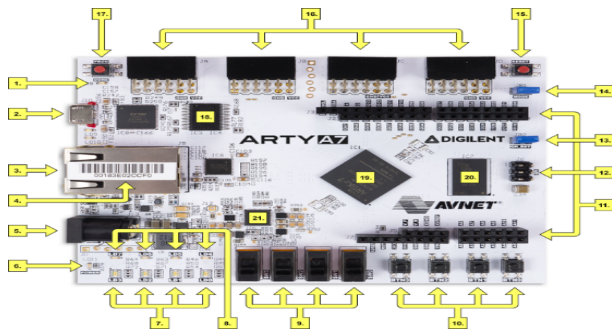
삼성전자

정 석 용

# Example\_2\_PWM

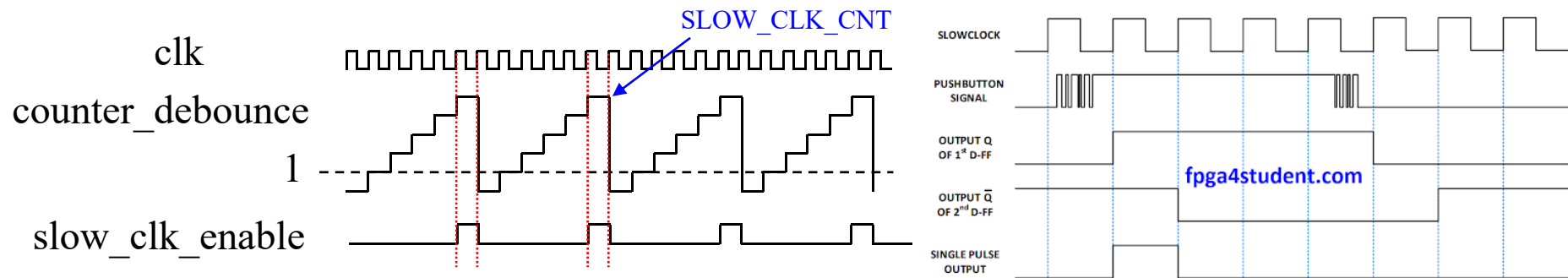
## ❑ Button Debouncing 모듈

- 스위치 신호를 그대로 사용하는 대신, `slow_clk_enable` 신호에 동기화 시켜 안정화 시킴
- 1) 노이즈 제거, 2) 버튼 클릭 → 단발성 동작(Delayed Edge detecting)

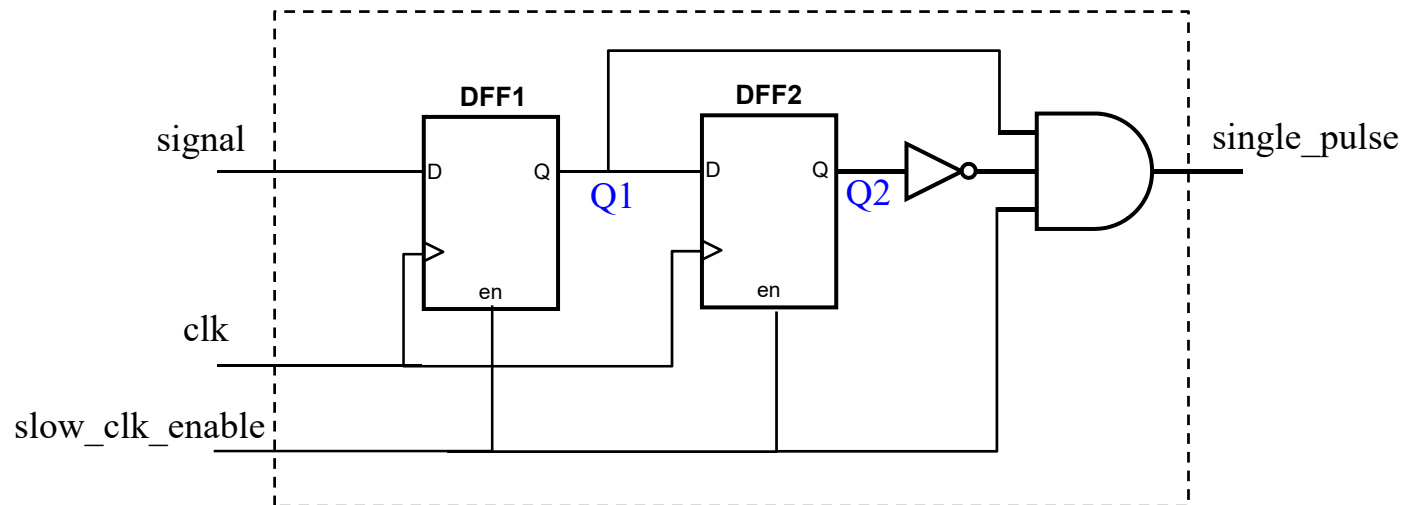


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## ❑ Button Debouncing 모듈



### Button Debouncing

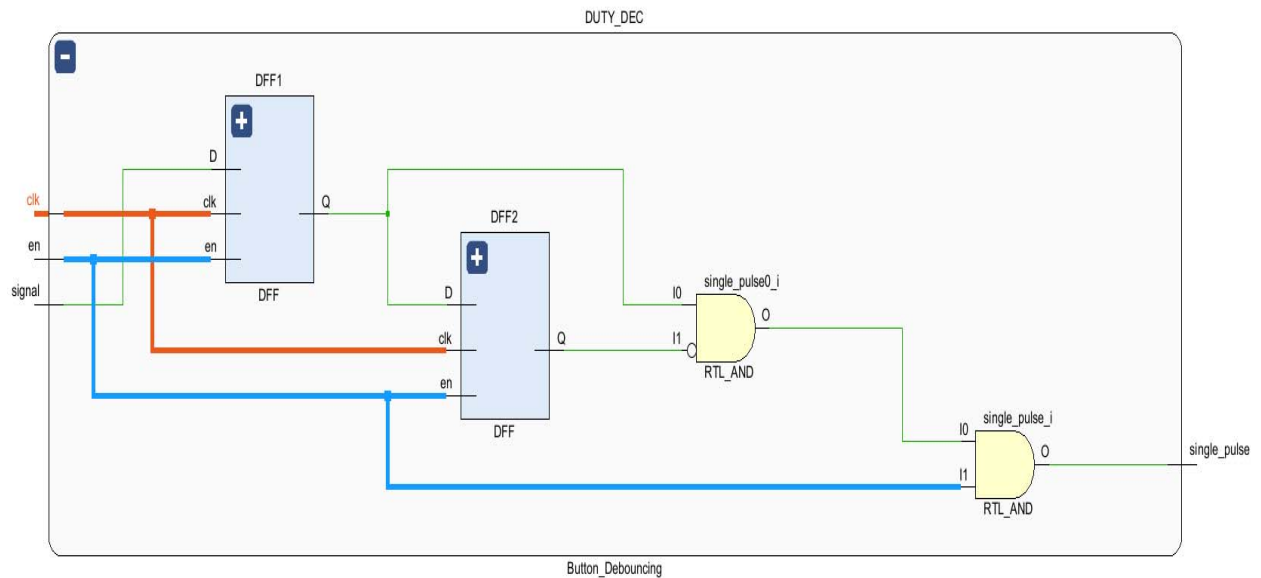


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## ❑ Button Debouncing 모듈

### ➤ Source Code 검증 RTL Simulation

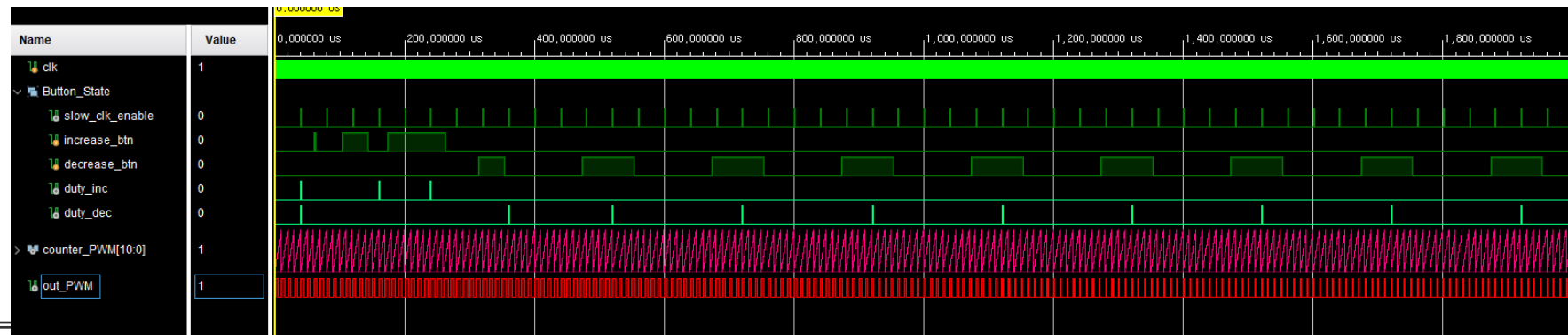
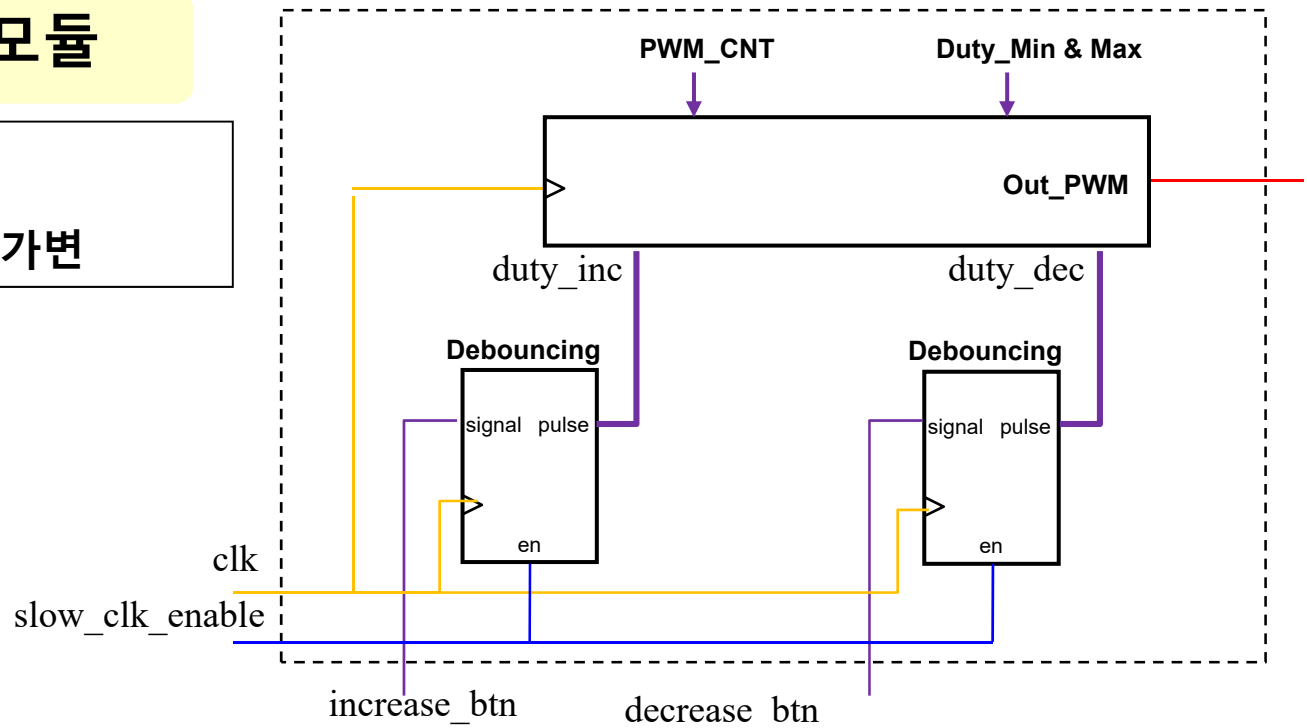
```
54 |  
55 | // D-FlipFlop  
56 | module DFF(  
57 |     input clk,  
58 |     input en,  
59 |     input D,  
60 |     output reg Q  
61 | );  
62 |  
63 | always @(posedge clk) begin  
64 |     if(en==1) // slow clock enable signal  
65 |         Q <= D;  
66 | end  
67 | endmodule  
68 |  
69 |  
70 | // Debouncing module for push buttons on FPGA  
71 | module Button_Debouncing(  
72 |     input clk,  
73 |     input en,  
74 |     input signal,  
75 |     output single_pulse  
76 | );  
77 |  
78 | wire Q1, Q2;  
79 |  
80 | DFF DFF1(clk, en, signal, Q1);  
81 | DFF DFF2(clk, en, Q1, Q2);  
82 | assign single_pulse = Q1 & (~ Q2) & en;  
83 | endmodule  
84 |
```



# Example\_2\_PWM

## ❑ PWM\_Generator 모듈

- 전체 코드 Simulation
- 버튼 입력에 따라 Duty 가변



# Example\_2\_PWM 수정

## ❑ PWM\_Generator 최종 결과

### ➤ Source코드를 3개로 분할

- Button\_Debouncing
- define
- PWM\_Generator

### ➤ Counter / Button / PWM State별 Simulation

