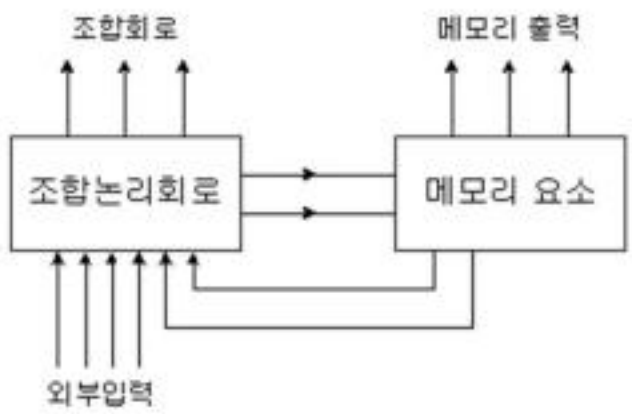
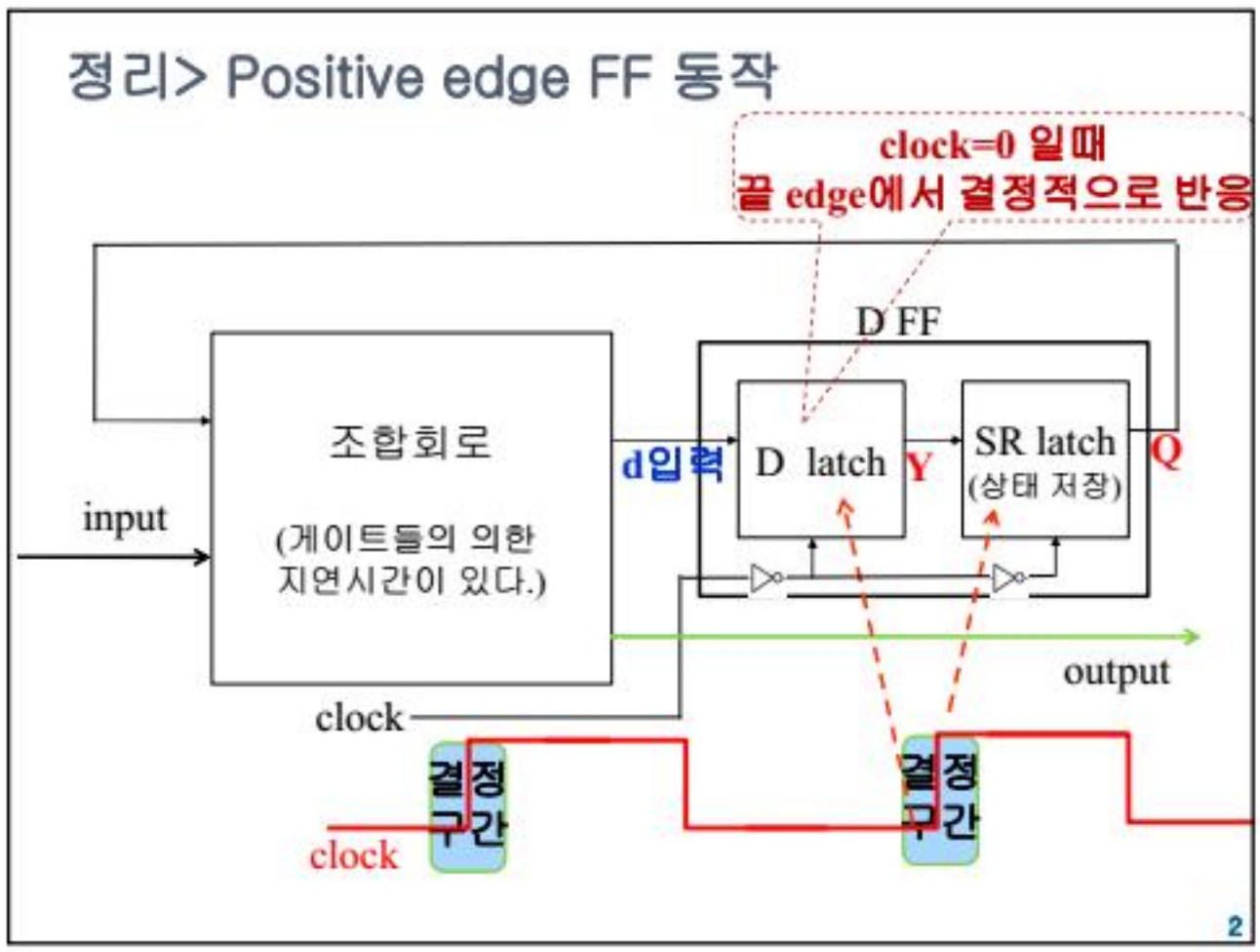
Sequential Circuits Analysis p.198



1

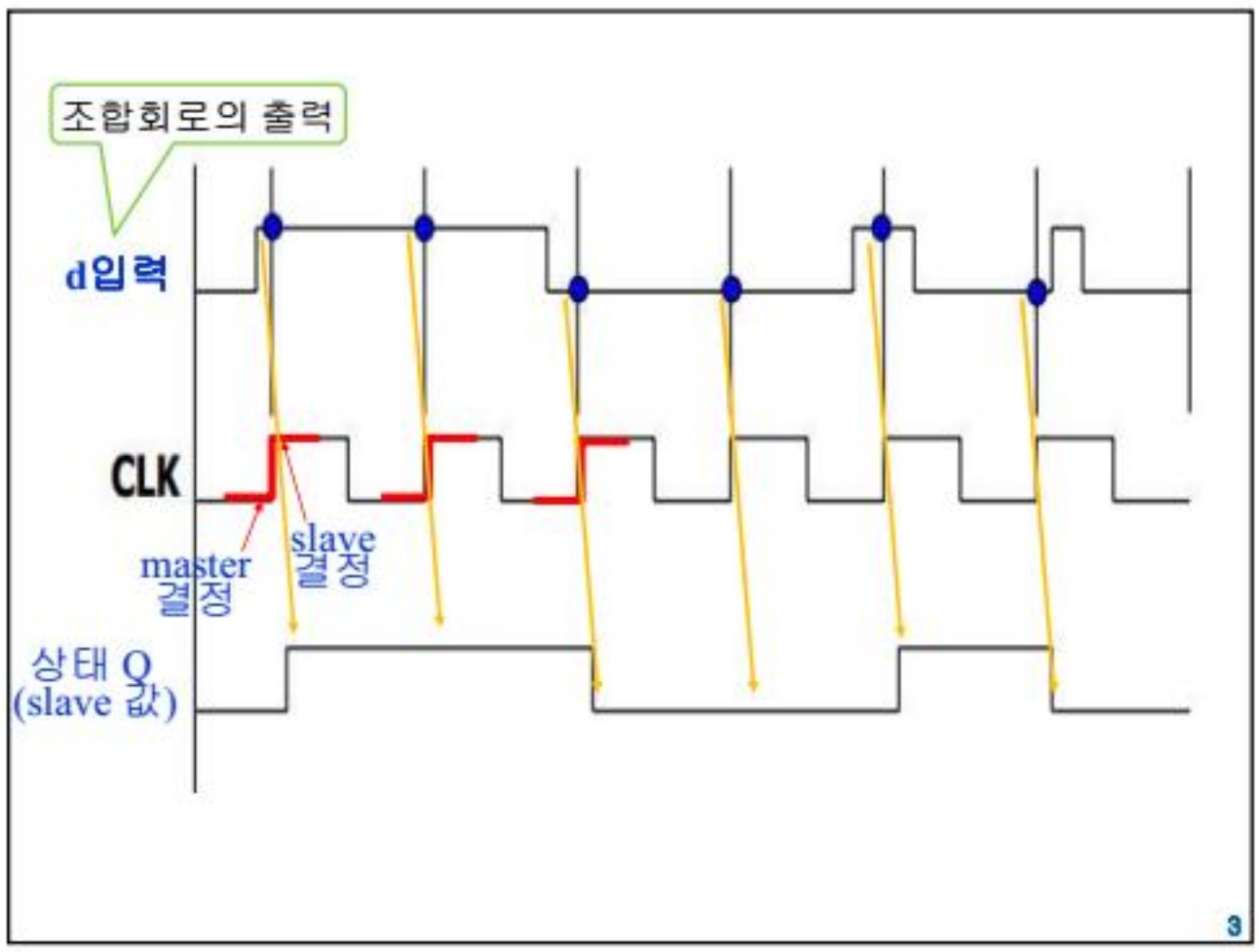
1

정리> Positive edge FF 동작

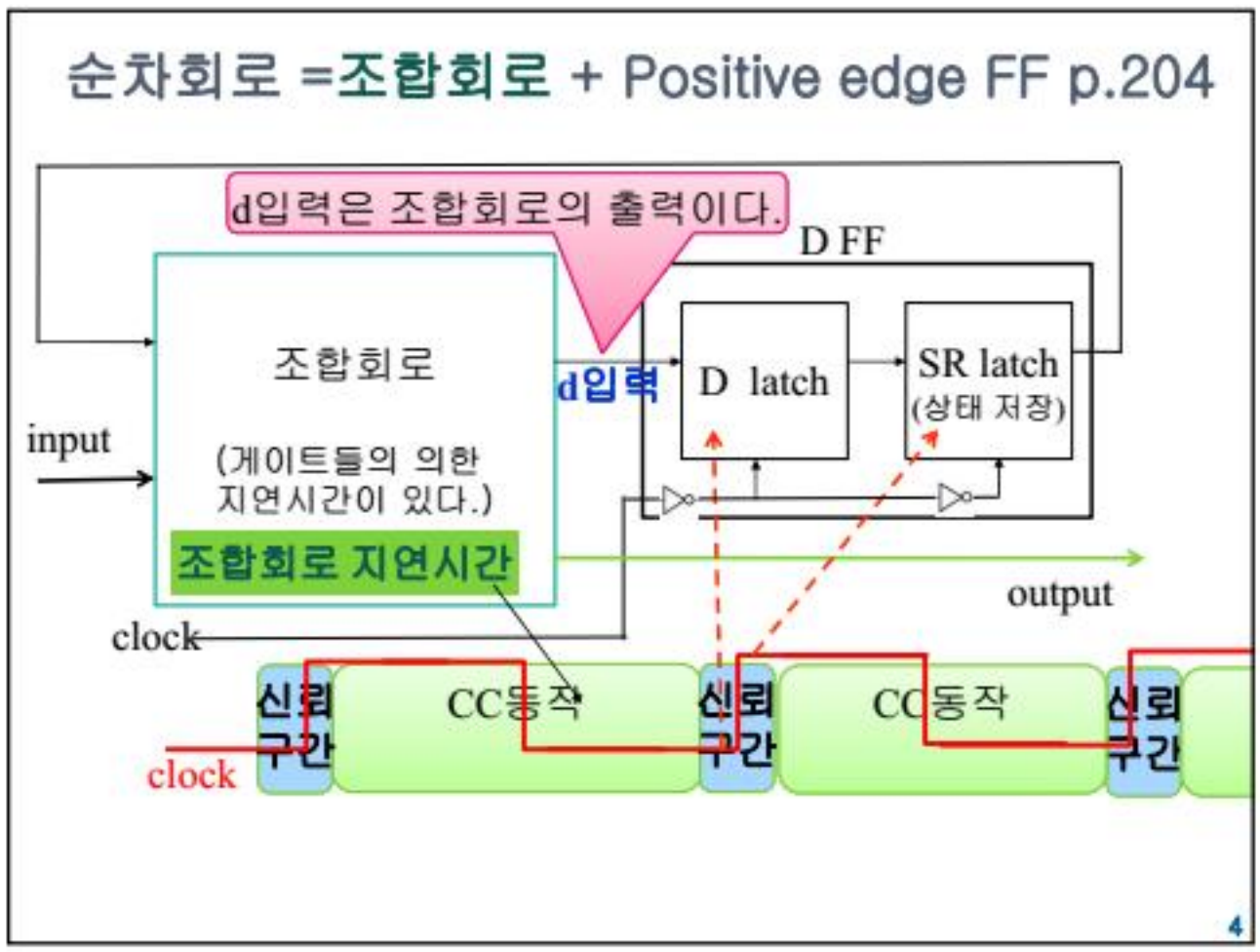


2

1

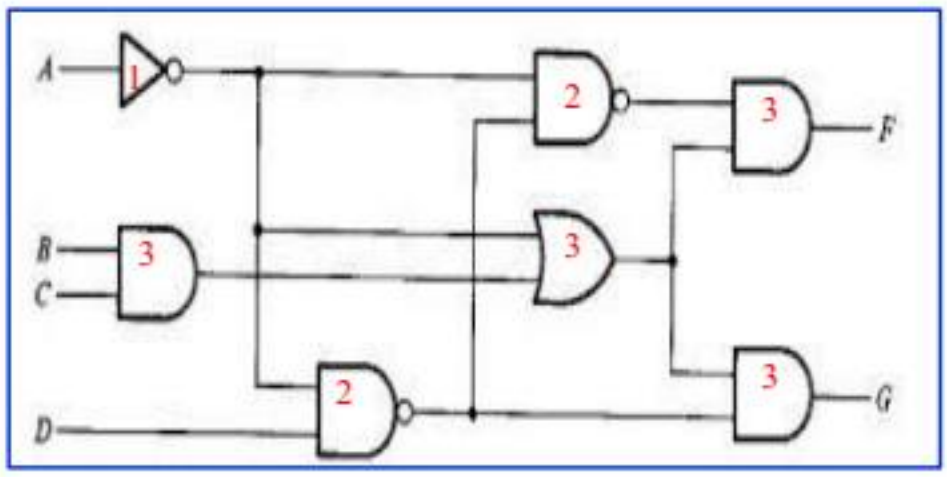

조합회로의 출력
d입력
CLK
master
결정
slave
결정
상태 Q
(slave 값)
3

3


순차회로 =조합회로 + Positive edge FF p.204
d입력은 조합회로의 출력이다.
D FF
조합회로
(게이트들의 의한
지연시간이 있다.)
조합회로 지연시간
input
d입력
D latch
SR latch
(상태 저장)
output
clock
clock
CC동작
CC동작
4

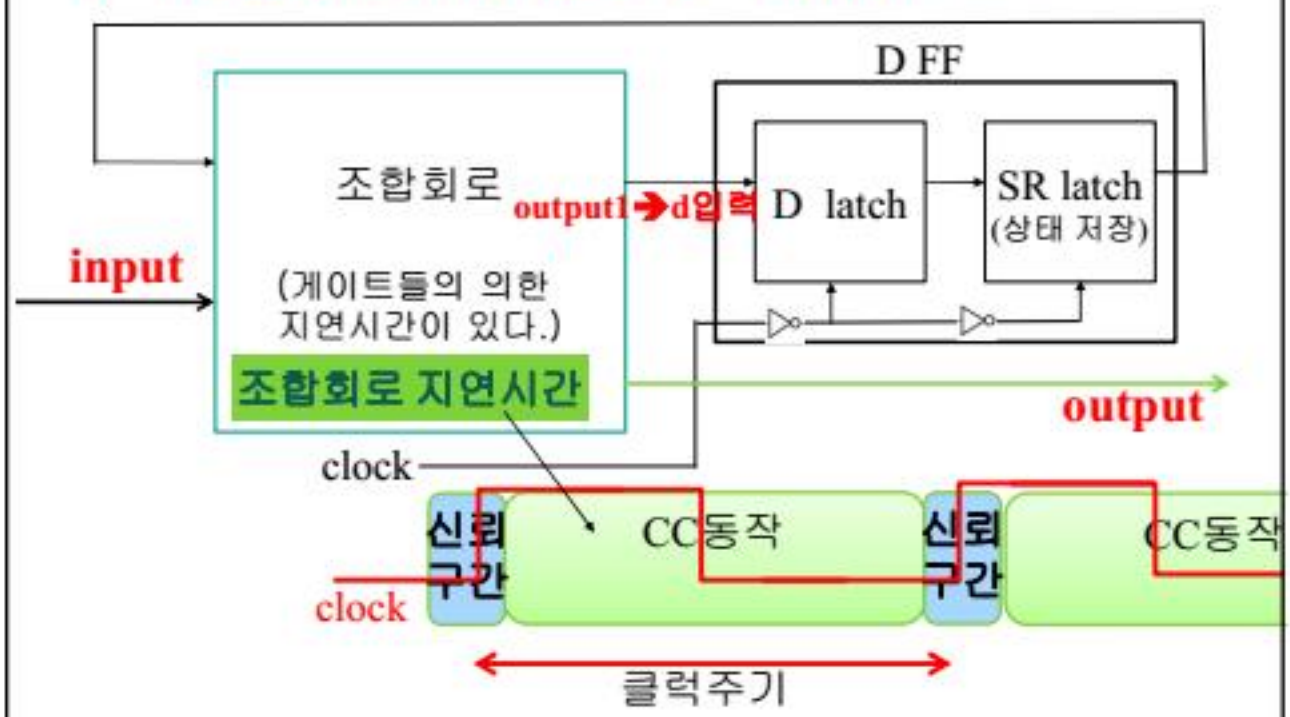
4

가정) 게이트 지연 시간
not:1, nand,nor:2
and,or:3 xor:4



5

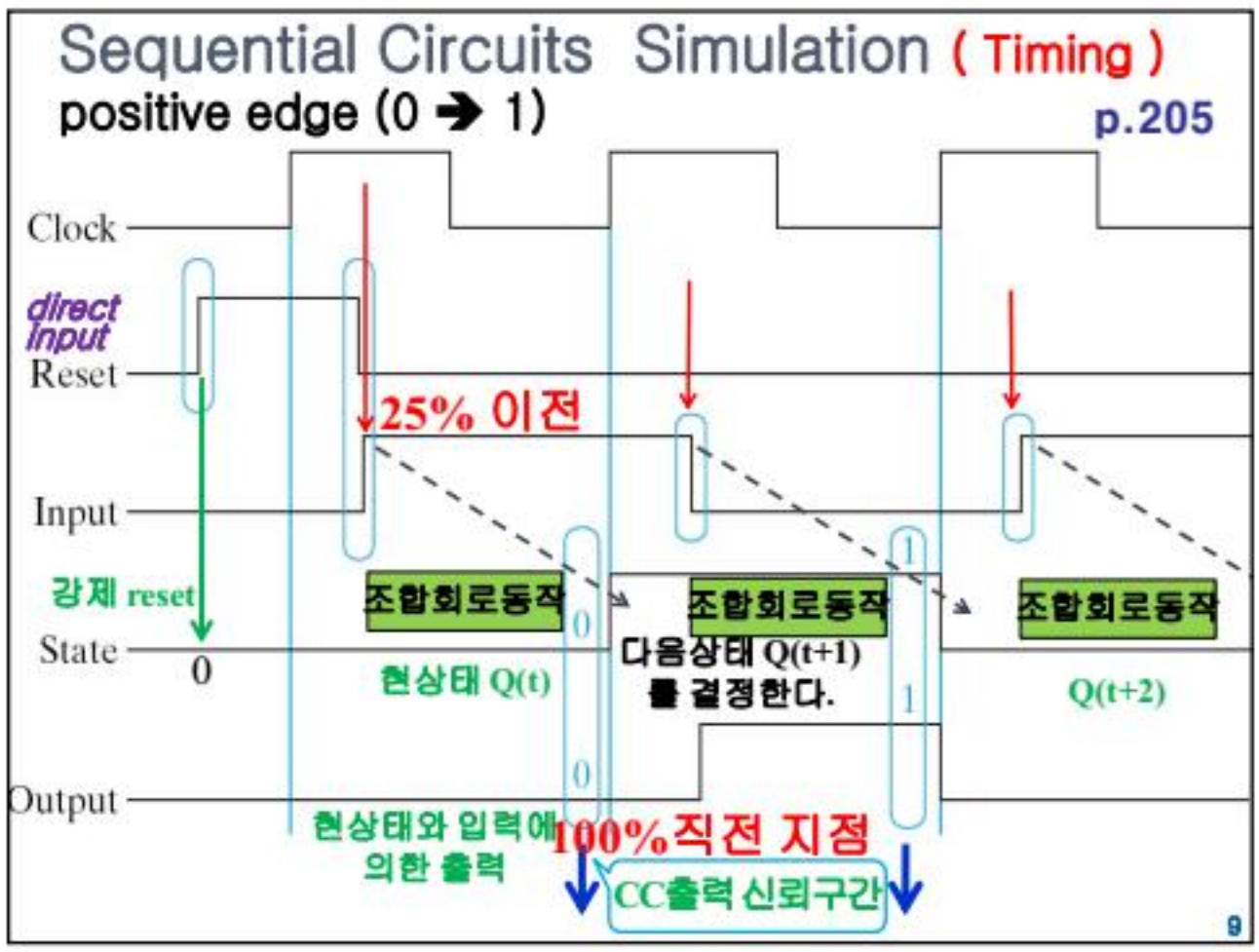
입력 시점, 출력 시점을 생각하자. p.204



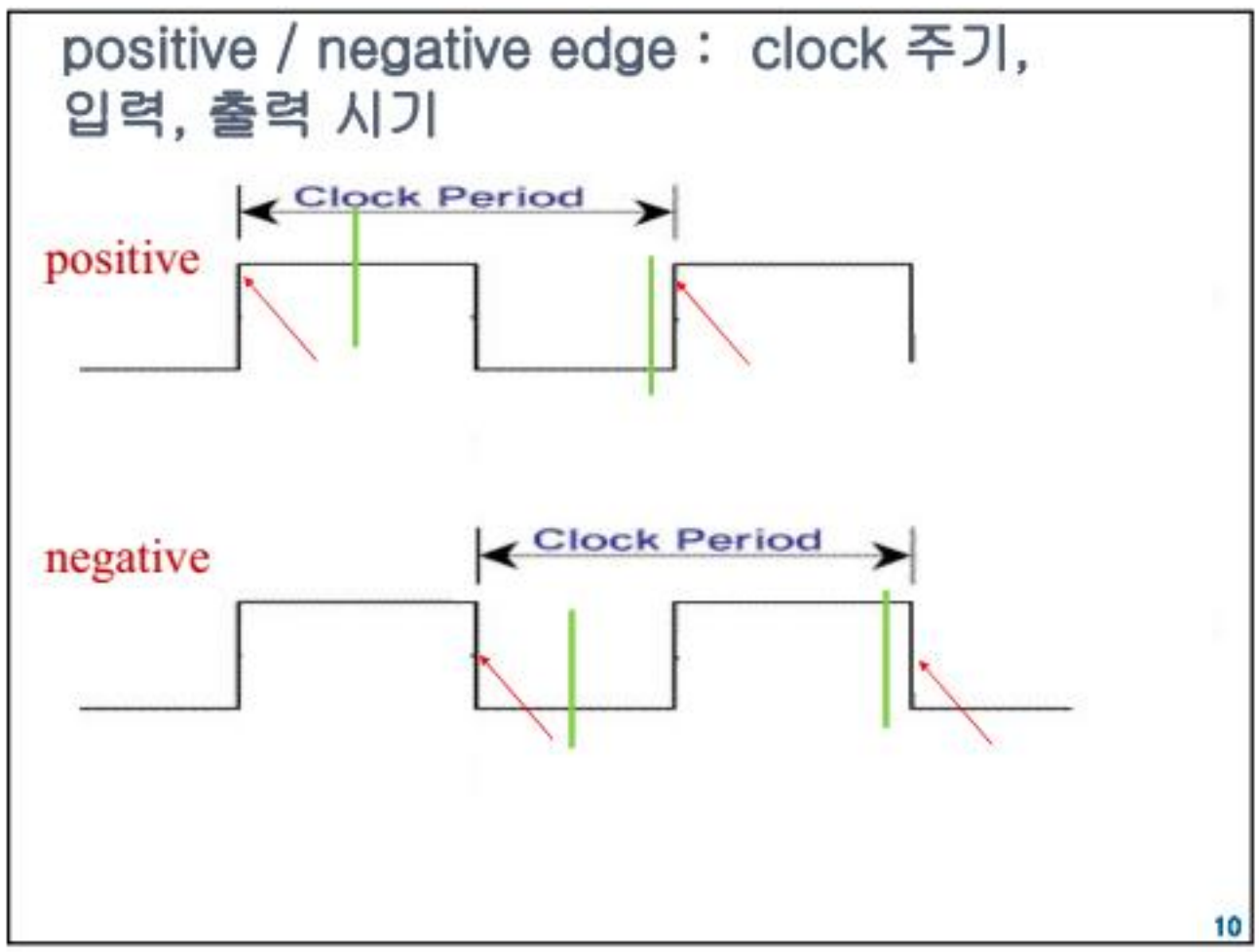
클럭주기 ≥ CC동작시간+M latch 지연시간+S latch 지연시간
+ 여유시간

7

7


Sequential Circuits Simulation (Timing)
positive edge (0 ➔ 1)
p.205
Clock
direct input
Reset
Input
State
Output
25% 이전
강제 reset
0
조합회로동작
현상태 Q(t)
조합회로동작
다음상태 Q(t+1)
를 결정한다.
조합회로동작
Q(t+2)
0
1
0
1
현상태와 입력에
의한 출력
100%직전 지점
CC출력 신뢰구간
9

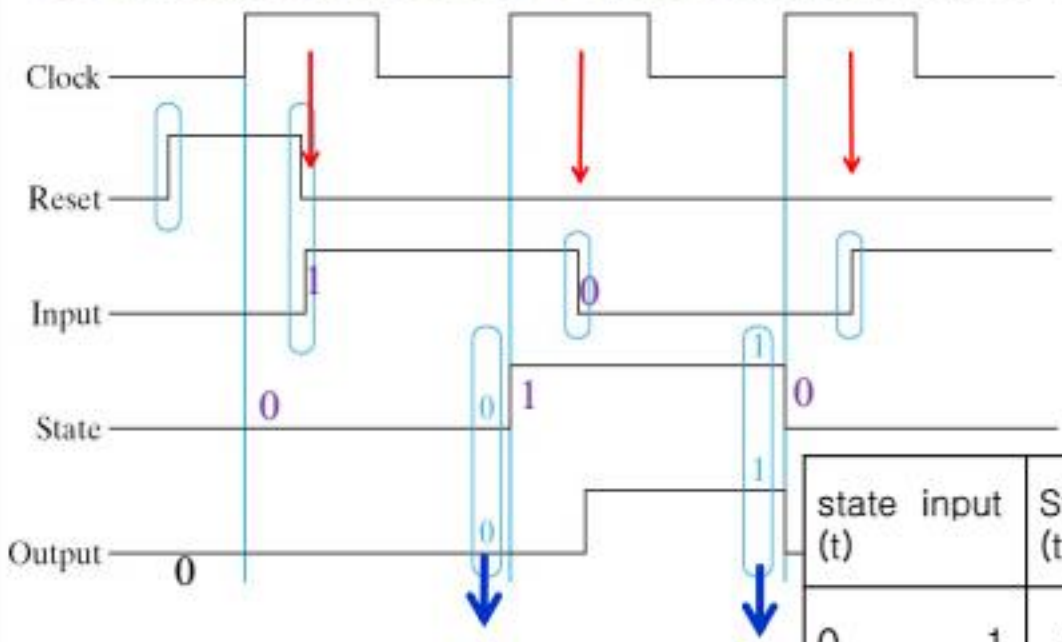
9


positive / negative edge : clock 주기,
입력, 출력 시기
Clock Period
positive
Clock Period
negative
10

10

Sequential Circuits Simulation positive edge

p.205



state input (t)	State output (t+1)
0 1	? ?
1 0	? ?

CC동작 CC동작

11

11

앞장의 시뮬레이션을 보고 …

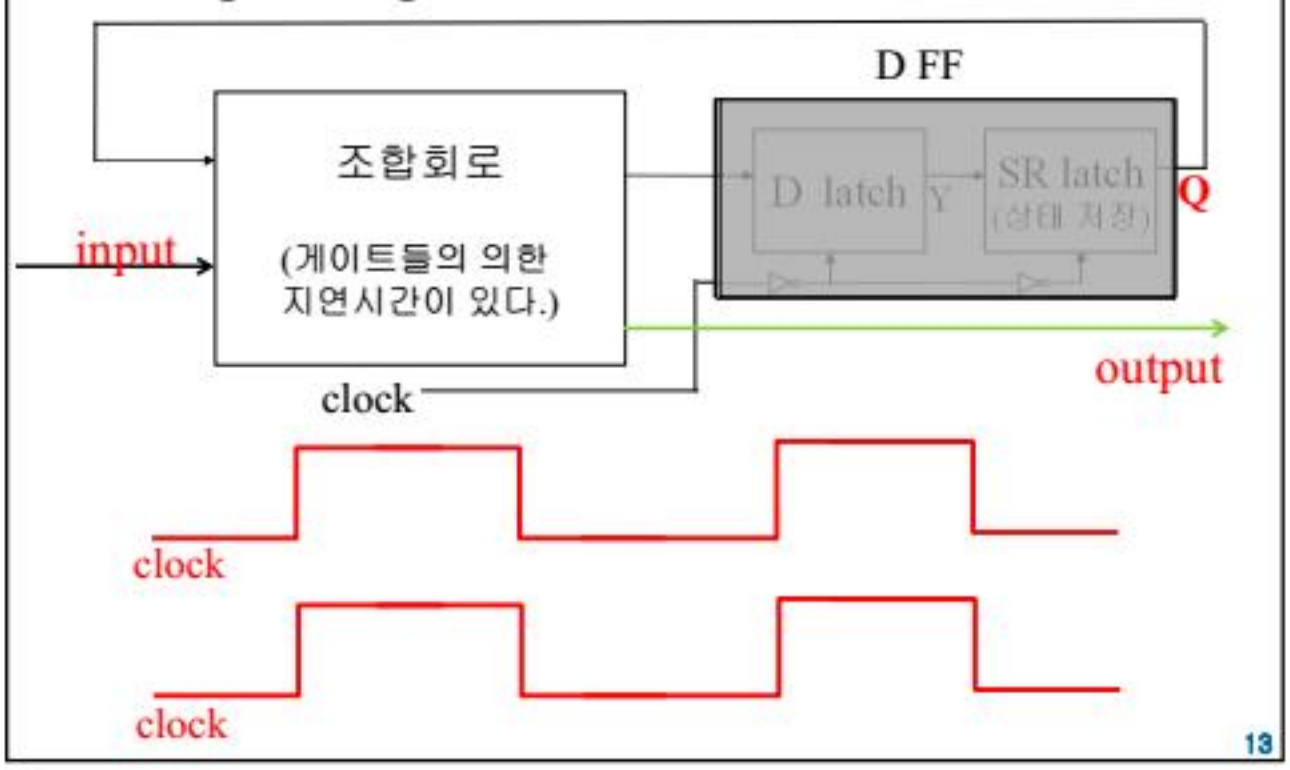
- **상태표**

State(t) input	State(t+1) output
0 0	알 수 없다
0 1	1 0
1 0	0 1
1 1	알 수 없다

12

12

정리> edge FF을 가진 순차회로에서 입력,출력,상태결정 시기는?
가정1: positive edge FF일 경우
가정2: negative edge FF일 경우



13