MIPI M-PHY, D-PHY and C-PHY Receiver Testing – Today and Tomorrow

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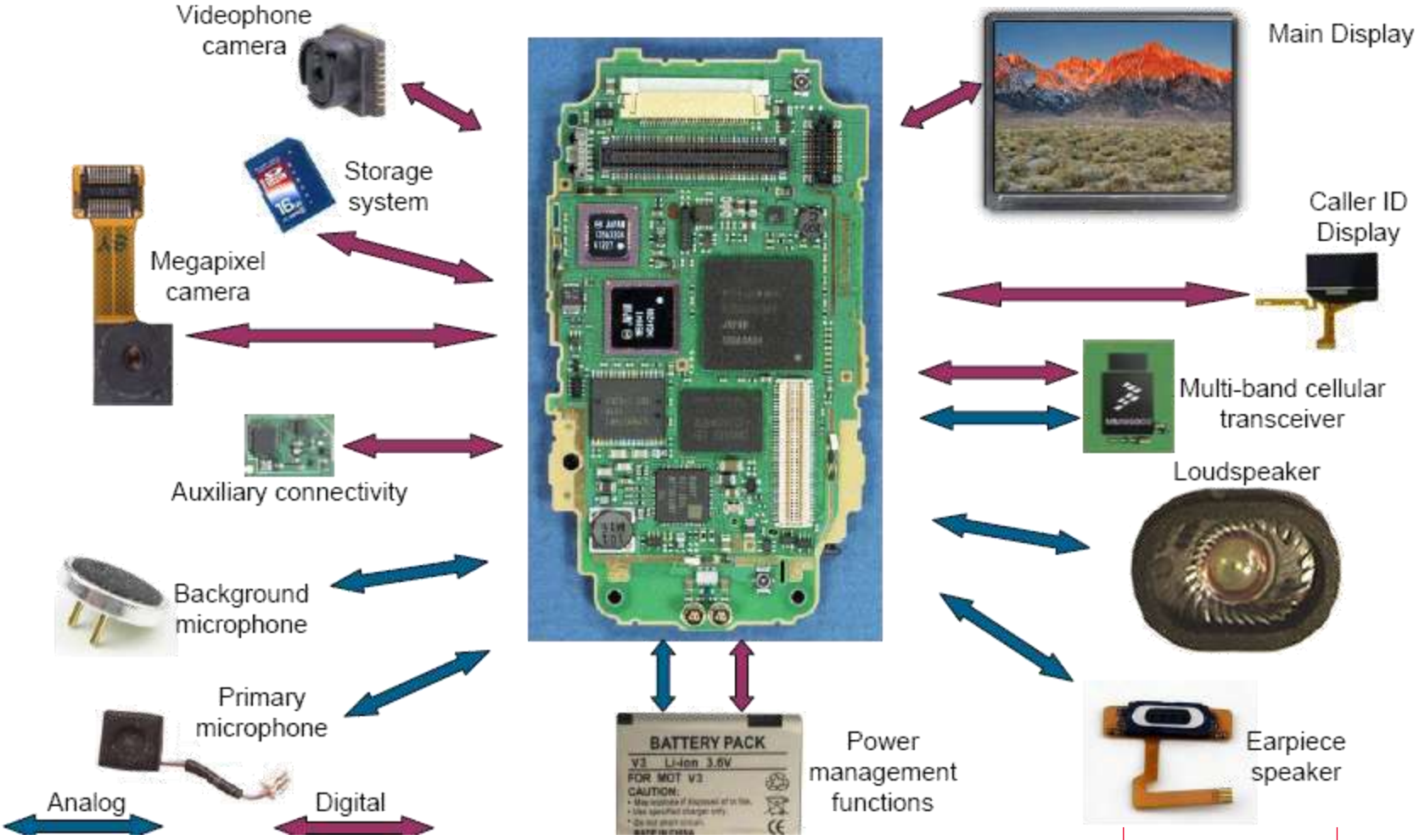
KEYSIGHT TECHNOLOGIES

Agenda

- MIPI Overview, history and recent changes
- RX test: recap of methodology
- M-PHY key features, changes in spec & methodology
- D-PHY recap of basics, signaling, LP- and HS- modes
- C-PHY intro on 3-wire 3-level signaling
- Keysight test solutions M8000 based
- Summary, links, QA

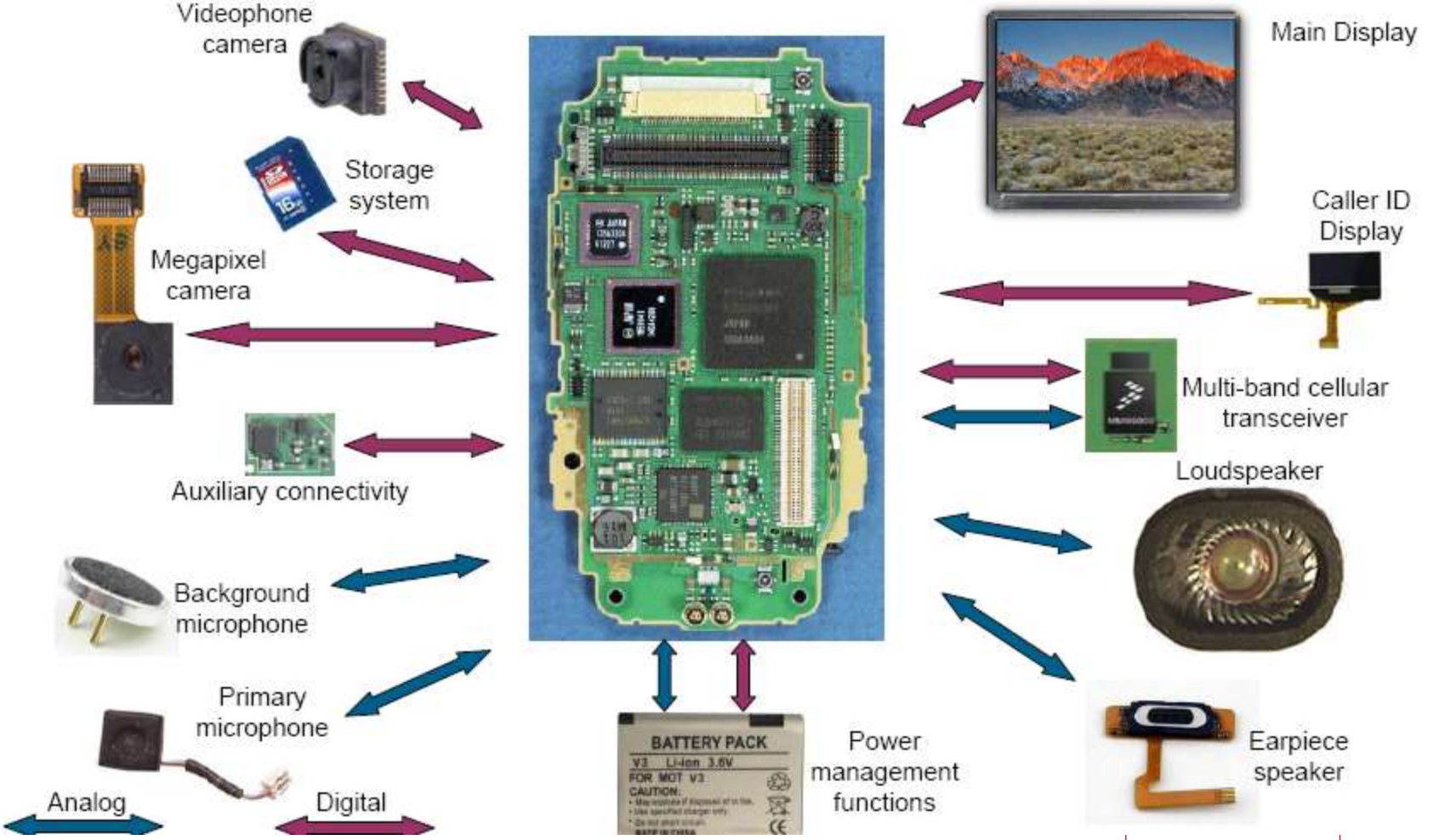
Technology Challenges in Mobile Computing



KEYSIGHT TECHNOLOGIES

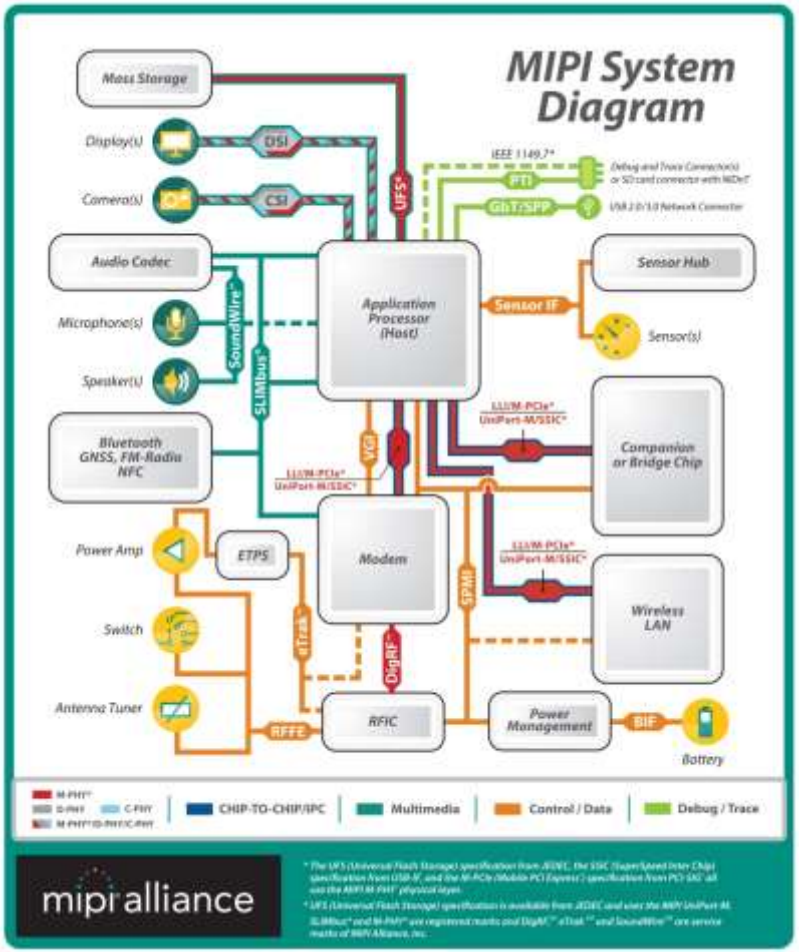
Technology Challenges in Mobile Computing

Too Many Interfaces, All Different



KEYSIGHT TECHNOLOGIES

MIPI = Mobile Industry Processor Interface -
Goals



- Structure the intestines of mobile devices ranging from smartphones to wireless-enabled tablets and netbooks
- Benefit the entire mobile industry by establishing standards for hardware and software interfaces
- Enabling reuse and compatibility making system integration less burdensome
- The distinctive requirements of mobile terminals drive the development of MIPI Specifications
  - Power saving / battery life
  - Bandwidth on demand

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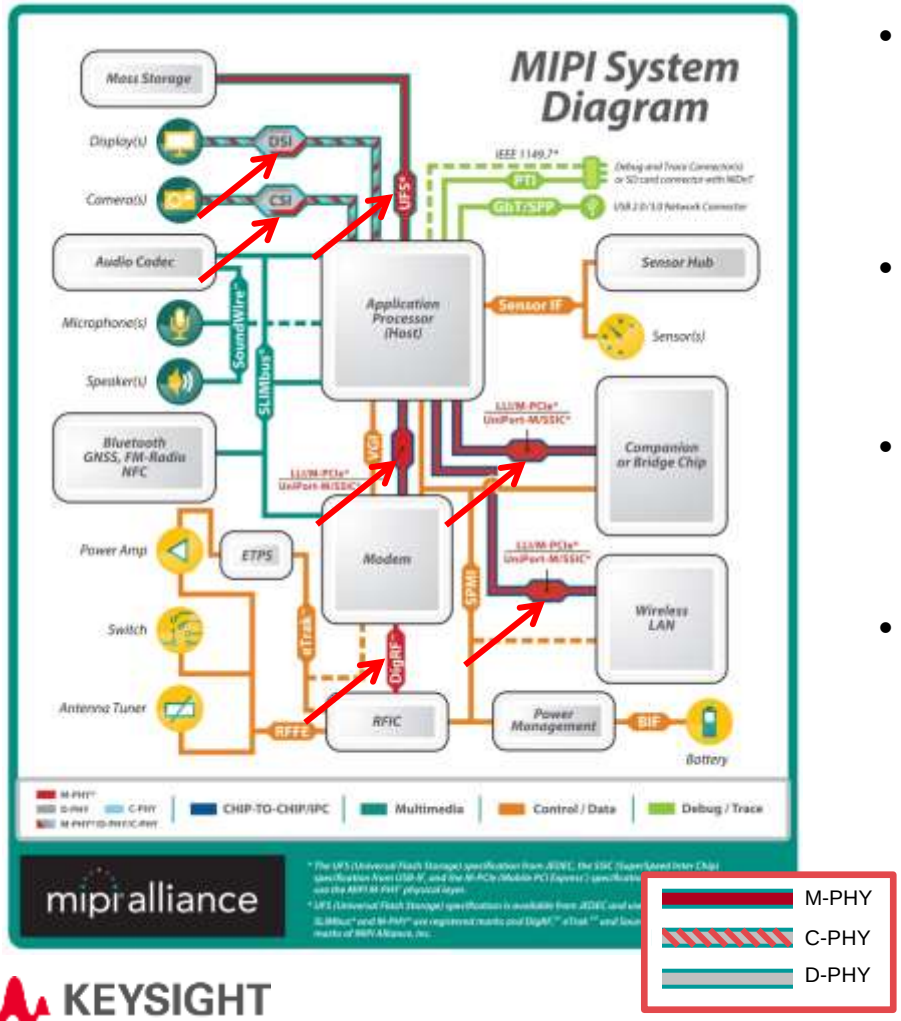

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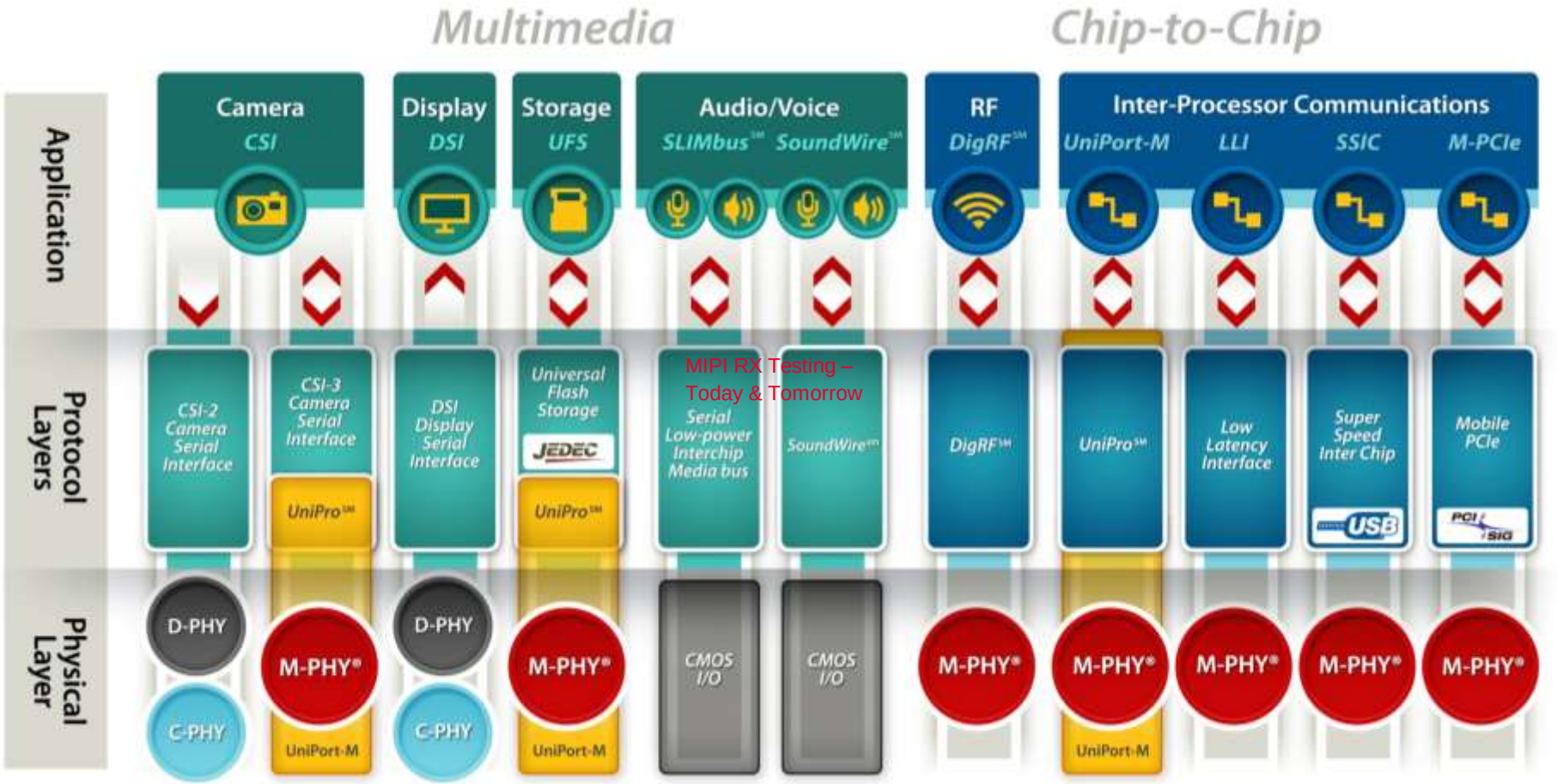
MIPI's Layered Approach for Application Standards



Why Three Different PHY-layer Standards?
2013 and before

- D-PHY
  - Used for camera (CSI-2) and display (DSI) applications
  - Source synchronous, forwarded ½ rate clock
  - Electrical specifications (parasitic capacitances and return loss (RL)) allow usage of established, relatively inexpensive semiconductor process
  - Complex signaling, different amplitudes and data format for Low Power (LP) and High Speed (HS) mode and non-differential “pattern sequence” signaling transition from LP to HS-mode and vice versa
  - Rev. 1.0 / 1.1 with a continuous data rate range up to 1.0 / 1.5Gb/s respectively
- M-PHY
  - Proposed high BW successor of D-PHY addressing camera and display applications
  - Embedded clock and PLL-type CDR
  - Discrete data rates (Gears) up to approximately 12Gb/s; sufficient for quite a while
  - Differential signaling and same amplitude in both HS- and LP- mode

Agilent / Keysight Solutions for MIPI RX PHY-test

2013 and before

M-PHY

J-BERT N4903B

D-PHY

ParBERT 81250

2013 2014 2015

Why three different PHY-layer standards?
2014 onwards

- M-PHY
  - Reluctance of camera group to adapt M-PHY because of
    - Specified lower parasitic capacitance / better RL demands more expensive semiconductor process than for D-PHY
    - Discrete instead a “agile” data rates
    - 8B/10B coding overhead of 25%
- C-PHY started
  - New 3-wire / 3 level data format allowing transmission of >1 bit / symbol
  - Embedded clock, CR based on logic and encoding rules
  - HS mode w/ toggle rates reaching continuously up to 2.5Gbaud / 5.75Gb/s
  - LP mode identical to D-Phy
  - Even more complex signaling (HS mode3 w/ 3 wire 3-level signaling) level)
- D-PHY extended
  - Rev. 1.2 w/ max data rate 2.5Gbs (achieved through RX deskew)
  - Rev. 2.x started, data rate project beyond 4.5 Gb/s (6.5Gb/s)

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About Receiver (RX) testing

– RX testing

An RX test is used to determine an RX's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing…

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1. A Bit Error Ratio Tester's (BERT) Pattern Generator (BERT PG) is used to emulate a system's TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system.
   This signal has to be calibrated according to the specification.

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   This signal has to be calibrated according to the specification
2. The input of the RX under test is stimulated with this signal
3. Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER

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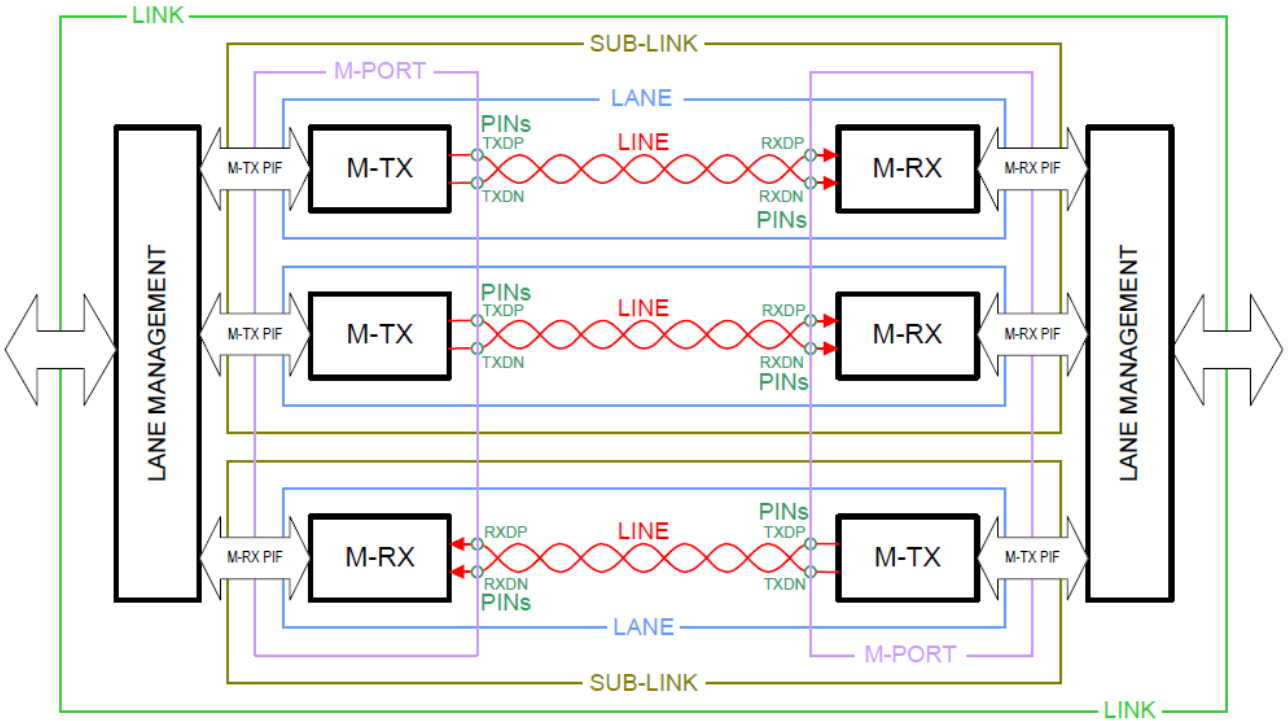
M-PHY Link Example



MIPI M-PHY

- Lanes are unidirectional
- Signaling: differential
- 8B/10B coded
- Transmisssion may appear in burst
- Embedded clock
- PLL type CDR, needs to synch at the beginning of every burst

MIPI M-PHY options

– High speed and (lower speed) low power mode (same as in D-PHY)
– High and low voltage swing operation can be commonly selected for both modes
– Terminated (100 Ohm) or not terminated operation (for power saving purposes) can individually be selected per mode

MIPI M-PHY Data Rates and Module Types

High Speed Modes

HS_Gear	data rate [Gb/s] A	data rate [Gb/s] B	termination default	termination optional
4	9984	11661	RT	
3	4992	5830	RT	NT
2	2496	2915	RT	NT
1	1248	1458	RT	NT

Low Power Modes

M-PHY-Type-I Module (PWM)

Type-I Baseline Module LP_Gear	data rate [Mb/s]	termination default	termination optional
0	0.01 - 3	NT	RT
1	3 - 9	NT	RT
2	6 - 18	NT	RT
3	12 - 36	NT	RT
4	24 - 72	NT	RT
5	48 - 144	NT	RT
6	96 - 288	NT	RT
7	192 - 576	NT	RT

M-PHY-Type-II Module (NRZ)

Type-II Baseline Module data rate = fsys[Mb/s]	termination default	termination optional
fsys = f ref	NT	RT

f_{ref} = 19.2, 26, 38.4 or 52 MHz

NT = Not Terminated
RT = Resistively terminated

- High Speed Gears / data rates valid for both module types
- Type II module only used for Dig_RF_v4

Jitter Cocktail for Receiver Tolerance Test

M-PHY Gear 1 & 2

Jitter Cocktail consists of

- ISI generated through Conformance Channel and Replica Trace
- Dual band RJ
- Dual-tone SJ

Step	Action	J-BERT parameter	Target Value	Pattern	TIE-HP-filter
1	Adjust wideband RJ (>f_{L_RX}) to achieve STRJ	RJ	0.10 UI_{pp} 7.9mUI_{rms}	clk/2 (1010)	1/30UI
2	Add low frequency RJ (<1/30UI) to achieve RJ=TJ-DJ	BUJ	0.17UI_{pp} 13.4mUI_{rms}	clk/2 (1010)	f_{L_RX} *
3	Turn all RJ off; calibrate SJ (f_SJ1, f_SJ2, f_SJ3, f_SJ4)	PJ2	0.15 $UI_{,pp}$	CJTPat	off
4	Keep all RJ off but keep PJ2 on; calibrate STSJ (240 MHz) to achieve STDJ=0.2UI (STSJ=STDJ-DDJ) or DJ=0.35UI	PJ1	0.35 $UI_{,pp}$	CJTPat	off
5	Turn all callibrated jitter on. Calibrate to prorated eye mask at BER 10^{-6}	PJ2, Amp	V_{DIF_AC}=43mV 1-TJ=0.52UI	CJTPat	off

*) $f_{L\_RX} = F_{C\text{-}RX}$ = 1/2MHz

Jitter Cocktail for Receiver Tolerance Test

M-PHY Gear 3 (and 4)

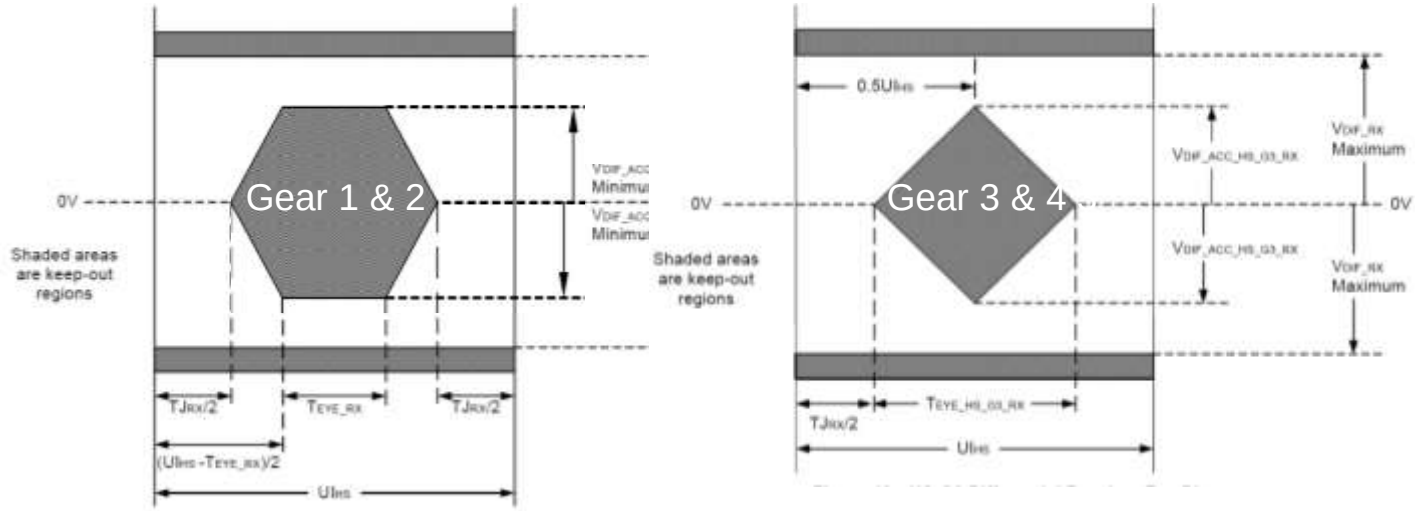
Jitter Cocktail consists of

- ISI generated through Conformance Channel and Replica Trace
- Single RJ (broad-band) ← Simplification
- Dual-tone SJ

Step	Action	J-BERT parameter	Target Value	Pattern	TIE-HP-filter
1	Add wideband RJ (> 10MHz) to achieve RJ=TJ-DJ	RJ	$0.17UI_{pp}$ $13.4mUI_{rms}$	clk/2 (1010)	f_{L_RX} *
2	Turn all RJ off; calibrate SJ (f_SJ1, f_SJ2, f_SJ3, f_SJ4)	PJ2	$0.15\ UI_{,pp}$	CJPat	off
3	Keep all RJ off but keep PJ2 on; calibrate STSJ (240 MHz) to achieve STDJ=0.2UI (STSJ=STDJ-DDJ) or DJ=0.35UI	PJ1	$0.35\ UI_{,pp}$	CJPat	off
4	Turn all callibrated jitter on. Calibrate to prorated eye mask at BER 10^{-6}	PJ2, Amp	V_{DIF_AC}=45mV 1-TJ=0.52UI	CJTPat	off

*) $f_{L\_RX} = F_{C\text{-}RX}$ = 1/2/4MHz

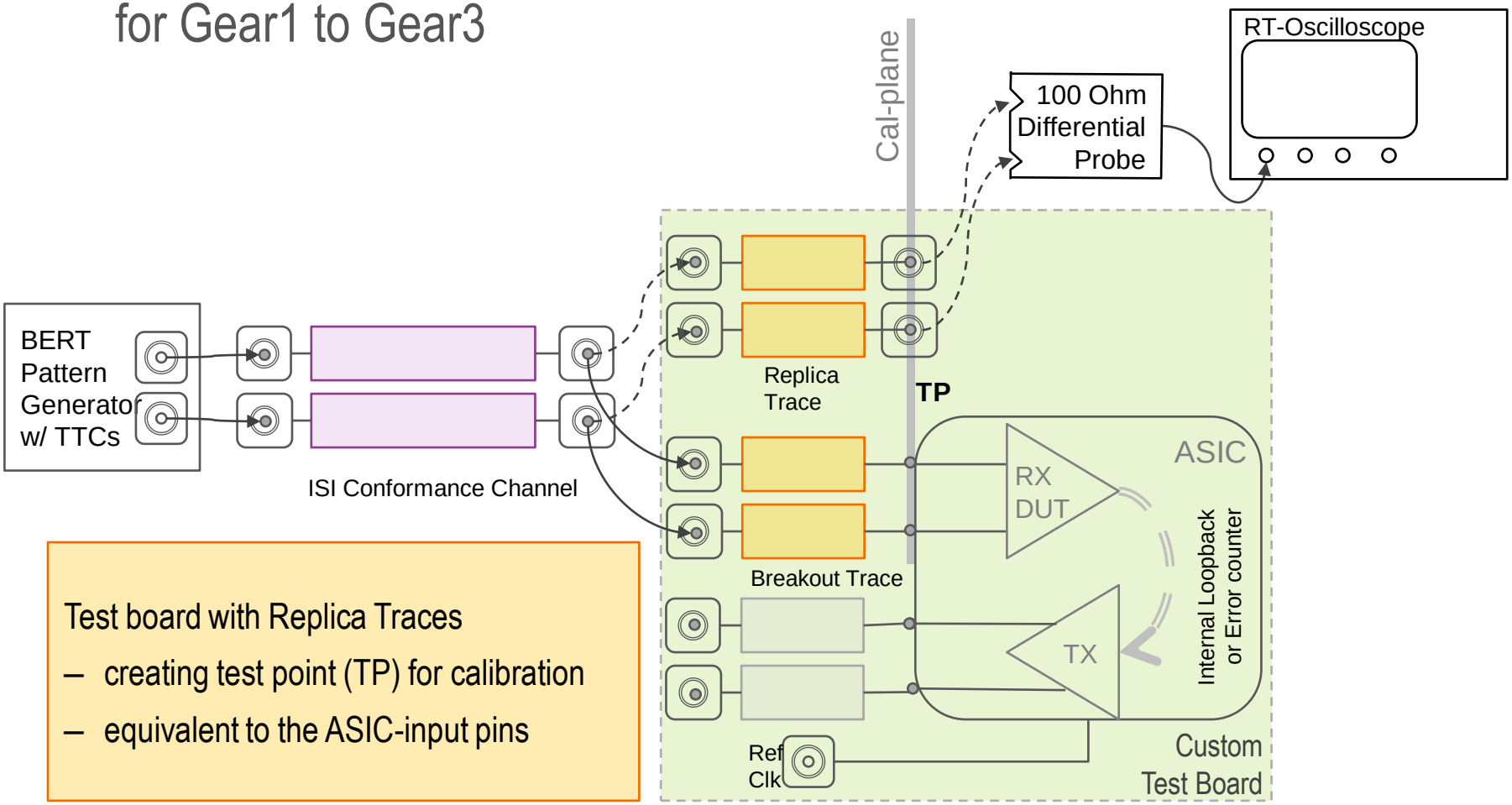
M-PHY Definition of RX Eye Diagram



- Geometry (channel lengths) supported is identical for all Gears despite increasing loss:
  - G3 requires TX de-emphasis (3.5 / 6dB depending on swing and actual channel)
  - G4 additionally requires receiver equalization (RX-EQ) with CTLE and one-tap DFE
- Target BER is 10^{-10}: however, to shorten measurement time, calibration is done with $3x10^6$ samples for BER = 10^{-6} using “prorated” mask w/ larger eye- width and –height (EW , EH) (CTS 3.0)
- Calibration for G4: post processing of measured data emulating reference package and RX-EQ
- TJ, DJ, STTJ and STDJ are normative with continuous signal
  DJ and STDJ are informative with burst using TIEpp method

Setup for M-PHY RX Test and Calibration

Stress Signal Generation and Calibration according to CTS for Gear1 to Gear3

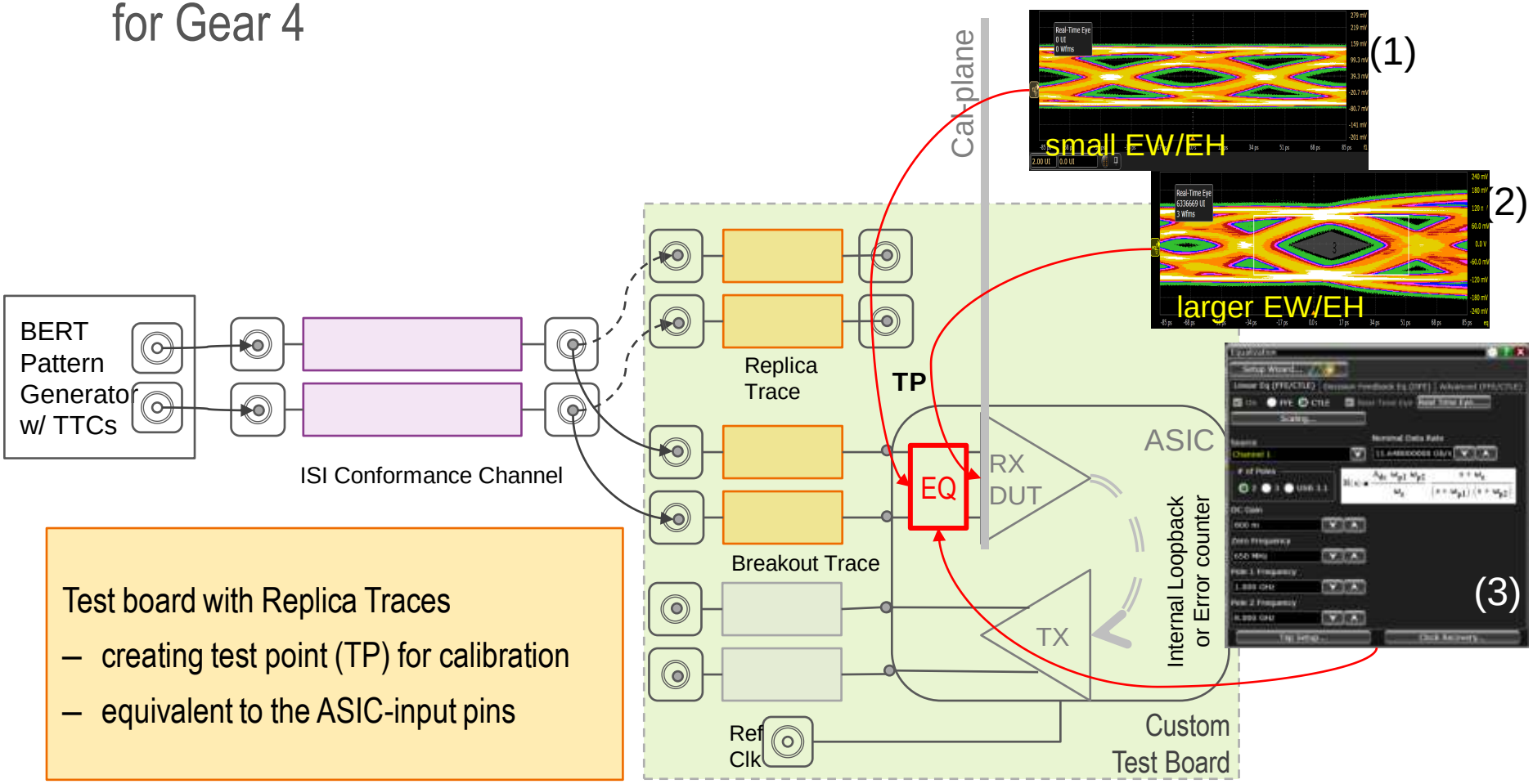


Test board with Replica Traces

- creating test point (TP) for calibration
- equivalent to the ASIC-input pins

Setup for M-PHY RX Test and Calibration

Stress Signal Generation and Calibration for Gear 4



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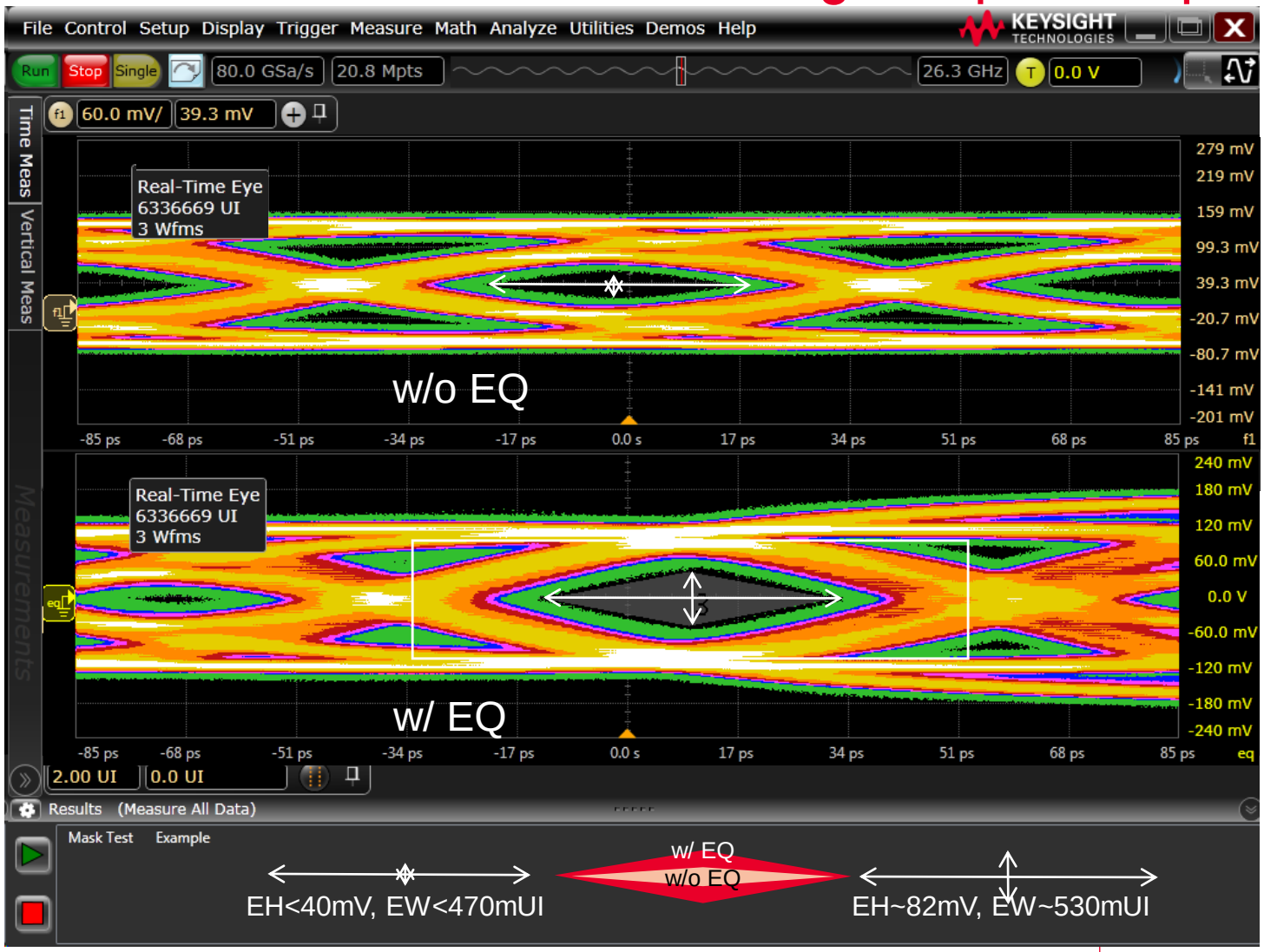
Gear 4 Stress Calibration using Scope Postprocessing



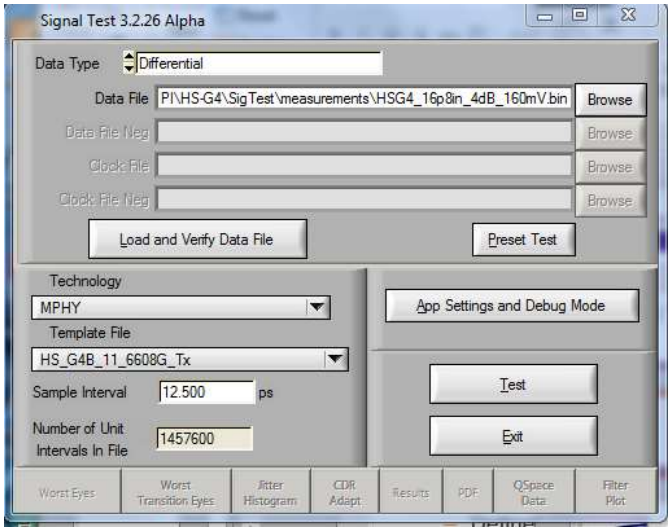
EH < 40mV!
EW < 0.47UI

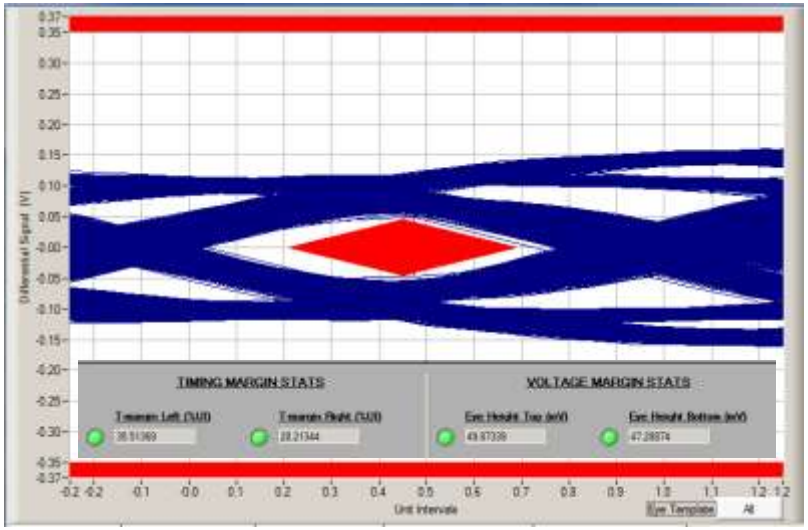
EH ~ 82mV
EW ~ .53UI

Setup for M-PHY RX Test

Stress Signal Generation and Calibration according to CTS

- At gear 4 rates subtle differences may already exist in waveforms measured with oscilloscopes from differrent vendors
- Vendor specific postprocessing SW may increase differencies
- In order to increase consistency SIGTest SW proposed to be used for postprocessing and analysis of eye parameters, i.e. EW and EH





PHY Layer Error Detection

- **Challenges with different protocols:**
  - Asymmetrical lane configuration (e.g. 2x HS upstream / 1x LS downstream)
  - Test modes not mandatory (optional normative / recommendation)
  - Specific method defined in protocol spec, not in PHY spec
- **Various error detection methods:**
  - Line Loopback (i.e. bit level loopback)
  - Logic Loopback (i.e. protocol layer loopback)
  - PPI (=Parallel Processor Interface i.e. parallel data output)
  - IBER (=Internal Bit Error Ratio Counter)
- **Not all MIPI applications have settled on preferred test option**
- **Not possible to provide turnkey solution, RX testing always has a custom portion**

Outlook Mipi M-PHY

M-PHY Spec Roadmap

- V4.0 WG approved draft to be ready by October 31st 2014
- V4.0 Spec December 2014
  - Aligns with UniPro 1.8 schedule, which depends on 8b10b
- V4.1 Spec October proposed for 2015
  - Tighten spec/conformance of digital interface (RMMI)
  - Protocol/PHY optimizations
    - Coding scheme w/ less overhead than 8B/10B
    - Fine data rate granularity (cont range of data rates??)

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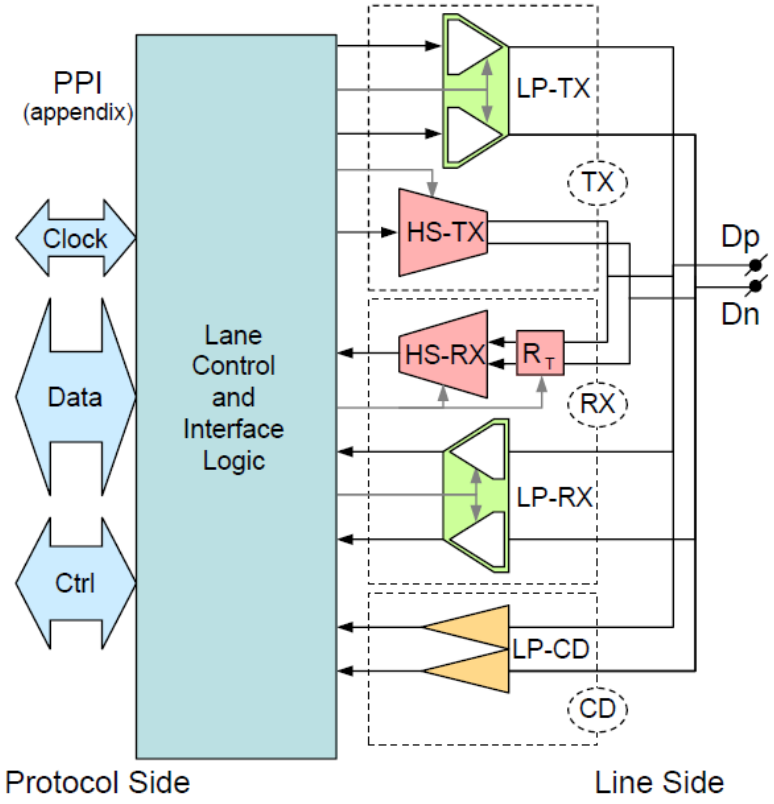
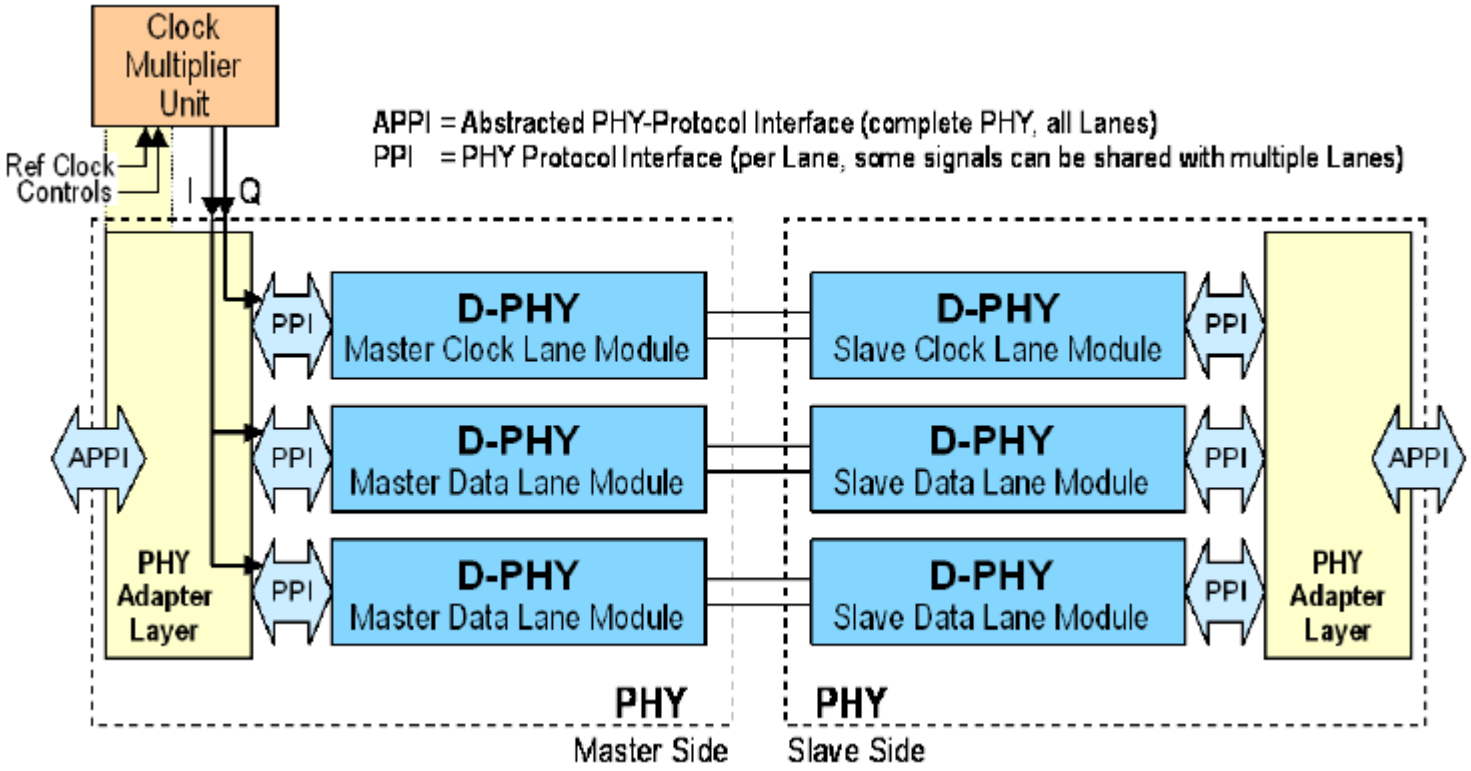
D-PHY Universal Lane Module Functions



- Lane consisting of 2 wires, Dp and Dn
- TXs and Rxs: Bidirectional
- Contention Detection (LP only)
- Two set‘s of TXs / RXs (HS & LP)
- HS-mode:
  - Small Amplitude, terminated (option)
  - Data format: NRZ
  - Signaling: differential
- LP-mode:
  - Large Amplitude, unterminated
  - Data format: RZ
  - Signaling: non-differential

D-PHY Two Data Lane Phy Configuration

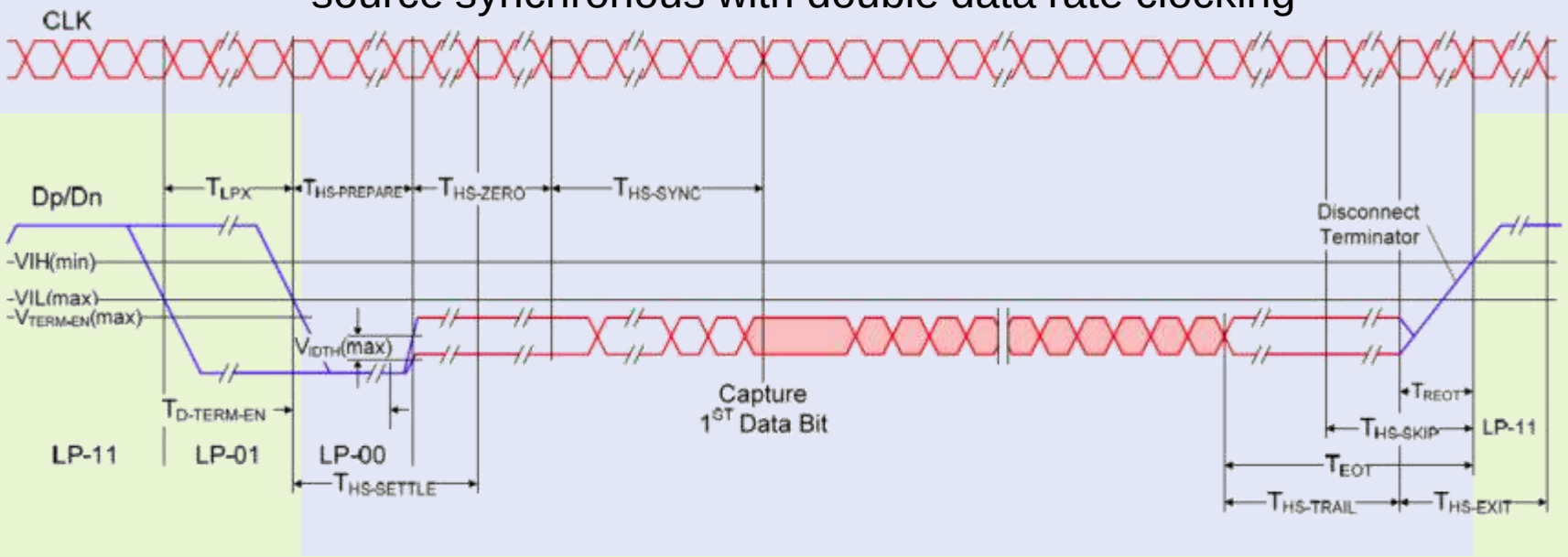


- Source synchronous forwarded double data rate clocking
- Data-rate completely agile, no discrete operating frequencies, continous range
- RX testing is basically stressing set-up- and hold- time conditions
  (eye closure mainly due to DDJ and skew between Data and Clock)

D-PHY Physical Layer Timing Diagram

Transition LP to HS mode, HS_clk active earlier / longer

High speed mode,
Differential signaling, 100 ohm termination,
source synchronous with double data rate clocking



Low power mode
Unterminated, not differential, clock embedded within data

D-PHY Physical Layer Timing Diagram

Transition HS to LP mode and back, no HS_clk in LP mode

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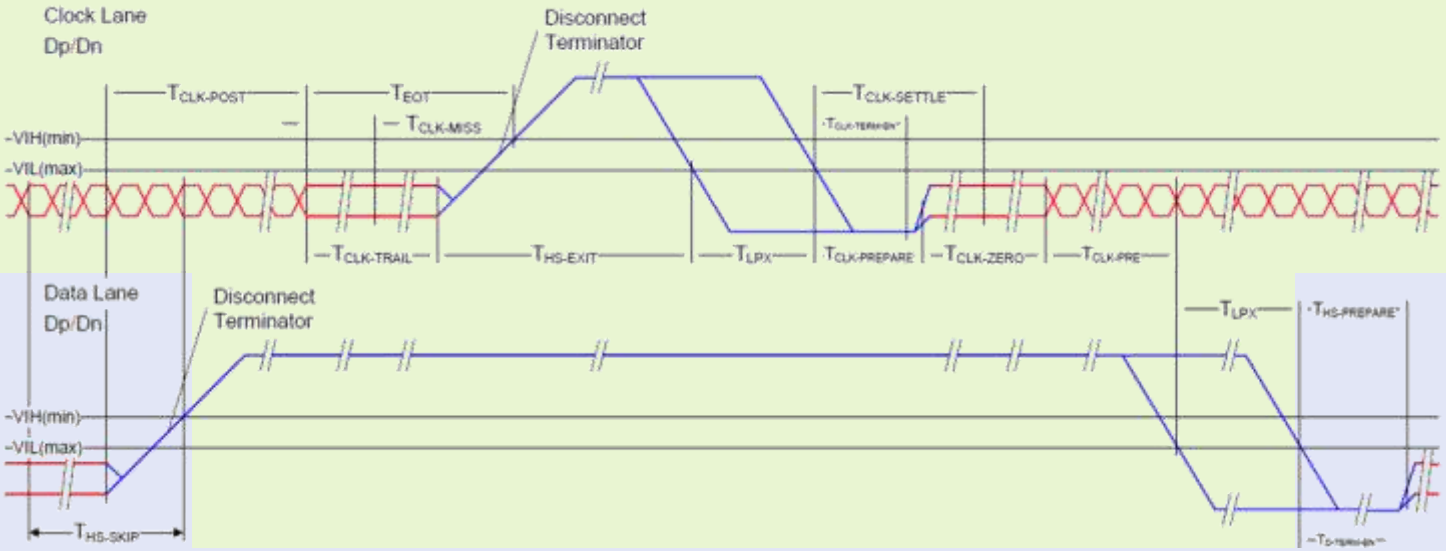

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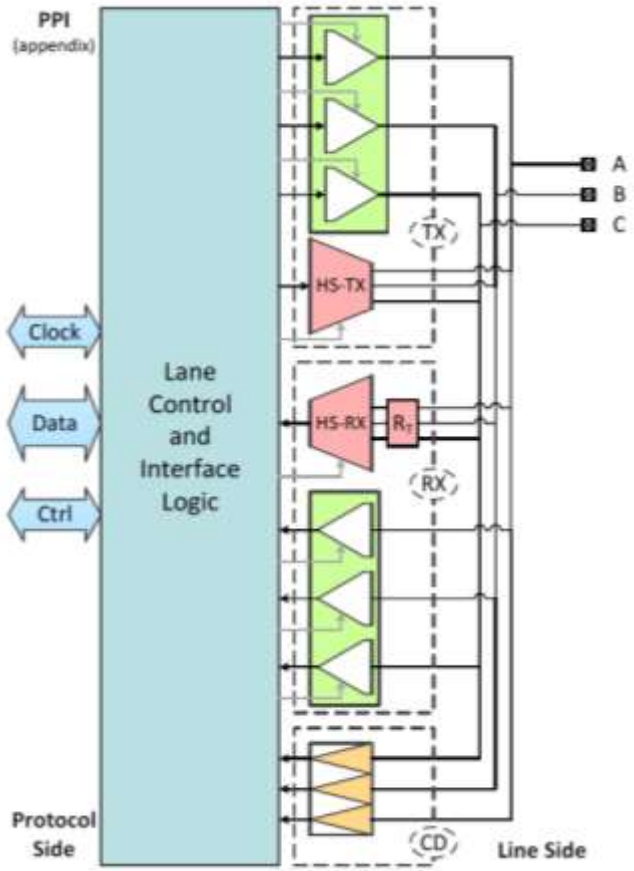
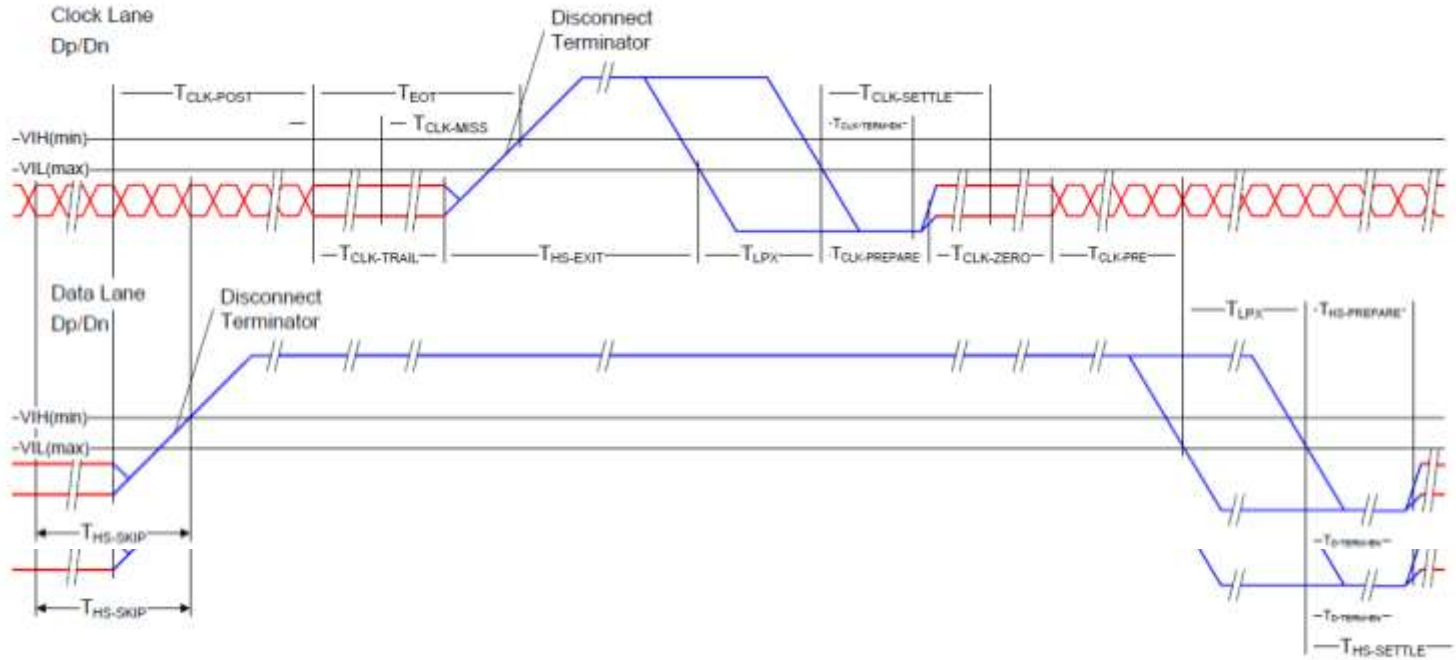


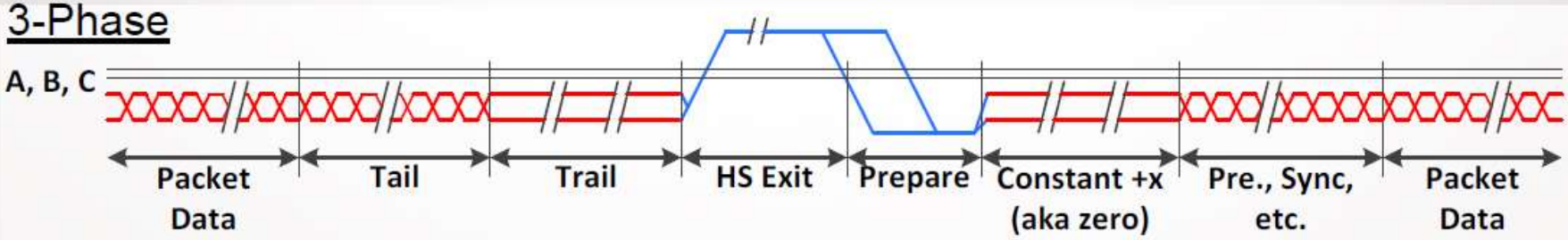
- TXs and RXs: Bidirectional
- Contention Detection (LP only)
- Two set‘s of TXs / RXs (HS & LP)
- HS-mode:
  - Small Amplitude, always 50 Ω “star-type“ termination
  - Data format: 3-phase / 3-level
  - Signaling: 3 wires forming a HS-lane
- LP-mode:
  - Large Amplitude, unterminated
  - Data format: RZ
  - Signaling non-differential

Transition HS to LP mode and back

D-PHY

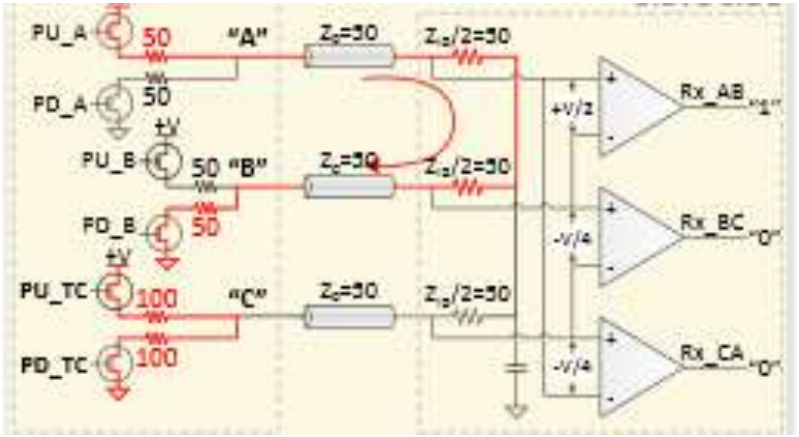


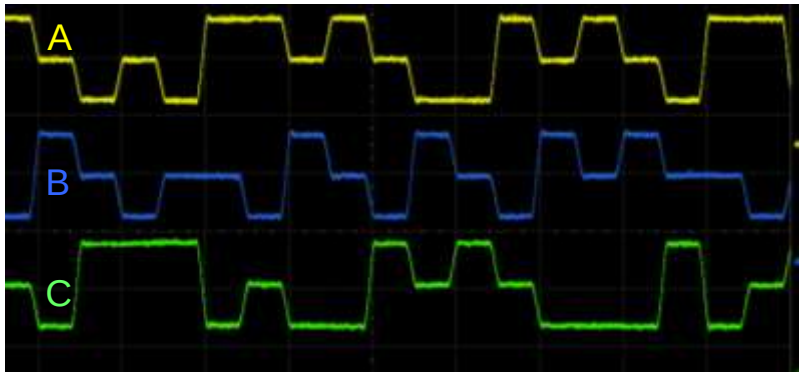
3-Phase



3 Phase Encoding Concept for C-PHY (HS-mode)

- A data encoding technique utilyzing trios rather than pairs of wires
  - 50 Ohm “star-type“termination
  - Utilyzes differential receivers, rejecting common mode noise
  - Drivers work similar to D-PHY but control 3 instead of 2 outputs
- Both clock and data are encoded and transported together in a single trio
  - Always a transition at every symbol boundary, which simplifies clock recovery and allows data rate to be completely agile



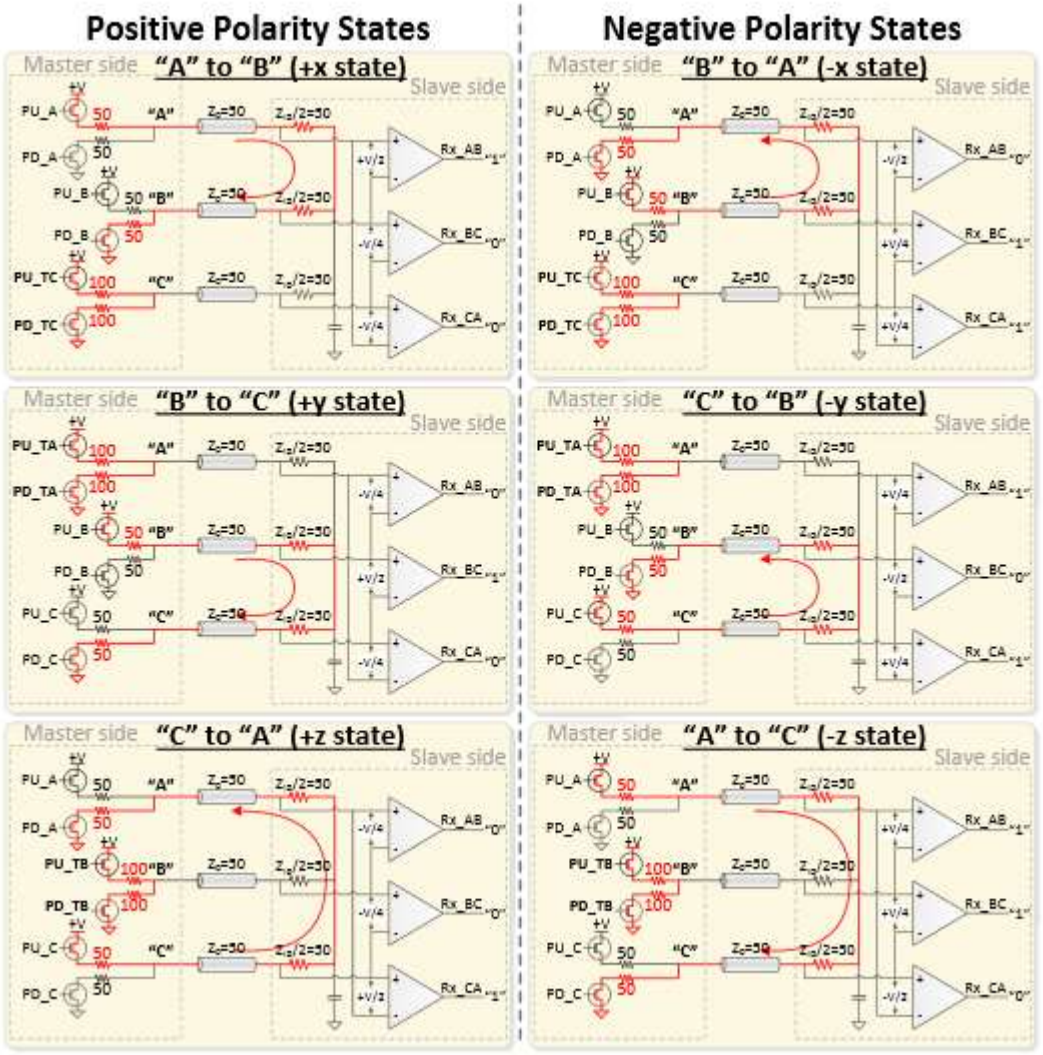


3-phase Signal Examples 1Gsym/s

HS signal only

- Clean HS signal no jitter no skew
- separated (offset-shifted, left) and overlaid (same offset, right)
  note: for each UI each voltage level appears exactly once!

C-PHY Block diagram

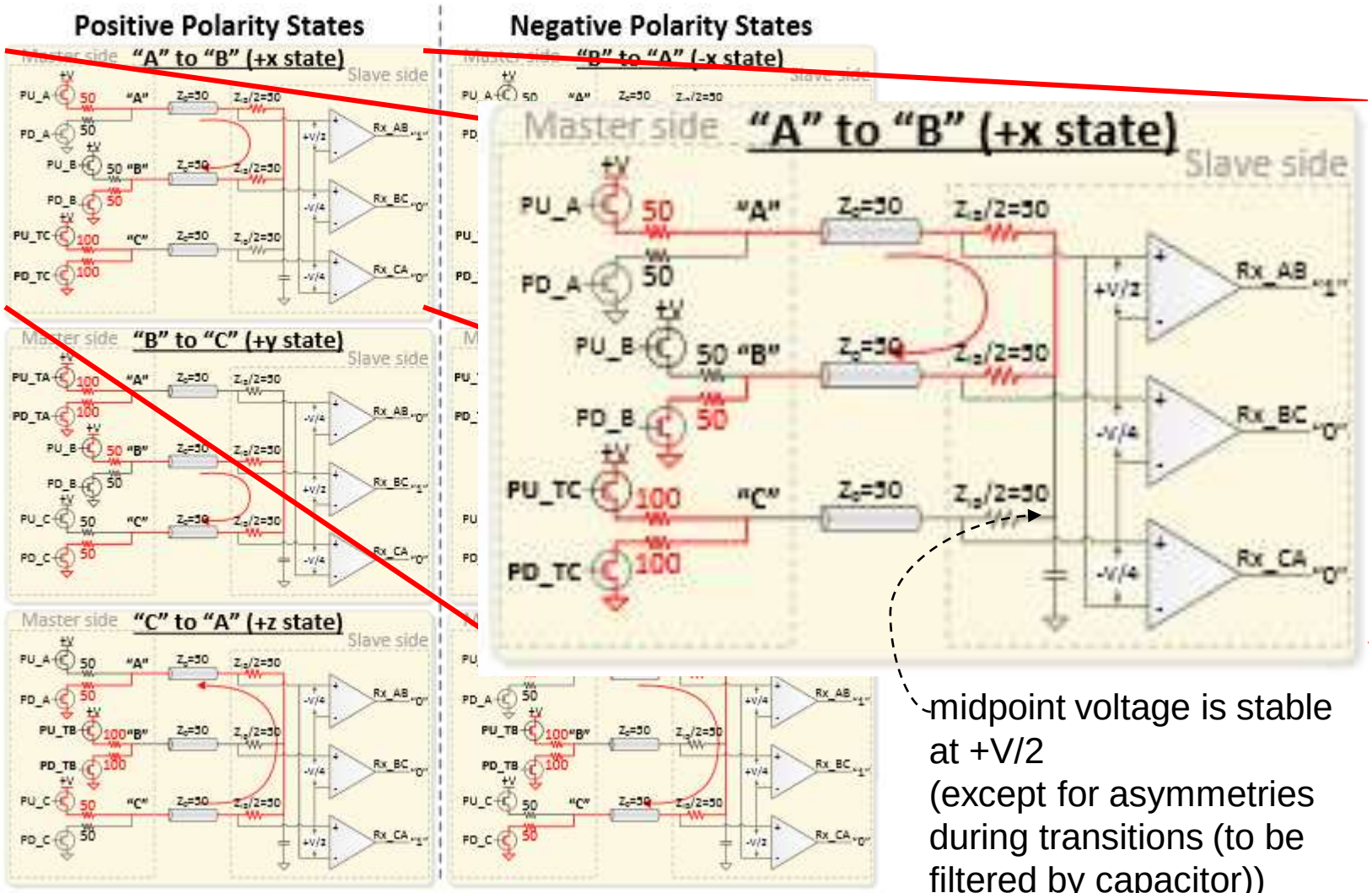


Drawing showing T2 Driver type w/ active mid-level

Coding rules and possible wire states:

- 27 possible wires states
- 6 allowed wire states (+x -x, +y, -y, +z, -z) only those states with different voltage on each wire
- From one symbol to the next symbol only 5 wire states are possible, because a transition is required for CR
- Theoretical coding gain: $\log_2(5) = 2.32$
- Practically usable gain is 2.28 by sending 16 bits in 7 symbols

C-PHY Block diagram



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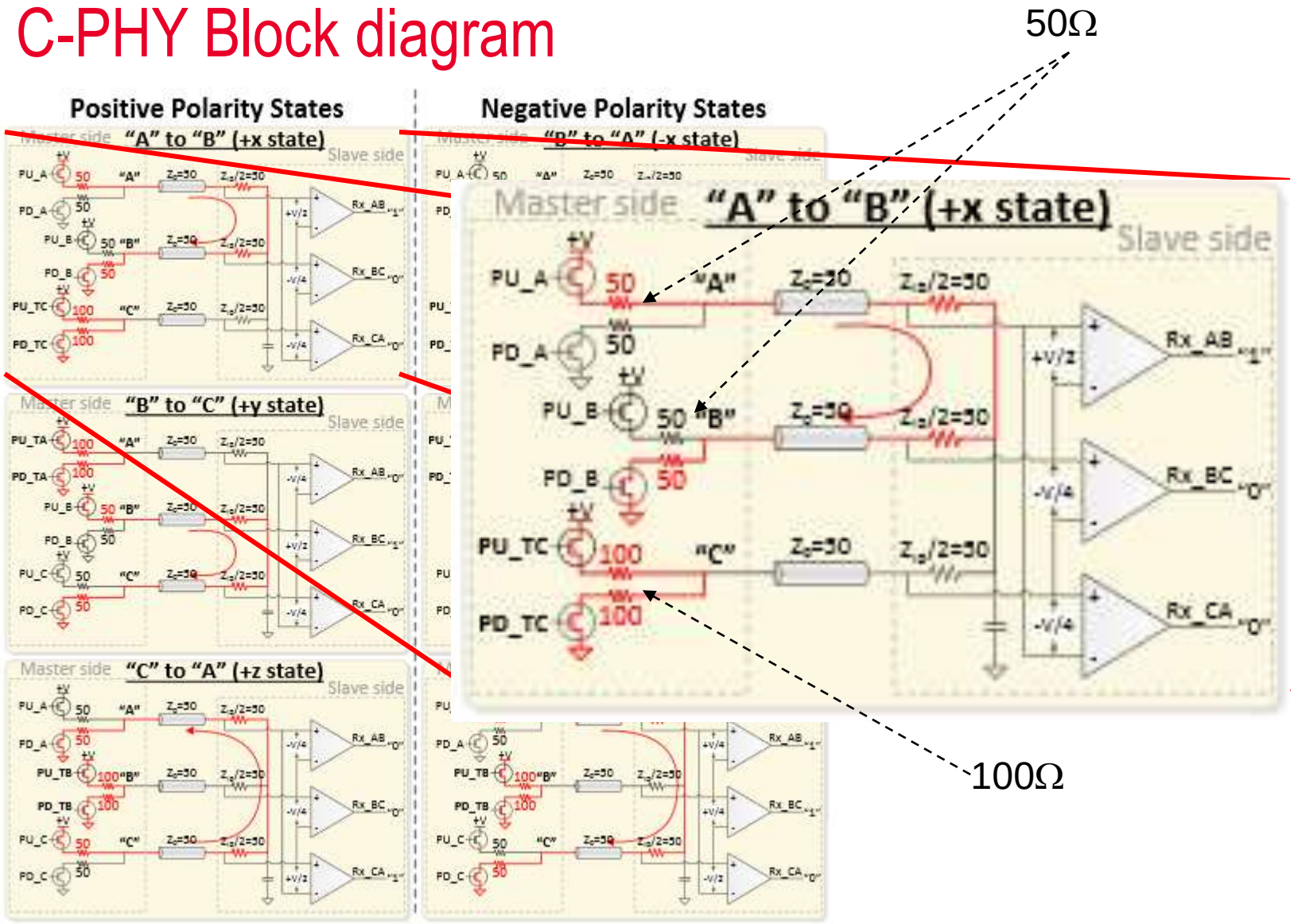

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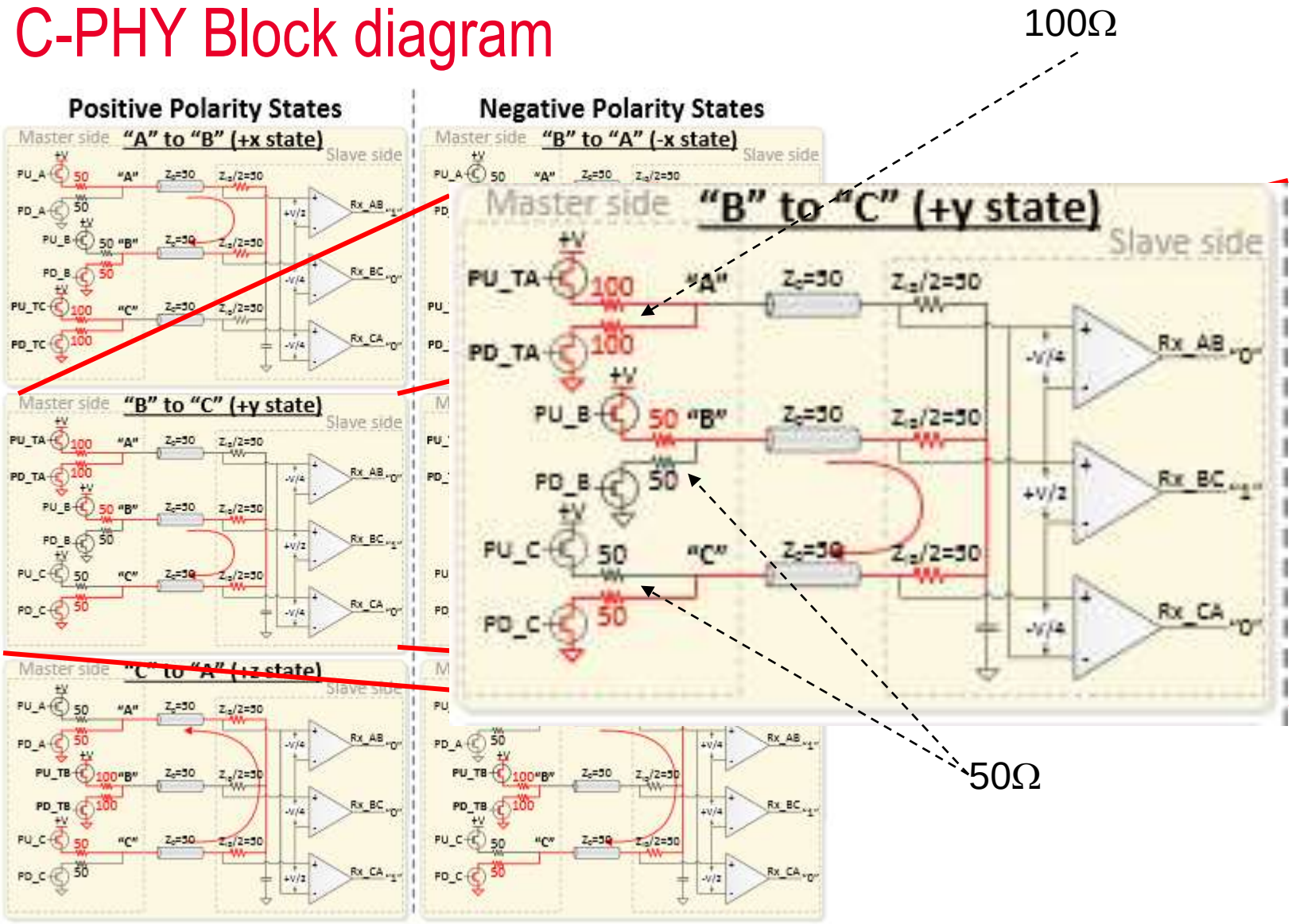
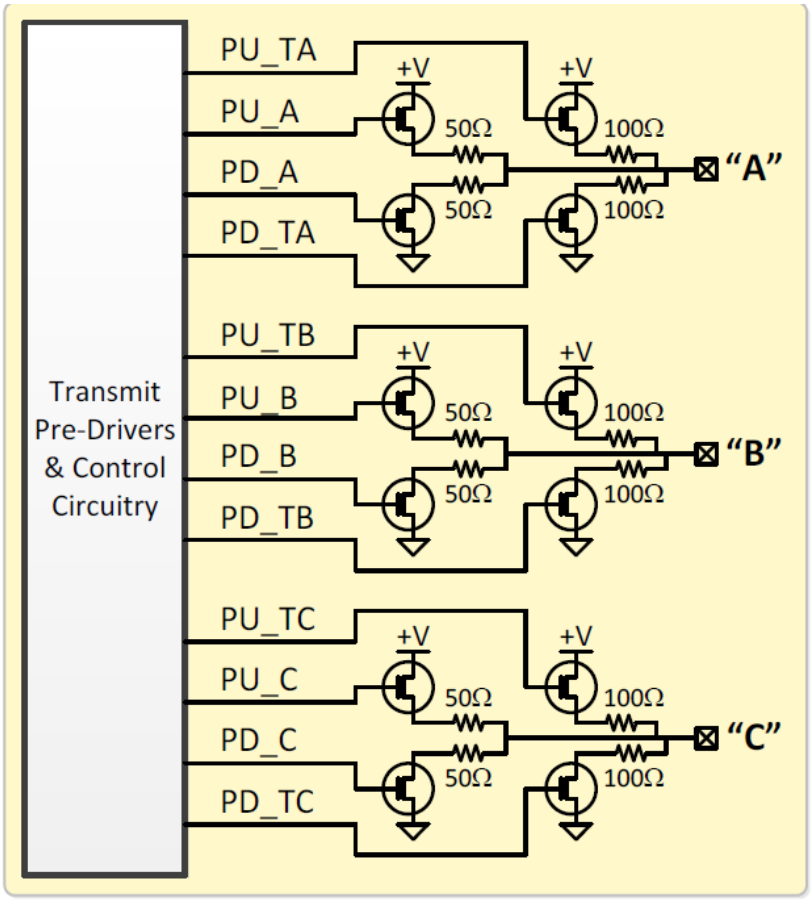
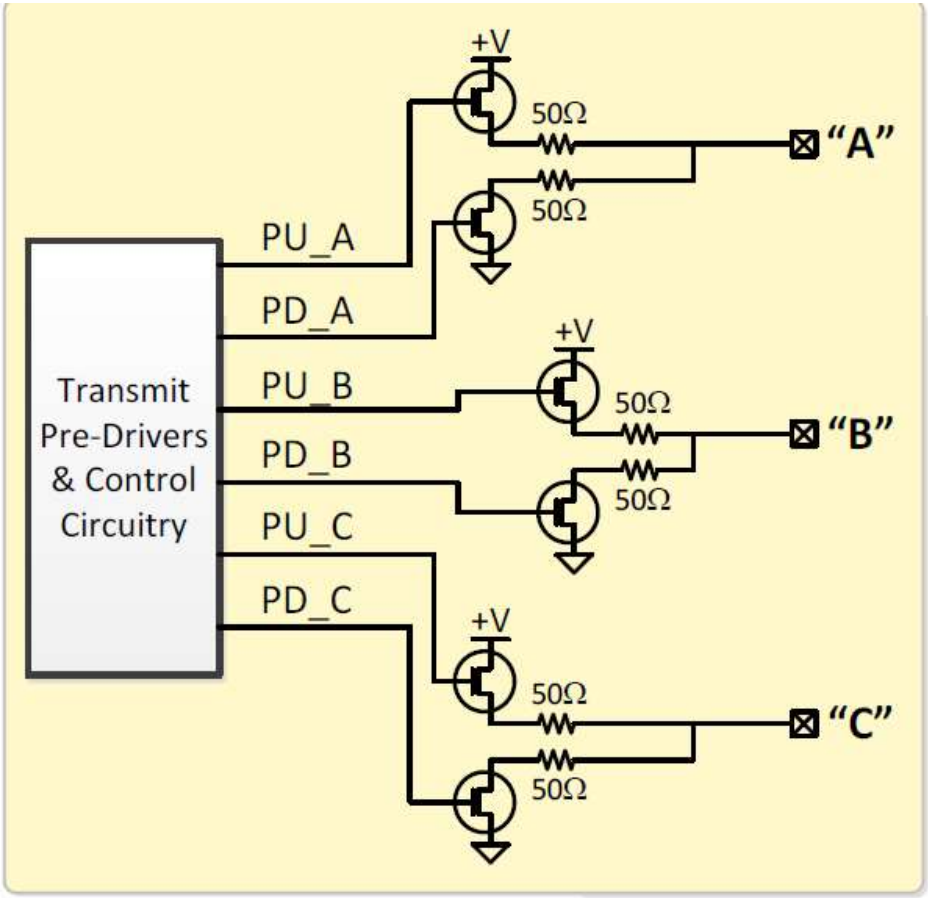


C-PHY possible TX Realization (principle)

T2 Driver type:
active mid-level, extra pair of Transistors w/ 100Ω

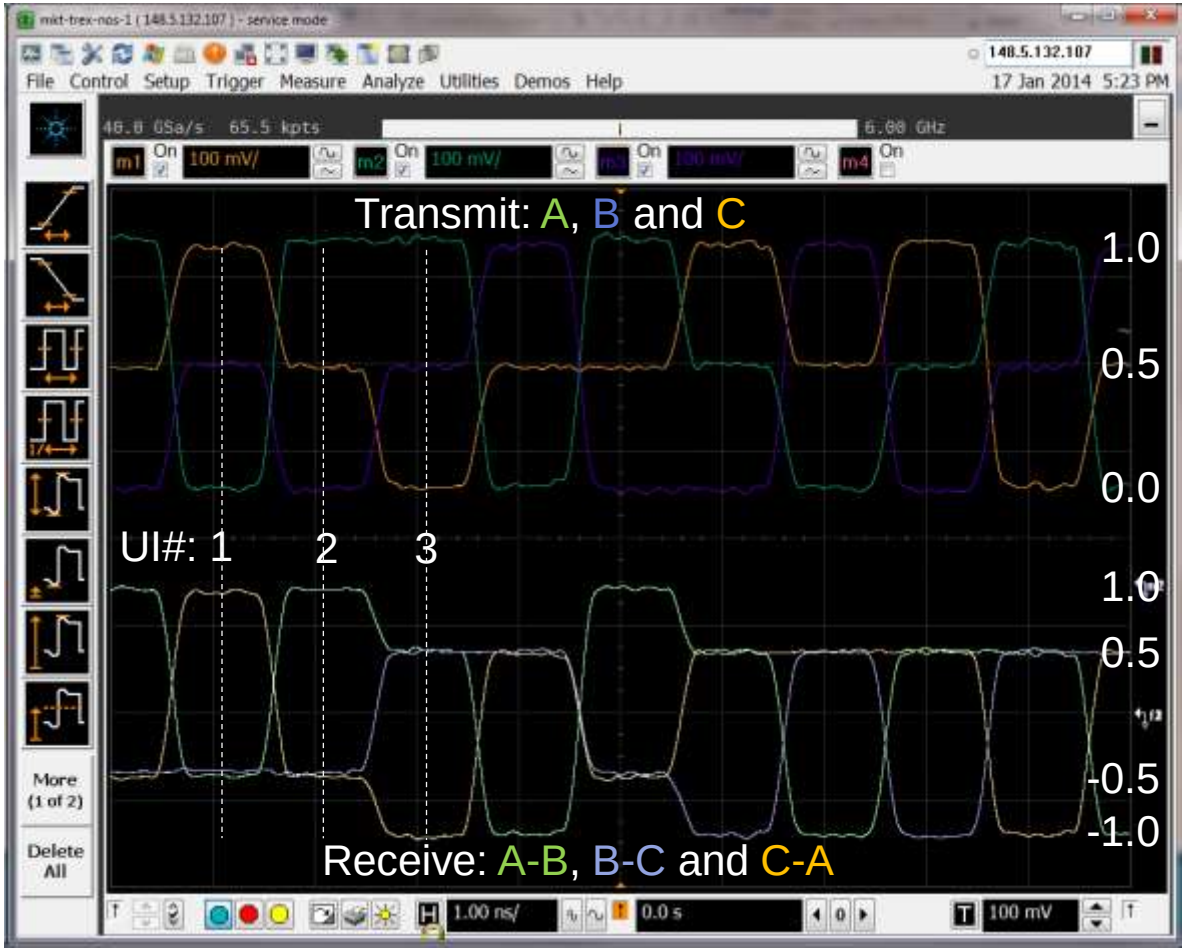
T1 Driver type:
passive mid-level w/ both transistors „open“





C-PHY Signal Characteristics

High Speed Only



Unit Intervall #1

A-B = 0.0-0.5 = -0.5 = weak 0

B-C = 0.5 – 1.0 = -0.5 = weak 0

C-A = 1.0 – 0.0 = 1.0 = strong 1

Unit Intervall #2

A-B = strong 1

B-C = weak 0

C-A = weak 0

Unit Intervall #3

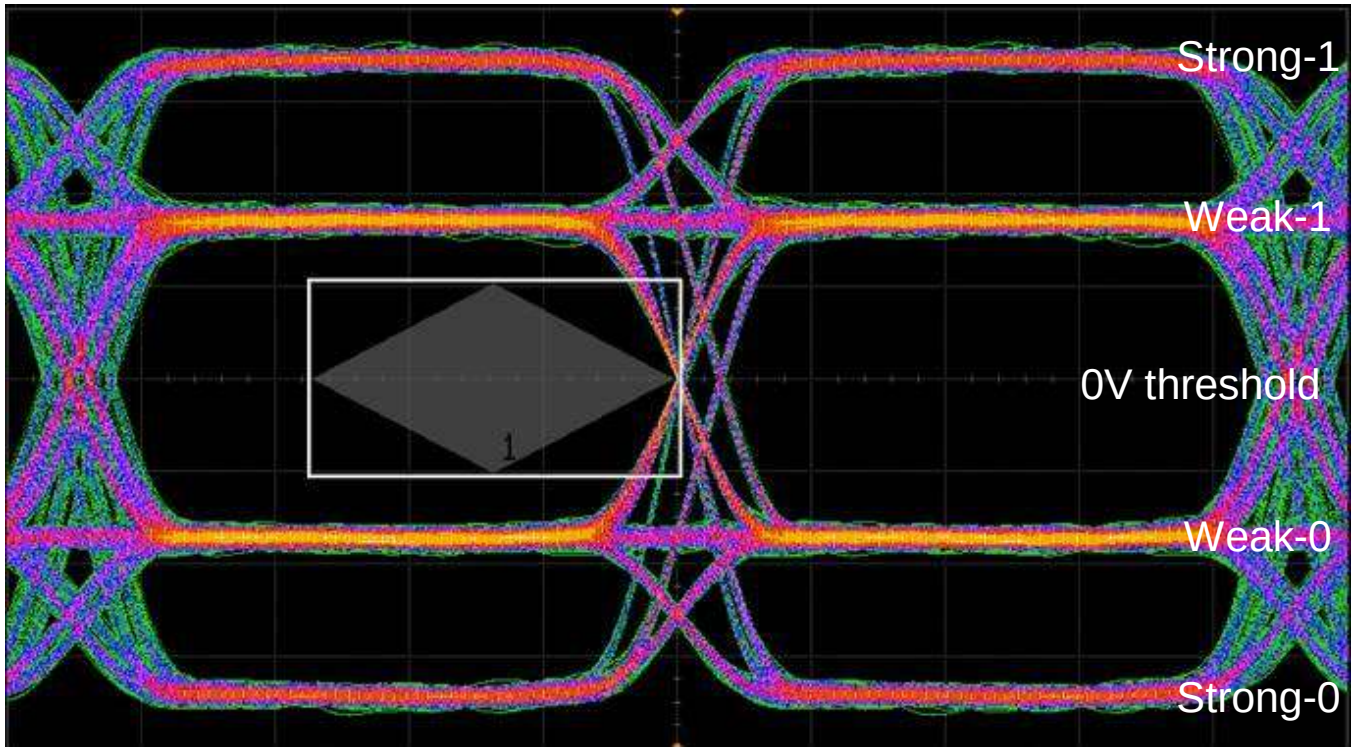
A-B = weak 1

B-C = weak 1

C-A = strong 0

C-PHY Eye Diagram and Mask Test

High Speed Only, A-B



- Clock is recovered from the earliest edge of a symbol transition.
- A delay circuit with negative hold time is used to sample data. Supposed to be more resistant to noise and jitter on the system.

Jitter Tolerance Calibration and Measurement

1. Calibrate the Rise/Fall times from the test equipment generator to approx. 115ps using 20%-80% transition time converter
2. Calibrate the Eye width of three differential signals A-B, B-C, A-C to be 0.7UI by adding Jitter (e.g. DCD) over the already present switching jitter, of course using proper C-PHY clock recovery algorithm.
3. Add ISI jitter by either using a HW channel or SW-programming of the generator to meet the 0.3UI of channel ISI requirement.
4. Tune the Amplitude and the amount of ISI to meet the eye mask requirement of +40 to -40mV for EH and 0.4UI for EW.
   (Allow 10% of variation in calibration over the time scale wrt. the targeted eye mask spec.)
5. After generating the worst case eye as per the mask requirements, Check for any errors in the receiver by comparing the received pattern with the receiver expected pattern and varying DC Common mode.

Key Features of PHY-Layer Standards

	Rev	Max Data Rate (Gb/s)	Data format		Clocking	Clock Recovery	EQ
		HS	LP	HS			
D-PHY	1.0, 1.1	1.5, continous	RZ	NRZ	Forward Source Synchronous (DDR)	NA	None
	1.2	2.5, continous					None
	2.0	4.5, continous					TX
C-PHY	1.0	2.5, continous	RZ	3-ph	embedded	Logical	None
M-PHY	1.0, 2.0	1.5/3 discrete	PWM	NRZ	embedded	PPL-based	None
	3.0	6, discrete					TX
	4.0	12, discrete					TX & RX

Release Status of Standards and Related CTSs

Standard	version	Status	CTS	Status
D-PHY	1.0, 1.1	released	rev 1.0	released
	1.2	released		wip
	2.0	wip		not started
C-PHY	1.0	wip	vers 1.0r0.5	wip
M-PHY	1.0	released	vers 1.0r0.95	released
	2.0	released	vers 1.0r0.95	released
	3.0	released	ver 3.0r16	wip
	4.0	wip		not started

wip = work in progress

Agenda

- MIPI Overview, history and recent changes
- RX test: recap of methodology
- M-PHY key features, changes in spec & methodology
- D-PHY recap of basics, signaling, LP- and HS- modes
- C-PHY intro on 3-wire 3-level signaling
- Keysight test solutions M8000 based
- Summary, links, QA

How Can All of This Be Tested?

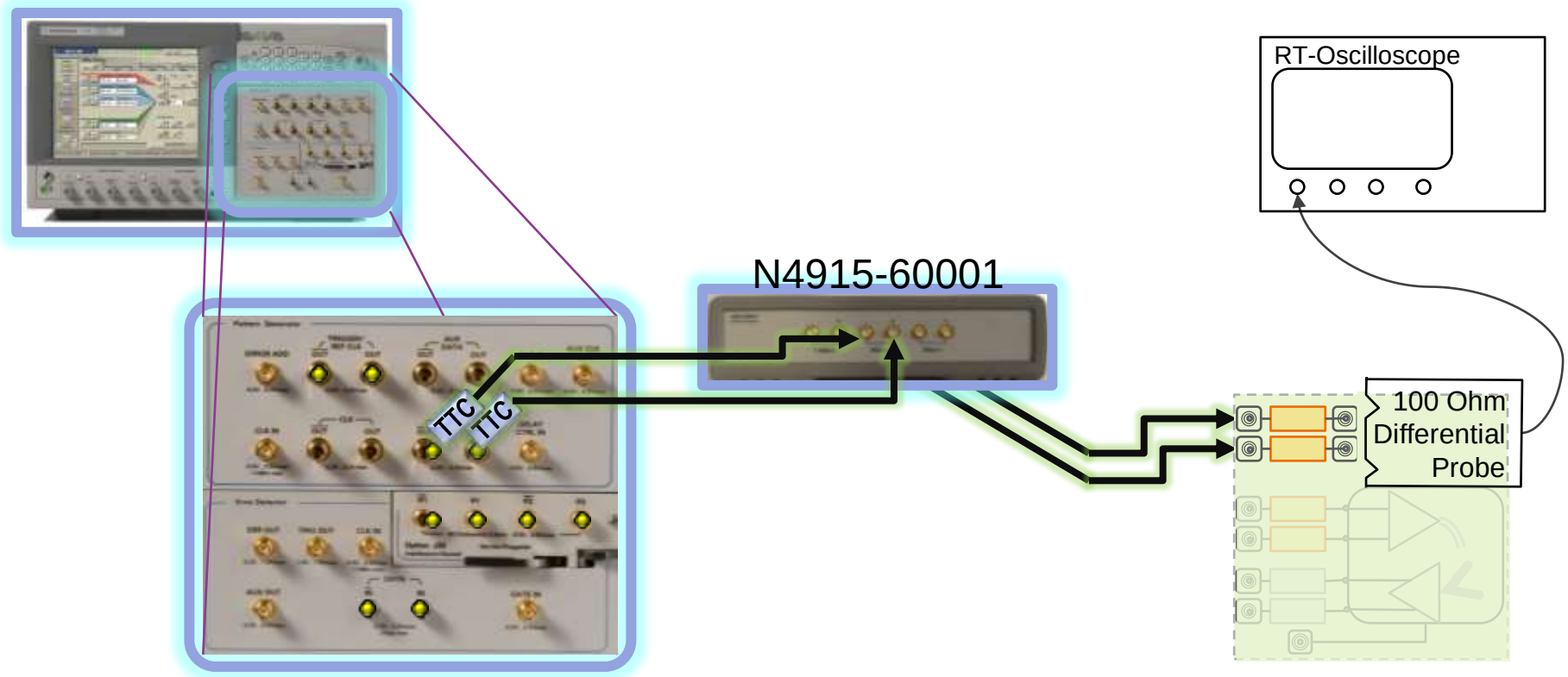
Keysight M8000 Series of BER Test Solutions

– Modular system in AXI form factor /frame consisting of
  - HW modules M8041A and M8051A plus M8070 SW forming Keysight J-BERT M8020A
  - modular up to 4 channels enabling channel skew measurements
  - Very much comparable to N4903

– Very well suited for M-PHY

– ...

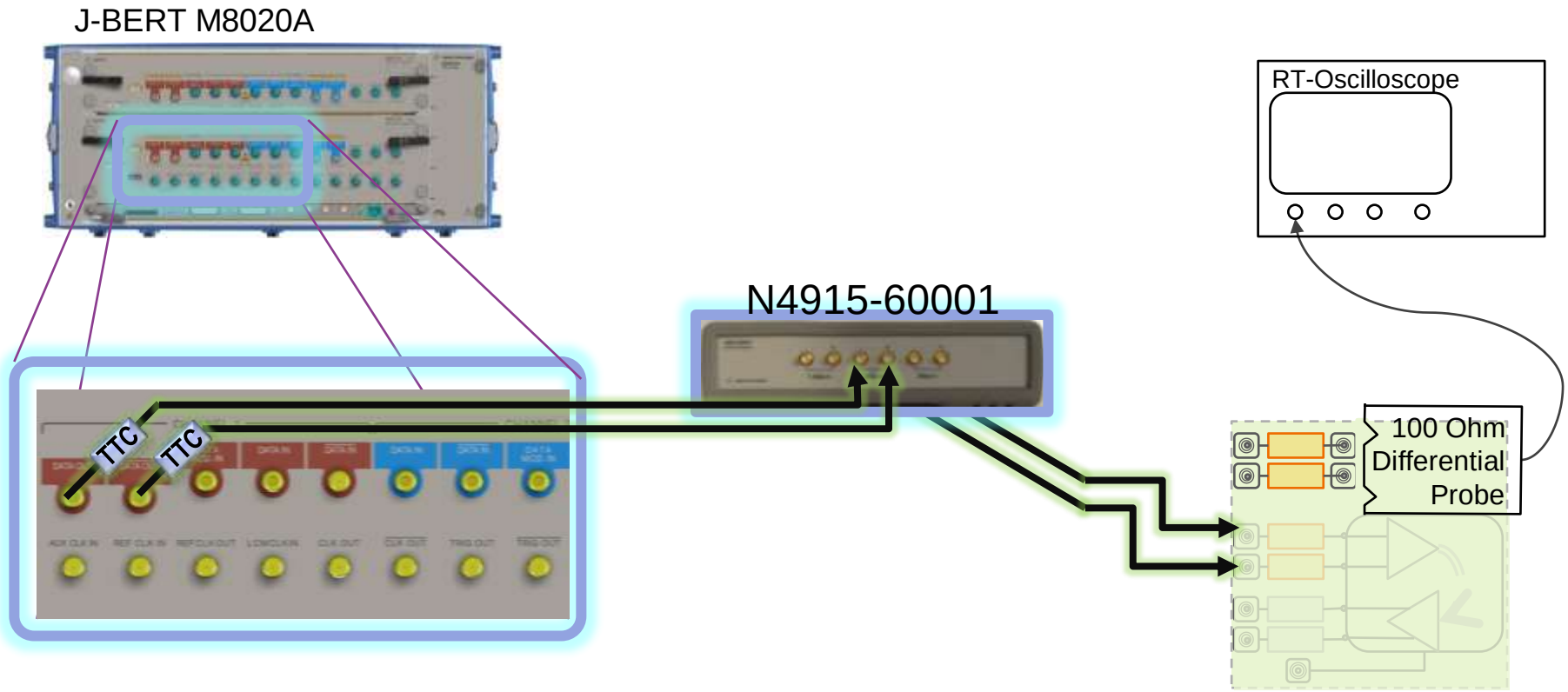
Test Setup Using Agilent J-BERT N4903B



1:1 match of CTS proposed set-up with actual Keysight J-BERT set-up

ISI conformance channel relaized through N4915 60001 SATA ISI trace (2)

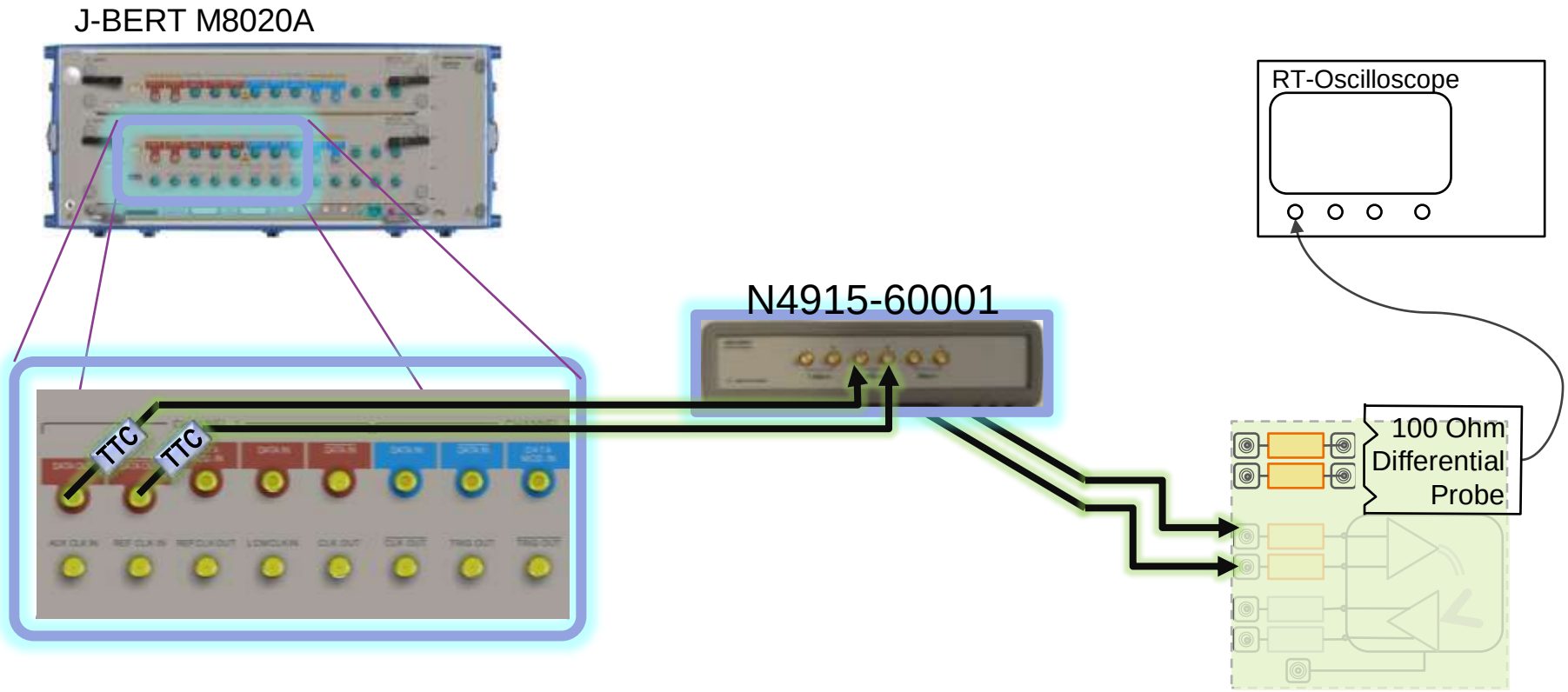
Test Setup Using Agilent J-BERT M8020A



1:1 match of CTS proposed set-up with actual Keysight J-BERT set-up

ISI conformance channel relaized through N4915 60001 SATA ISI trace (2)

Test Setup Using Agilent J-BERT M8020A



M8020A‘s modularity addresses multichannel applications

Jitter Cocktail for Receiver Tolerance Test

M-PHY Gear 1 & 2

Jitter Cocktail consists of

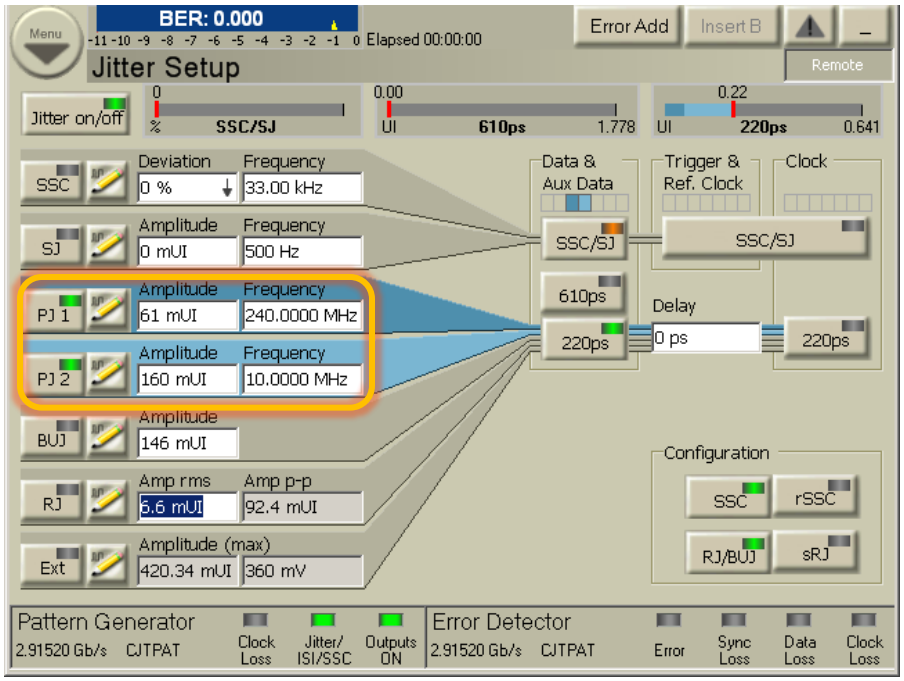
- ISI generated through Conformance Channel and Replica Trace
- Dual band RJ
- Dual-tone SJ

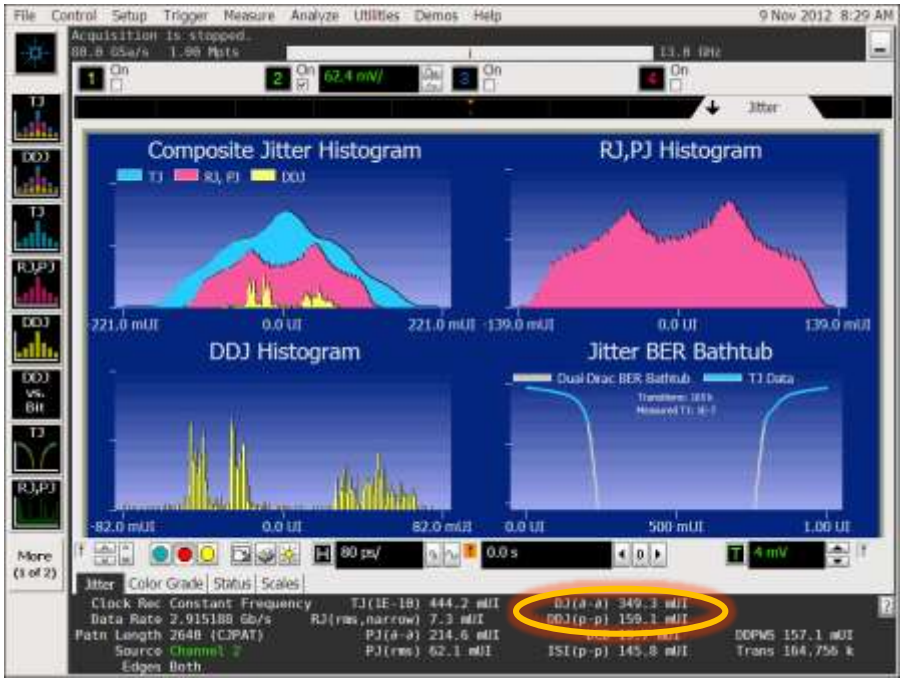
Step	Action	J-BERT parameter	Target Value	Pattern	TIE-HP-filter
1	Adjust wideband RJ (>f_{L_RX}) to achieve STRJ	RJ	0.10 UI_{pp} 7.9mUI_{rms}	clk/2 (1010)	1/30UI
2	Add low frequency RJ (<1/30UI) to achieve RJ=TJ-DJ	BUJ	0.17UI_{pp} 13.4mUI_{rms}	clk/2 (1010)	f_{L_RX} *
3	Turn all RJ off; calibrate SJ (f_SJ1, f_SJ2, f_SJ3, f_SJ4)	PJ2	0.15 $UI_{,pp}$	CJTPat	off
4	Keep all RJ off but keep PJ2 on; calibrate STSJ (240 MHz) to achieve STDJ=0.2UI (STSJ=STDJ-DDJ) or DJ=0.35UI	PJ1	0.35 $UI_{,pp}$	CJTPat	off
5	Turn all callibrated jitter on. Calibrate to prorated eye mask at BER 10^{-6}	PJ2, Amp	V_{DIF_AC}=43mV 1-TJ=0.52UI	CJTPat	off

*) $f_{L\_RX} = F_{C\text{-}RX}$ = 1/2MHz

4. Short Term DJ Cal w/ J-BERT N4903B

Caused by CJPAT over Board Trace + HSSJ



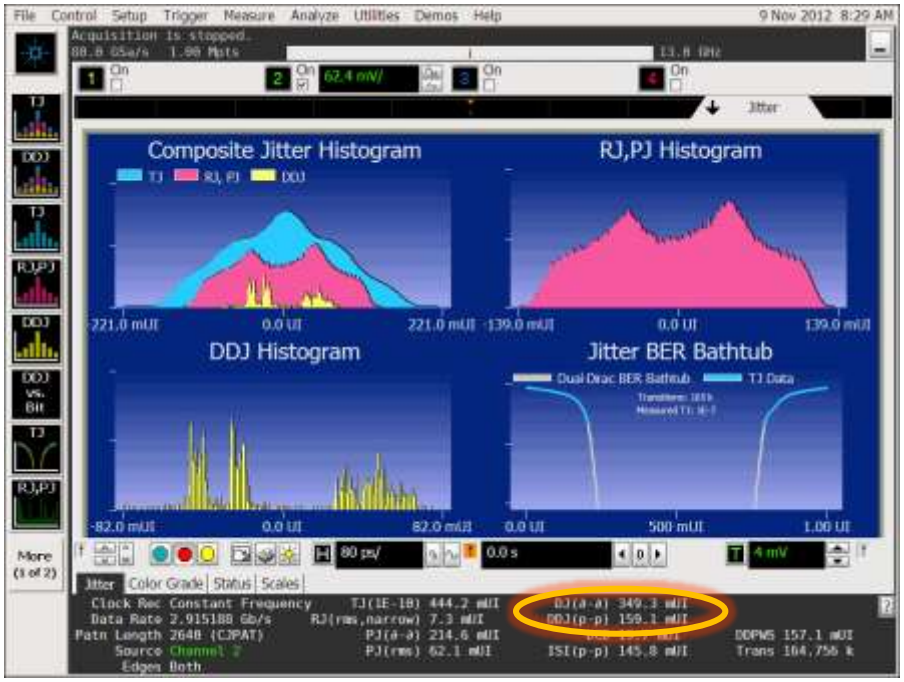


Keep RJ/BUJ off and PJ2 on
Turn on PJ1 with frequency set to >1/30UI e.g. 240MHz

Measure DJ with TIE turned off
Calibrate DJ to target value of MTDJ = 350mUI

4. Short Term DJ Cal w/ J-BERT M8020A

Caused by CJPAT over Board Trace + HSSJ



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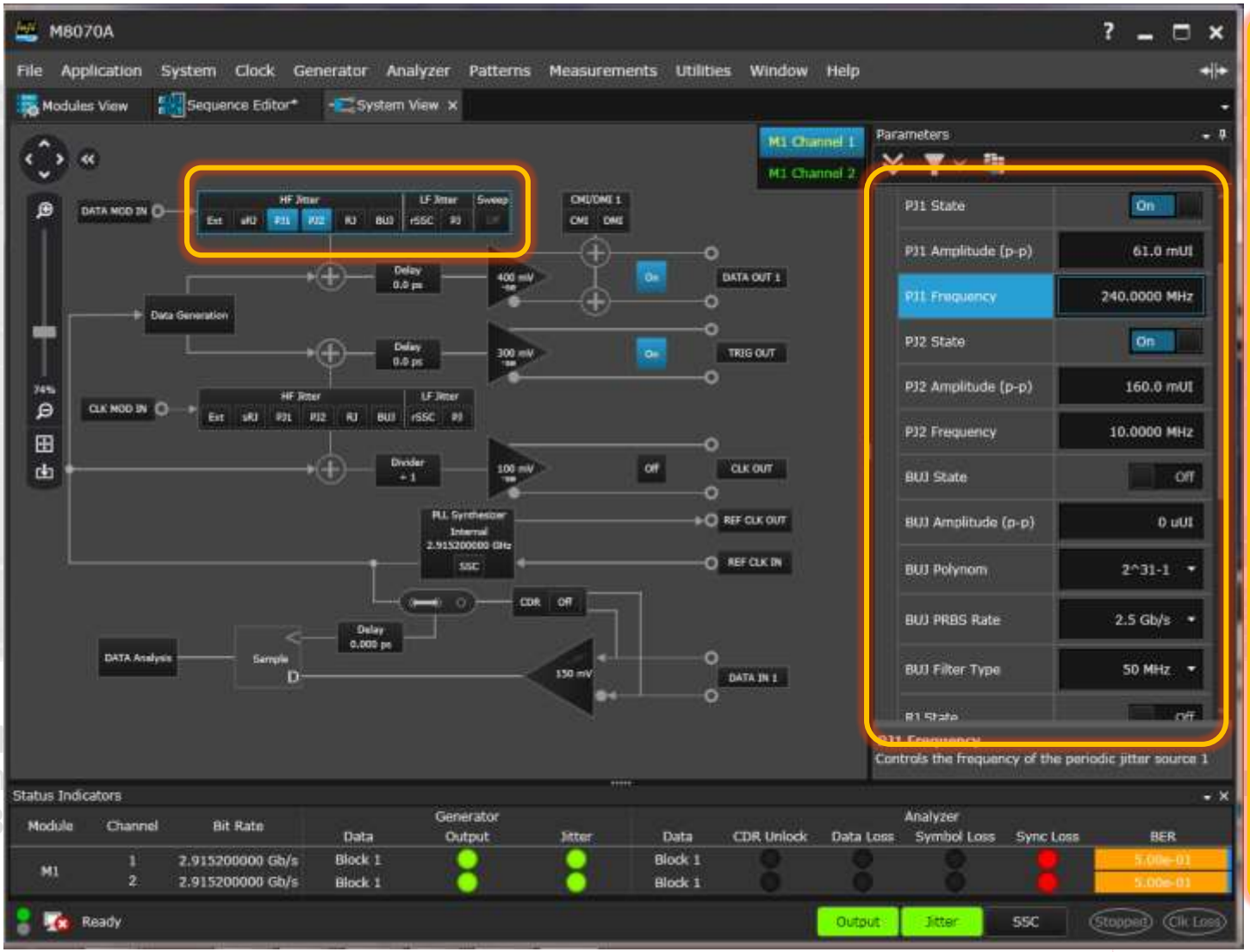


Property list

PJ1 On

PJ2 On

BUJ Off

RJ Off

MTDJ = 350mUI

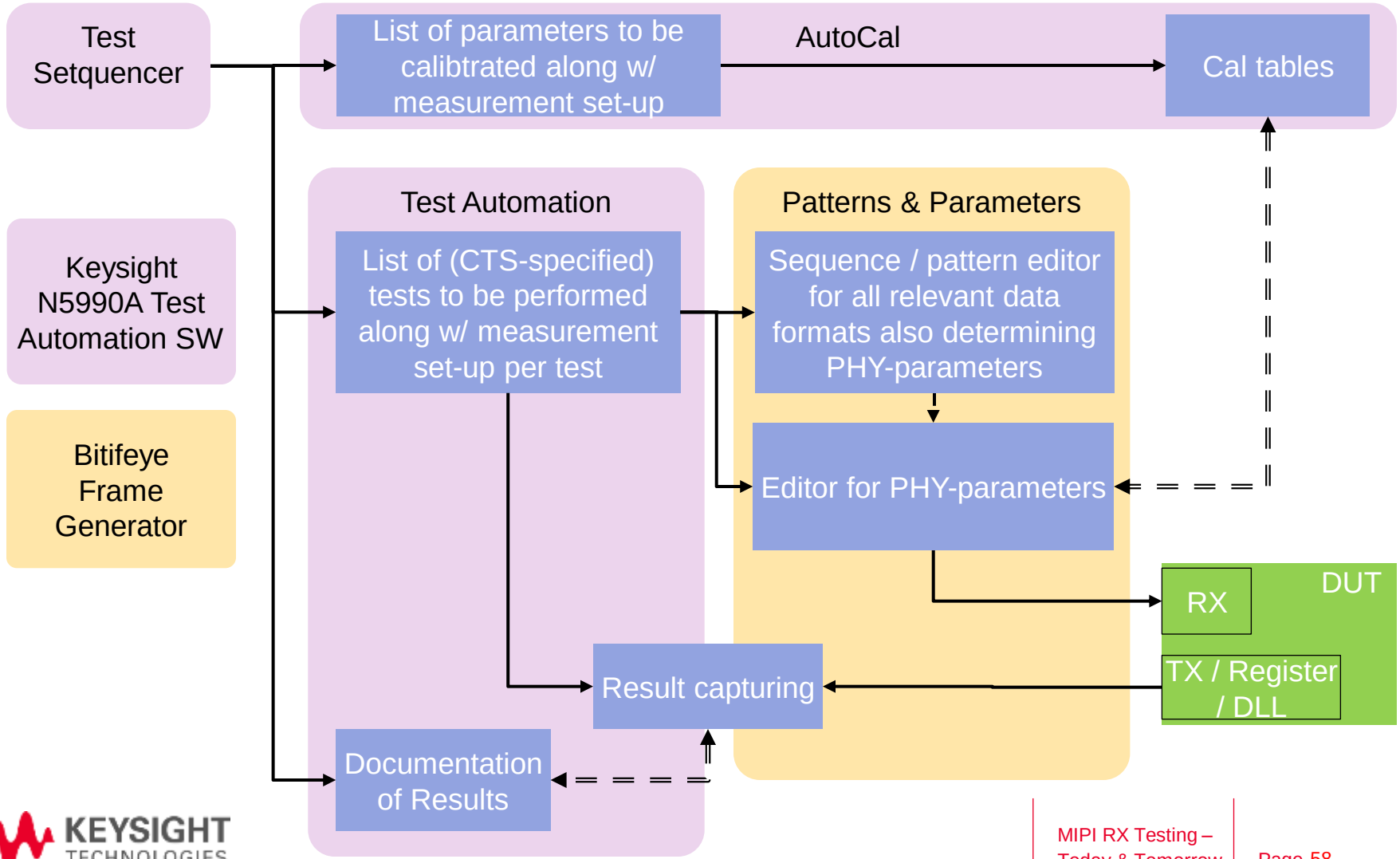
How Can All of This Be Tested?

Keysight M8000 Series of BER Test Solutions

- Modular system in AXI form factor /frame consisting of
  - HW modules M8041A and M8051A plus M8070 SW forming Keysight J-BERT M8020A
  - modular up to 4 channels enabling channel skew measurements
  - Very much comparable to N4903

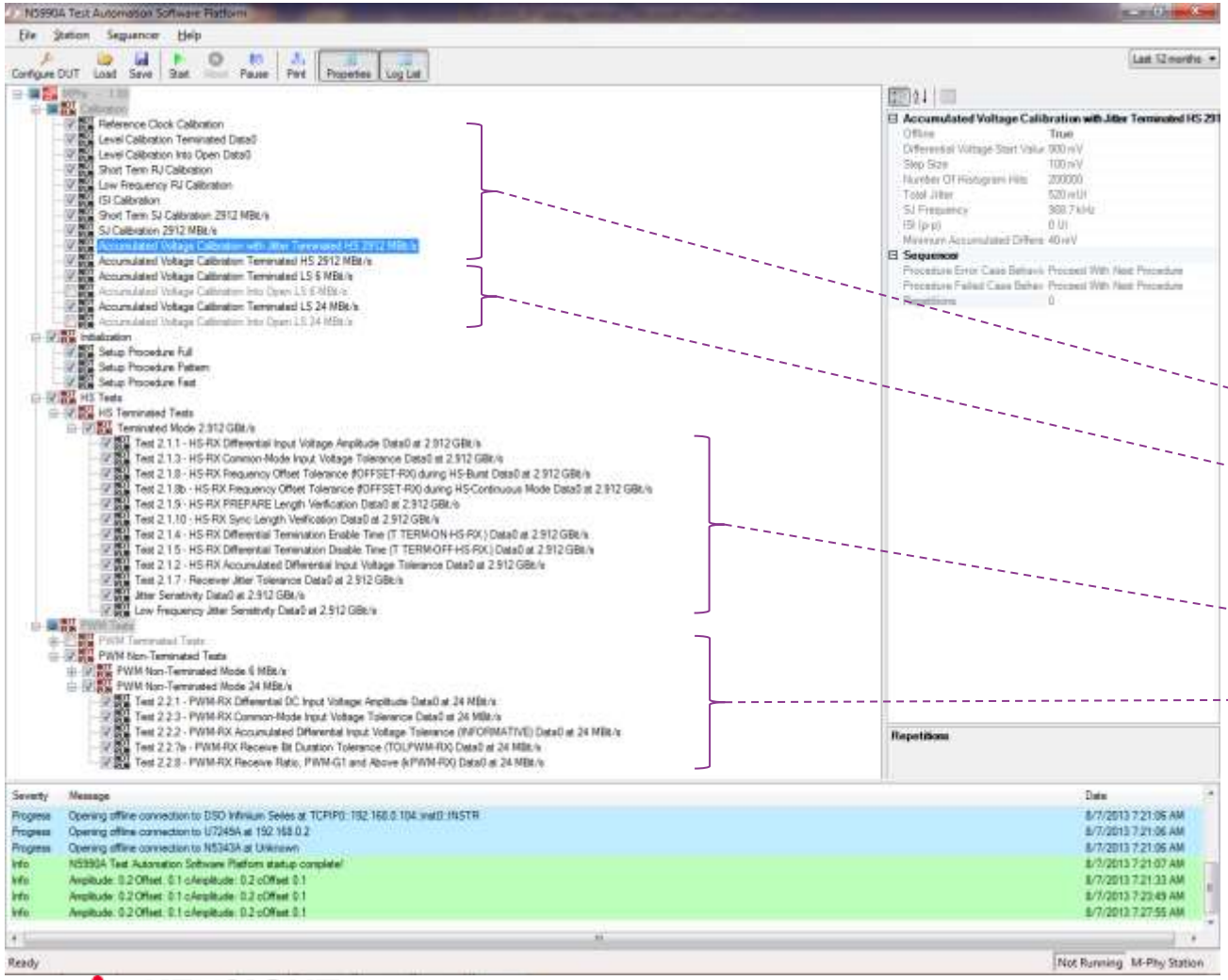
- Very well suited for M-PHY
- Test Automation: SW Keysight N5990A option 165 & Bitifeye Frame Generator BIT-2060-0001-0
- ...

Building Blocks for a Test and Related SW Products



N5990A Automation Software

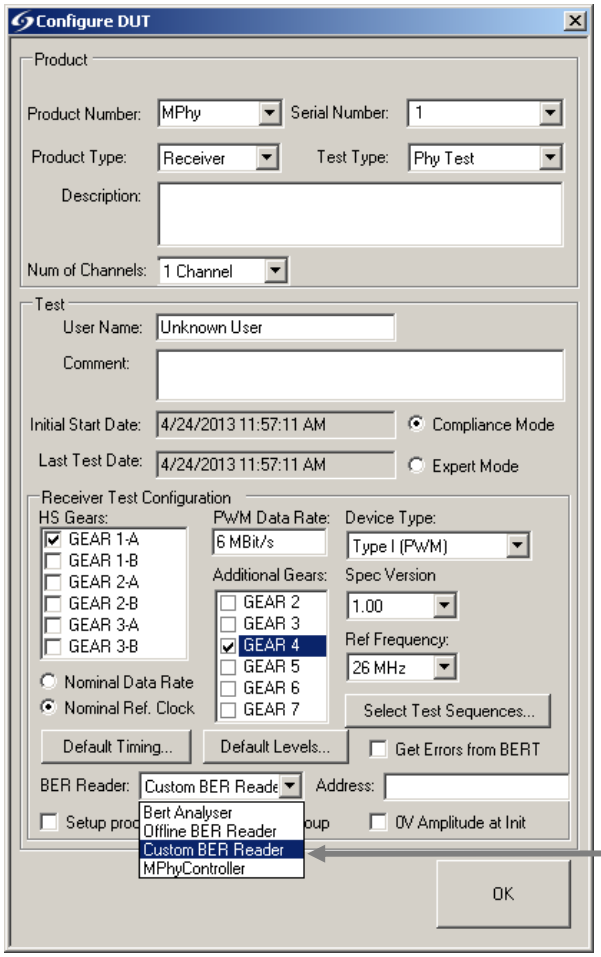
Setup of Test Flow



- Parameters of selected item
- Calibrations
  - HS, NRZ (RT)
  - LP, PWM (NT)
- RX tests
  - HS, NRZ (RT)
  - LP, PWM (NT)

N5990A Automation Software

DUT Configuration, Integration of IBERReader



- Connect (string connection): will be called once at the beginning of the test run. The connection string can contain a customized address (like a COM port) to access to the tool which is able to read out the internal counters of the DUT
- Init (string mode): will be called once at the beginning of each test. This allows to configure the DUT into the test mode of a particular test (HS or PWM, Gear, Functional Test)
- ResetDUT (): will be called once at each test point. This allows to reset error counters, or set the DUT in a defined mode to be ready for the next test point
- GetCounter (out double errorCounter, out double bitCounter) will be called after or during a test point execution. The errorCounter value can contain a CRC- or symbol-error, and the bitCounter can contain a bit or burst counter. The counters can provide just simple indicators, if errors happened and if the DUT was able to receive data, or in case of both error and bit counters being implemented, to calculate BER

- Copy the compiled MPhyBerReader.dll into the ValiFrame Program Files folder

- A new entry in the BER Reader List will be visible
- After selection of the Custom BER Reader the N5990A automation software can connect with the DUT

How Can All of This Be Tested?

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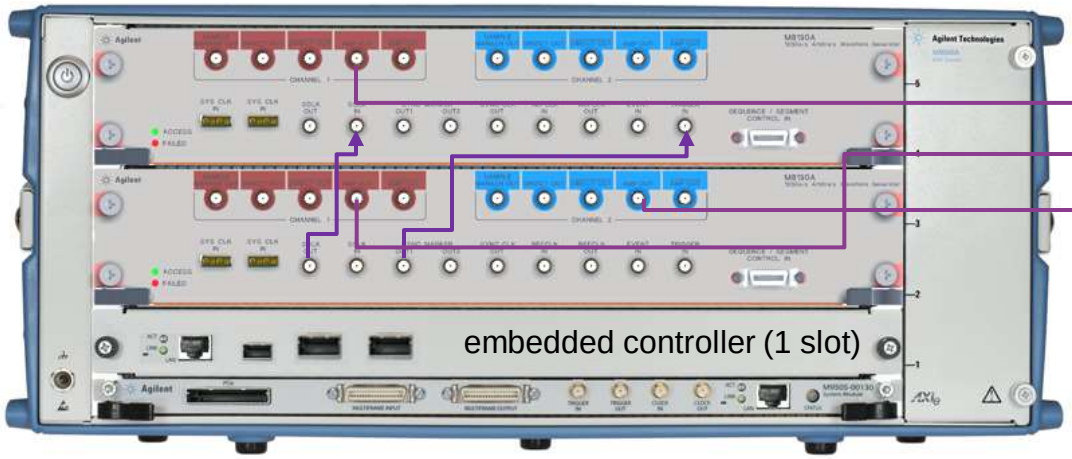
  - modular up to 4 channels enabling channel skew measurements
  - Very much comparable to N4903

- Very well suited for M-PHY
- Test Automation: SW Keysight N5990A option 165 & Bitifeye Frame Generator BIT-2060-0001-0
- How to address **C-PHY / D-PHY ?**
  - **We now integrate Keysight AWG modules substituting 8041/51A's NRZ PGs while still operating under a typical BERT use model**

Setup for C-PHY: M8190A, 5 Slot Frame, Embedded Controller

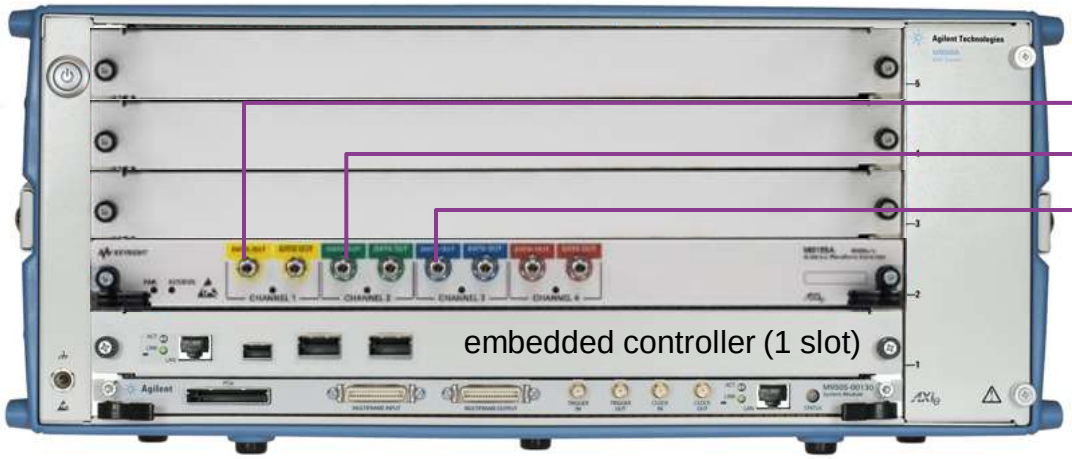


1-lane C-PHY DUT

Setup for C-PHY: M8195A, 5 Slot Frame, Embedded Controller

4X channel density (4 channels in 1 slot module vs 2 channels in 2 slot module)

Setup for C-PHY: M8195A, 5 Slot Frame, Embedded Controller



1-lane C-PHY DUT

Alternative setup: M8195A, 2 slot frame, embedded Controller

1-lane C-PHY DUT

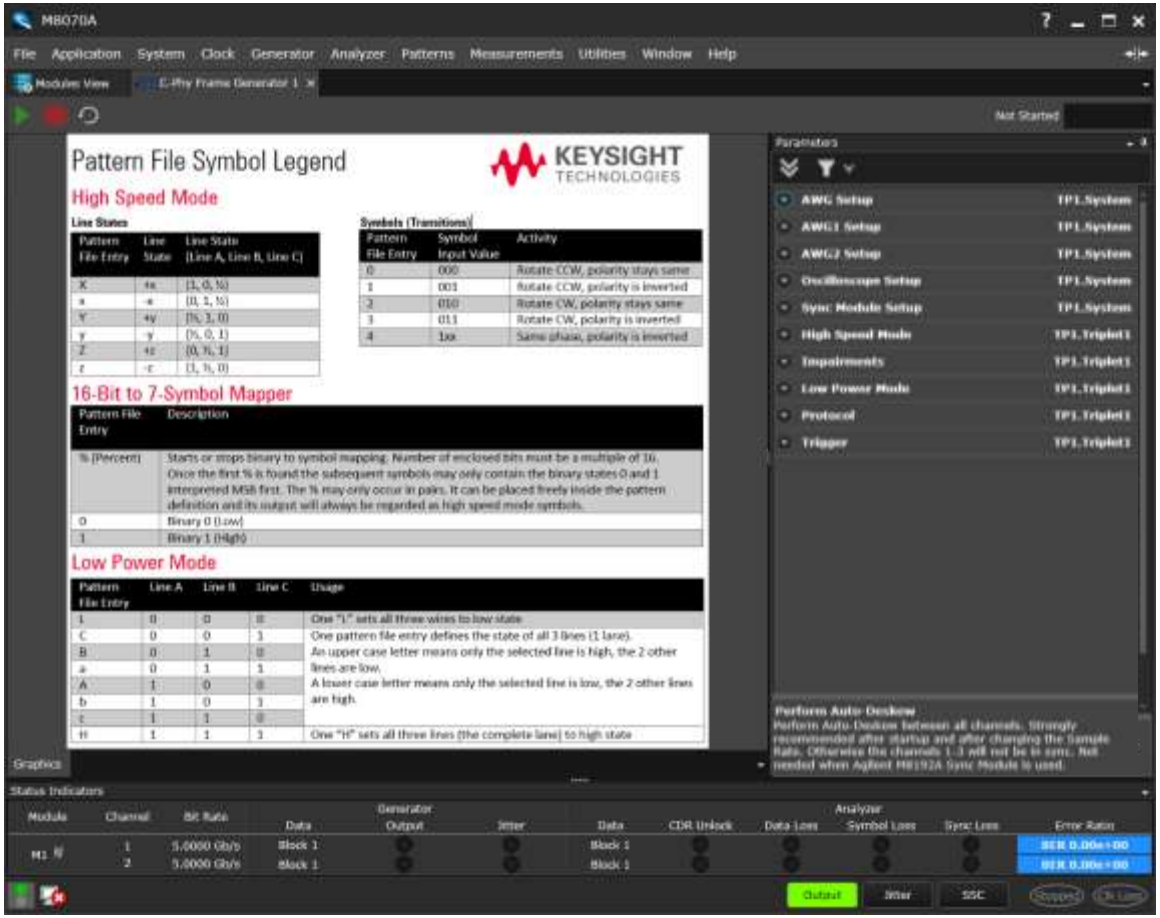
Setup for C-PHY: M8195A, 5 Slot Frame, Embedded Controller

3 AWG modules capable of driving up to 12 wires (up to 4x C-PHY lanes)

required synchronization module not shown

Realization of "C-PHY-GUI" within M8070A SW

C-PHY Frame Generator integrated M8070 SW / M8000 BER solution



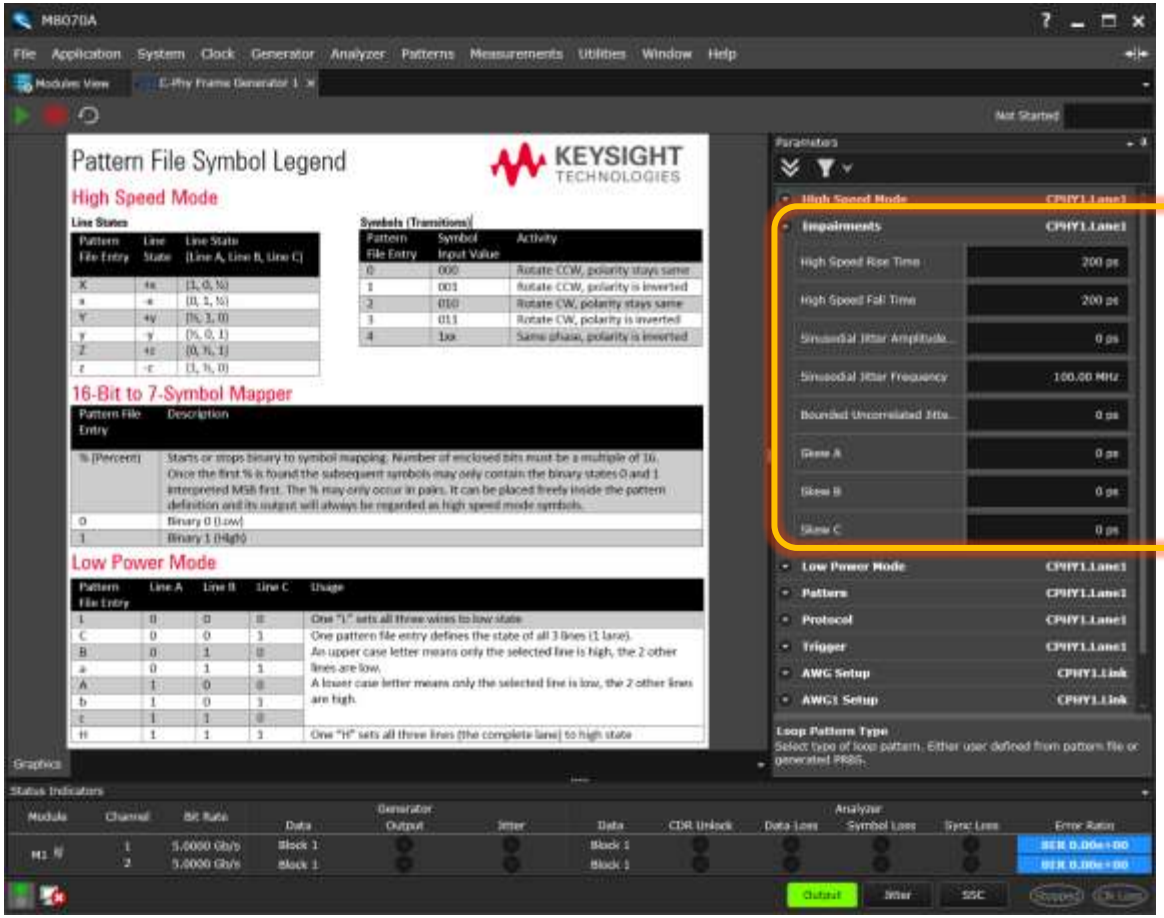
Definitions available for:

– Pattern & coding

– Low Power to High Speed mode transition

Realization of "C-PHY-GUI" within M8070A SW

C-PHY Frame Generator integrated M8070 SW / M8000 BER solution



Definitions available for:

– Pattern & coding

Parameter editor for Impairments

– Low Power to High Speed mode transition

Agilent / Keysight Solutions for MIPI RX PHY-test

2013 and before

M-PHY

J-BERT N4903B

D-PHY

ParBERT 81250

2013 2014 2015

Agilent / Keysight Solutions for MIPI RX PHY-test

2015: Complete Solutions

			M8000 family of BER test solutions
M-PHY	 J-BERT N4903B	 J-BERT M8020A	 J-BERT M8020A / M8070 / 85A
C-PHY		 AWG M8190A w/ M8085 special SW	 AWG M8195A / M8070 / 85A
D-PHY	 ParBERT 81250	AWG M8190A w/ MATLAB script	

2013 2014 2015

Agenda

- MIPI Overview, history and recent changes
- RX test: recap of methodology
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- Keysight test solutions M8000 based
- Summary, links, QA

Advantages of Keysight Solution

- All PHY-standards to be addressed from M8000 platform
- CTS-conformant test setup, characterization and test
- Simple, repeatable automated and unattended calibration and test execution using automation SW N5990A opt 165
- Variety of error counting methods from BERT ED to IBER reader interface supported by N5990A test automation SW
- For M-PHY: direct match between J-BERT N4903B / M8020A capabilities and M-PHY required jitter cocktail
- Flexible Jitter generation to characterize RX beyond specifications to determine margins
- BitifEye Frame Generator SW BIT-2060-0001-0 allowing to choose and mix LP and HS traffic as in real application and to place custom data hassle-free into compliant M-PHY bursts

Summary

We discussed

- Goals of MIPI alliance
- Recent development and reasoning of PHY-layer standards
- Important capabilities and aspects of RX testing of different PHY-layers
- Introduction to C-PHY
- Rx test requirements, current and future keysight solutions

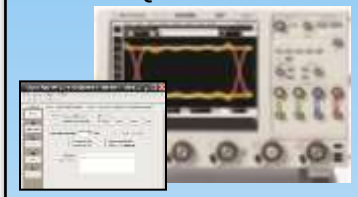
Literature

- www.keysight.com/find/J-BERT
- www.keysight.com/find/M8020A
- www.keysight.com/find/mipi-mphy
- http://mipi.org/
- Application Brief M8020: http://cp.literature.agilent.com/litweb/pdf/5991-3959EN.pdf
- Application note: http://cp.literature.agilent.com/litweb/pdf/5991-2848EN.pdf
- Recorded Webinar, M-PHY: http://techonline.com/electrical-engineers/education-training/webinars/4416663/Demystify-MIPI-M-PHY-Receiver-Physical-Layer-Test-Challenges
- Data sheet M8020A: http://literature.cdn.keysight.com/litweb/pdf/5991-3647EN.pdf
- Data sheet N5990A : http://literature.cdn.keysight.com/litweb/pdf/5989-5483EN.pdf

Keysight MIPI Total Solution Coverage

Transmitter Characterization

DSAQ93204A Infiniium



U7238B D-PHY, U7249B M-PHY, N5467B C-PHY UDA InfiniiMax Probes

Switch matrix
N5465A InfiniiSim
N2809A PrecisionProbe

Industry's highest analog bandwidth, lowest noise floor/sensitivity, jitter measurement floor with unique cable/probe correction

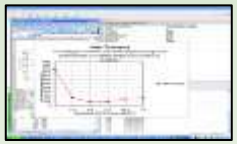
Receiver Characterization

N4903B/M8020A JBERT

M8190 AWG

81250A ParBERT

N5990A Automated characterization



Highest precision jitter lab source with automated compliance software for accurate, efficient, and consistent measurement

Impedance/Return Loss Validation

E5071C ENA Option TDR

DCA 86100D Wideband sampling oscilloscope

N1055A TDR/TDT

54754A TDR/TDT

Precision impedance measurements and S-Parameter capability

Protocol Stimulus and Analysis

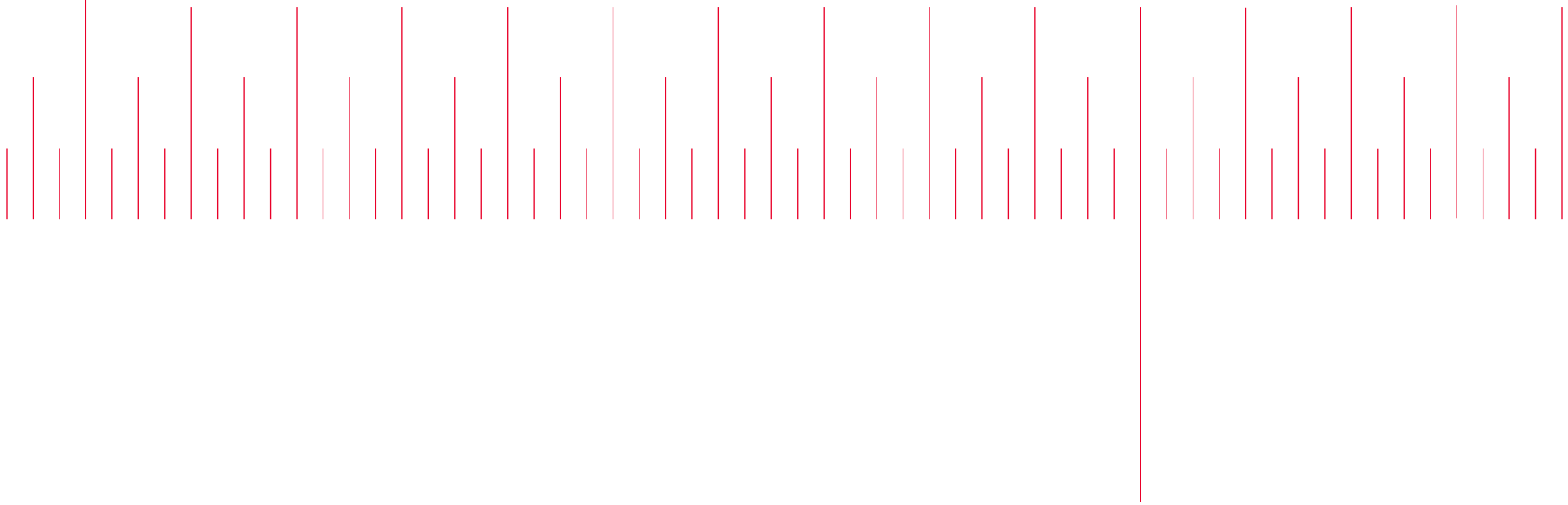
U4421A D-PHY CSI-2 / DSI Analyzer and Exerciser
U4431A M-PHY Analyzer (UFS, UniPro, CSI-3, SSIC, M-PCIe)

Scope Protocol Decoder
N8802A CSI-2 / DSI
N8807A DigRF v4
N8808A UniPro
N8818A UFS
N8809A LLI
N8819A SSIC
N8820A CSI-3
N8824A RFFE

Fast upload and display, accurate capture, intuitive GUI and customizable hardware. Correlate physical and protocol layer.

KEYSIGHT TECHNOLOGIES

The End



KEYSIGHT TECHNOLOGIES

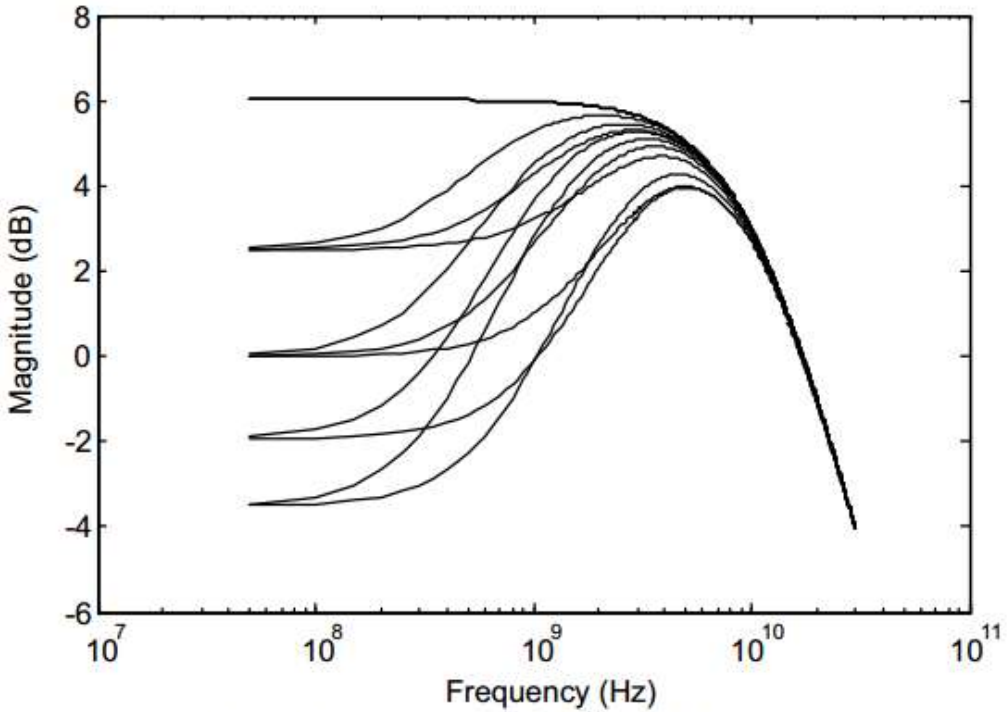
Thank you!
Questions?

Contact:
Michael_Fleischer-Reumann@keysight.com
Phone: +49 7031 464 8420

Three PHYs “at a glance”

Characteristic	M-PHY v3.1	D-PHY v1.2	C-PHY v1.0
Primary use case	Performance driven, bidirectional packet/network oriented interface	Efficient unidirectional streaming interface, with low speed in-band reverse channel	Efficient unidirectional streaming interface, with low speed in-band reverse channel
HS clocking method	Embedded Clock	DDR Source-Sync Clock	Embedded Clock
Channel compensation	Equalization	Data skew control relative to clock	Encoding to reduce data toggle rate
Minimum configuration and pins	1 lane per direction, dual-simplex, 2 pins each (4)	1 lane plus clock, simplex, 4 pins	1 lane (trio), simplex, 3 pins
Maximum transmitter swing amplitude	SA: 250mV (peak) LA: 500mV (peak)	LP: 1300mV (peak) HS: 360mV (peak)	LP: 1300mV (peak) HS: 425mV (peak)
Data rate per lane (HS)	HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s (Line rates are 8b10b encoded)	80 Mbps to ~2.5 Gbps (aggregate)	80 Mbps to 2.5 sym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)
Data rate per lane (LS)	10kbps – 600 Mbps	< 10 Mbps	< 10 Mbps
Bandwidth per Port (3 or 4 lanes)	~ 4.0 – 18.6 Gb/s (aggregate BW)	Max ~10 Gbps per 4-lane port (aggregate)	Max ~ 17.1 Gbps per 3-lane port (aggregate)
Typical pins per Port (3 or 4 lanes)	10 (4 lanes TX, 1 lane RX)	10 (4 lanes, 1 lane clock)	9 (3 lanes)

Reference CTLE



$$H(s) = \frac{A_{DC}\omega_{P1}\omega_{P2}}{\omega_z}\frac{s+\omega_z}{(s+\omega_{P1})(s+\omega_{P2})}$$

Figure 42 Examples of CTLE Frequency Responses

HS-RX Reference Equalizer					
A_{AC}			6	dB	CTLE AC gain
A_{DC}	-4		6	dB	CTLE DC gain
f_Z	0.4		1.2	GHz	CTLE zero frequency
f_{P2}			10	GHz	CTLE second pole frequency

KEYSIGHT TECHNOLOGIES

Reference CTLE and DFE

The DFE characteristics are defined by the following equation:

$$y_k = x_k - V_{DFE\_RX}$$
$$y_k = x_k - d_1 sgn(y_{k-1}) \quad \text{(Equation 25)}$$

where y_k is the output voltage signal of the DFE, x_k is the input voltage signal to the DFE, V_{DFE_RX} is the DFE feedback voltage signal, k is the sample index of a data bit and d_1 is the DFE feedback coefficient. ***Figure 43*** illustrates the Reference DFE diagram.

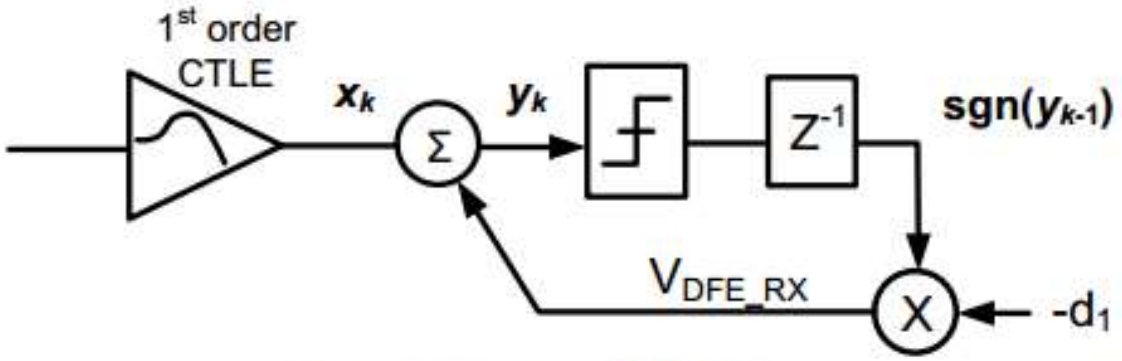


Figure 43 Reference DFE Diagram

HS-RX Reference Equalizer					
V_{DFE_RX}	-60		60	mV	DFE feedback voltage signal