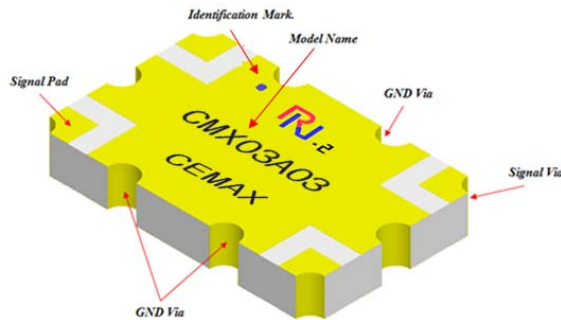


## 1. Description

### . Part number: CMX03A03



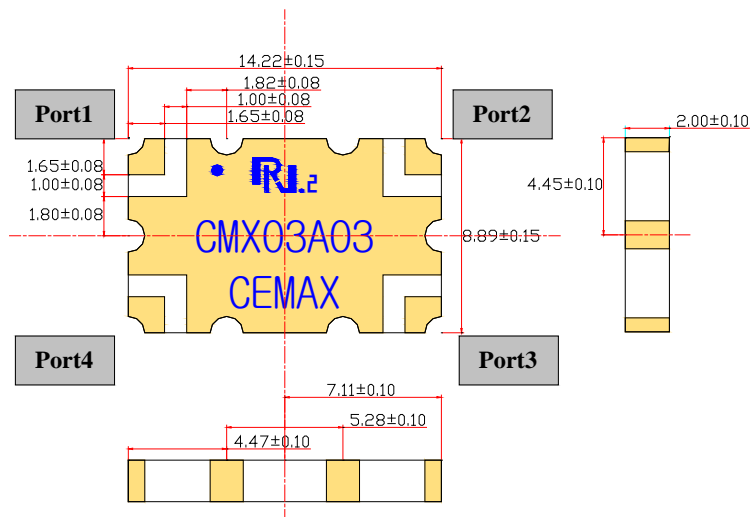
### . Features

- Surface mount type
- **RoHS** Compliance (Pb Free)
- LTCC base (Er = 6)
- Low loss Silver (Ag) Conductor
- Gold (Au) plating finish

## 2. Electrical Specification

Freq. (MHz)	Amplitude Balance max (dB)	Isolation min (dB)	Insertion Loss max (dB)	VSWR Max	Phase (degrees)
250 – 470	± 0.80	-20	-0.30	1.20	90 ± 3
250 – 300	± 0.50	-25	-0.20	1.10	90 ± 2
300 – 450	± 0.50	-20	-0.25	1.20	90 ± 3
450 – 470	± 0.80	-20	-0.30	1.20	90 ± 3
<b>Power Capacity</b>					
Avg. (Watt)		<b>Characteristic Imp.</b>	<b>Operating Temp.</b>		
200		(ohm)	(°C)		
		50	-55 to +125		

## 3. Mechanical Specification



[Unit = mm]

#### 4. Schematic Drawing

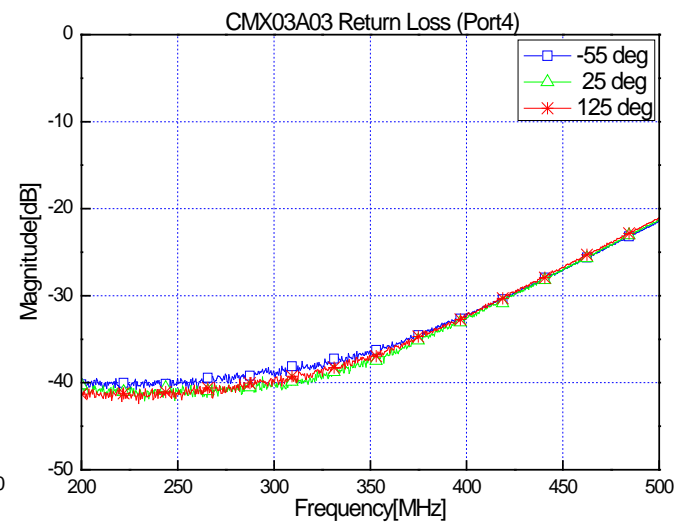
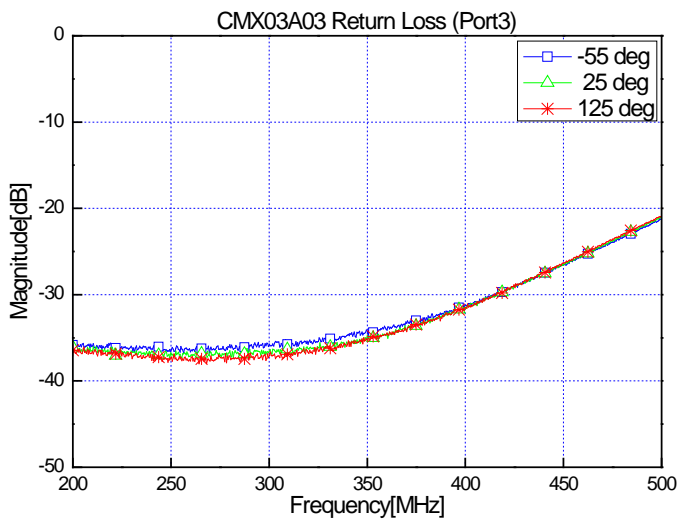
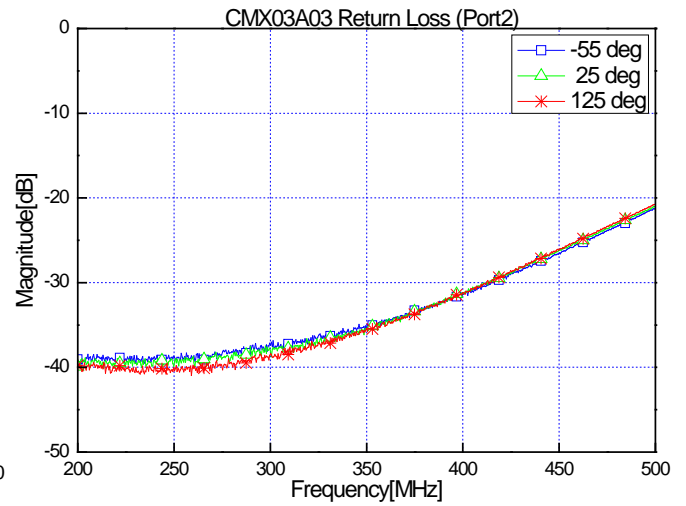
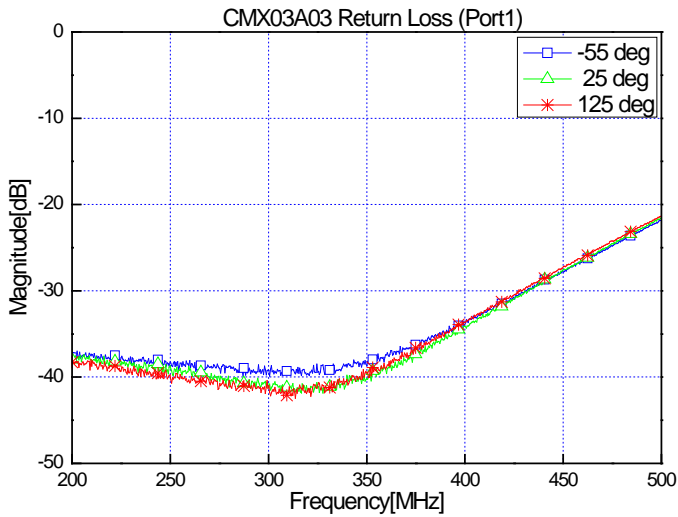


#### 5. Port Configuration

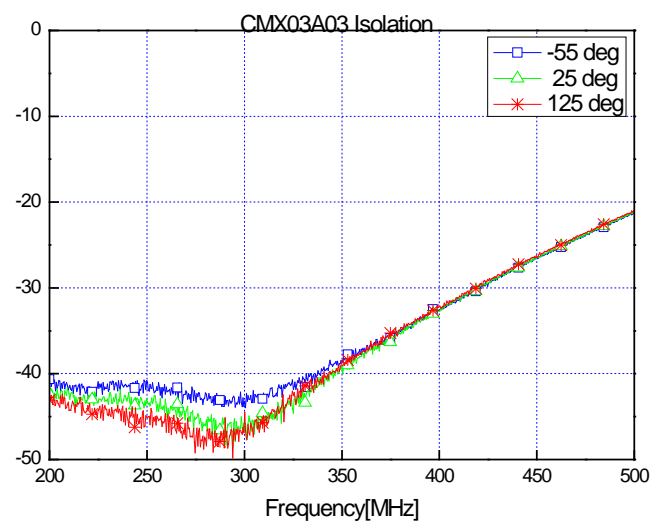
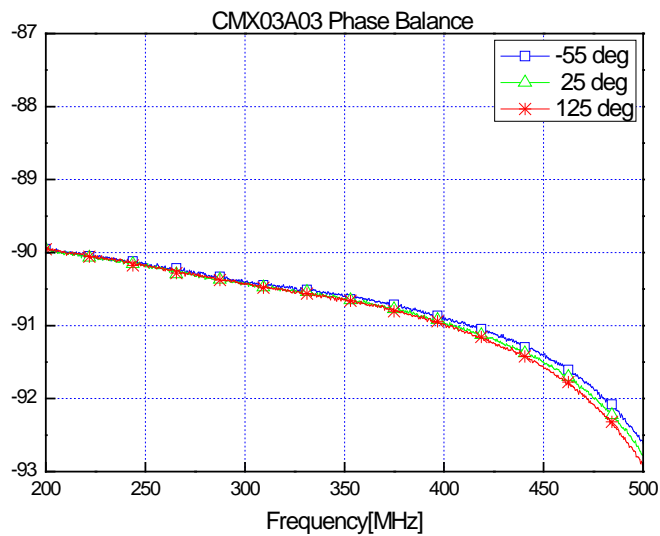
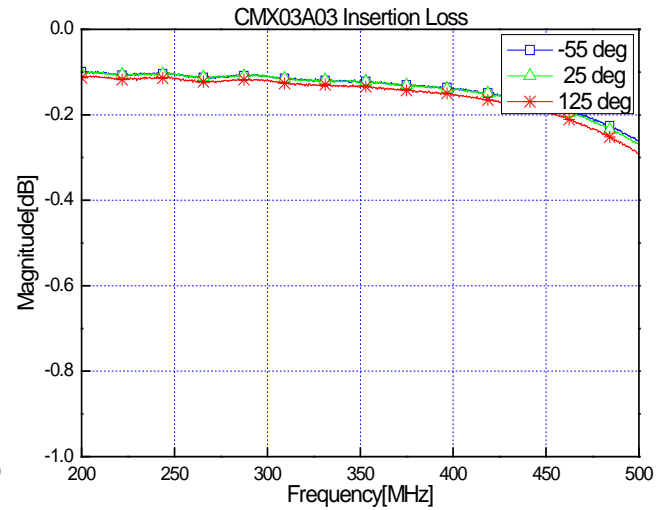
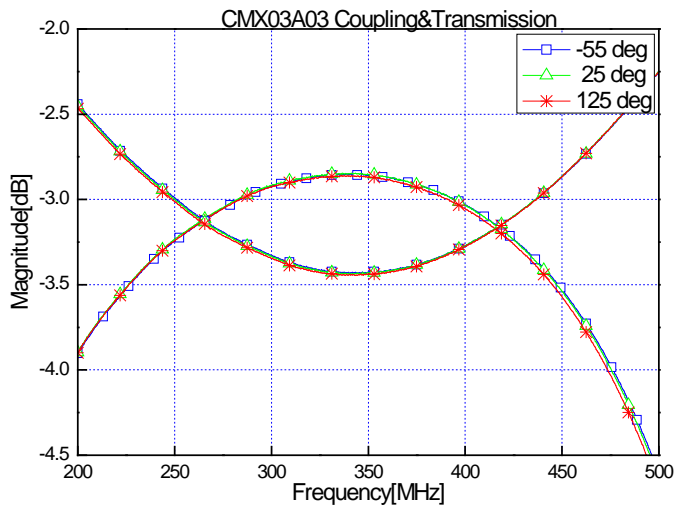
Configuration	Port 1	Port 2	Port 3	Port 4
Case 1.	Input	Isolated	Output -3dB, -90°	Coupling -3dB, 0°
Case 2.	Isolated	Input	Coupling -3dB, 0°	Output -3dB, -90°
Case 3.	Output -3dB, -90°	Coupling -3dB, 0°	Input	Isolated
Case 4.	Coupling -3dB, 0°	Output -3dB, -90°	Isolated	Input

\* Once Port 1 is determined, the other three ports are defined automatically.

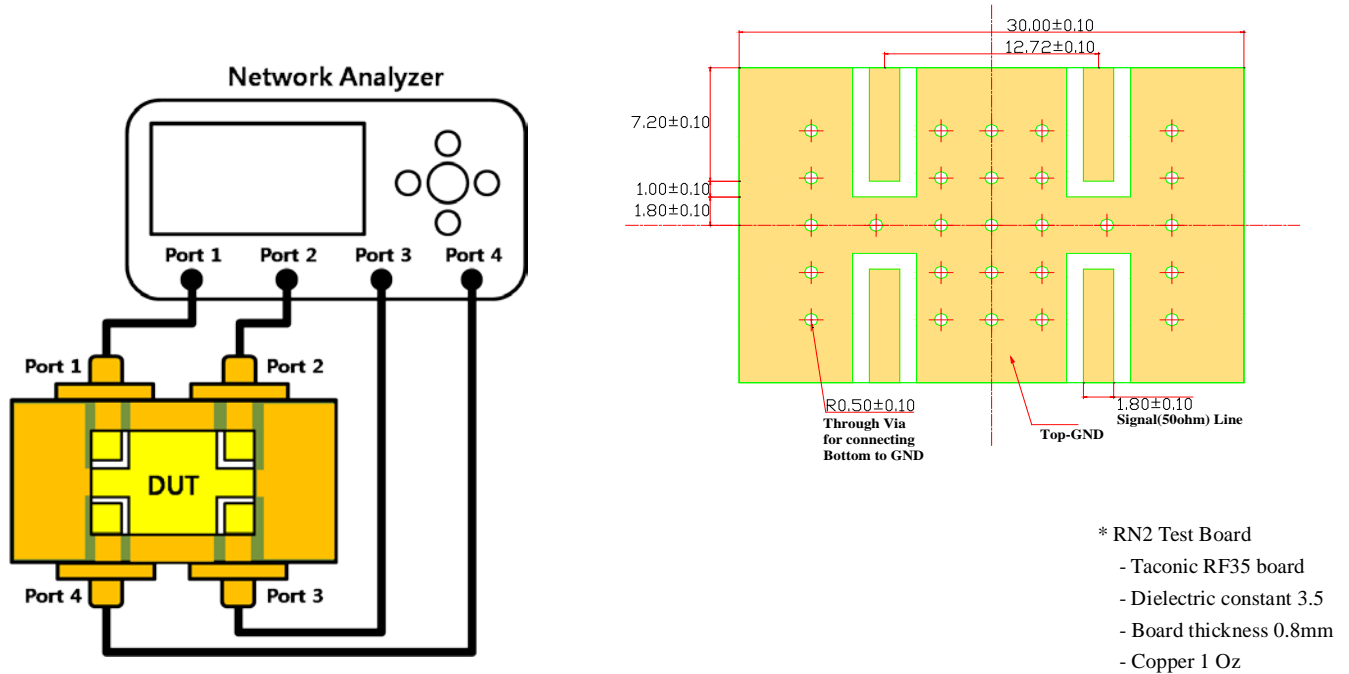
## 6. Operating Temperature Curve (1)



## 7. Operating Temperature Curve (2)



## 8. Test Method



To recognize the specified performance of the part, it has to be evaluated on the RN2 test board shown above.

1. Calibrate the network analyzer
2. Measure the data of **Return Loss** through Port 1 to Port 1 (S11)
3. Measure the data of **Coupling** through Port 1 to Port 4 (S41)
4. Measure the data of **Transmission** through Port 1 to Port 3 (S31)
5. Measure the data of **Isolation** through Port 1 to Port 2 (S21)
6. Calculate **Insertion Loss** and **Amplitude Balance** in function of the below mathematical formula.

Parameter	Mathematical formula
Insertion Loss (dB)	$10 \cdot \log \left( \frac{P_{in}}{P_{cou} + P_{out}} \right)$
Amplitude Balance (dB)	$10 \cdot \log \left( \frac{P_{cou}}{\frac{P_{cou} + P_{out}}{2}} \right)$

## 9. Recommended PCB layout and Solder mask pattern

