BMT332

700-2400 MHz 2W High Linearity 5V 2-Stage Power Amplifier

Device Features

- +5V/680mA at operating bias condition
- Gain = 27.3 dB @ 1850 MHz
- P1dB = 33.1 dBm @ 1850MHz
- LTE 10M ACLR = 23.5dBm Output Power at -50dBc @ 1850MHz
- Intergrated interstage matching
- Green/RoHS2-compliant QFN5x5 SMT package

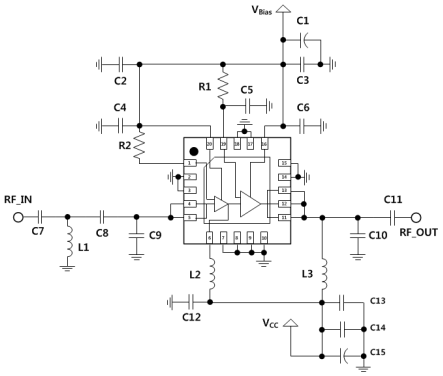
Product Description

The BMT332 is a high dynamic range two-stage power amplifier housed in RoHS2 compliant 20 pin, 5x5mm QFN package. The BMT332 uses a high reliability InGaP/GaAs HBT process technology. The BMT332 is designed for use where high linearity and gain is required. The BMT332 is able to deliver over 23 dBm output power from 700 to 2400MHz while maintaining superior ACLR performance with a few external matching components. All devices are 100% RF/DC screened.

Applications

- Base station /Repeaters Infrastructure
- Commercial/Industrial/Military wireless system
- LTE / WCDMA /CDMA Wireless Infrastructure

Application Circuits



*external matching circuit: refer to the page 4 to 19.

Typical Performance[1]

Parameter	Frequency						Unit
	850	1750	1850	1960	2140	2350	MHz
Gain	33.5	28.0	27.3	26.7	26.0	24.0	dB
S11	-18.0	-30.0	-30.0	-26.0	-17.0	-17.0	dB
S22	-14.5	-11.5	-11.5	-12.0	-11.0	-12.5	dB
OIP3[2]	50.0	50.0	49.0	49.0	47.5	47.5	dBm
P1dB	33.6	33.2	33.1	33.1	33.2	33.1	dBm
LTE 10M ACLR	23.4	23.4	23.5	23.2	23.8	23.2	dBm
WCDMA ACLR	23.5	23.7	23.7	23.5	24.0	23.5	dBm
Noise Figure	7.0	5.6	5.6	5.5	5.5	5.3	dB

[1] Device performance _ measured on a BeRex evaluation board at 25°C, 50 Ω .

[2] OIP3 _ measured on two tones with a output power 23dBm/ tone , F2-F1 = 1 MHz..

*ACLR Channel Power measured at -50dBc.

- LTE set-up: 3GPP LTE, FDD E-TM3.1, 10MHz BW, ±5MHz offset, PAR 9.75 @0.01% Prob.
- WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 9.78 at 0.01% Prob.

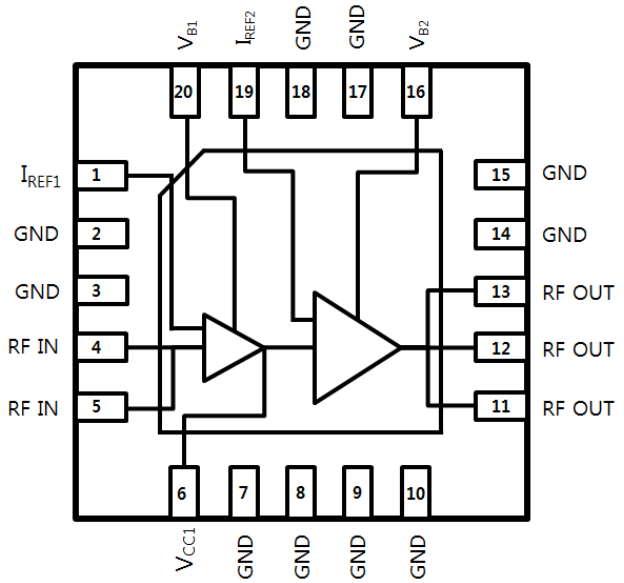
	Min.	Typical	Max.	Unit
Bandwidth	700		2400	MHz
I_{bias} @ ($I_{REF1\&2}$ + $I_{B1\&2}$)		33		mA
I_C @ (I_{C1} + I_{C2})		680		mA
V_{CC}/V_{Bias}		5.0		V
R_{TH}		7.9		°C/W

Absolute Maximum Ratings

Parameter	Rating	Unit
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +155	°C
Junction Temperature	+180	°C
Operating Voltage	+6	V
Supply Current	2000	mA
Input RF Power	23	dBm

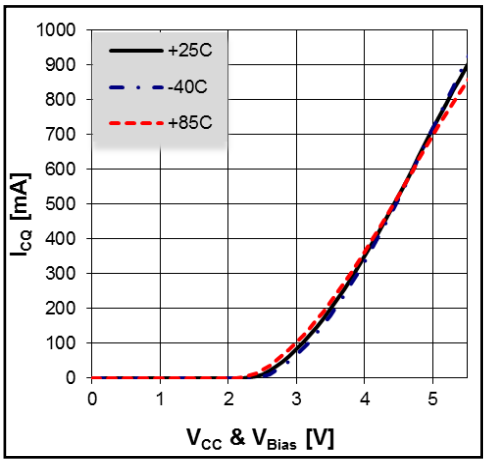
*Operation of this device above any of these parameters may result in permanent damage.

Pin Configuration



Pin No.	Label
1	I_{REF1}
4,5	RF IN
6	V_{CC1}
11,12,13	RF OUT/V_{CC2}
16	V_{B2}
19	I_{REF2}
20	V_{B1}
2,3,7,8,9,10,14, 15,17,18	GND
Backside Paddle	GND

V-I Characteristics



BeRex Evaluation Board

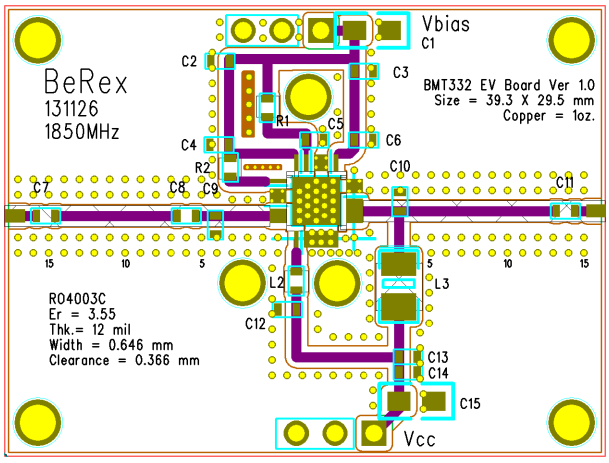
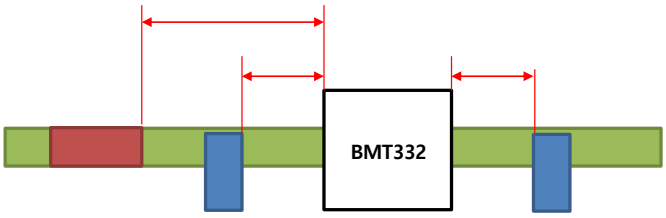
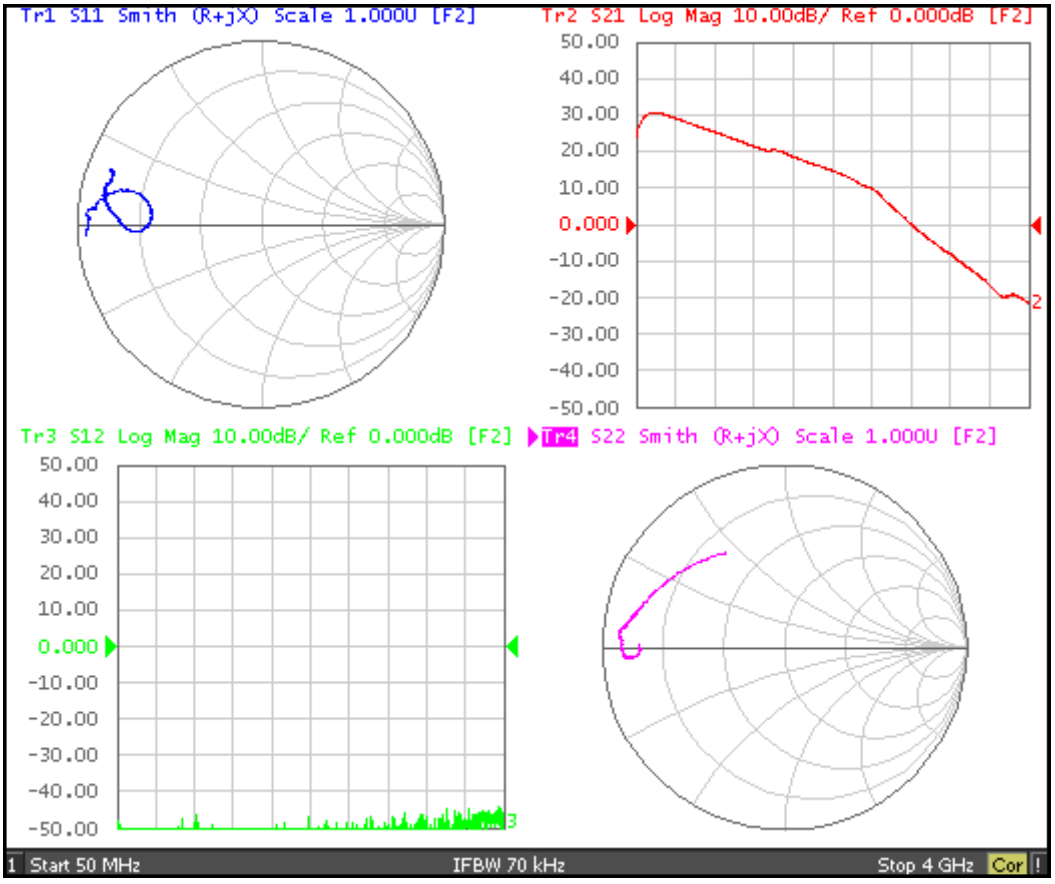


Figure about the reference position of components



Typical Device Data

S-parameters (V_{cc} & V_{Bias} =+5V, I_{cq}=680mA, T_a=25°C)



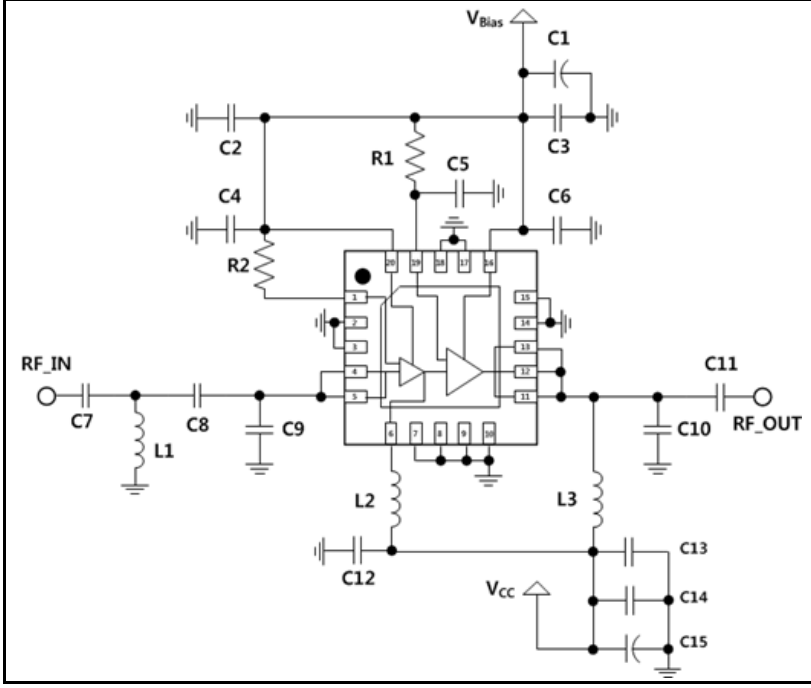
S-Parameter

(V_{cc} & $_{VBias}$ = 5.0V, I_{cq} = 680mA, T_a= 25 °C, calibrated to device leads)

Freq [MHz]	S11 [Mag]	S11 [Ang]	S21 [Mag]	S21 [Ang]	S12 [Mag]	S12 [Ang]	S22 [Mag]	S22 [Ang]
100	0.913	173.761	24.816	32.166	0.003	79.828	0.801	-178.428
500	0.619	171.121	26.921	-92.025	0.001	-44.058	0.869	-176.093
1000	0.701	-177.176	15.441	-178.364	0.002	59.383	0.879	-177.489
1500	0.784	177.684	10.073	107.582	0.001	119.430	0.895	179.724
2000	0.826	174.821	5.629	28.494	0.001	52.589	0.901	177.048
2500	0.877	167.581	2.533	-60.751	0.002	52.748	0.909	174.926
3000	0.856	164.082	0.614	-113.048	0.003	73.959	0.876	171.808
3500	0.863	160.570	0.198	-148.521	0.002	48.291	0.800	161.758
4000	0.868	160.252	0.085	179.517	0.004	44.770	0.607	121.233

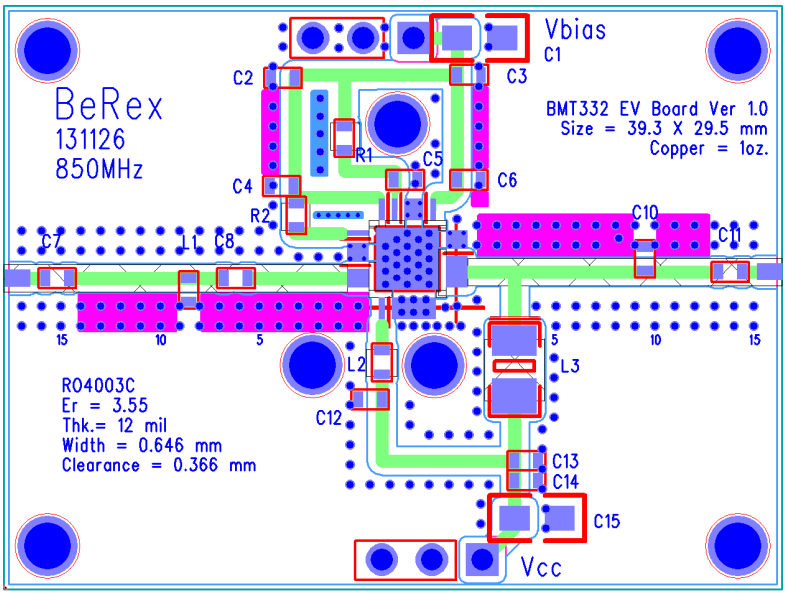
Application Circuit: 850 MHz

Schematic Diagram



BOM			Marks
C1	1206	10uF	Tantalum
C2	0603	N/A	
C3	0603	68pF	
C4	0603	1nF	
C5	0603	N/A	
C6	0603	3.3pF	
C7	0603	100pF	
C8	0603	5pF	
C9	0603	N/A	
C10	0603	10pF	High Q
C11	0603	100pF	
C12	0603	1uF	
C13	0603	100pF	
C14	0603	1nF	
C15	1206	10uF	Tantalum
L1	0603	5.6nH	
L2	0603	22nH	
L3	1008	22nH	Coil
R1	0603	100 Ω	±5%
R2	0603	270 Ω	±5%

PCB Diagram



Notice

Below information is subject to change as conditions of the substrate.

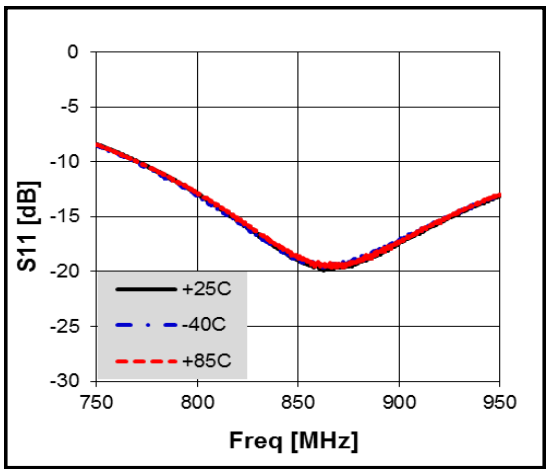
Reference	Object	Distance
Input pin	L1	8.0mm
Input pin	C8	5.3mm
Output pin	C10	9.0mm
Pin 16	C3	7.2mm
Pin 16	C6	2.0mm
Pin 20	C4	5.0mm

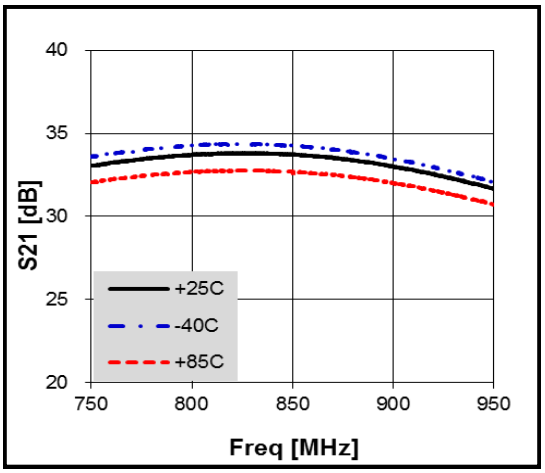
1. Pin 16 & 20 is used for Vce of the inner bias circuit. To eliminate bias line resonance you need above 10mm transmission line and adjust the position of C2, C3, C4 ,C5 and C6. Also you can adjust spectrum regrowth about bandwidth of signals which you want.

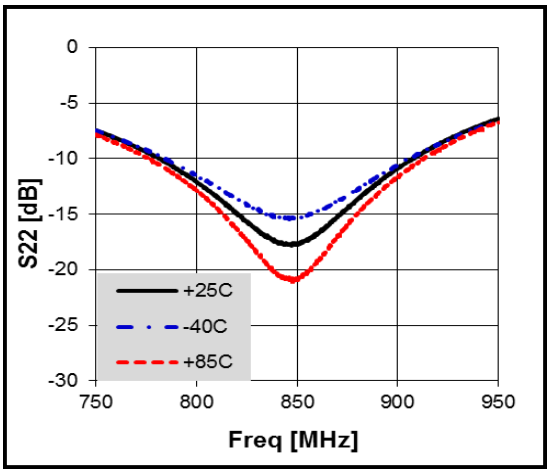
2. C10 : We recommend High-Q capacitor for better output power performance. In this document we used '10pF(251R14S100JV4, EIA 0603) of Johanson Technology.

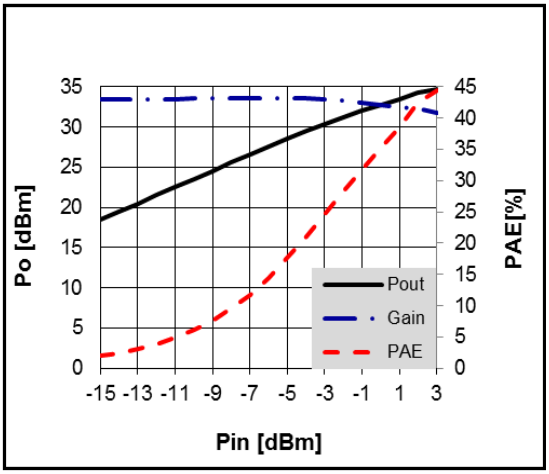
3. You could change C7 from 100 pF to 0 Ω or a line if you have other DC block front of BMT332.

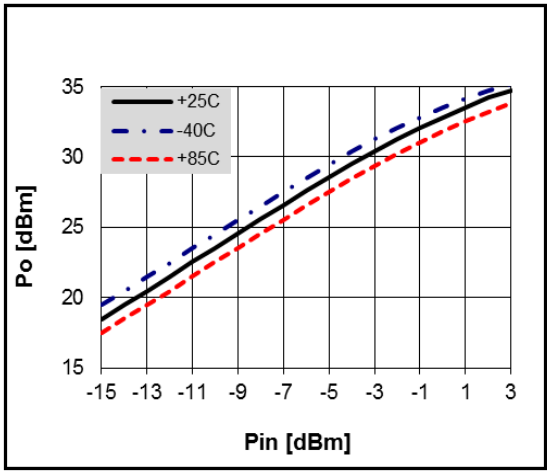
Typical Performance

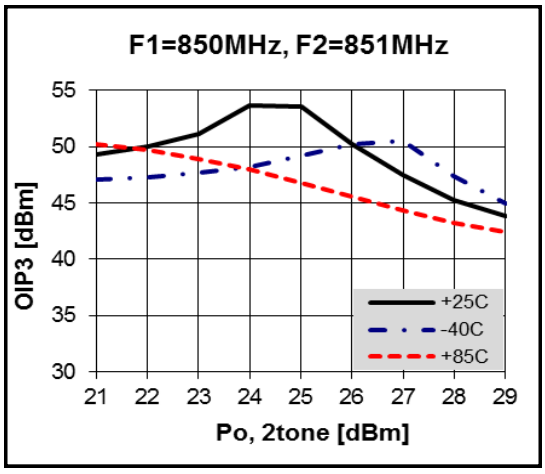




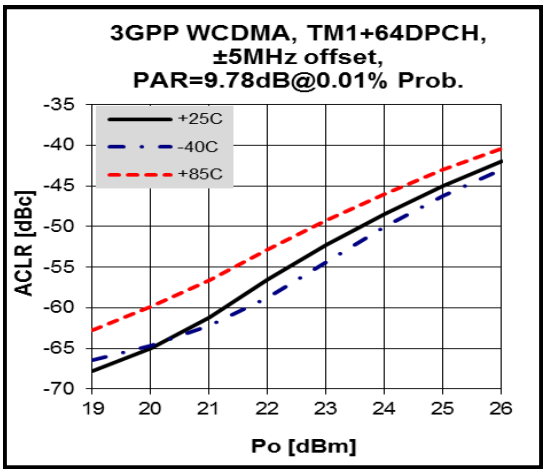




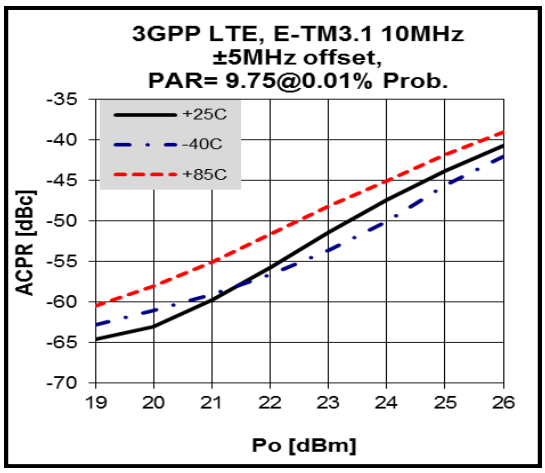




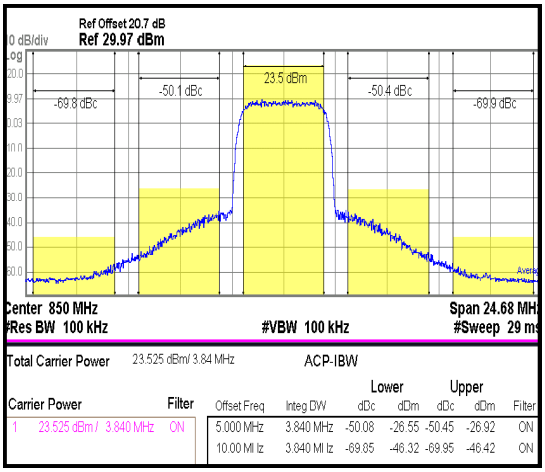
Typical Performance



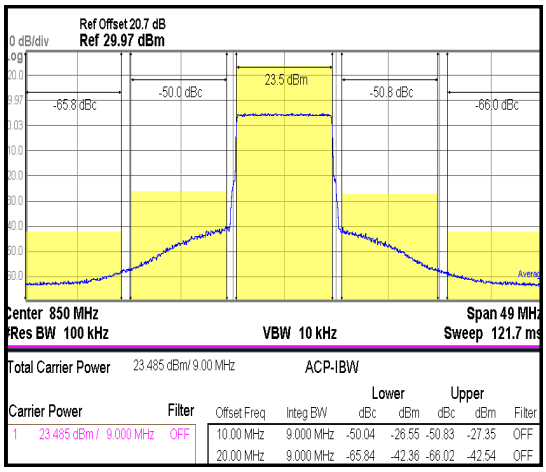
3GPP WCDMA TM1 +64DPCH 1FA



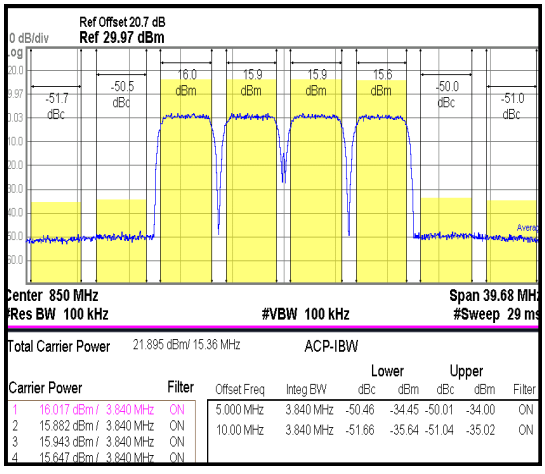
3GPP LTE E-TM3.1 10MHz



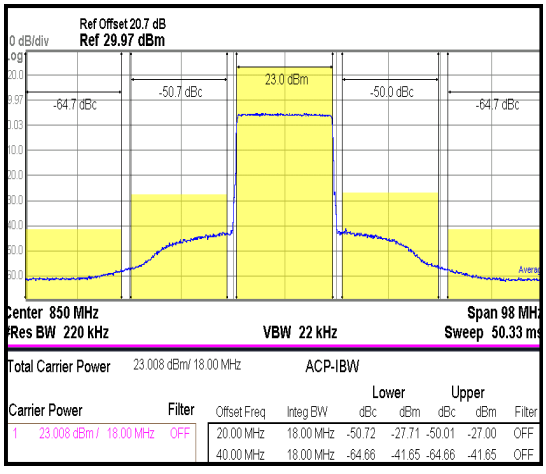
3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz

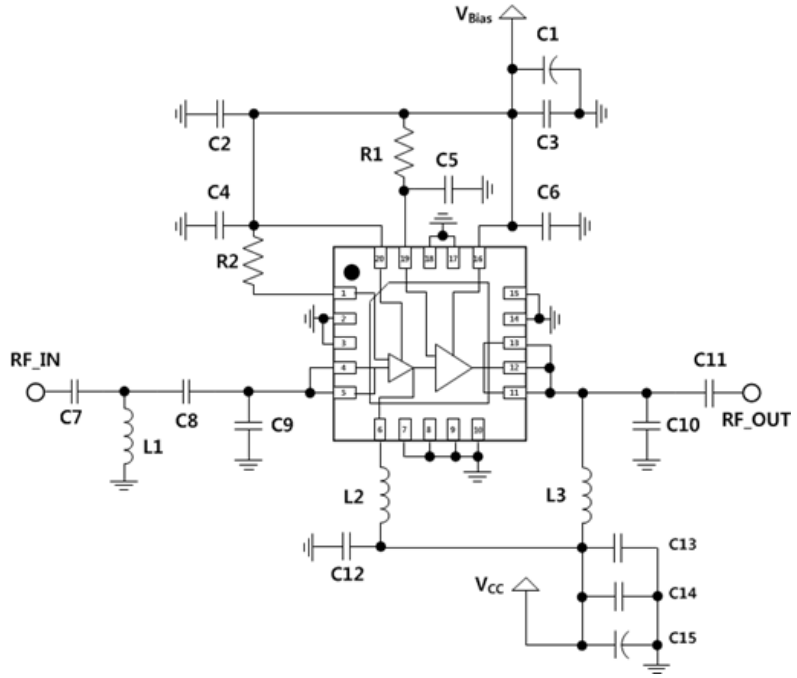


3GPP LTE E-TM3.1 20MHz



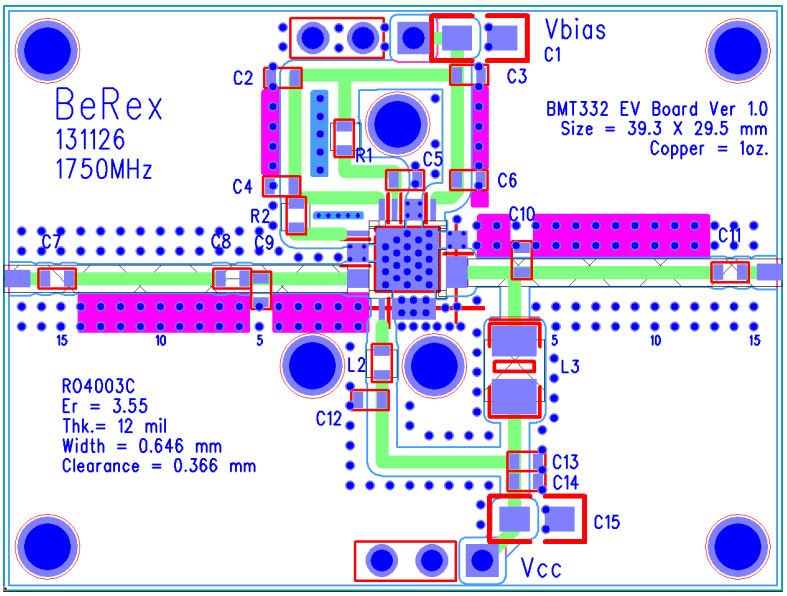
Application Circuit: 1750 MHz

Schematic Diagram



BOM			Marks
C1	1206	N/A	
C2	0603	1nF	
C3	0603	1nF	
C4	0603	N/A	
C5	0603	1nF	
C6	0603	2pF	
C7	0603	0 Ω	±5%
C8	0603	3.3pF	
C9	0603	2.7pF	
C10	0603	4.3pF	High Q
C11	0603	3.9pF	
C12	0603	1uF	
C13	0603	100pF	
C14	0603	1nF	
C15	1206	10uF	Tantalum
L1	0603	N/A	
L2	0603	12nH	
L3	1008	22nH	Coil
R1	0603	100 Ω	±5%
R2	0603	270 Ω	±5%

PCB Diagram



Notice

Below information is subject to change as conditions of the substrate.

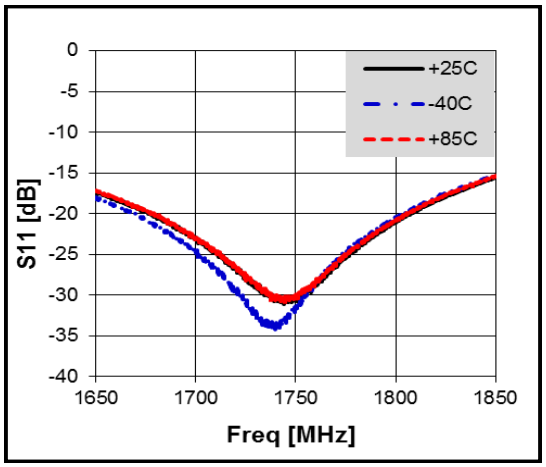
Reference	Object	Distance
Input pin	C8	5.5mm
Input pin	C9	4.4mm
Output pin	C10	2.8mm
Pin 16	C3	7.2mm
Pin 16	C6	2.0mm
Pin 19	C5	1.0mm
Pin 20	C2	10.6mm

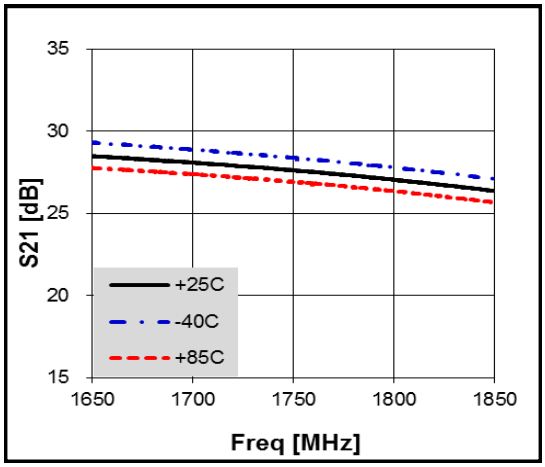
1. Pin 16 & 20 is used for Vce of the inner bias circuit. To eliminate bias line resonance you need above 10mm transmission line and adjust the position of C2, C3, C4 ,C5 and C6. Also you can adjust spectrum regrowth about bandwidth of signals which you want.

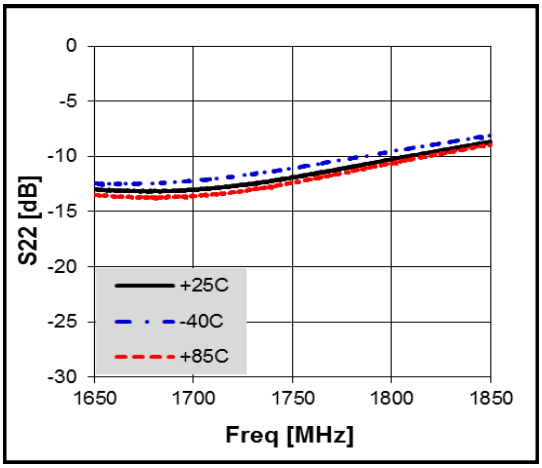
2. C10 : We recommend High-Q capacitor for better output power performance. In this document we used '4.3pF(251R14S4R3BV4, EIA 0603) of Johanson Technology.

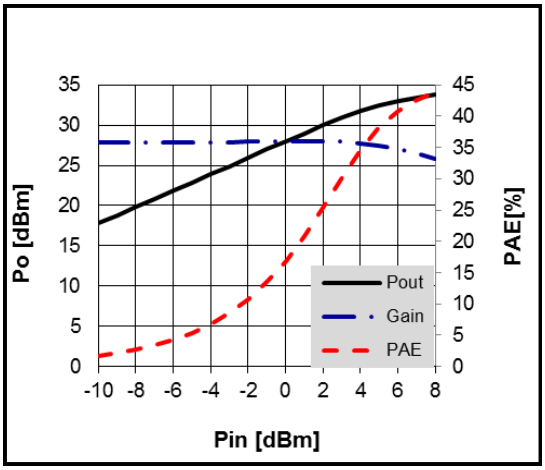
3.C7 : Non-critical 0 Ω.

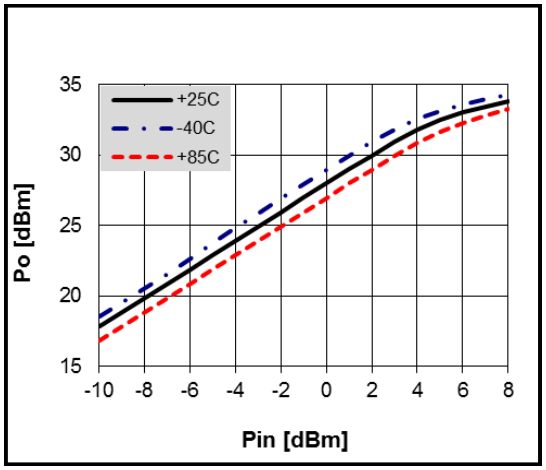
Typical Performance

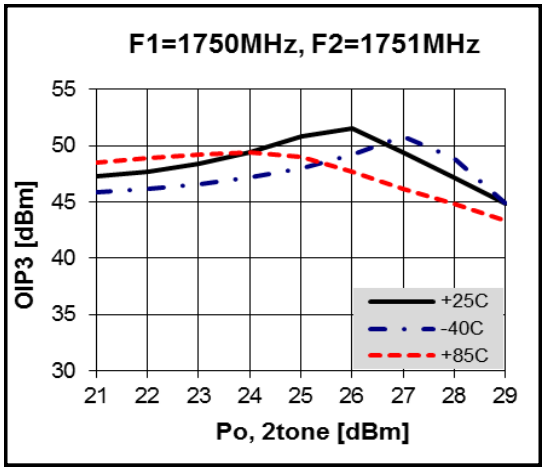




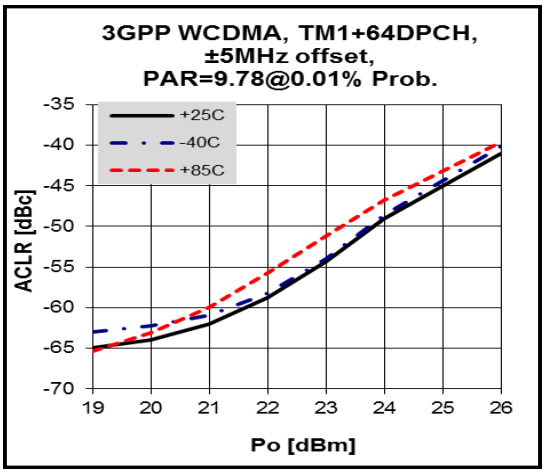




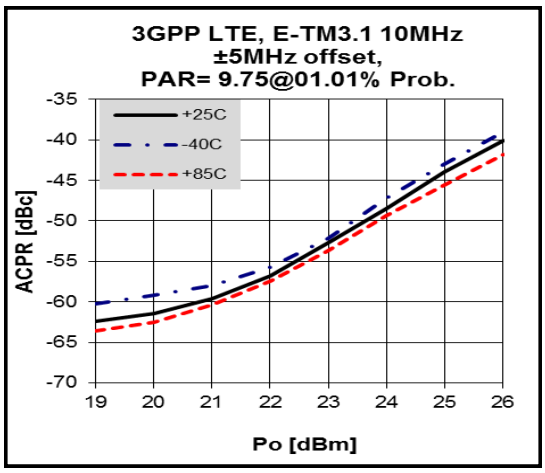




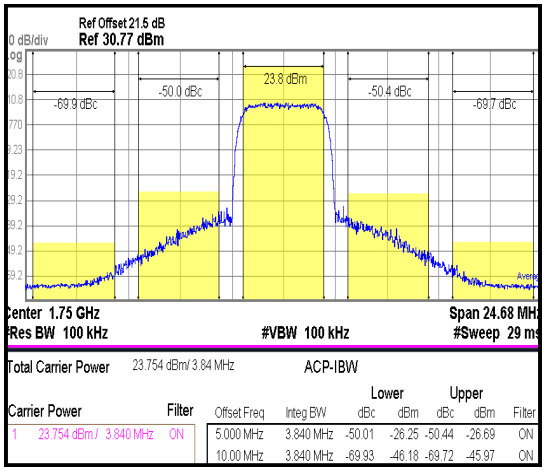
Typical Performance



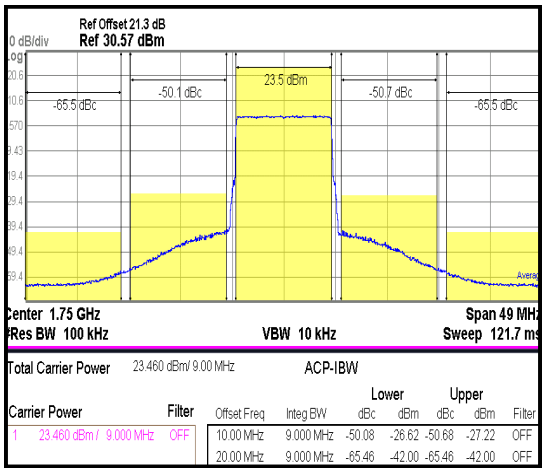
3GPP WCDMA TM1 +64DPCH 1FA



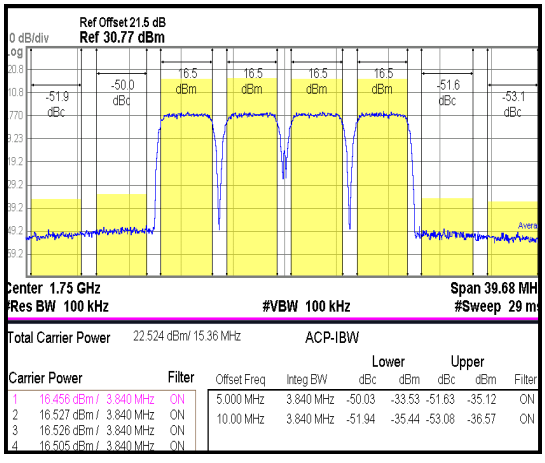
3GPP LTE E-TM3.1 10MHz

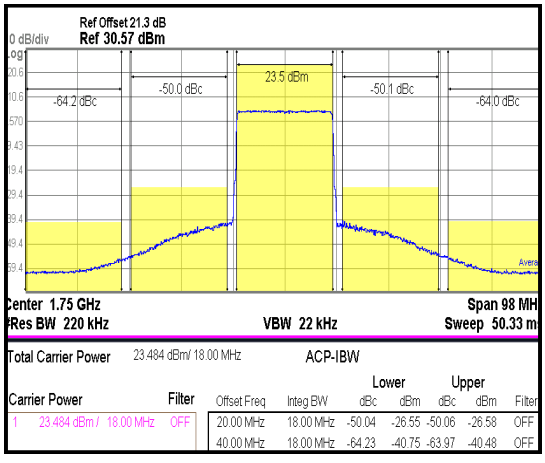


3GPP WCDMA TM1 +64DPCH 4FA



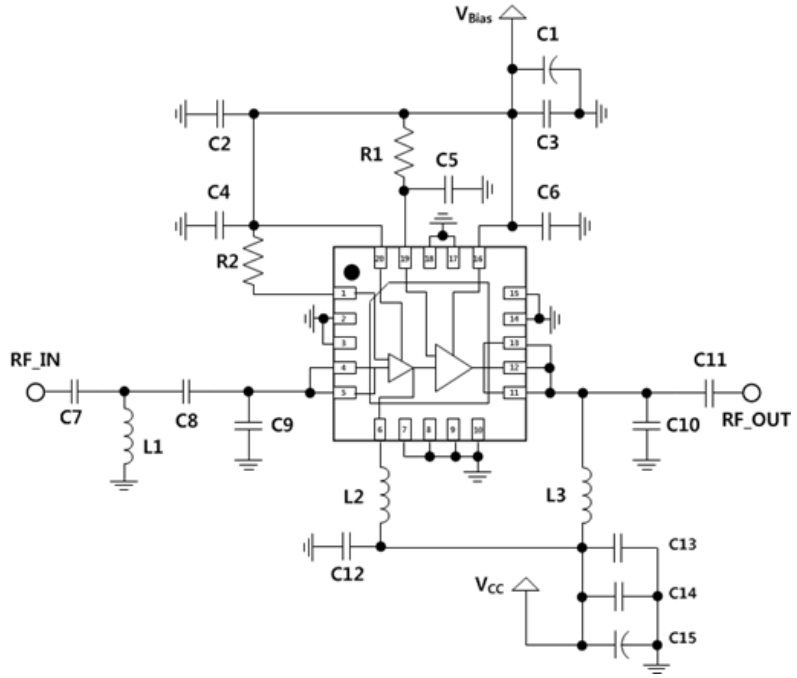
3GPP LTE E-TM3.1 20MHz





Application Circuit: 1850 MHz

Schematic Diagram



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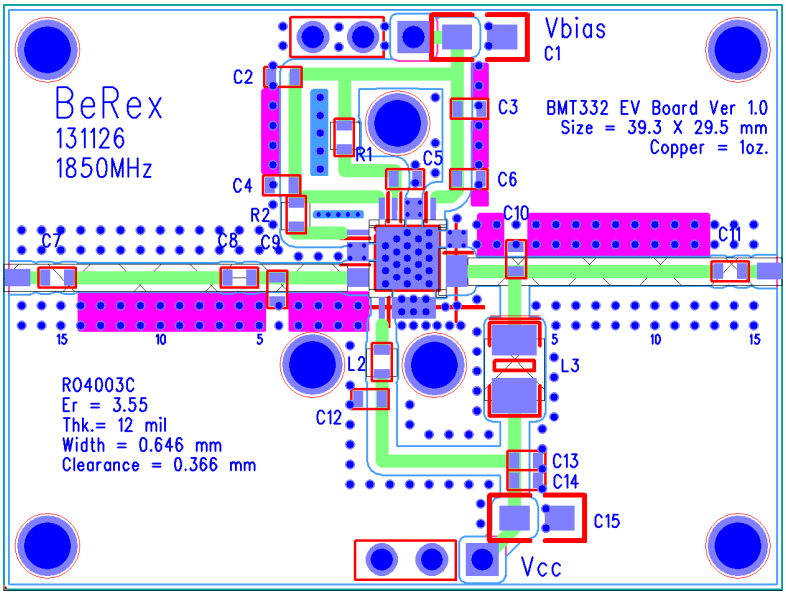
C1	1206	N/A	
C2	0603	1nF	
C3	0603	1nF	
C4	0603	N/A	
C5	0603	1nF	
C6	0603	3pF	
C7	0603	0 Ω	±5%
C8	0603	3.3pF	
C9	0603	2.7pF	
C10	0603	4.3pF	High Q
C11	0603	3.9pF	
C12	0603	1uF	
C13	0603	100pF	
C14	0603	1nF	
C15	1206	10uF	Tantalum
L1	0603	N/A	
L2	0603	12nH	
L3	1008	12nH	Coil
R1	0603	100 Ω	±5%
R2	0603	270 Ω	±5%

PCB Diagram



Notice

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Reference	Object	Distance
Input pin	C8	5.0mm
Input pin	C9	3.5mm
Output pin	C10	2.5mm
Pin 16	C3	5.5mm
Pin 16	C6	2.0mm
Pin 19	C5	1.0mm
Pin 20	C2	10.6mm

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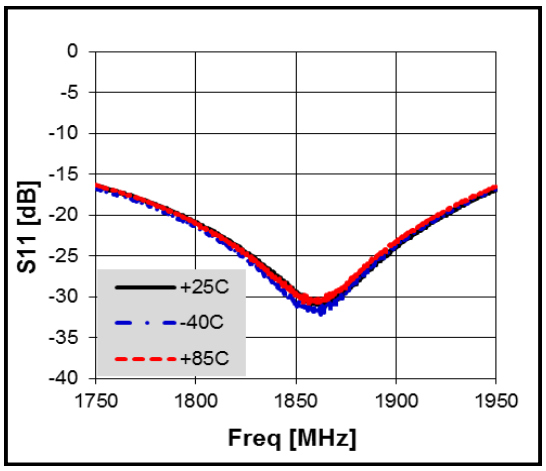
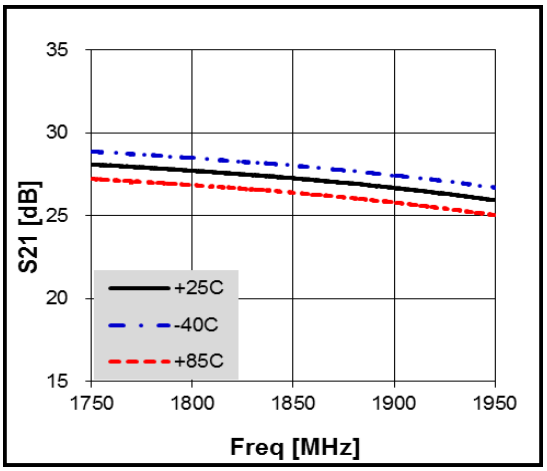
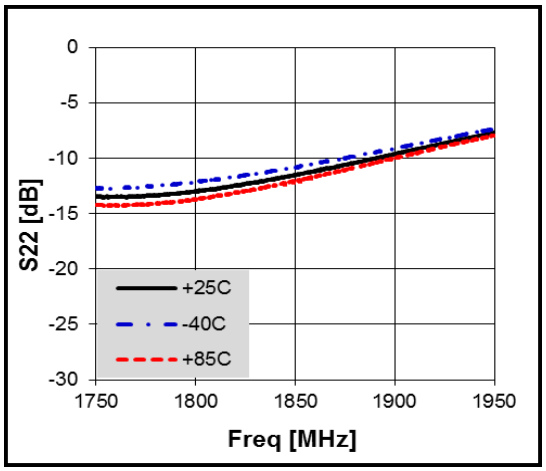
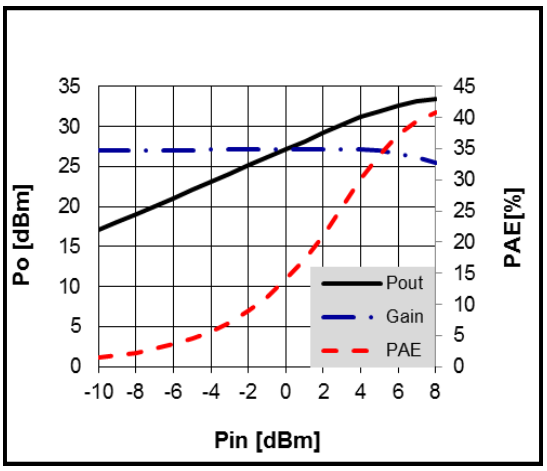
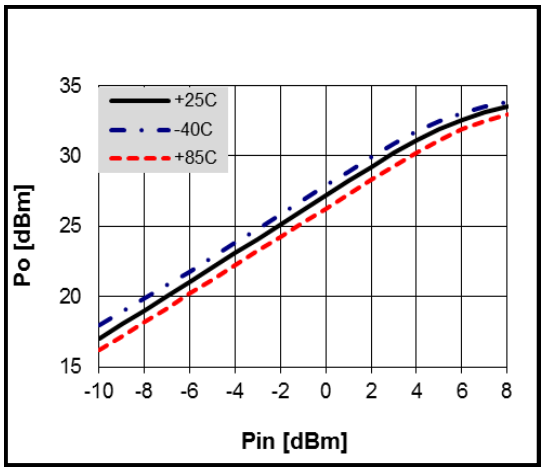
Typical Performance

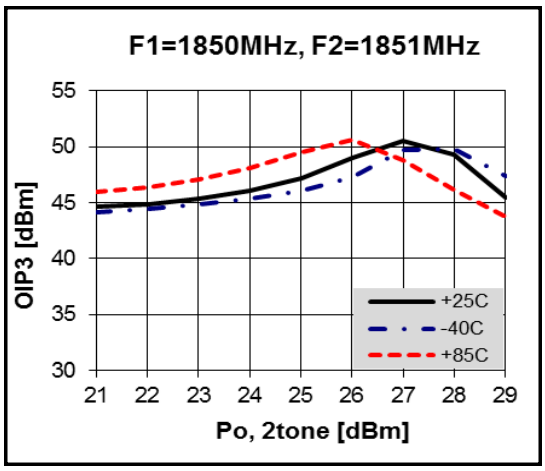




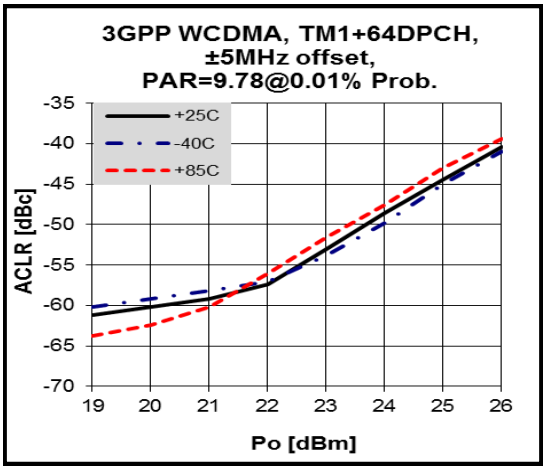




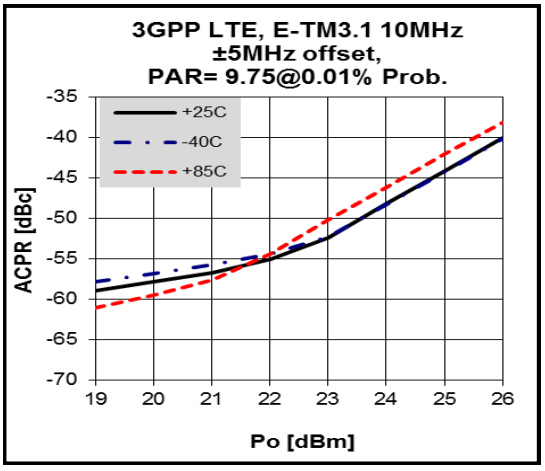




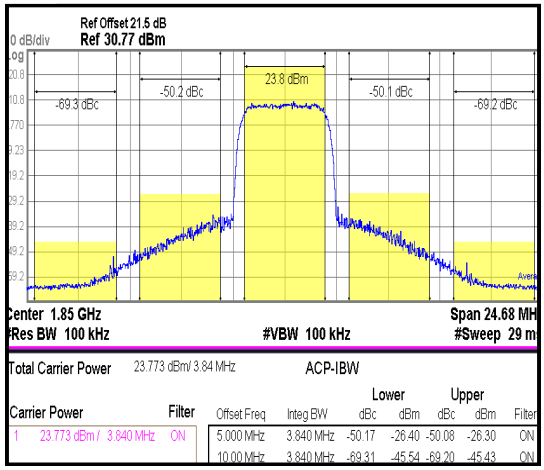
Typical Performance



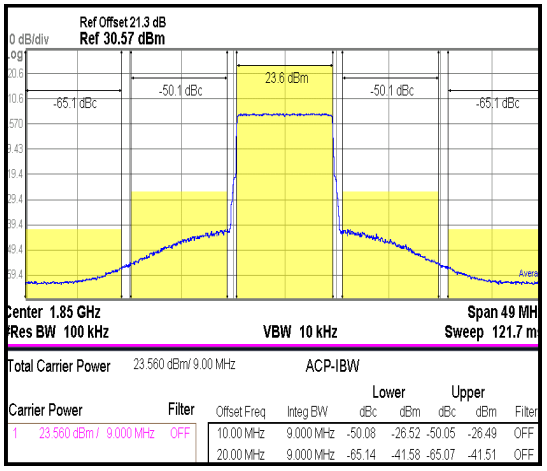
3GPP WCDMA TM1 +64DPCH 1FA



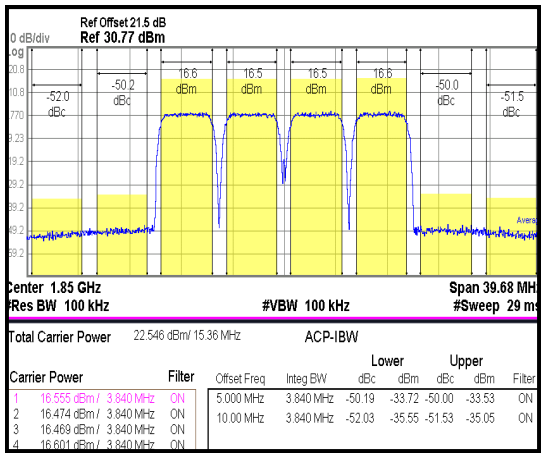
3GPP LTE E-TM3.1 10MHz

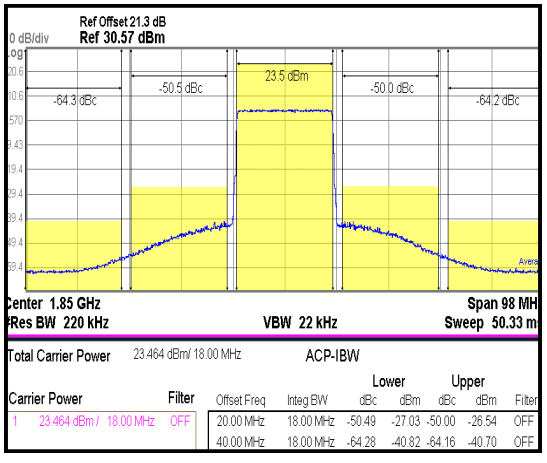


3GPP WCDMA TM1 +64DPCH 4FA



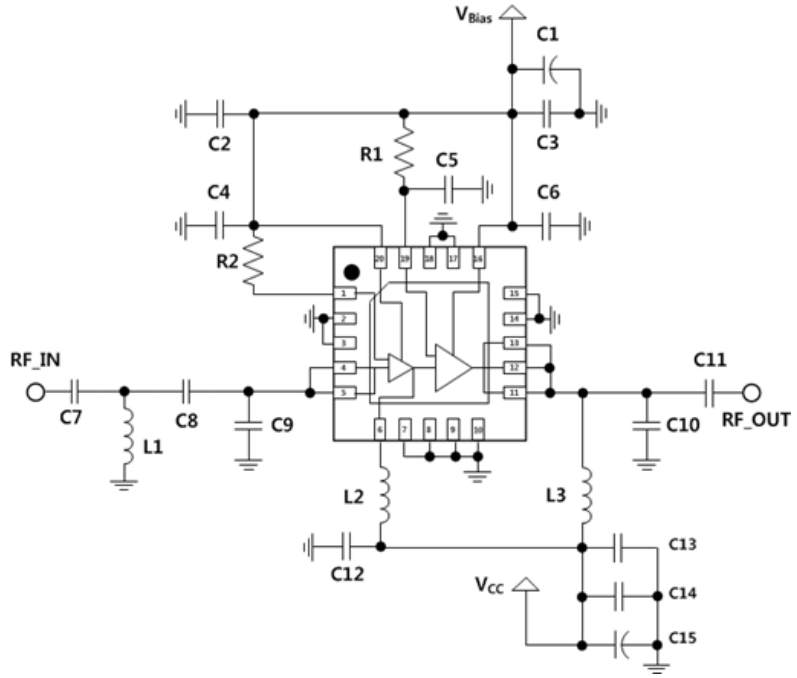
3GPP LTE E-TM3.1 20MHz





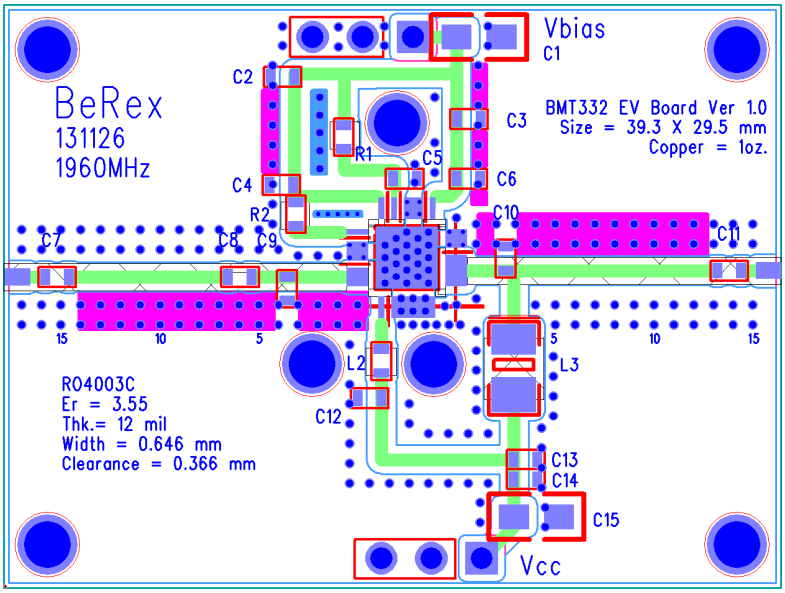
Application Circuit: 1960 MHz

Schematic Diagram



BOM			Marks
C1	1206	N/A	
C2	0603	1nF	
C3	0603	1nF	
C4	0603	N/A	
C5	0603	1nF	
C6	0603	2pF	
C7	0603	0 Ω	±5%
C8	0603	3.3pF	
C9	0603	2.7pF	
C10	0603	4.3pF	High Q
C11	0603	3.9pF	
C12	0603	1uF	
C13	0603	100pF	
C14	0603	1nF	
C15	1206	10uF	Tantalum
L1	0603	N/A	
L2	0603	12nH	
L3	1008	12nH	Coil
R1	0603	100 Ω	±5%
R2	0603	270 Ω	±5%

PCB Diagram



Notice

Below information is subject to change as conditions of the substrate.

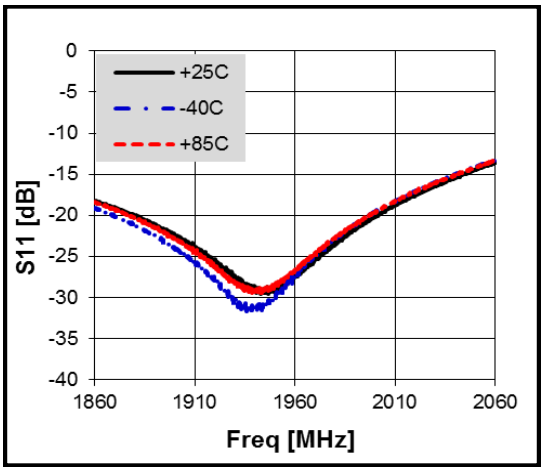
Reference	Object	Distance
Input pin	C8	5.0mm
Input pin	C9	3.1mm
Output pin	C10	2.0mm
Pin 16	C3	5.0mm
Pin 16	C6	2.0mm
Pin 19	C5	1.0mm
Pin 20	C2	10.6mm

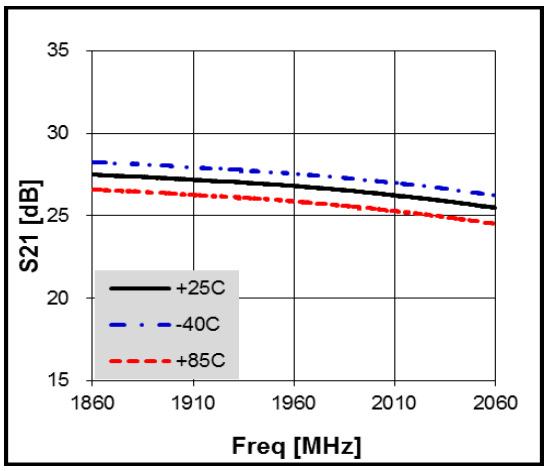
1. Pin 16 & 20 is used for Vce of the inner bias circuit. To eliminate bias line resonance you need above 10mm transmission line and adjust the position of C2, C3, C4 ,C5 and C6. Also you can adjust spectrum regrowth about bandwidth of signals which you want.

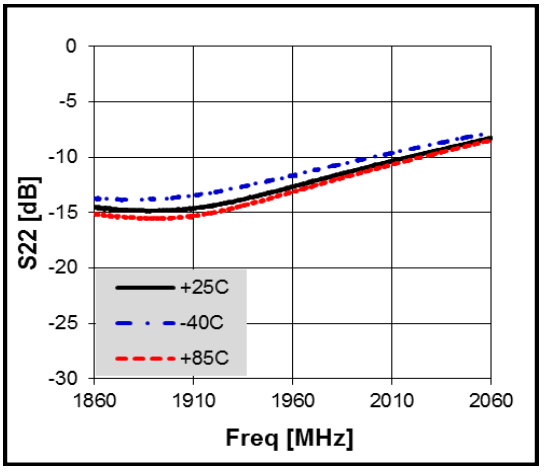
2. C10 : We recommend High-Q capacitor for better output power performance. In this document we used '4.3pF(251R14S4R3BV4, EIA 0603) of Johanson Technology.

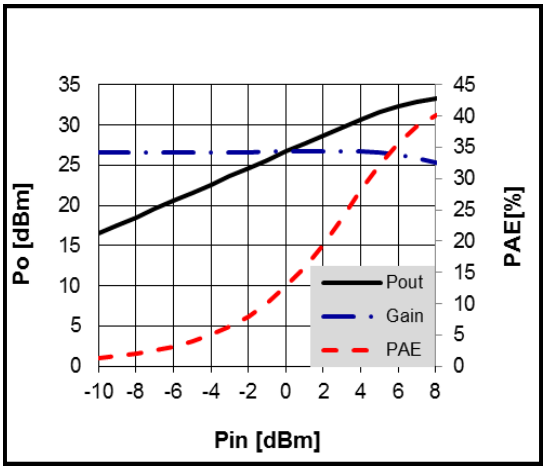
3.C7 : Non-critical 0 Ω.

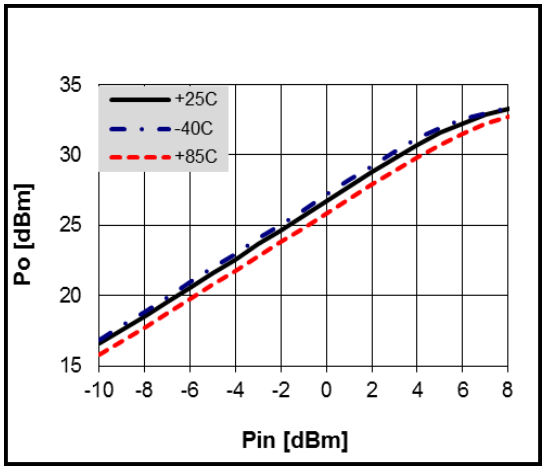
Typical Performance

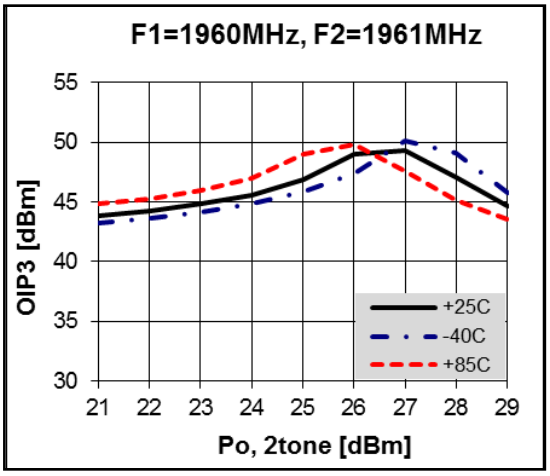




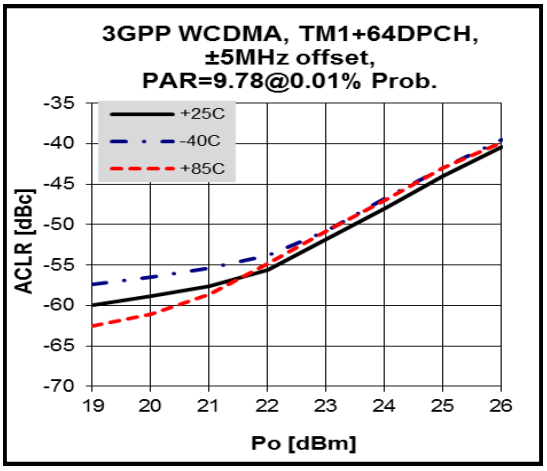




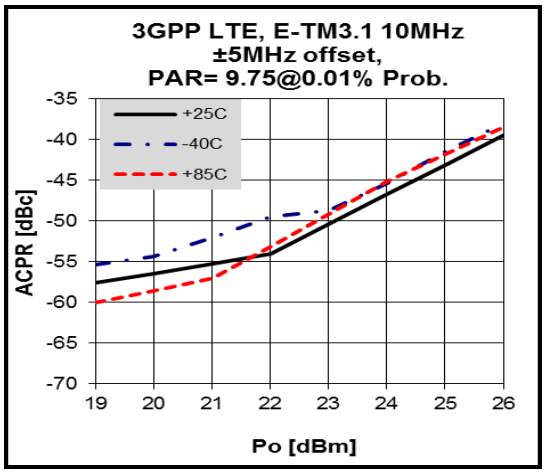




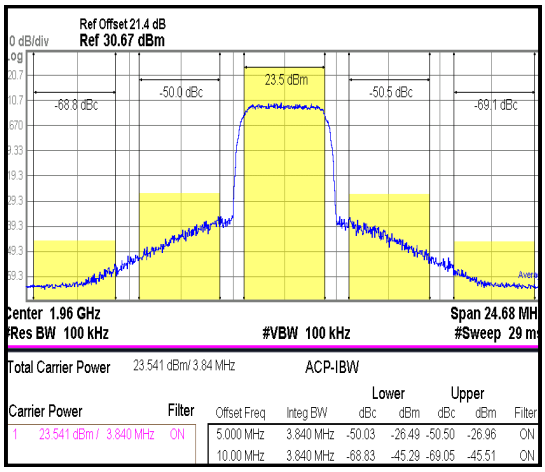
Typical Performance



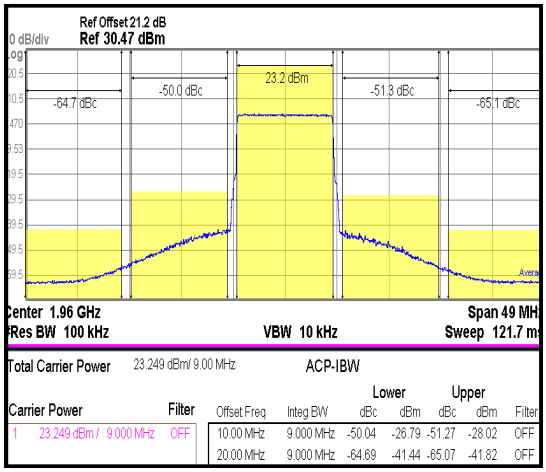
3GPP WCDMA TM1 +64DPCH 1FA



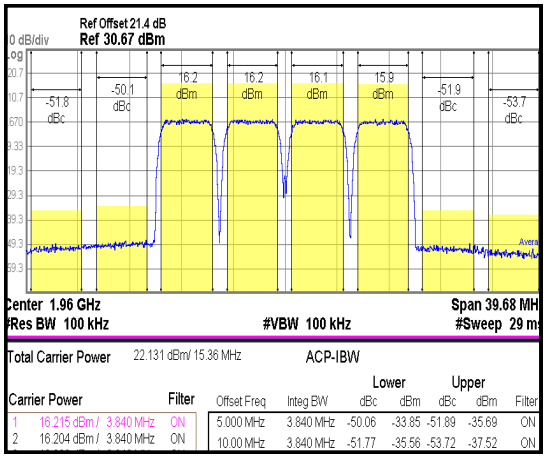
3GPP LTE E-TM3.1 10MHz

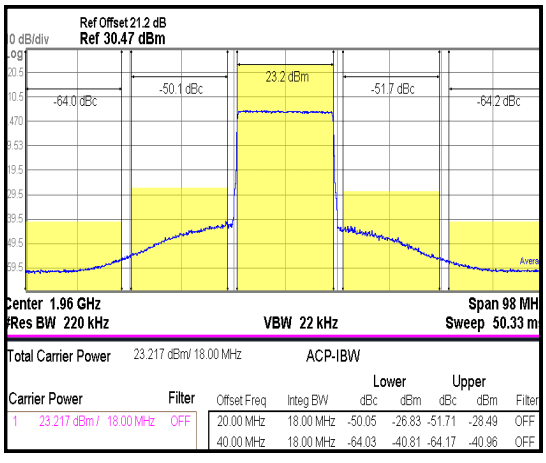


3GPP WCDMA TM1 +64DPCH 4FA



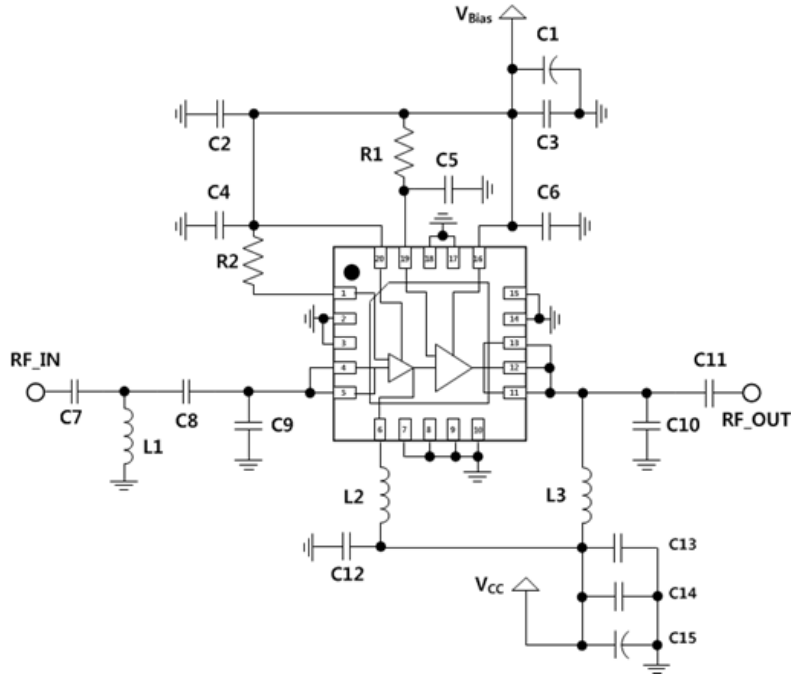
3GPP LTE E-TM3.1 20MHz





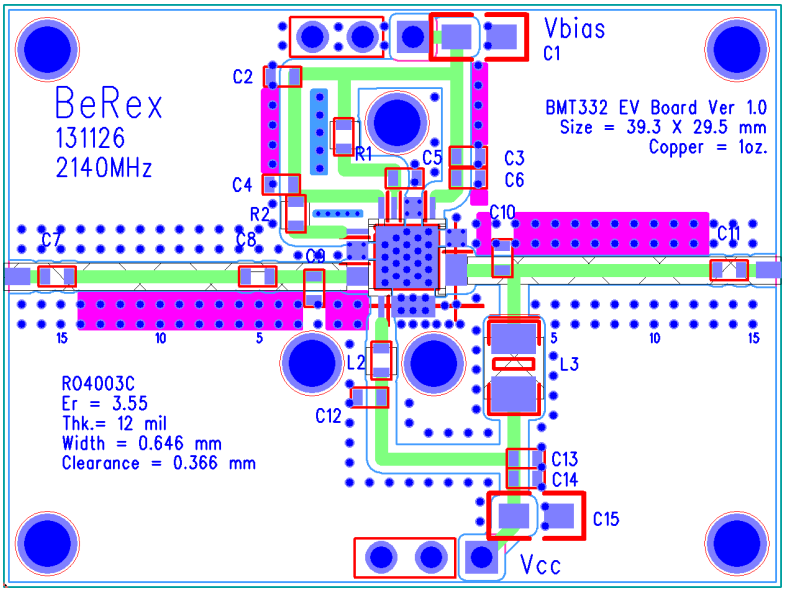
Application Circuit: 2140 MHz

Schematic Diagram



BOM			Marks
C1	1206	10uF	Tantalum
C2	0603	N/A	
C3	0603	1nF	
C4	0603	1nF	
C5	0603	1nF	
C6	0603	3pF	
C7	0603	0 Ω	±5%
C8	0603	3pF	
C9	0603	2.7pF	
C10	0603	3.9pF	High Q
C11	0603	4.3pF	
C12	0603	1uF	
C13	0603	100pF	
C14	0603	1nF	
C15	1206	10uF	Tantalum
L1	0603	N/A	
L2	0603	12nH	
L3	1008	10nH	Coil
R1	0603	100 Ω	±5%
R2	0603	270 Ω	±5%

PCB Diagram



Notice

Below information is subject to change as conditions of the substrate.

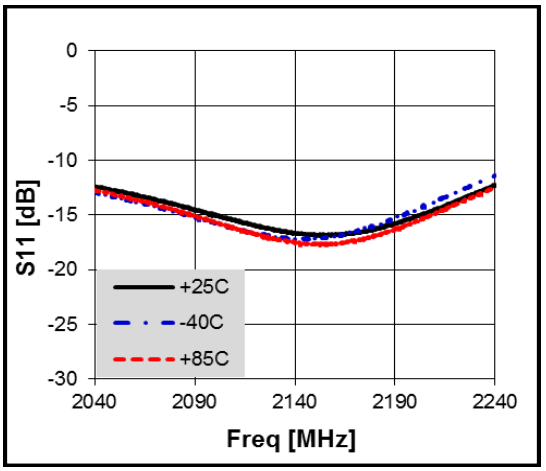
Reference	Object	Distance
Input pin	C8	4.1mm
Input pin	C9	2.2mm
Output pin	C10	1.8mm
Pin 16	C3	3.0mm
Pin 16	C6	2.0mm
Pin 19	C5	1.0mm
Pin 20	C4	5.0mm

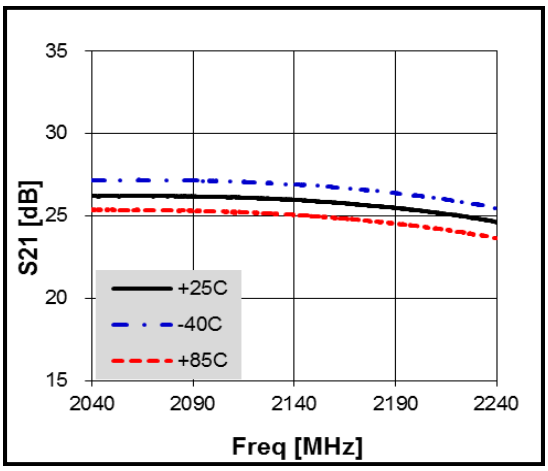
1. Pin 16 & 20 is used for Vce of the inner bias circuit. To eliminate bias line resonance you need above 10mm transmission line and adjust the position of C2, C3, C4 ,C5 and C6. Also you can adjust spectrum regrowth about bandwidth of signals which you want.

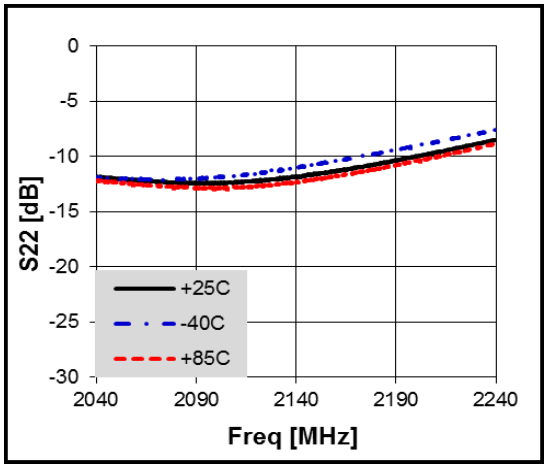
2. C10 : We recommend High-Q capacitor for better output power performance. In this document we used '3.9pF(251R14S3R9BV4, EIA 0603) of Johanson Technology.

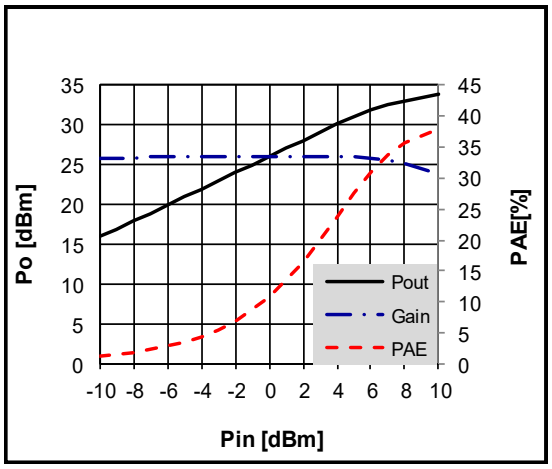
3.C7 : Non-critical 0 Ω.

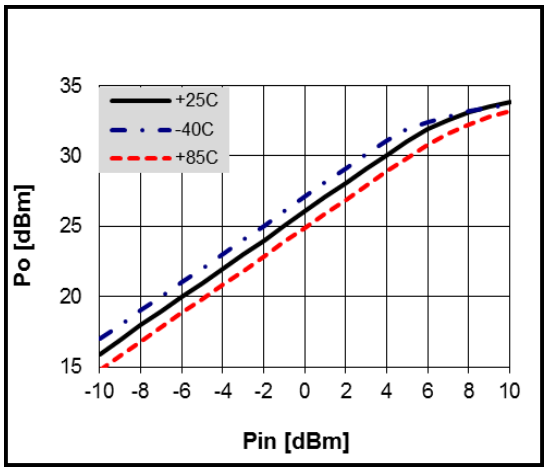
Typical Performance

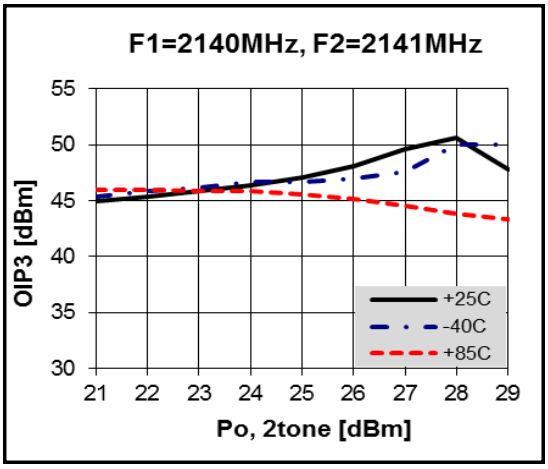




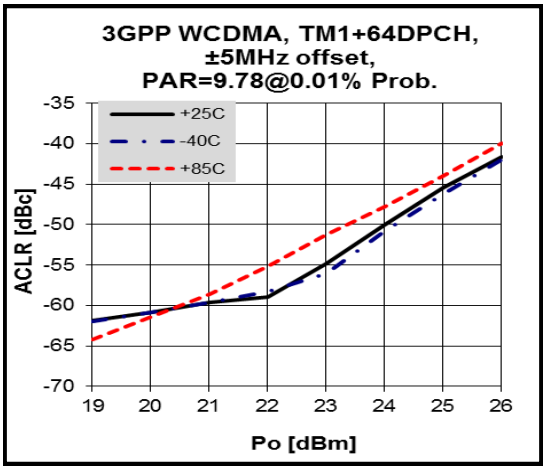




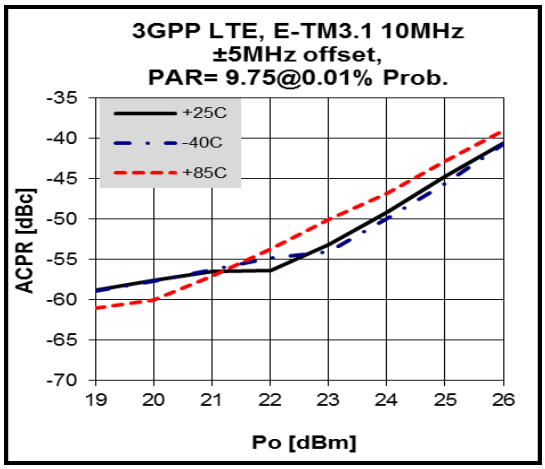




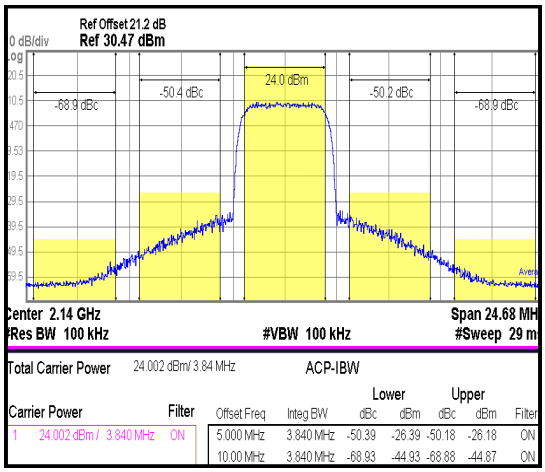
Typical Performance



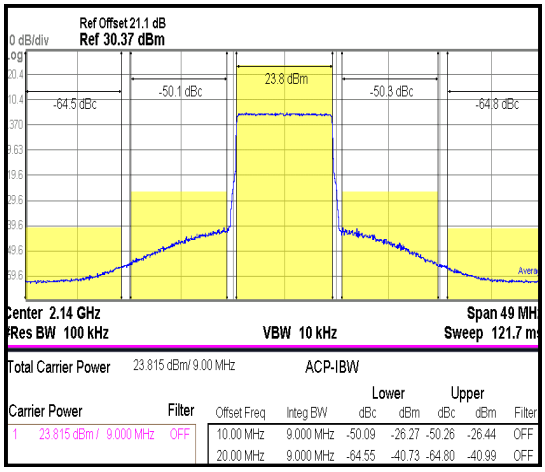
3GPP WCDMA TM1 +64DPCH 1FA



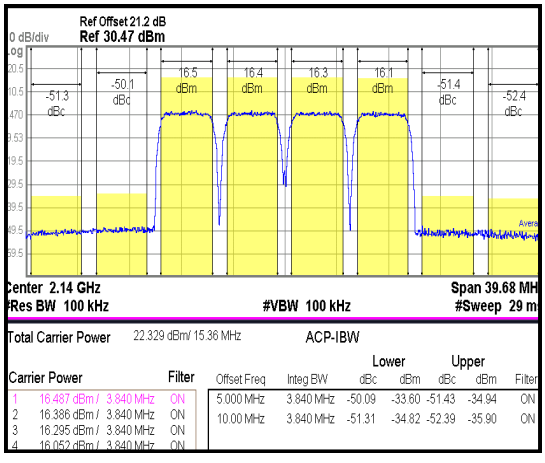
3GPP LTE E-TM3.1 10MHz



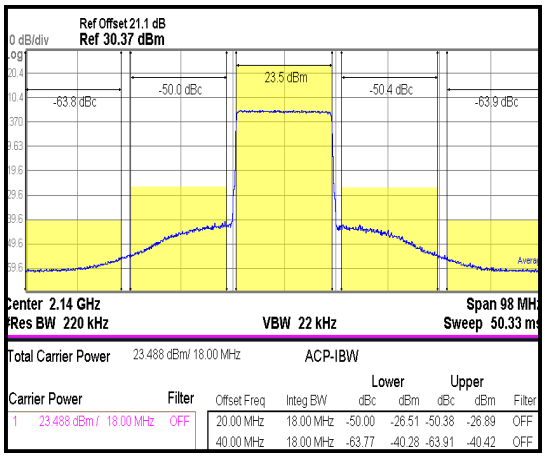
3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz



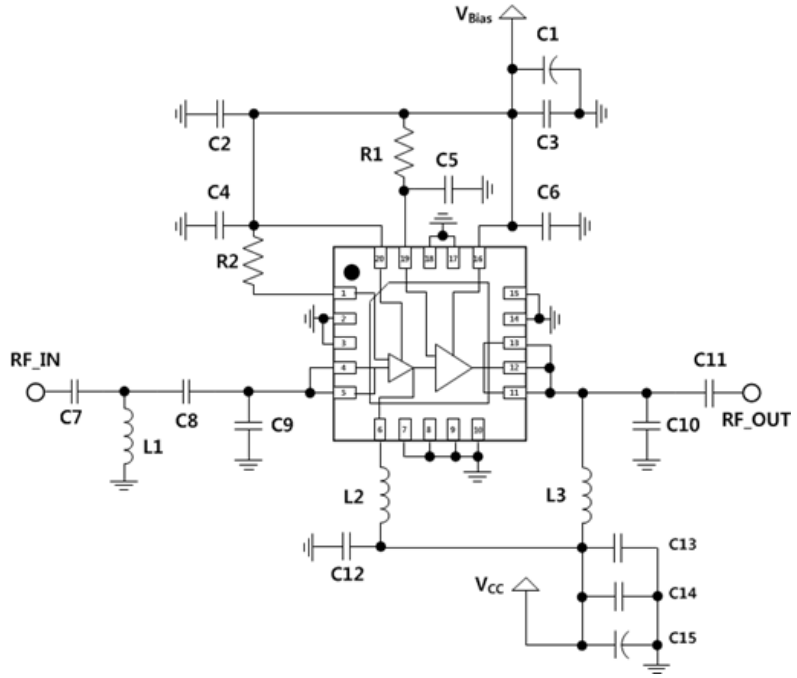
3GPP WCDMA TM1 +64DPCH 4FA



LTE E-TM3.1 20MHz

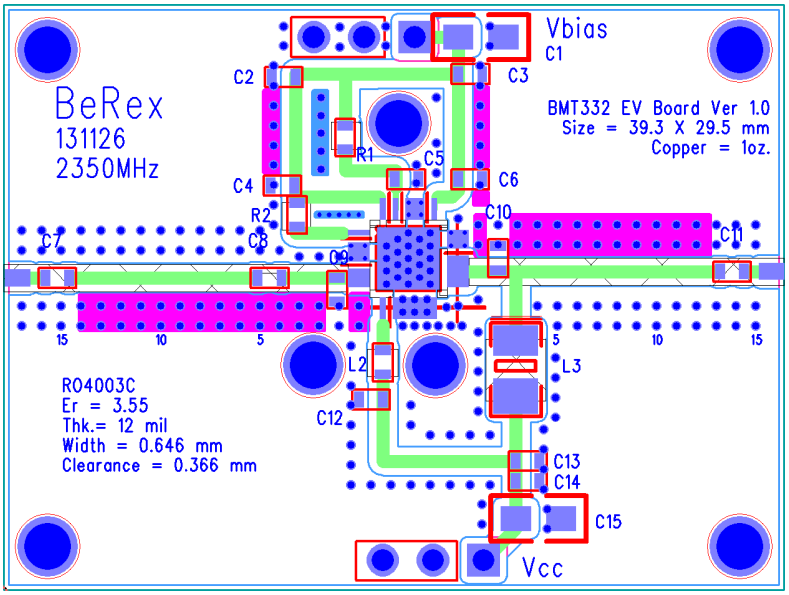
Application Circuit: 2350 MHz

Schematic Diagram



BOM			Marks
C1	1206	10uF	Tantalum
C2	0603	N/A	
C3	0603	N/A	
C4	0603	0.75pF	
C5	0603	1nF	
C6	0603	1nF	
C7	0603	0 Ω	±5%
C8	0603	2.2pF	
C9	0603	2.7pF	
C10	0603	3.3pF	High Q
C11	0603	22pF	
C12	0603	1uF	
C13	0603	100pF	
C14	0603	1nF	
C15	1206	10uF	Tantalum
L1	0603	N/A	
L2	0603	15nH	
L3	1008	10nH	Coil
R1	0603	100 Ω	±5%
R2	0603	270 Ω	±5%

PCB Diagram



Notice

Below information is subject to change as conditions of the substrate.

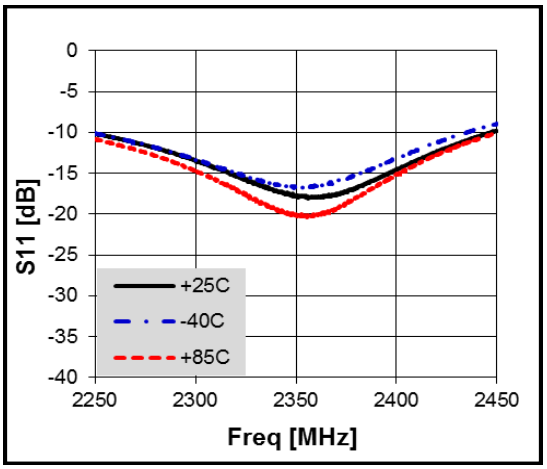
Reference	Object	Distance
Input pin	C8	3.6mm
Input pin	C9	0.6mm
Output pin	C10	1.3mm
Pin 16	C6	2.0mm
Pin 19	C5	1.0mm
Pin 20	C4	5.0mm

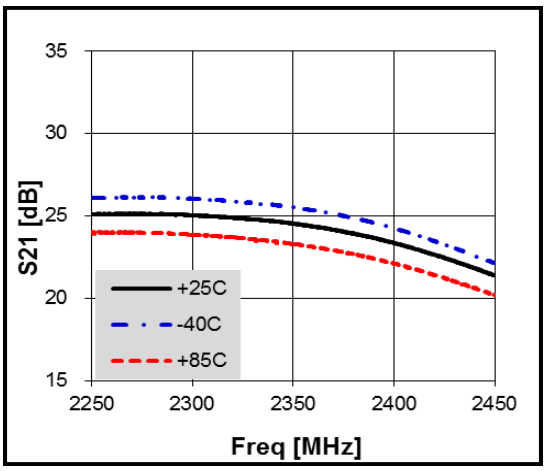
1. Pin 16 & 20 is used for Vce of the inner bias circuit. To eliminate bias line resonance you need above 10mm transmission line and adjust the position of C2, C3, C4 ,C5 and C6. Also you can adjust spectrum regrowth about bandwidth of signals which you want.

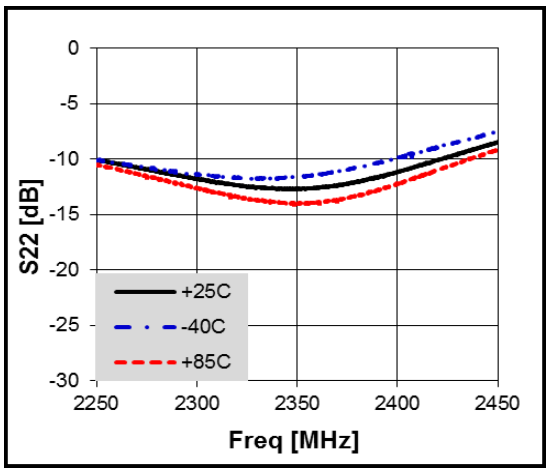
2. C10 : We recommend High-Q capacitor for better output power performance. In this document we used '3.3pF(251R14S3R3BV4, EIA 0603) of Johanson Technology.

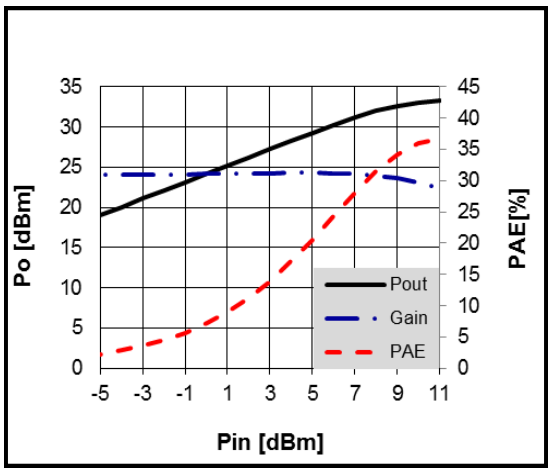
3.C7 : Non-critical 0 Ω.

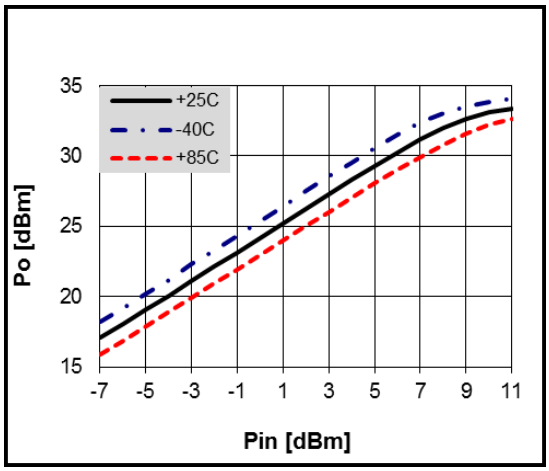
Typical Performance

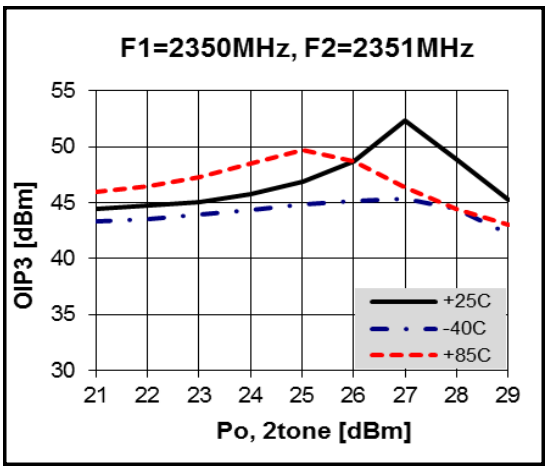




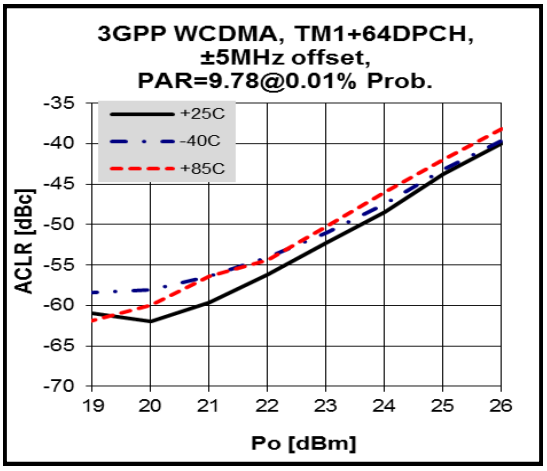




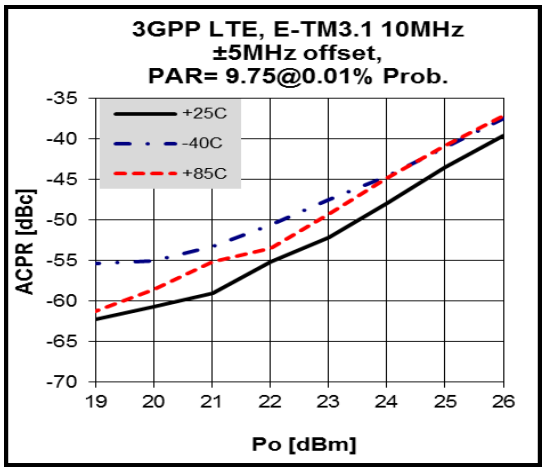




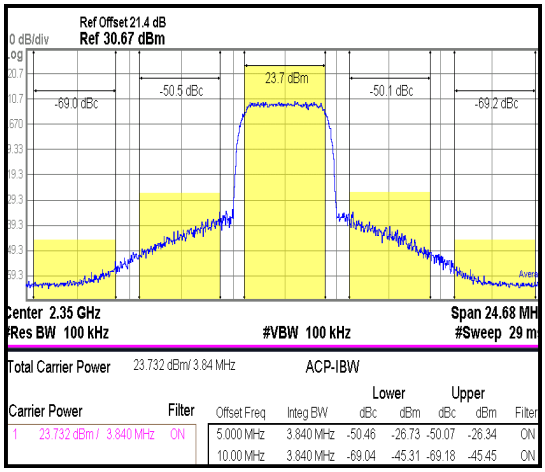
Typical Performance



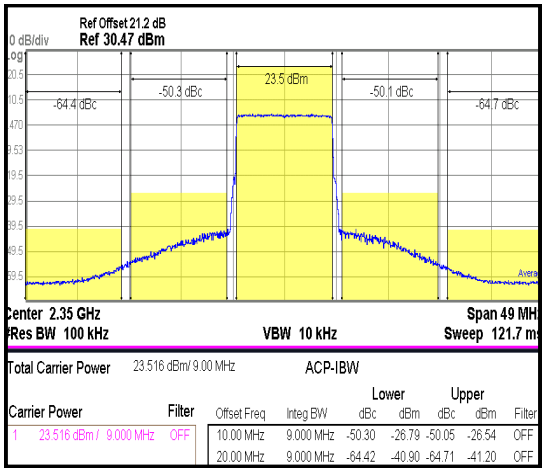
3GPP WCDMA TM1 +64DPCH 1FA



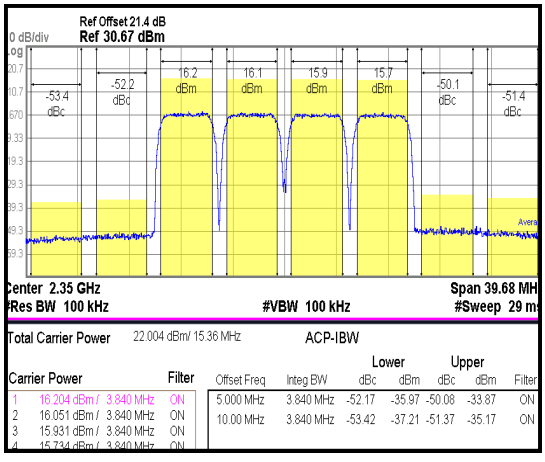
3GPP LTE E-TM3.1 10MHz

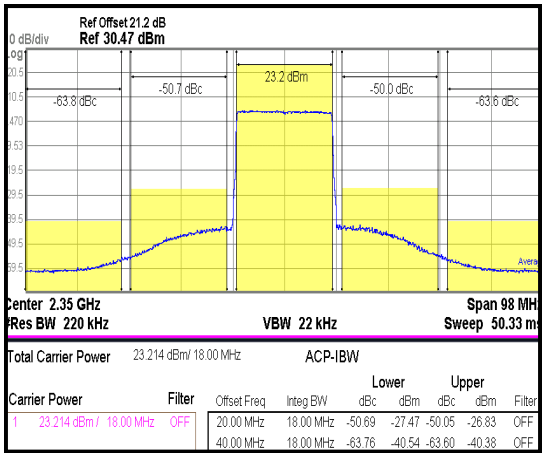


3GPP WCDMA TM1 +64DPCH 4FA

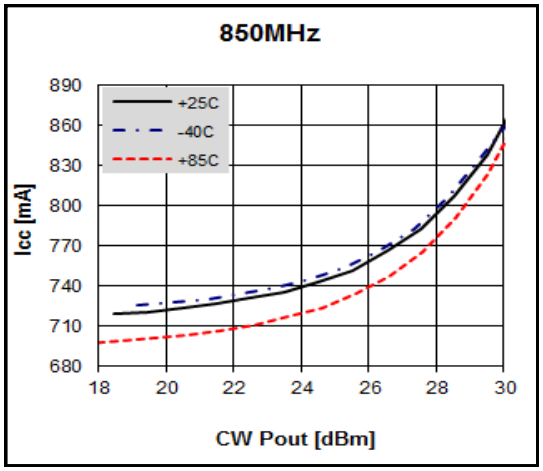


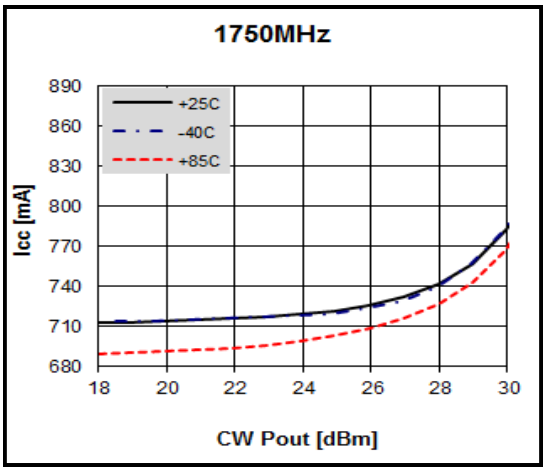
3GPP LTE E-TM3.1 20MHz

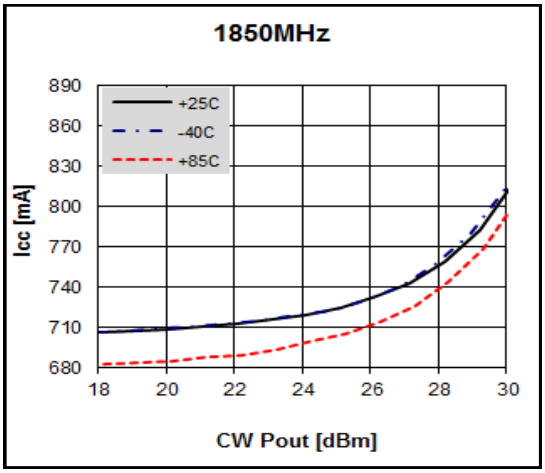


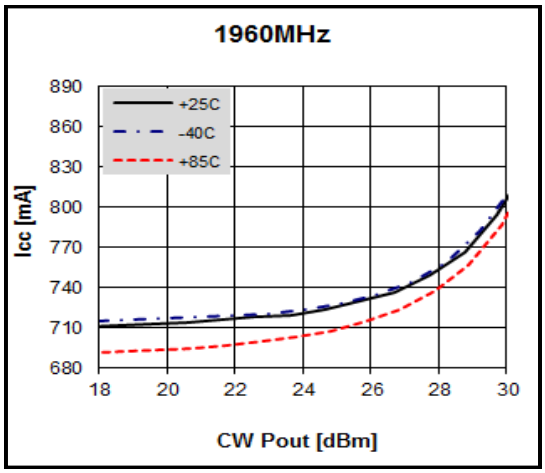


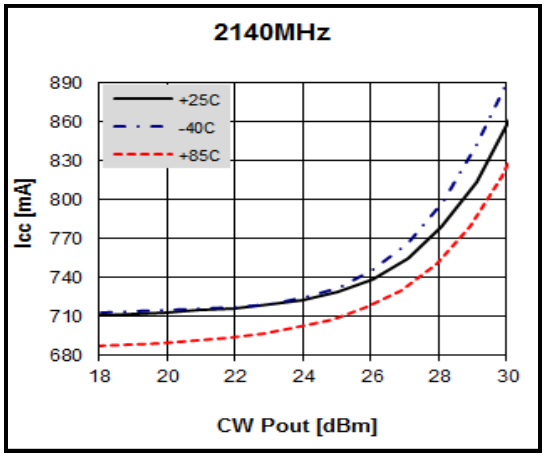
Typical Performance (Pout vs Icc)

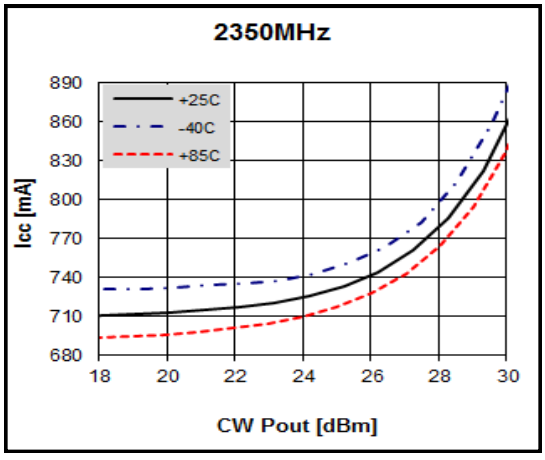




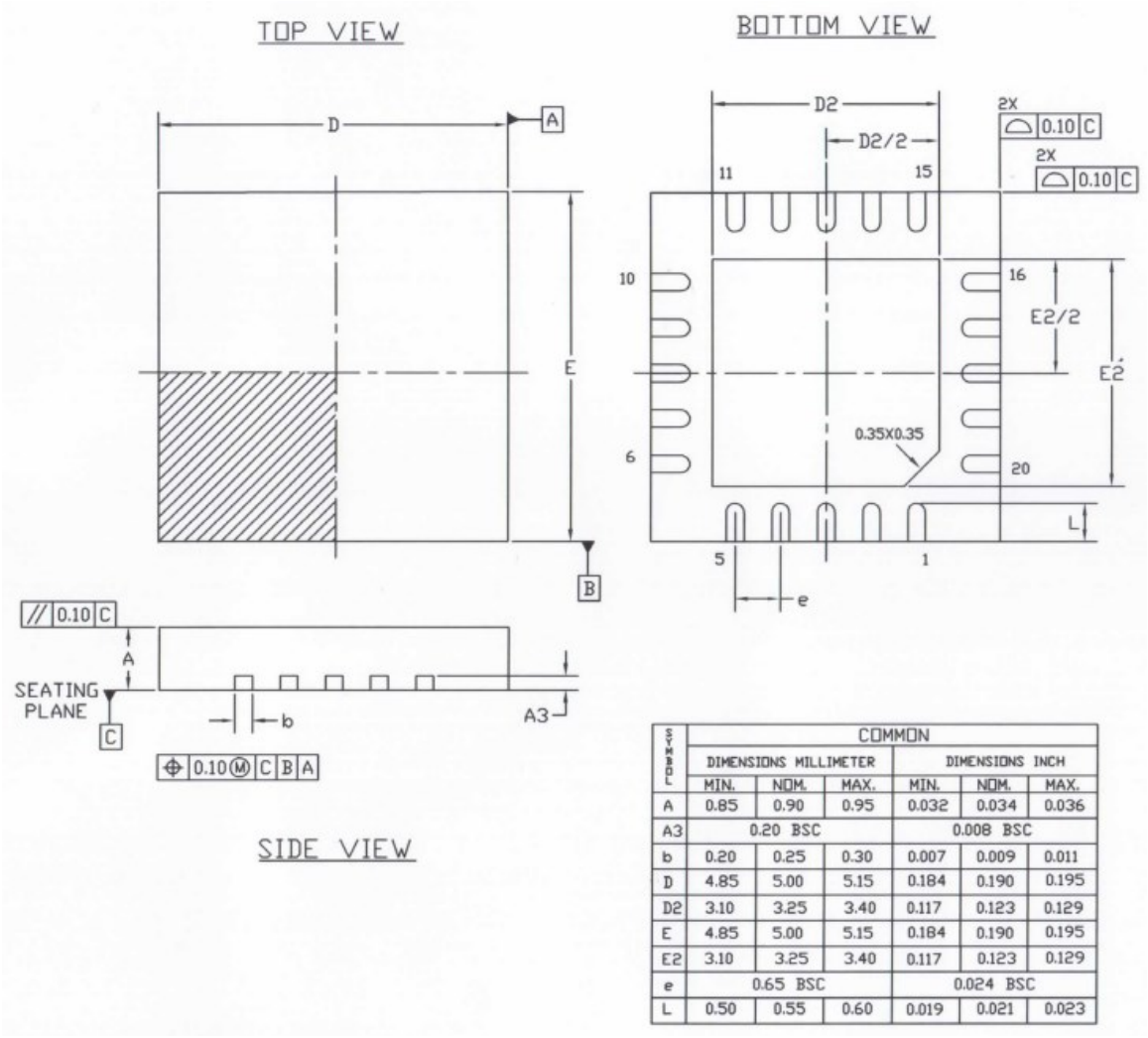








Package Outline Dimension

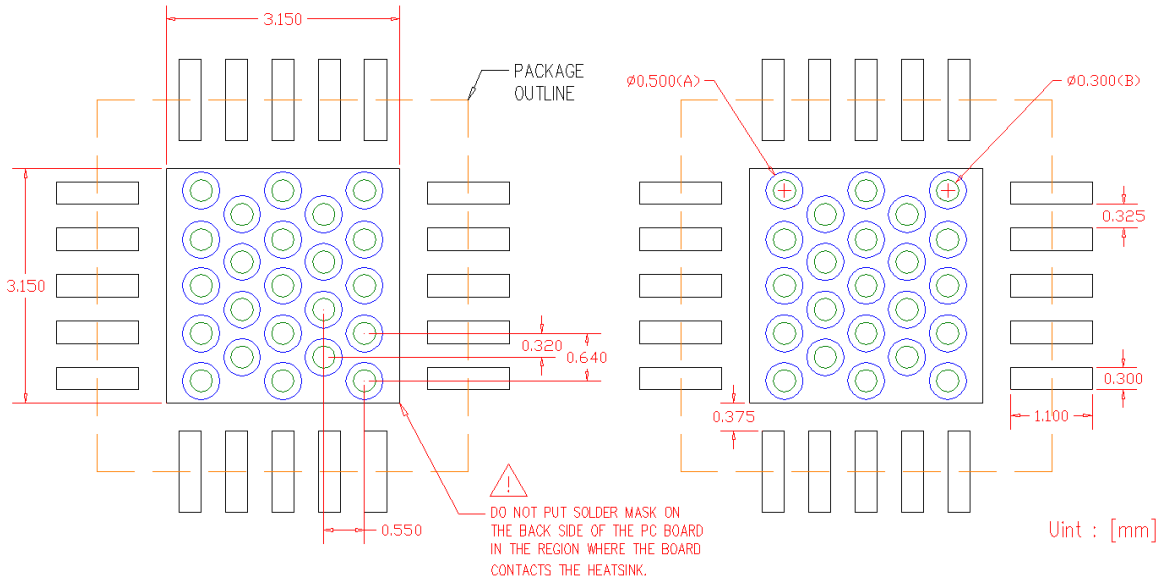


SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.032	0.034	0.036
A3	0.20 BSC			0.008 BSC		
b	0.20	0.25	0.30	0.007	0.009	0.011
D	4.85	5.00	5.15	0.184	0.190	0.195
D2	3.10	3.25	3.40	0.117	0.123	0.129
E	4.85	5.00	5.15	0.184	0.190	0.195
E2	3.10	3.25	3.40	0.117	0.123	0.129
e	0.65 BSC			0.024 BSC		
L	0.50	0.55	0.60	0.019	0.021	0.023

NOTES :

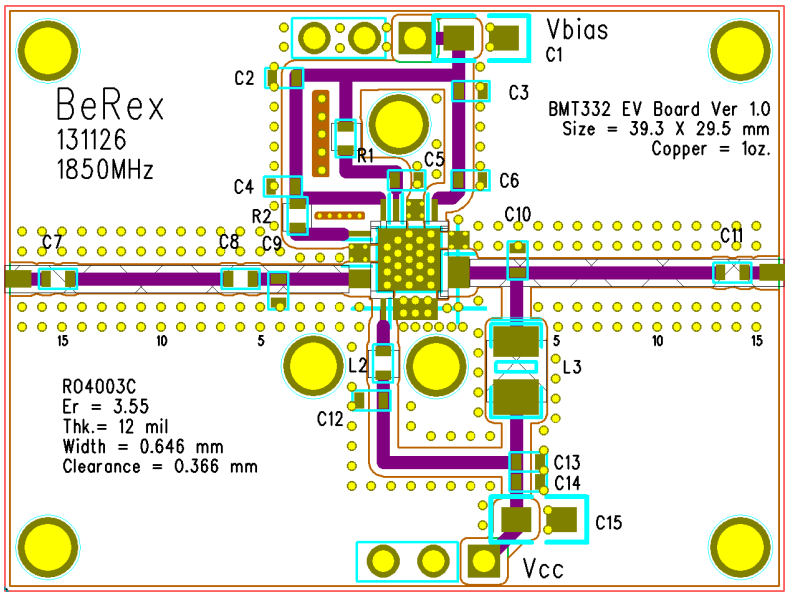
1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM. FROM TERMINAL TIP.
4. INSULATION THICKNESS, CLEARANCE OF OVERLAP ARE USER DEFINED.
5. INSULATION NOT COMPLETELY SHOWN FOR REASONS OF CLARITY.

Suggested PCB Land Pattern and PAD Layout

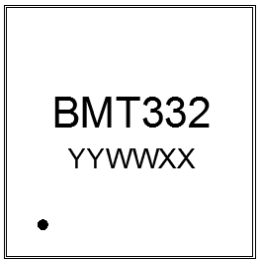


- Notes

1. Use 1 oz. copper minimum for top and bottom layer metal.
2. A heatsink underneath the area of the PCB for the mounted device is required for proper thermal operation.
3. Ground / thermal vias are critical for the proper performance of this device.



Package Marking



YY = Year, WW = Working Week,
XX = Wafer No.

Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	Passes ≥ 1000V to < 2000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114B
ESD Rating:	Class IV
Value:	Passes >1000V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101F
MSL Rating:	Level 1 at +260°C convection reflow
Standard:	JEDEC Standard J-STD-020

Proper ESD procedures should be followed when handling this device.

NATO CAGE code:

2	**N**	**9**	**6**	**F**