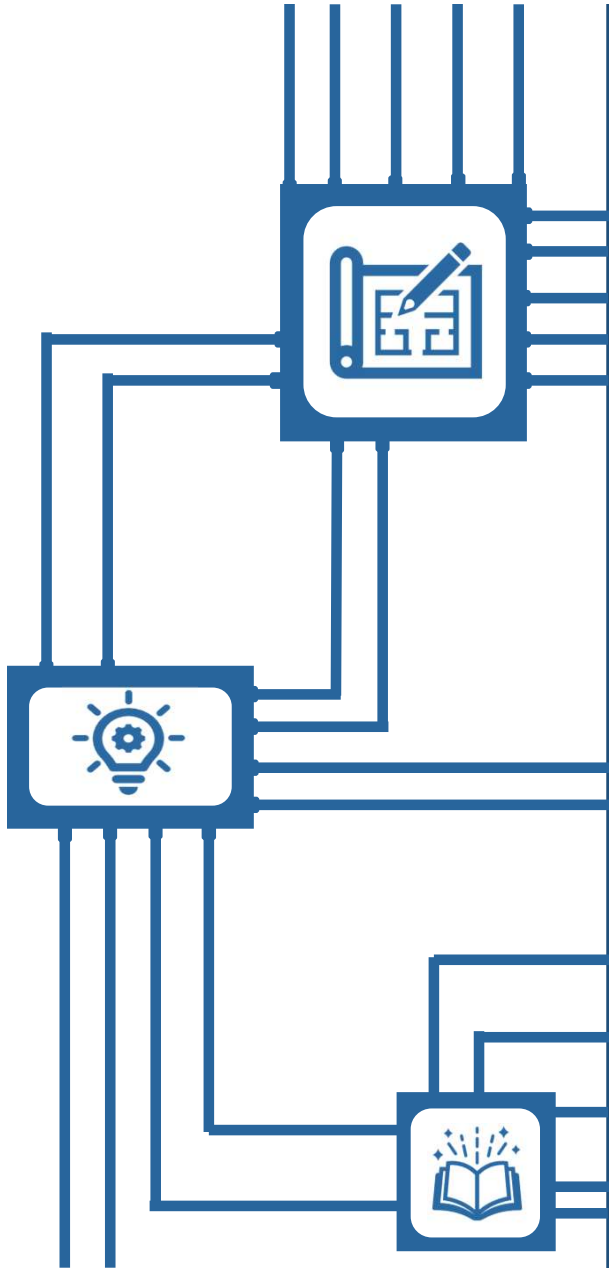
Wafer Defect Classification By Deep Learning

Capstone Design in Industrial Engineering

- 12195267 / Kim Min Seop
- 12195268 / Kim Sung Hyun
- 12173209 / Song Ui Chan
- 12195269 / Han Seong Hun
- 12170607 / Hwang Chan Won

INDEX



Problem Description

- ✓ The most important part in semiconductor manufacturing is the **"YIELD"**($Normal\ DIE / Total\ DIE$)
- ✓ A lot of work is being done to increase the yield to improve profitability.
- ✓ Technology that predicts defects before final production of semiconductors is becoming more important nowadays.
- ✓ In this project, We built a CNN Modeling to enable classify and prediction of the causes of wafer defects by using Deep Learning(CNN Modeling).

반도체 수급 좋아진다더니
더 늘어난 현대차 신차 대기
· · "싼타페 HEV 20개월"

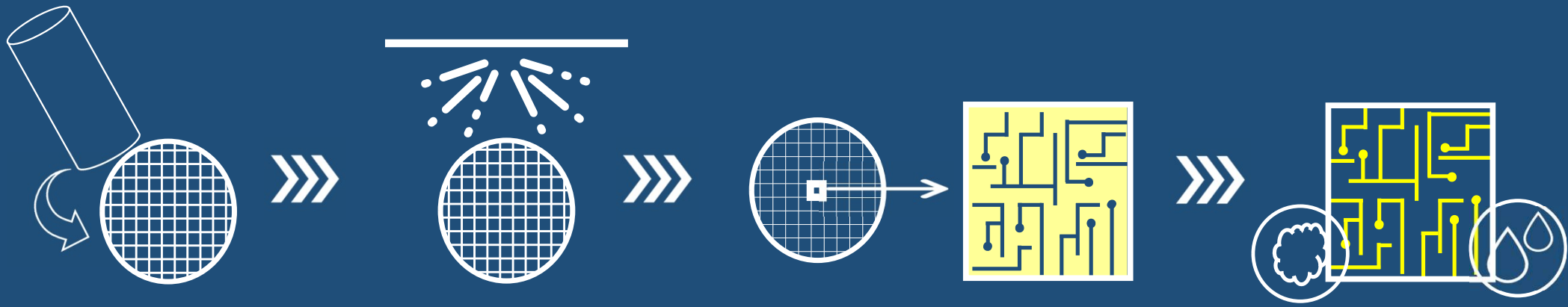
(02/Sep/22_Hankook Ilbo)

삼성전자 3나노 수율 탓에
양산 지연, 올해 자체 반도체만
적용 가능성

(14/Apr/22_Business Post)

What is Semiconductor Process?

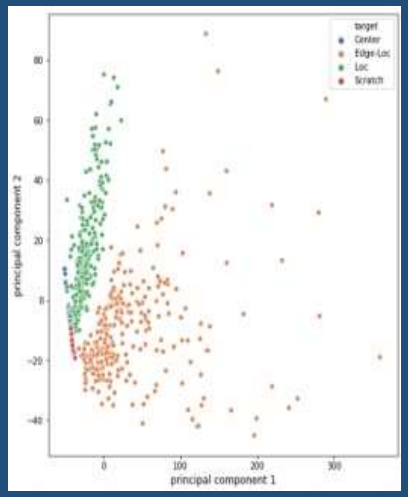
✓ For manufacturing of each semiconductor products, there are processes divided into 8 steps

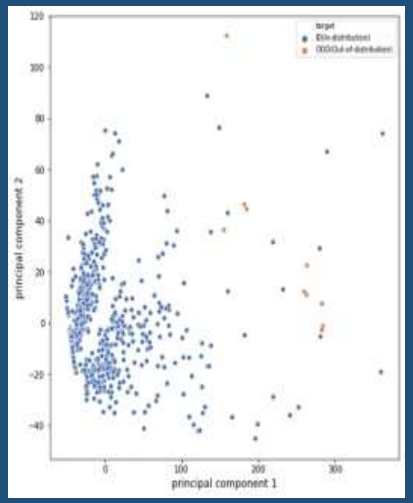


1. Wafer Processing
2. Oxidation
3. Photography
4. Etching
5. Film Deposition
6. Metalization
7. Test
8. Package

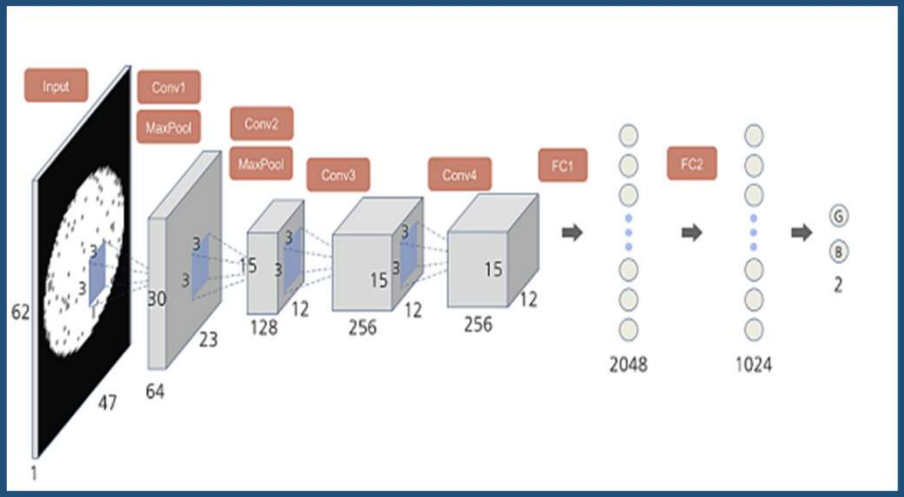
Prior Technology & Reference

A Multi-Class Data Description Based Method for Classifying Predefined Defect Patterns and Detecting New Defect Patterns of Wafer Bin Maps





Wafer Map-based Defect Detection Using Convolutional Neural Networks



Data Analysis & Preprocessing

	waferMap	dieSize	lotName	waferIndex	trianTestLabel	failureType
0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...	1683.0	lot1	1.0	[[Training]]	[[none]]
1	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...	1683.0	lot1	2.0	[[Training]]	[[none]]
2	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...	1683.0	lot1	3.0	[[Training]]	[[none]]
3	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...	1683.0	lot1	4.0	[[Training]]	[[none]]
4	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...	1683.0	lot1	5.0	[[Training]]	[[none]]
...	...	...	...	...	...	...
811452	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 2, 1, 1,...	600.0	lot47542	23.0	[[Test]]	[[Edge-Ring]]
811453	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 2, 2, 1, 1,...	600.0	lot47542	24.0	[[Test]]	[[Edge-Loc]]
811454	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 2, 1, 1,...	600.0	lot47542	25.0	[[Test]]	[[Edge-Ring]]
811455	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1,...	600.0	lot47543	1.0	[]	[]
811456	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 2, 1, 1,...	600.0	lot47543	2.0	[]	[]

811457 rows × 6 columns

Data Analysis & Preprocessing

✓ In the semiconductor industry, 1 lot usually means 25 sheets. The lots used in the project are 47,543 [47,543(lots) * 25 = 1,188,575(sheets)]

✓ Therefore 1,188,575 indexing should occur, but the total number is about 811k.
So deleted the lotName and waferIndex.

	waferMap	dieSize	lotName	waferIndex
0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...	1683.0	lot1	1.0
⋮				
811456	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 2, 1, 1,...	600.0	lot47543	2.0

811457 rows × 6 columns

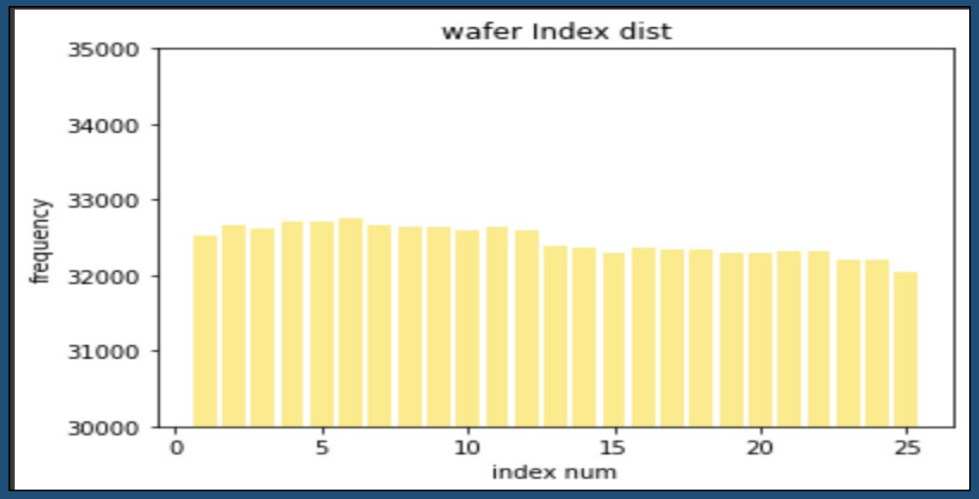


Figure 2. Wafer Index dist

Data Analysis & Preprocessing

※ Result※

Defect Type	Num
Center	90
Donut	1
Edge-Loc	296
Edge-Ring	31
Loc	297
Near-full	16
Random	74
Scratch	72
None	13,489

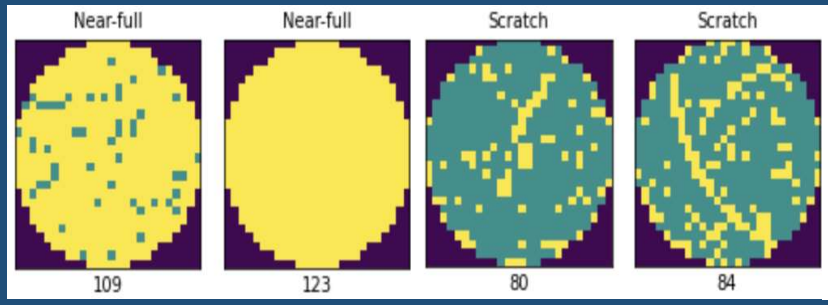
※ Type of Wafer Defect ※

0 ⋙ Blank

1 ⋙ Normal

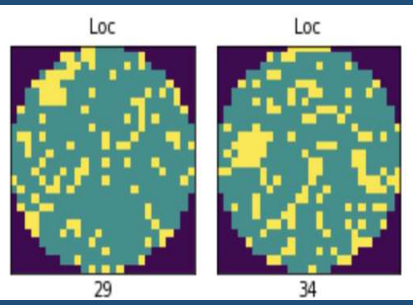
2 ⋙ Defect

Near-full : 16

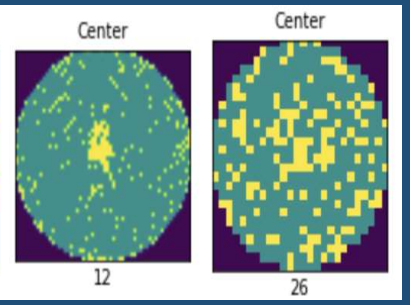


Scratch : 72

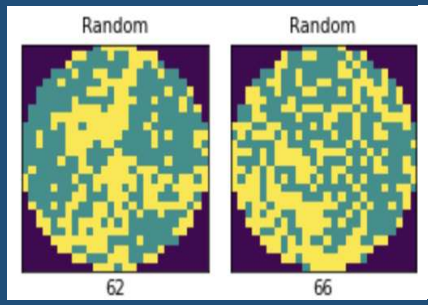
Loc : 297



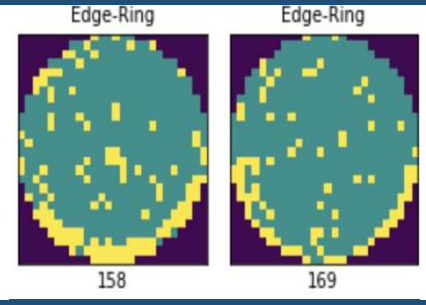
Center : 90



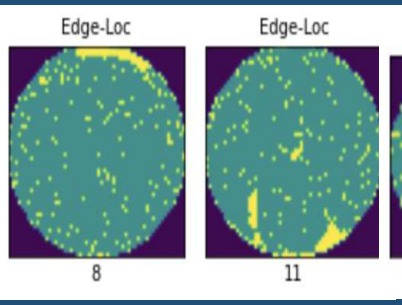
Random : 74



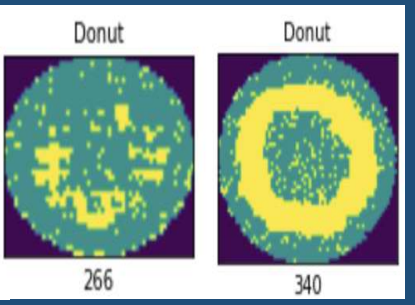
Edge-Ring : 31



Edge-Loc : 296

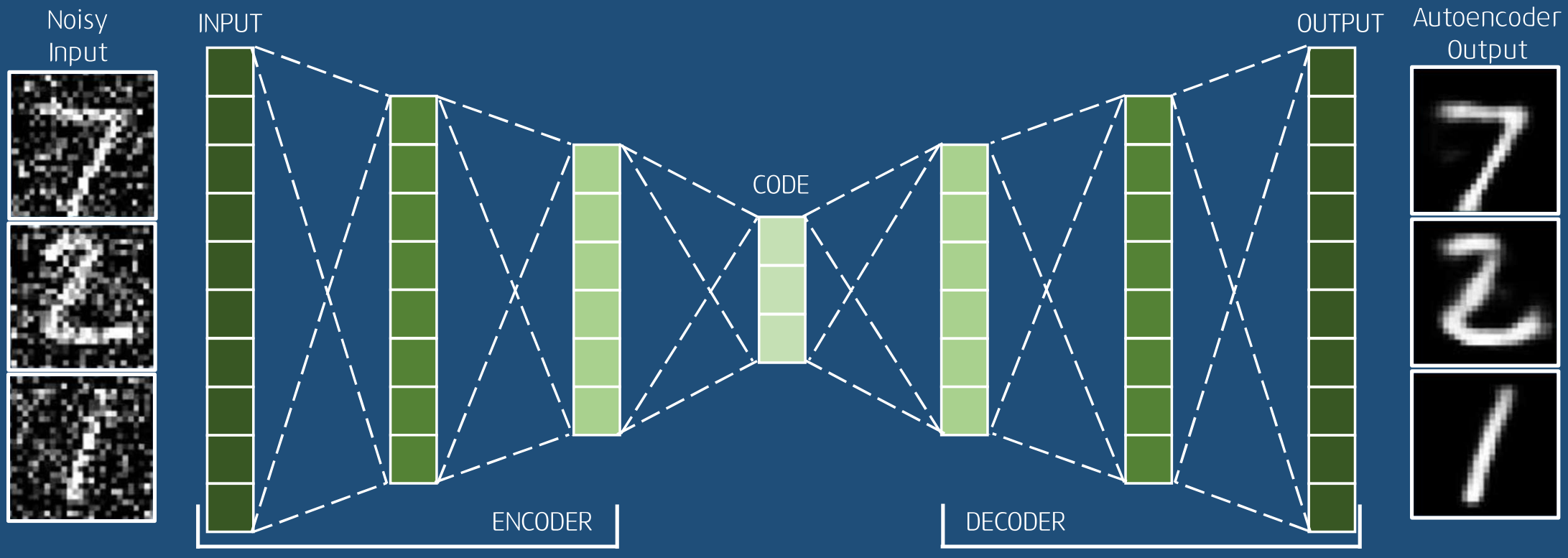


Donut : 1



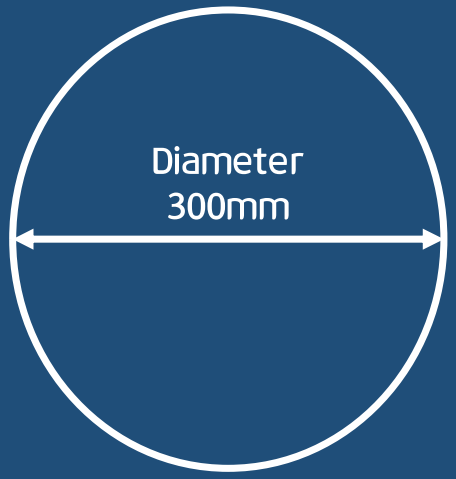
Data Analysis & Preprocessing

- ✓ For data augmentation, artificially added noise to the high-quality image and proceeded with encoder/decoder process.

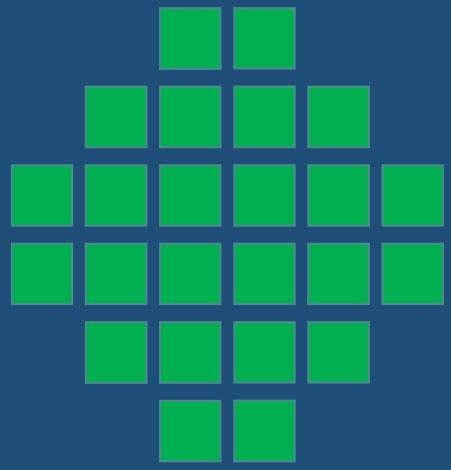


Data Analysis & Preprocessing

- ✓ From an economic point of view, Net Die is important because it is directly related to the Wafer unit price.
- ✓ The number of Net Die is Wafer Area / Die-Size, Therefore net die is inversely proportional to the Die-Size. (Die-Size increases as it gets smaller)



Wafer Area = 70,659mm^2

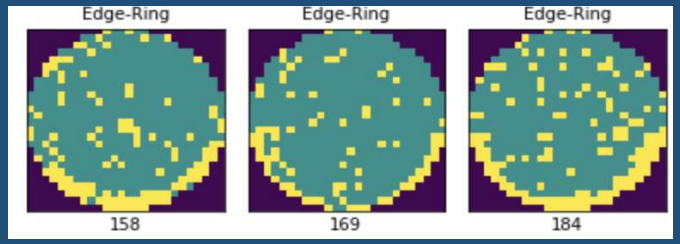
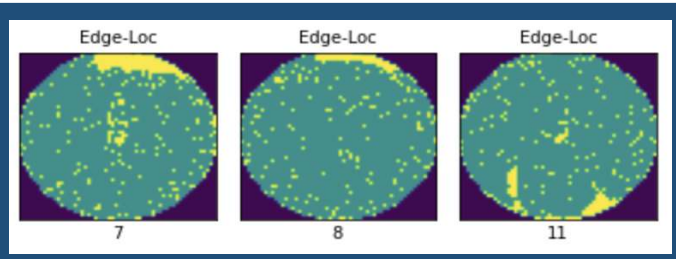


number of Net Die = 70,659mm^2 / x → Die-Size

Die-Size	number of Net Die (x)
130mm^2	543개
100mm^2	706개

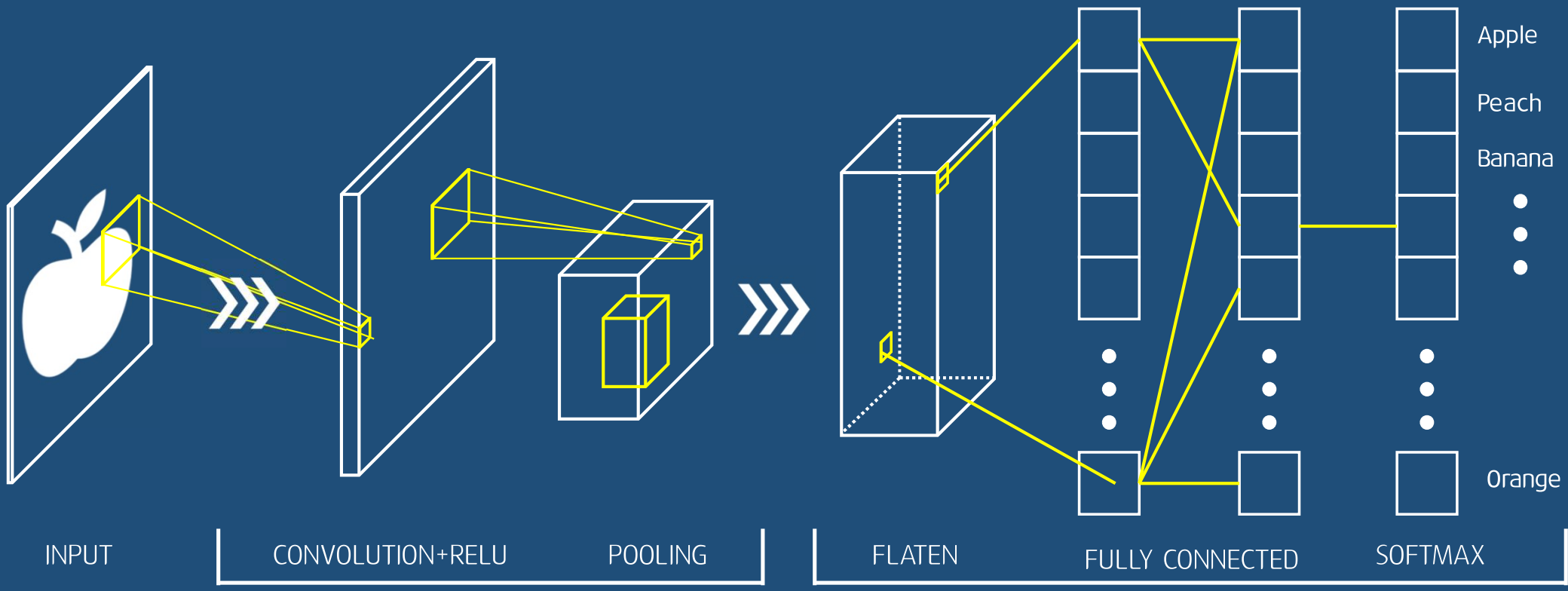
Data Analysis & Preprocessing

- ✓ In checking Net Die($^{\text{Normal Die Size}}/_{\text{Wafe Size}}$) to ensure that all defect types are critical, We found that large numbers of abnormal chips are not always valid.
- ✓ Edge-log and edge-ring defects showed higher values than other types of Net Die, So focused on that type and performed augmented learning by using autoencoder.

	Edge-Ring	Edge-Loc
Image of defect		
Net Die	4.00	3.98
Before Autoencoder	31	296
After Autoencoder	7,037	7,400

Modeling

✓ We used CNN Modeling Construction that One of the type of deep learning model.



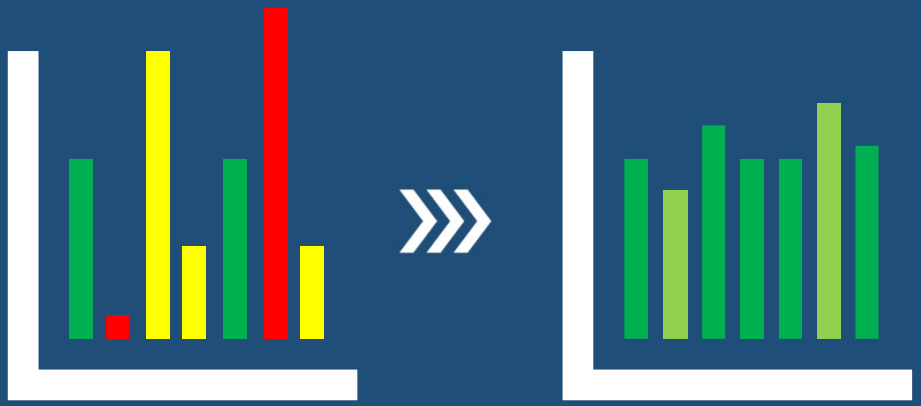
Evaluation

※ Performance Results ※

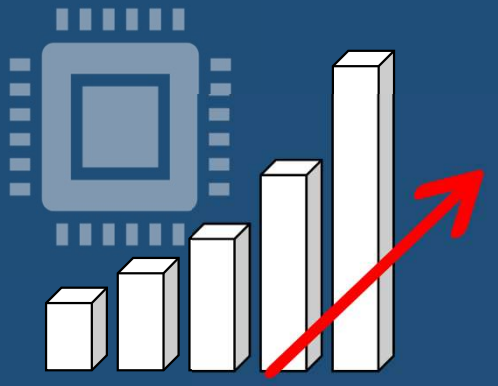
Number of Bad Classes & Whether it is augmented	Forecast Accuracy
Bad Class 2 / Argumentation X	**90%**
Bad Class 2 / Argumentation ○ : 3,000EA	**89%**
Bad Class 2 / Argumentation ○ : 5,000EA	**92%**
Bad Class 2 / Argumentation ○ : 7,000EA	**93%**

Solution

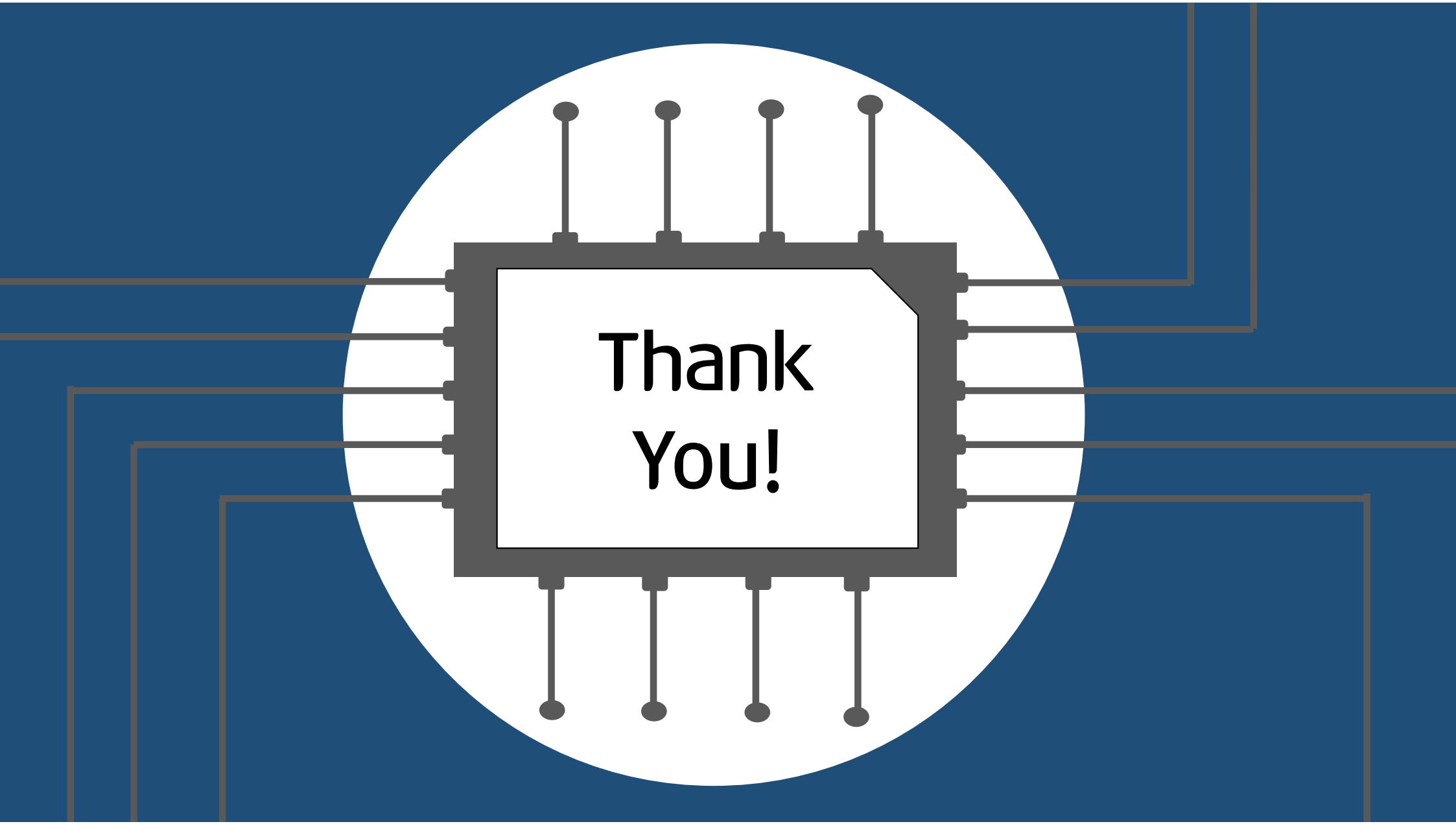
- ✓ The prediction accuracy of the model can be trusted by resolving the imbalance of target classes that occur in actual industrial sites.
- ✓ It is possible to improve the yield by detecting wafer defect patterns before the process is finished and request an engineer or department in charge to prevent defects in advance.



Balanced change in target class



Increased yield through pre-detection


Thank
You!