Seohyun Park

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Education

Georgia Institute of Technology | Atlanta, GA *August 2024 – Present*
Bachelor of Science in Computer Engineering (4.0 GPA) Expected Graduation: May 2027
Threads: Computing Hardware & Emerging Architectures + Systems & Architecture

Skills

Hardware: FPGA Development, Cadence Virtuoso (**RTL-to-GDSII Certified**), ModelSim, Oscilloscope, Logic Analyzer, MPI, Multisim
Programming: Python, Java, C, RISC-V Assembly, VHDL, SystemVerilog, Google Test
Software/Frameworks: Git, Linux, Firebase
Languages: English (fluent), Korean (native)

Relevant Coursework

- **ECE 3058 – Architecture, Systems, Concurrency and Energy in Computation:** Multi-cycle & pipelined processor datapaths, hazard handling, cache design, virtual memory, OS-level I/O, performance/energy trade-offs.
- **ECE 2035 – Programming for Hardware/Software Systems:** Memory management, procedural abstraction, OS concepts, performance optimization in C and RISC-V assembly.
- **ECE 2031 – Digital Design:** Digital circuit design and testing in VHDL using FPGAs and CAD tools.
- **CS 1332 – Data Structures & Algorithms:** Sorting algorithms, recursion, hash tables, linked lists, graphs, trees, dynamic programming.
- **ECE 2040 – Circuit Analysis:** DC/AC circuit analysis with node/mesh methods, Thevenin/Norton theorems, Laplace transforms.

Projects

5-Stage Pipelined RSC-V Processor | Georgia Tech, ECE 3058 *May 2025 – July 2025*
- Implemented a 5-stage pipelined RV32I processor in SystemVerilog with hazard detection, stalling, data forwarding, and pipeline flushing; validated using ModelSim and benchmark programs.
- Built on a prior single-cycle RV32I design supporting ADD, ADDI, SUB, LW, SW, SLT, and JAL, with integrated instruction/data memory.

FPGA Morse Code LED Controller | Georgia Tech, ECE 2031 *January 2025 – May 2025*
- Programmed a VHDL-based LED peripheral on the DE10 FPGA that converts ASCII input into Morse code patterns and displays them via LEDs and a 7-segment display.
- Implemented static and flashing modes via state machine design to interface with an SCOMP processor without altering internal architecture.

Snake Game on Mbed Platform | Georgia Tech, ECE 2035 *January 2025 – May 2025*
- Developed an interactive Snake game in C++, integrating hardware elements (Mbed microcontroller, nav-switch input, uLCD display), with game features including score tracking, win/lose states, and real-time collision detection.

Parallelized Ligand Docking Pipeline | Emory Department of Biochemistry, Liang Lab *December 2022 – Present*
- Developed an OpenMPI-based parallel docking pipeline using VinaLC and MPIVina for screening large small-molecule libraries against the RSV RdRp polymerase within a 192-core supercomputer cluster.
- Automated compound conversion, filtering, and redocking with OpenBabel and Python.

Experience

URS Compliance Services | Duluth, Georgia *June – July 2022*
Data Analysis Intern
- Verified and managed 500+ legal entity records in state/internal systems.
- Built Excel/Python macros to streamline contract processing for 300+ documents.

Activities

GT Silicon Jackets (Chip Fabrication Club) | Fetch Block - Physical Design Team *August 2024 – Present*
- Scripted parsing of timing-report violations and averaged path depth; optimized chip area and clock frequency.

GT IOS (App Development Club) | Loop Team/Gauge Team *August 2024 – Present*
- Developed profile pages, worked with Google Firebase to integrate user information for the Loop App (Fall 2024).
- Developed animated views for “Take Match” of the Gauge App – awarded Best App at Spring Demo Day 2025.