Spring 2020 EEE3530

Computer Architecture

Project 1-1

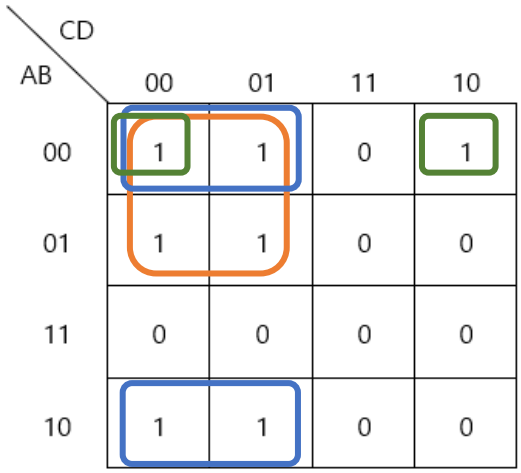
2018142059

김서영

1. Truth Table and K-map

Since the four bits signal produces 1 when the input signal represents digit in my student ID, 2018142059, the truth table and K-map is just like follows.

Input				Output
A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



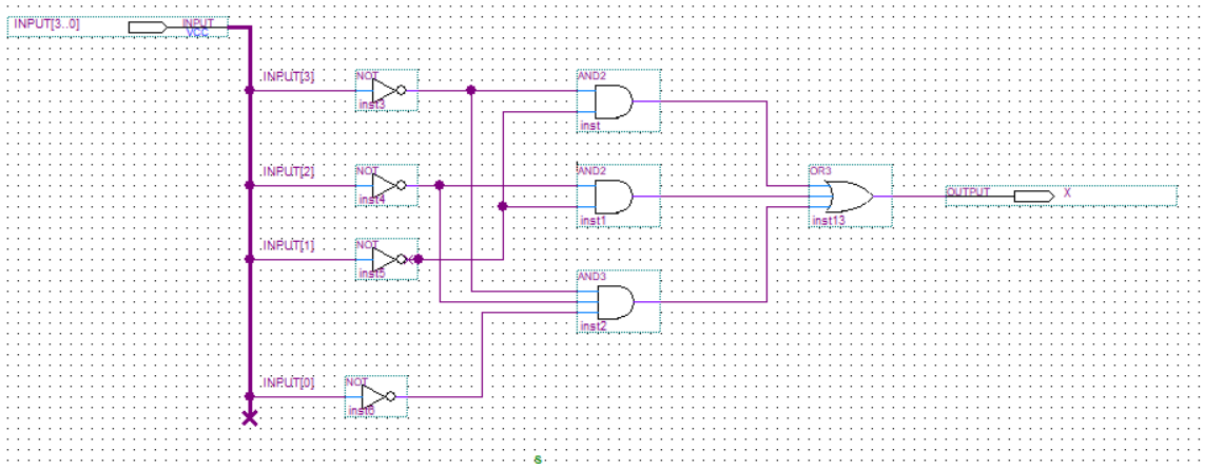
From the K-map, the signal can be simplified as a function F(A, B, C, D) below.

F(A, B, C, D)= A'C'+B'C'+A'B'D'

2. Schematic Diagram from Quartus II

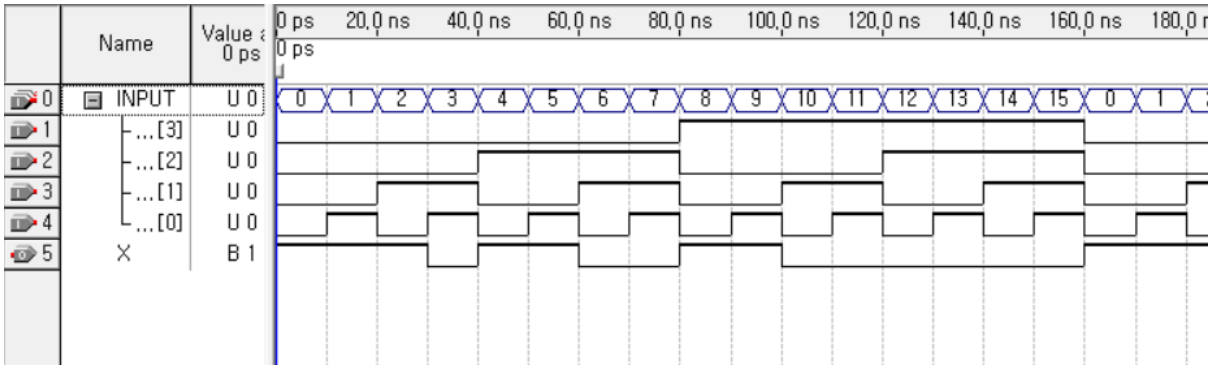
By using the simplified function, the schematic diagram can be obtained and drown in Quartus II.

Input A, B, C, and D is connected to the INPUT[3], INPUT[2], INPUT[1], INPUT[0].



3. simulation results (the wave form)

Since the simulation is about functional output of the logic, the simulation was implemented in functional simulation mode.



4. Discussion

Since the usual order used in computer program is starting from 0, I put the signal in the opposite order, but the result was difficult and different from I expected.