Computer Architecture (EEE3530-01)

Project #1-2

2018142059

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1. Schematic Diagram from Quartus II

① 8-bit ALU

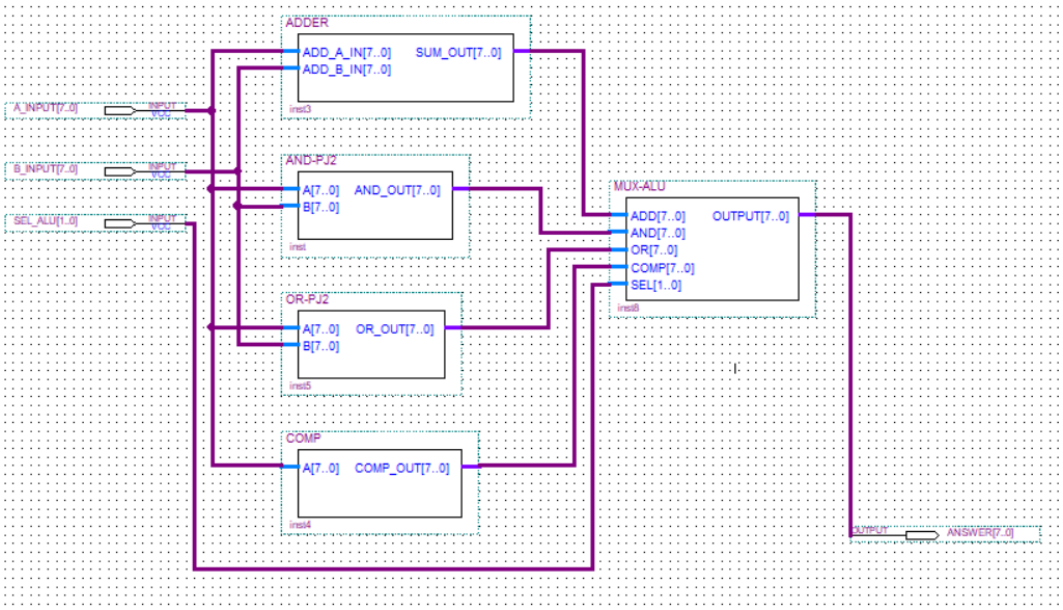

Figure 1 8-bit ALU schematic diagram

All the inputs (input A and B), SEL_ALU control input, and OUTPUTs has 8bits, every wire that connects between the blocks and the pins should be bus wire.

The ALU includes adder, and, or, complement calculation. With control input SEL_ALU, it decides which output to print out at MUX-ALU.

② OR-PJ2

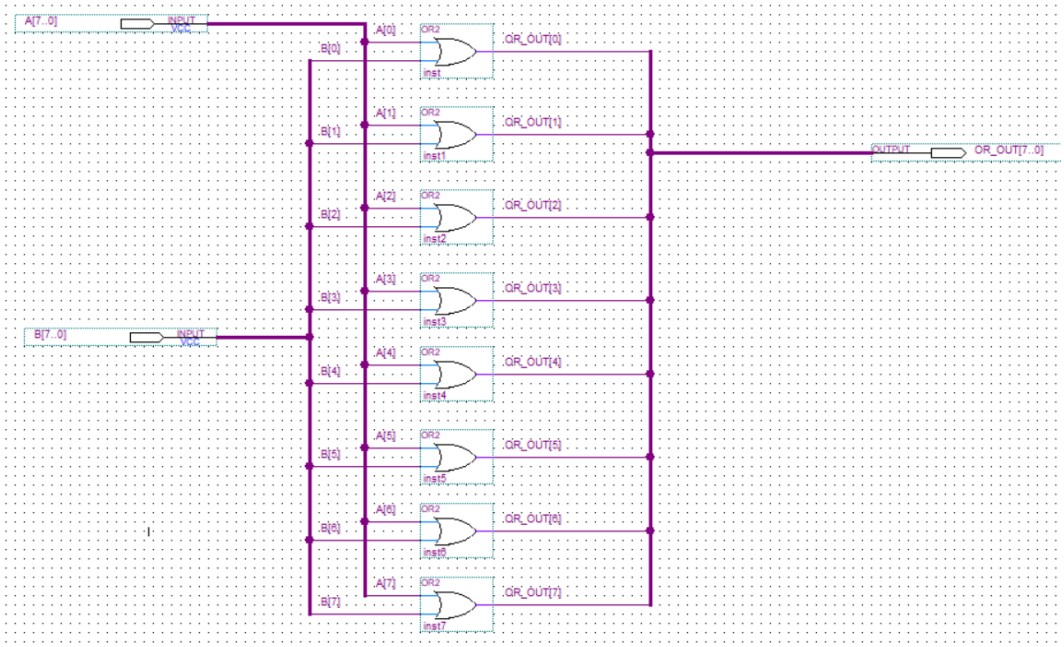

Figure 2 OR-PJ2 schematic diagram

This schematic should operate 'OR' logical operation for each bit of inputs. Therefore, OR logic symbol should be connected to each corresponding bit of A and B. Input and output wires for each OR logic symbol should be node wire. Every node wire should clarify its node name.

③ AND-PJ2

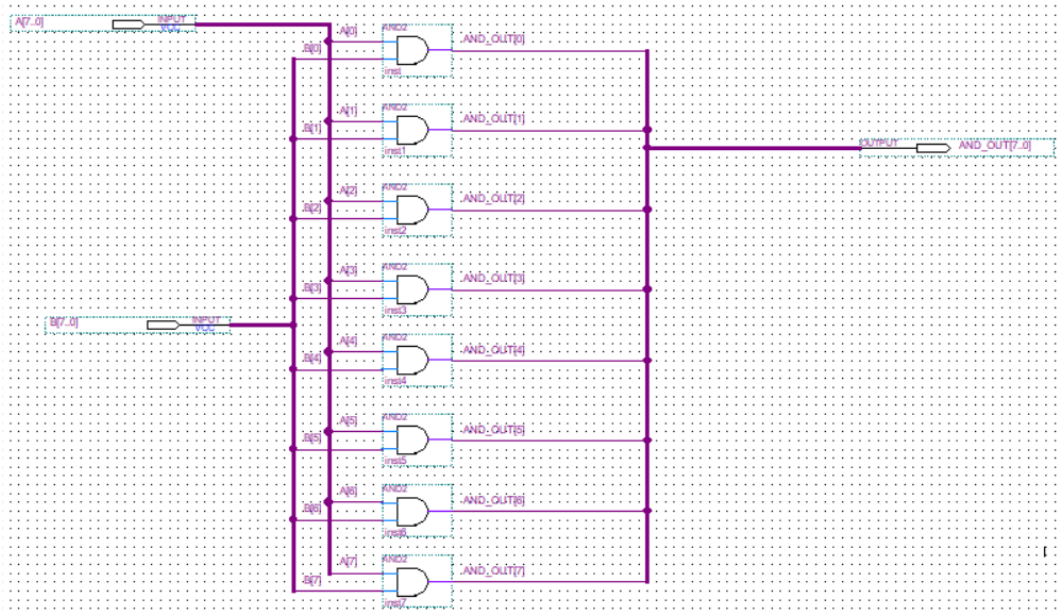

Figure 3 AND-PJ2 schematic diagram

This schematic should operate 'AND' logical operation for each bit of inputs. Therefore, AND logic symbol should be connected to each corresponding bit of A and B. Input and output wires for each AND logic symbol should be node wire.

④ ADDER

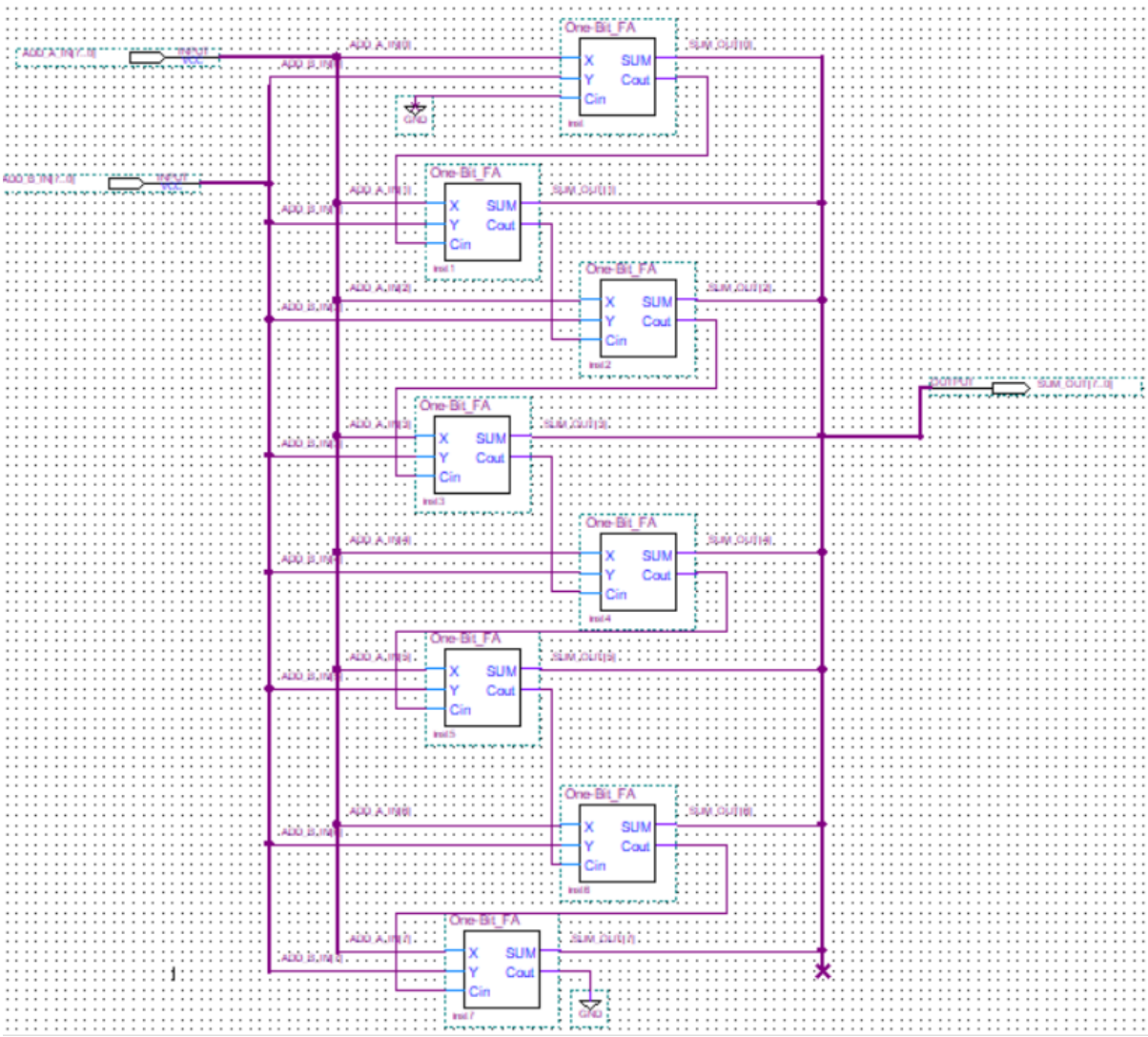

Figure 4 Adder schematic diagram

In adder, each one-bit-full-adder should get two input from input source and Carry-in input from precede one-bit-full-adder. Therefore, X and Y of each adder get input from A_IN bus wire and carry in from the precede. Each full adder has two output, sum and carry-out. Every sum output are connected to output pin, and Carry-out output are connected to next full-bit adder. Since there is no precede adder for 0^{th} full-adder and no next adder for 7^{th} full adder, both should be grounded.

⑤ MUX-ALU

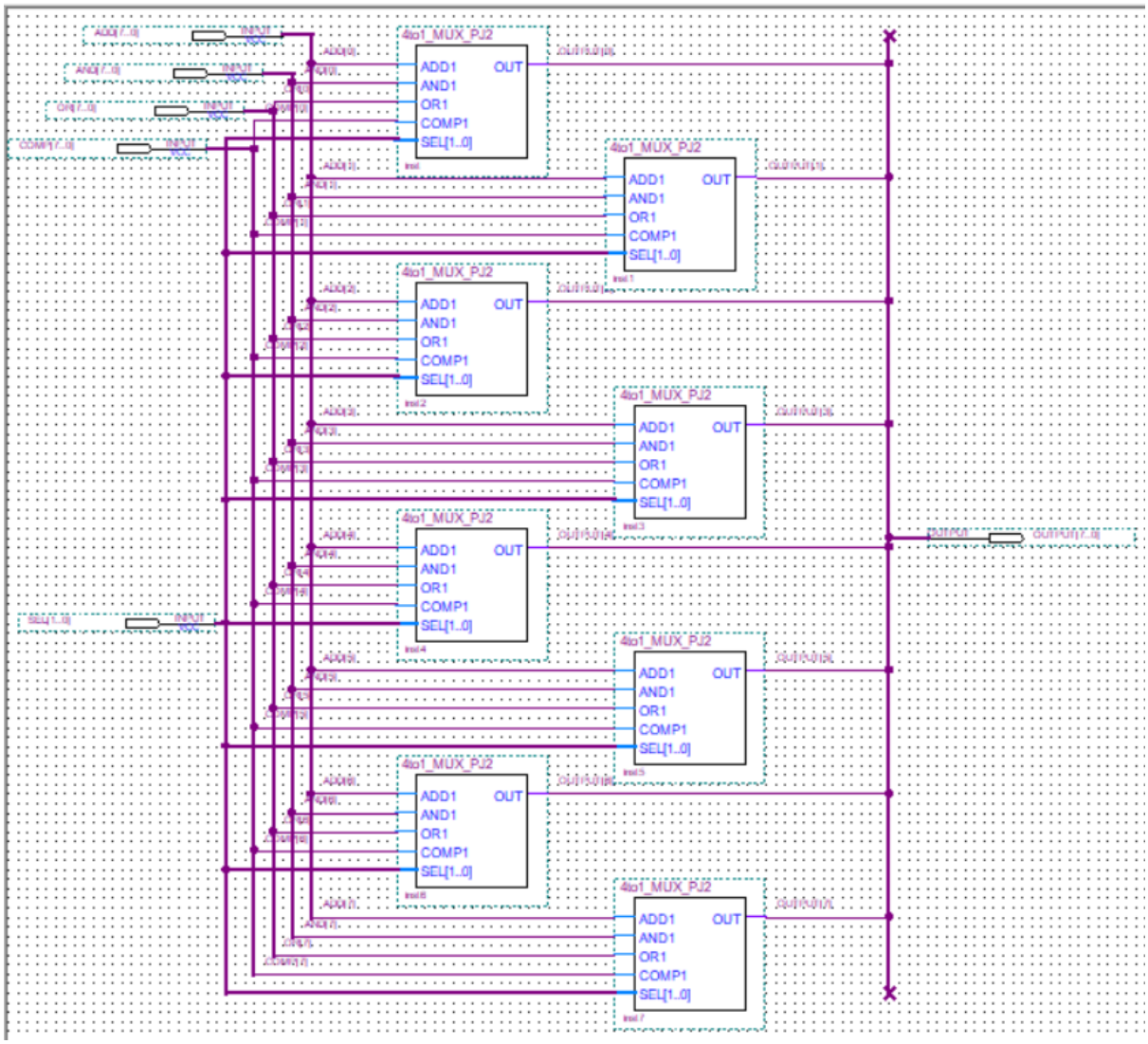

Figure 5 MUX-ALU schematic diagram

Every 4 to 1 MUX get its ADD, AND, OR, COMP, and SEL inputs. Also, outputs from 4 to 1 MUXs are combined at output pin. With the SEL input, the MUX-ALU part choose the output among the ADD, AND, OR, and COMP input.

2. Simulation

① Simulator

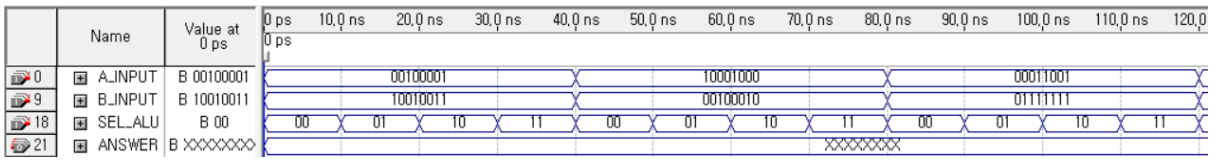

Figure 6 Simulatior (A, B input and SEL_ALU shown)

To get the results of three different simulations at once, I made the input signals A and B change their value for every 40ns. Therefore, input combination changes two times for every 40ns. Also, I put ANSWER node from pin: output to see the result of the simulation at once. Also, the simulation was in functional mode.

② Simulation Result

i) A: 00100001, B: 10010011 (0ns to 40ns)

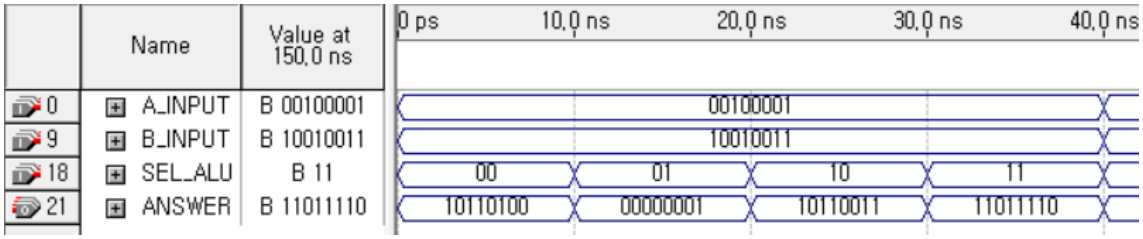

Figure 7 Simulation Result of 1st input combination (A: 00100001, B: 10010011)

ii) A: 10001000, B: 00100010 (40ns to 80ns)

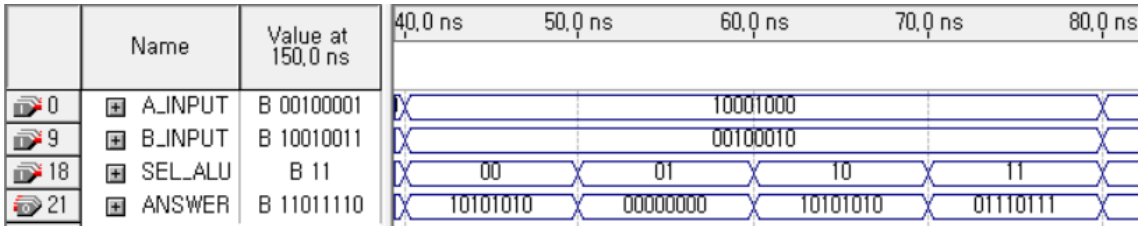

Figure 8 Simulation Result of 2nd input combination (A: 10001000, B: 00100010)

iii) A: 00011001, B: 01111111 (80ns to 120ns)

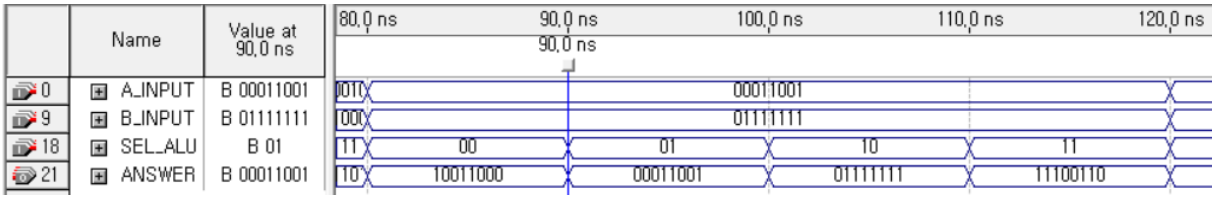

Figure 9 Simulation Result of 3rd input combination (A: 00011001, B: 01111111)

All the results and expected result I calculated is just like following table.

Input combination	SEL_ALU	Expected result	Simulation result
A: 00100001 B: 10010011 (0 to 40ns)	00 (ADD)	10110100	10110100
	01 (AND)	00000001	00000001
	10 (OR)	10110011	10110011
	11 (A Complement)	11011110	11011110
A: 10001000 B: 00100010 (40ns to 80ns)	00 (ADD)	10101010	10101010
	01 (AND)	00000000	00000000
	10 (OR)	10101010	10101010
	11 (A Complement)	01110111	01110111
A: 00011001 B: 01111111 (80ns to 120ns)	00 (ADD)	10011000	10011000
	01 (AND)	00011001	00011001
	10 (OR)	01111111	01111111
	11 (A Complement)	11100110	11100110

Figure 10 Expected and Simulation Output of each input combination

Since every expected result and corresponding simulation result has same values, the ALU schematic works well.

3. Discussion

In the project, there were largely two part was given. The first part was to complete all the schematic in the 8-bit ALU. During the process, especially in adder and mux schematic which are complicated, arranging wires regularly was helpful not to get confused.

The second part was simulating the whole schematic and comparing the simulation result with the calculated result. Since there was no difference, the ALU would be designed properly. Also, I put ANSWER node in pin: output while designing simulator. As I didn't do it on project 1-1, there was difficulty to read the output. With this project, my Quartus II skill is improved.