Experiment #1 - Clock and Periodic Signal Generation

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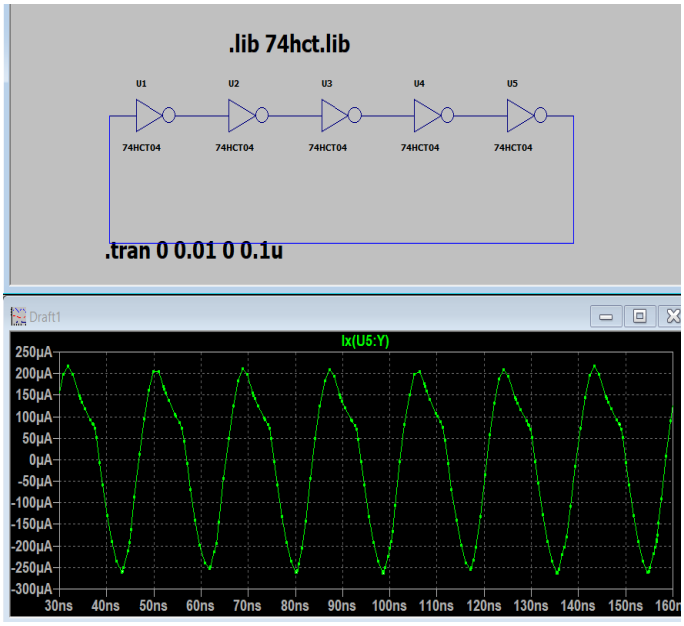
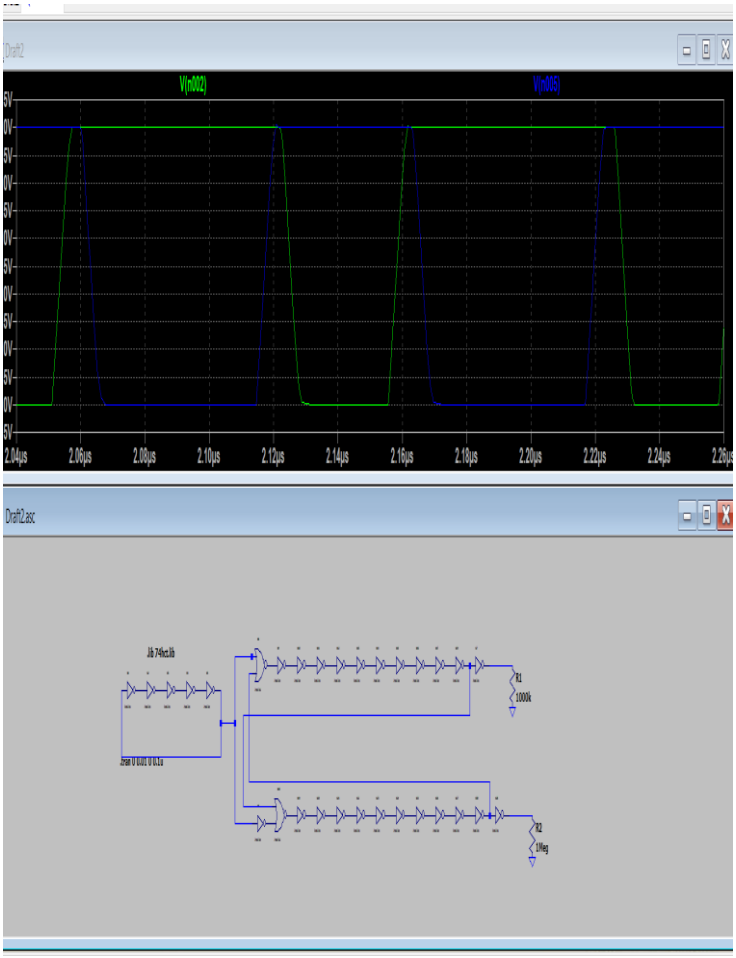
1_ clock generation using ICs and analog components

1.1 Ring oscillator



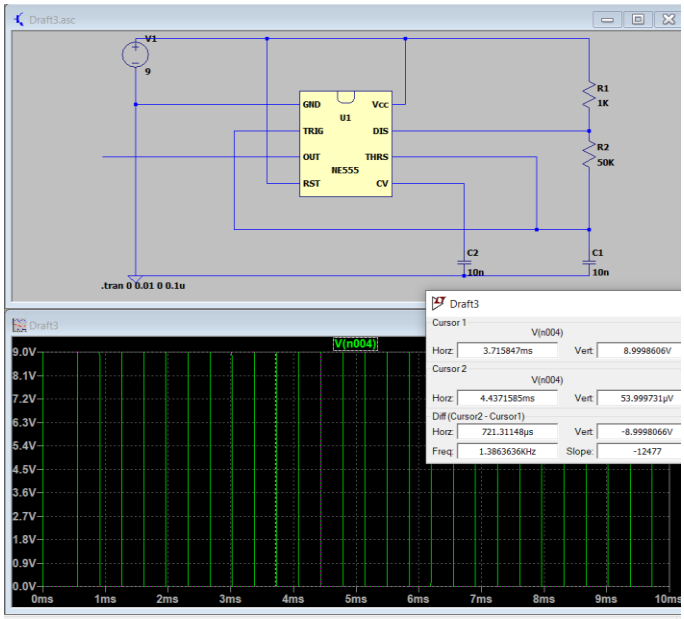
1) T = 98.56ns – 80.19ns = 18.37 ns
   f = 1/T = 1000/18.37 * 10^6 = 54.43 MHz
2) T = 2*N* ∗ *Delay of each inv = 2*5* X =18.37 ns*
   Delay of each inv = 1.837 ns

1.1.2 Two-phase clock generator



در واقع ما اینجا یه flip-flopداریم و همان طور که میدانیم خروجی ها flip-flopعکس هم هستند یعنی اگه یکی شون Q باشه دیگر Qbarمیباشد. پس بدین شکل دوتا کلاک درست میکنیم که فاز هاشون باهم فرق میکنه و اشتراکی نداره.البته اگه دقت کنیم در نقاط مرزی (rise,fall) ، اندکی اشتراک وجود دارد که اون به خاطر دیلی componentها هست(inv). و همچنین به خاطر اینکه کلی گیت جلوی Ring oscقرار دارد دیگه کلاک 18nsنمیباشد.

1.2 LM555 timer



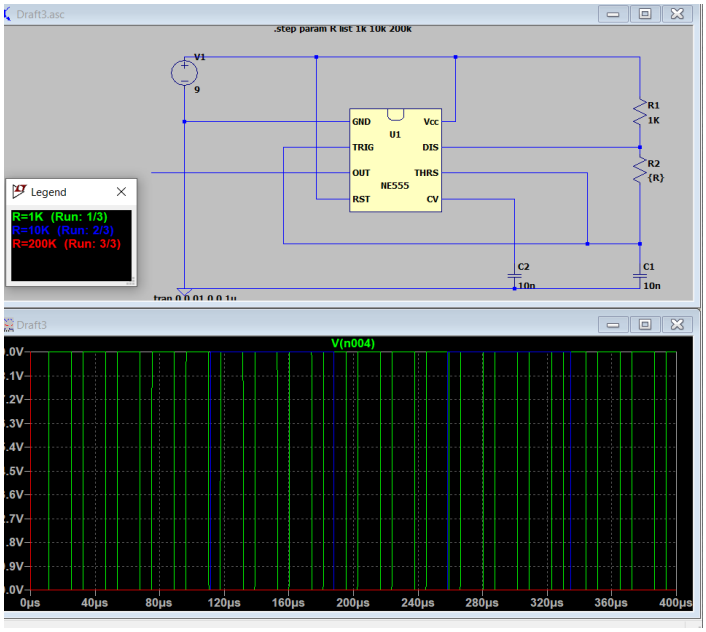
1)

R2 = 50k
T = 4.437ms – 3.715ms = 0.727 = 0.73ms
Frequency = 1 / T = 1.3755 = 1.4 kHz
Duty cycle = (4.437 – 4.0804.437) / T = 0.491%

T = 0.693 * (R1 + 2R2) * C;
duty cycle = (R1 + R2) / (R1+2R2);
R2 = 200k
T = 5.020 – 2.220 = 2.8ms
Expected T = $0.693 * (1k + 400\text{k}) * 10n = 2.778ms$
Frequency = 1 / T = 357Hz
Expected frequency = 359.9Hz
Duty cycle = 1.39 / T = 49.85%
Expected Duty cycle = (200+1) / (1+400) =50.12%

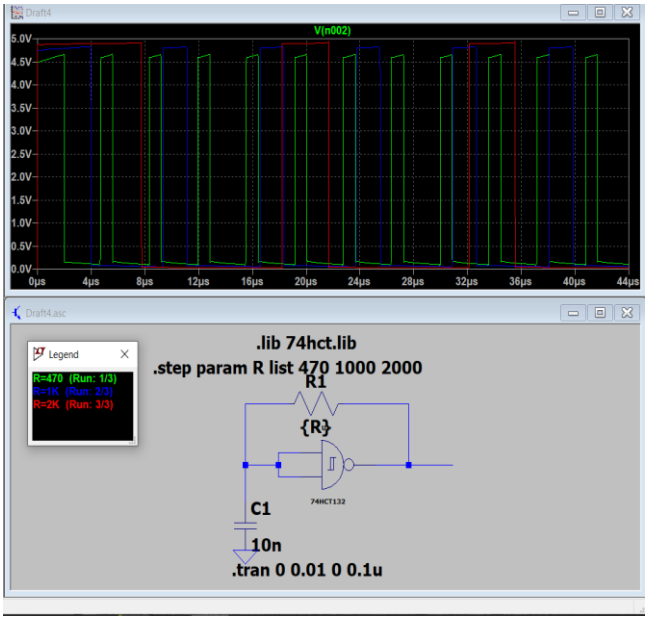
R2 = 10k
T = 0.405 - 0.258 = 0.147ms
Expected T = $0.693 * (1k + 20\text{k}) * 10nF = 0.145ms$
Frequency = 1/ T = 6.8kHz
Expected frequency = 6.871kHz
Duty cycle = 0.076 / 0.147 = 51.7%
Expected Duty cycle = (10+1) / (1+20) =52.38%

R2 = 1k
T = 0.0211ms
Expected T = $0.693 * (1k + 2\text{k}) * 10nF = 0.02ms$
Frequency = 1/ T = 47.619kHz
Expected frequency = 48.1kHz
Duty cycle = 0.0139 / T = 66.19%
Expected Duty cycle = (1+1) / (1+2) = 66.6%



1.3 Schmitt Trigger Oscillator

1)



2)

f = a / RC => a = f * RC
c = 10nf

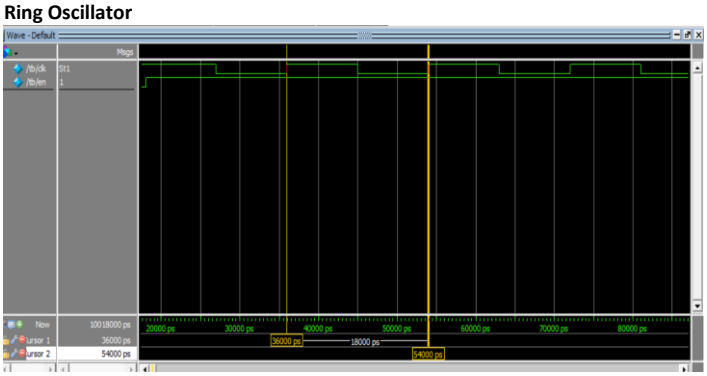
R = 470
freq = 1/T ;T = 3.6us
Frequency = 277.777kHz
α = 1.3

R = 1000
freq = 1/T ;T = 7.138us
Frequency = 140kHz
α = 1.4

R = 2000
freq = 1/T ;T = 13.8us
Frequency = 72.45kHz
α = 1.45

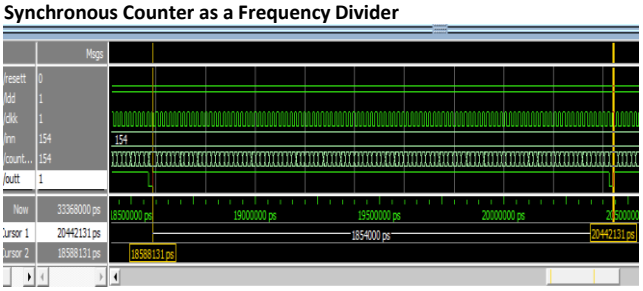
2 FPGA Design

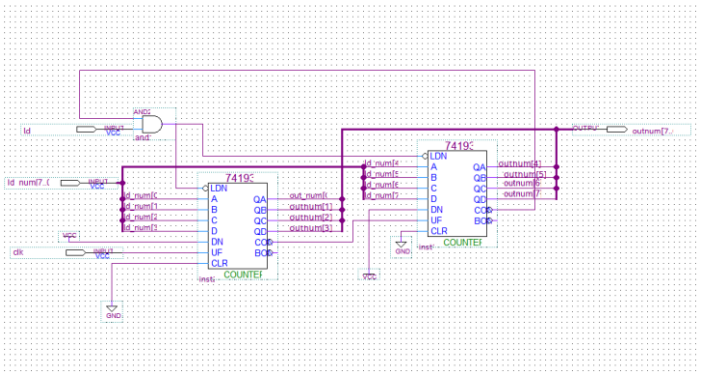
2.1 Ring Oscillator



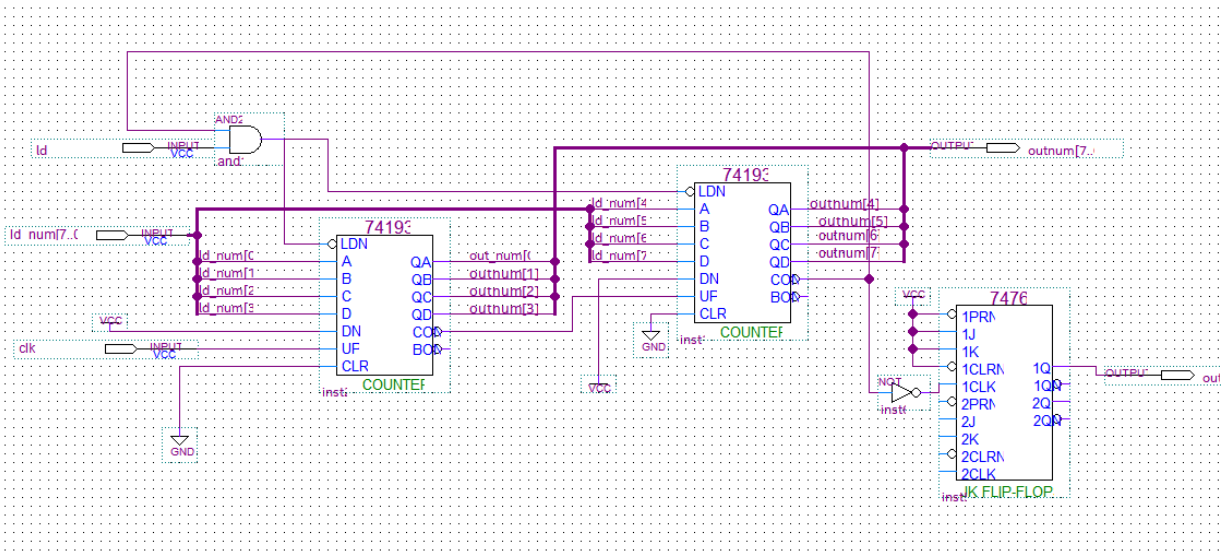
T = 18 ns
Frequency = 55.55555 = 55.6MHz

2.2 Synchronous Counter as a Frequency Divider





2.3 T Flip-Flop



(hint: to convert j-k flip flop to t flip flop we should connect j and k to one signal)