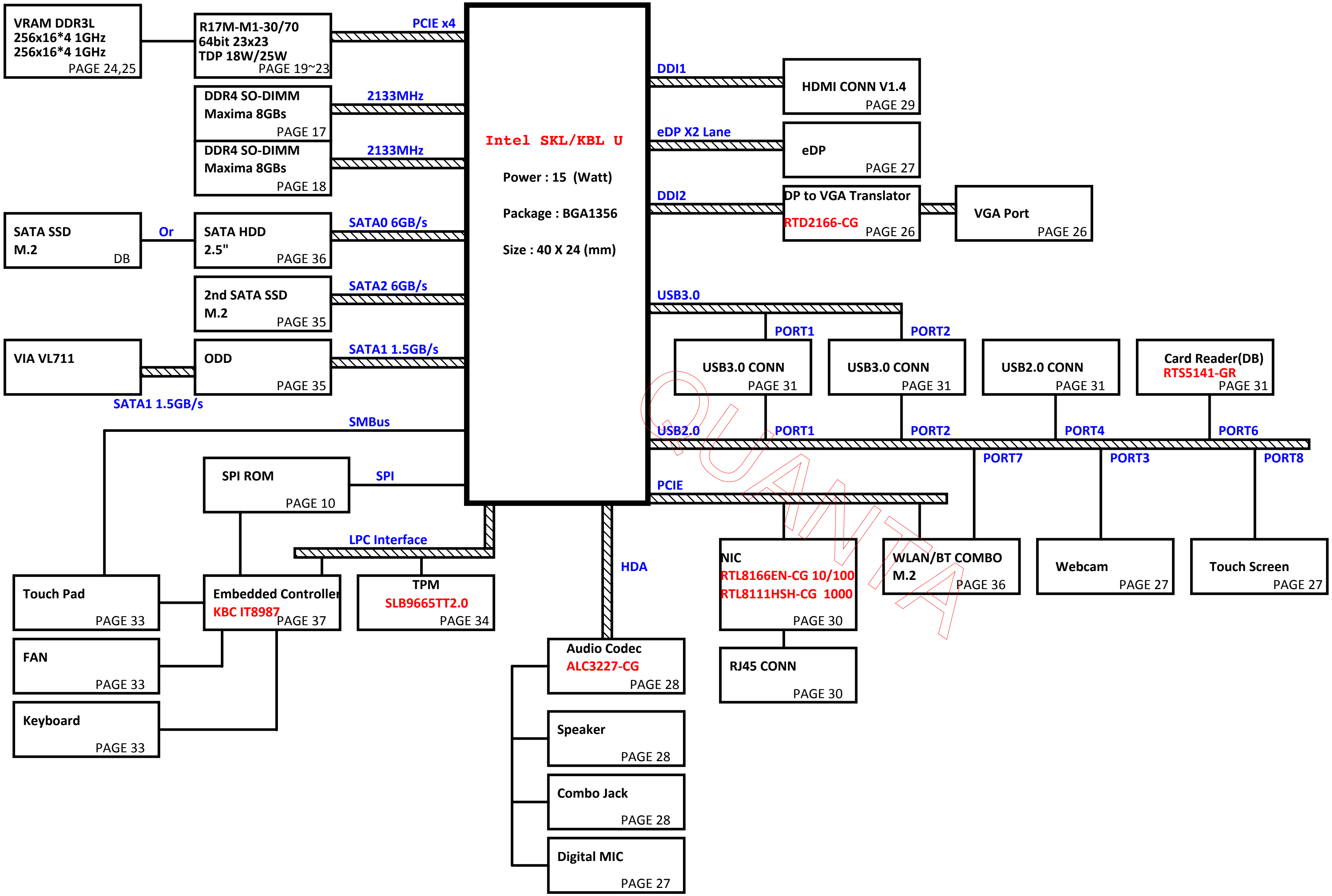
Intel SKL-U/KBL-U Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Block Diagram**	1A

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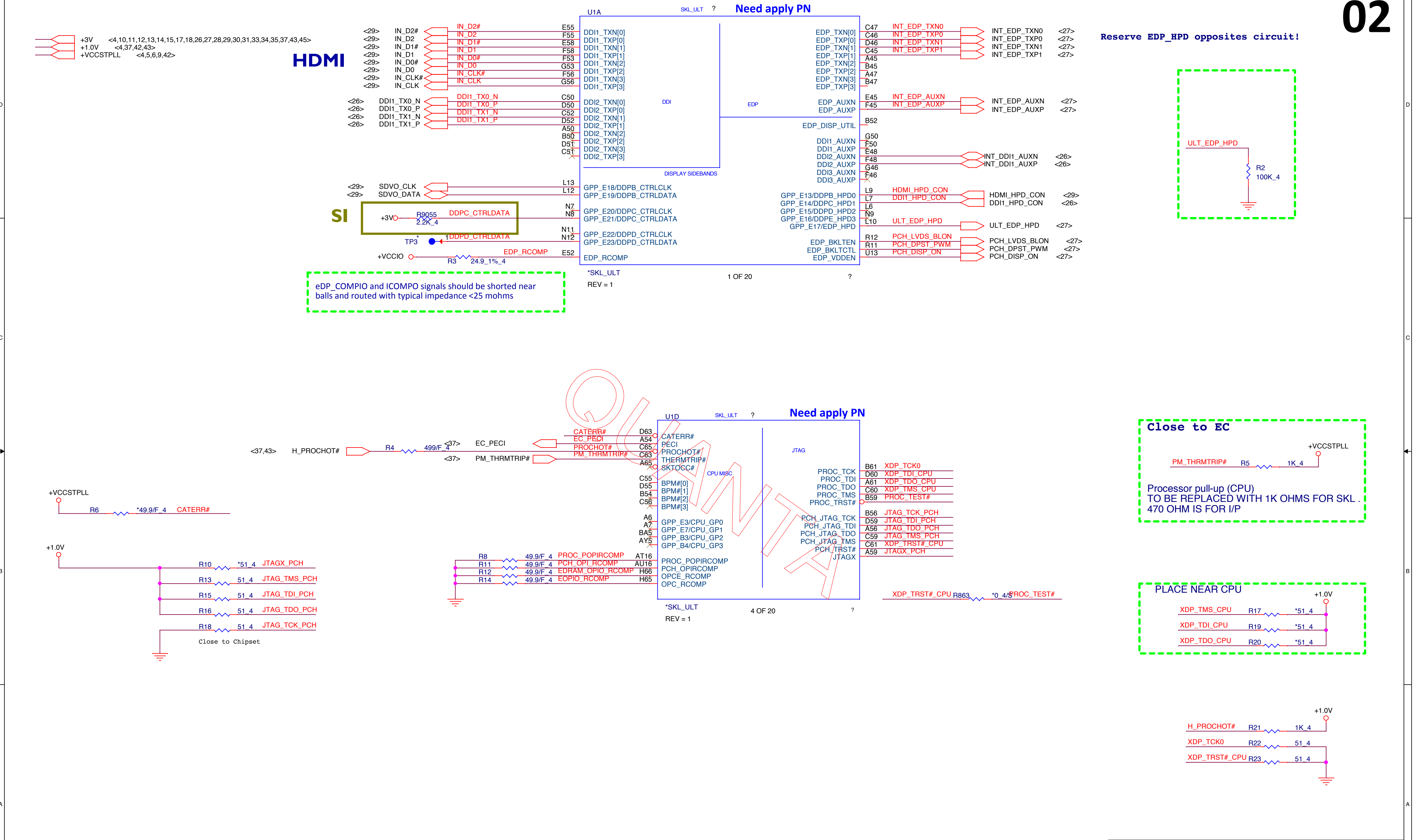
+3V <4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
+1.0V <4,37,42,43>
+VCCSTPLL <4,5,6,9,42>
HDMI
U1A
SKL_ULT
Need apply PN
IN_D2# IN_D2 IN_D1# IN_D1 IN_D0# IN_D0 IN_CLK# IN_CLK <29>
DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]
DDI1_TX0_N DDI1_TX0_P DDI1_TX1_N DDI1_TX1_P <26>
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]
DDI
EDP
DISPLAY SIDEBANDS
EDP_TXN[0] EDP_TXP[0] EDP_TXN[1] EDP_TXP[1] EDP_TXN[2] EDP_TXP[2] EDP_TXN[3] EDP_TXP[3]
INT_EDP_TXN0 INT_EDP_TXP0 INT_EDP_TXN1 INT_EDP_TXP1 <27>
EDP_AUXN EDP_AUXP
INT_EDP_AUXN INT_EDP_AUXP <27>
EDP_DISP_UTIL
DDI1_AUXN DDI1_AUXP DDI2_AUXN DDI2_AUXP DDI3_AUXN DDI3_AUXP
INT_DDI1_AUXN INT_DDI1_AUXP <26>
SDVO_CLK SDVO_DATA <29>
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
SI
+3V R9055 2.2K_4 DDPC_CTRLDATA
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
TP3 DDPD_CTRLDATA
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA
+VCCIO R3 24.9_1%_4 EDP_RCOMP
GPP_E13/DDPB_HPD0 GPP_E14/DDPC_HPD1 GPP_E15/DDPD_HPD2 GPP_E16/DDPE_HPD3 GPP_E17/EDP_HPD
HDMI_HPD_CON <29>
DDI1_HPD_CON <26>
ULT_EDP_HPD <27>
EDP_BKLTEN EDP_BKLTCTL EDP_VDDEN
PCH_LVDS_BLON PCH_DPST_PWM PCH_DISP_ON <27>
*SKL_ULT
REV = 1
1 OF 20
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
Reserve EDP_HPD opposites circuit!
ULT_EDP_HPD R2 100K_4
U1D
Need apply PN
CATERR# PECI PROCHOT# THERMTRIP# SKTOCC#
EC_PECI <37>
<37,43> H_PROCHOT# R4 499/F_4
PM_THRMTRIP# <37>
CPU MISC
BPM#[0] BPM#[1] BPM#[2] BPM#[3]
GPP_E3/CPU_GP0 GPP_E7/CPU_GP1 GPP_B3/CPU_GP2 GPP_B4/CPU_GP3
R8 R11 R12 R14 49.9/F_4
PROC_POPIRCOMP PCH_OPI_RCOMP EDRAM_OPIO_RCOMP EOPIO_RCOMP
PROC_POPIRCOMP PCH_OPIRCOMP OPCE_RCOMP OPC_RCOMP
JTAG
PROC_TCK PROC_TDI PROC_TDO PROC_TMS PROC_TRST#
XDP_TCK0 XDP_TDI_CPU XDP_TDO_CPU XDP_TMS_CPU PROC_TEST#
PCH_JTAG_TCK PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TMS PCH_TRST# JTAGX
JTAG_TCK_PCH JTAG_TDI_PCH JTAG_TDO_PCH JTAG_TMS_PCH XDP_TRST#_CPU JTAGX_PCH
XDP_TRST#_CPU R863 *0_4/S PROC_TEST#
*SKL_ULT
REV = 1
4 OF 20
+VCCSTPLL R6 *49.9/F_4 CATERR#
+1.0V R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset
Close to EC
+VCCSTPLL PM_THRMTRIP# R5 1K_4
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P
PLACE NEAR CPU
+1.0V XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4
+1.0V H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4
QUANTA

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PROJECT : 0P1B
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Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A

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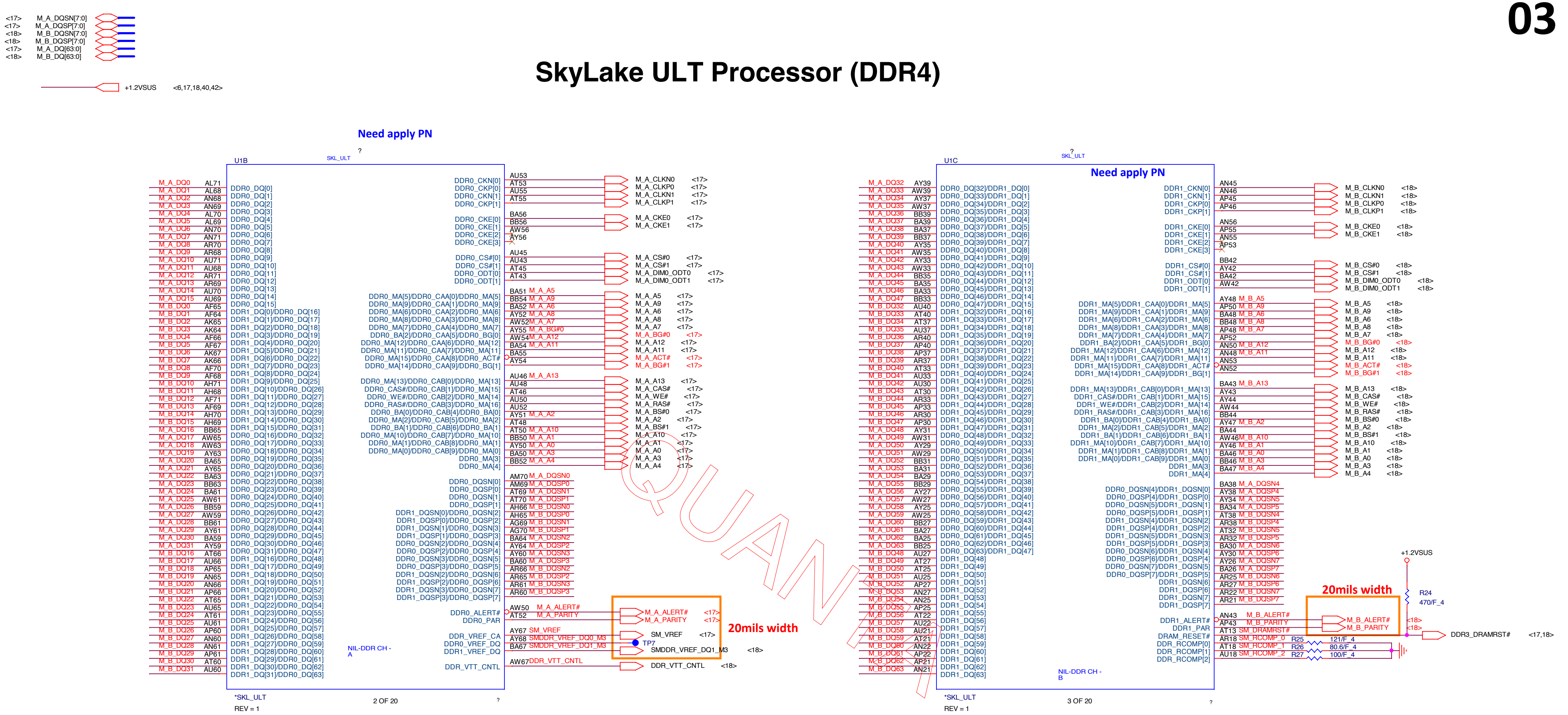
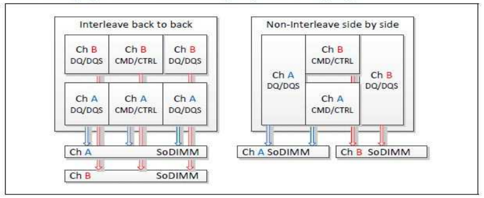
SkyLake ULT Processor (DDR4)



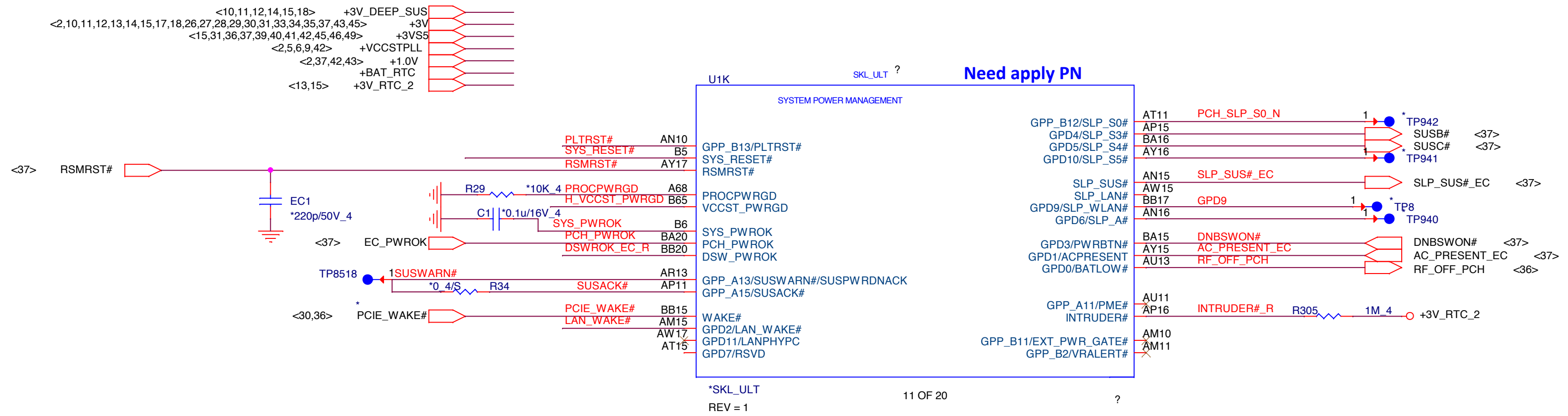
Interleave (IL) and Non-Interleave (NIL) Modes Mapping



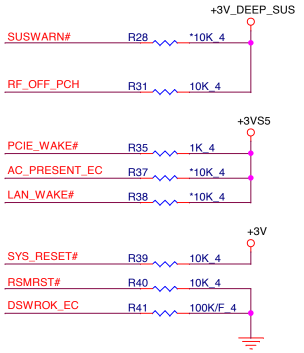
PROJECT : 0P1B
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	03 -- SKYLAKE 2/15(DDR4 I/F)	1A

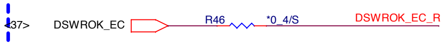
Date: Wednesday, March 08, 2017 Sheet 3 of 51



PCH Pull-high/low(CLG)

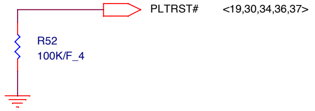


For DS3 Sequence

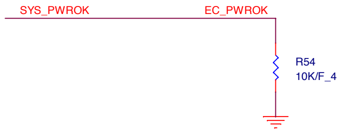


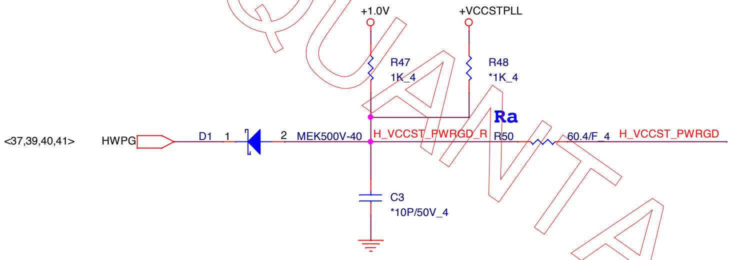
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

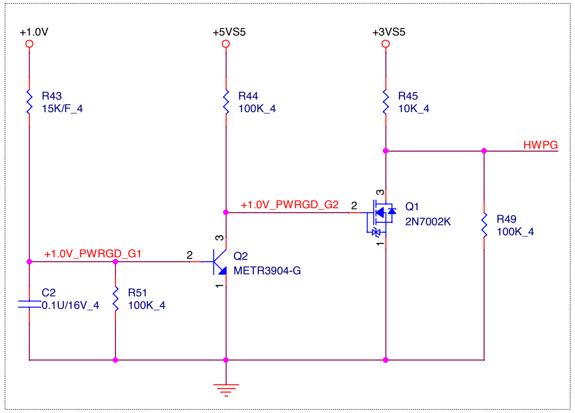


System PWR_OK(CLG)





Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

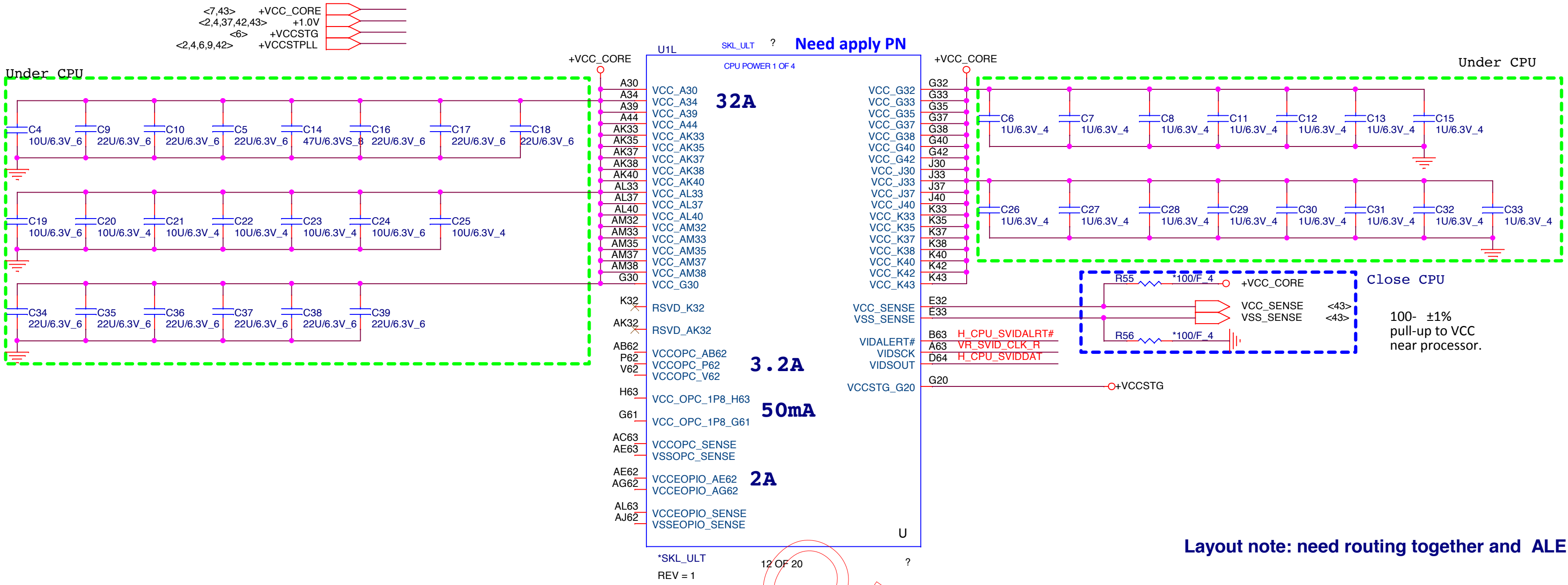


NB5

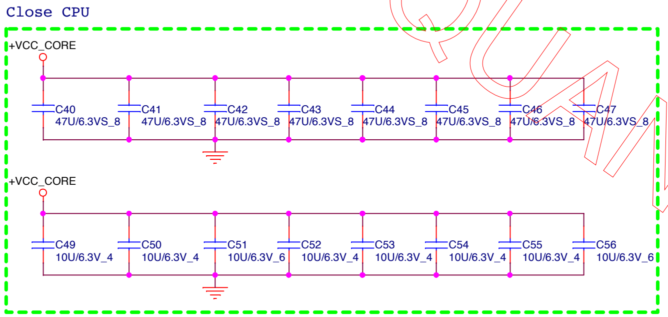
PROJECT : 0P1B
Quanta Computer Inc.

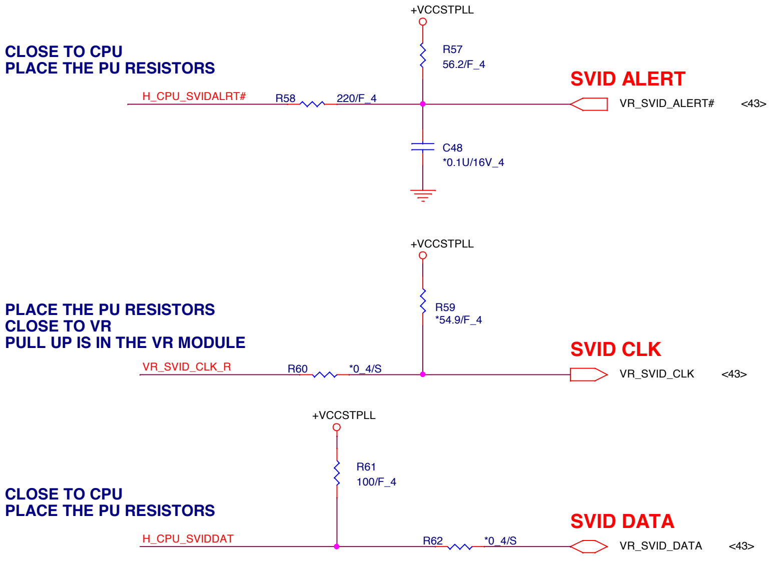
Size	Document Number	Rev
Custom	04 -- SKYLAKE 3/15(PowerManger)	1A

Date: Wednesday, March 08, 2017 Sheet 4 of 51



Layout note: need routing together and ALERT need between CLK and DATA.





Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
V_{CCGT}	Processor Graphics Power Rails	SVID
V_{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V_{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V_{CCIO}	IO Power Rail	Fixed
V_{CCST}	Sustain Power Rail	Fixed
V_{CCPLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V_{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V_{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CCEOPIO}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

PROJECT : 0P1B
Quanta Computer Inc.
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Size	Document Number	Rev
Custom	05 -- SKYLAKE 4/15 (POWER-1)	1A

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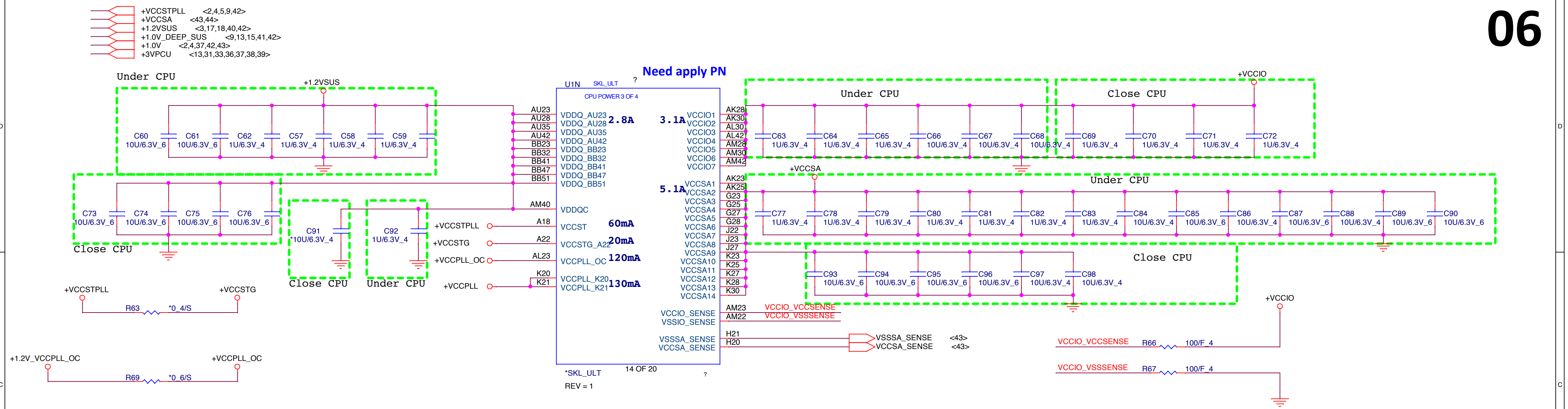

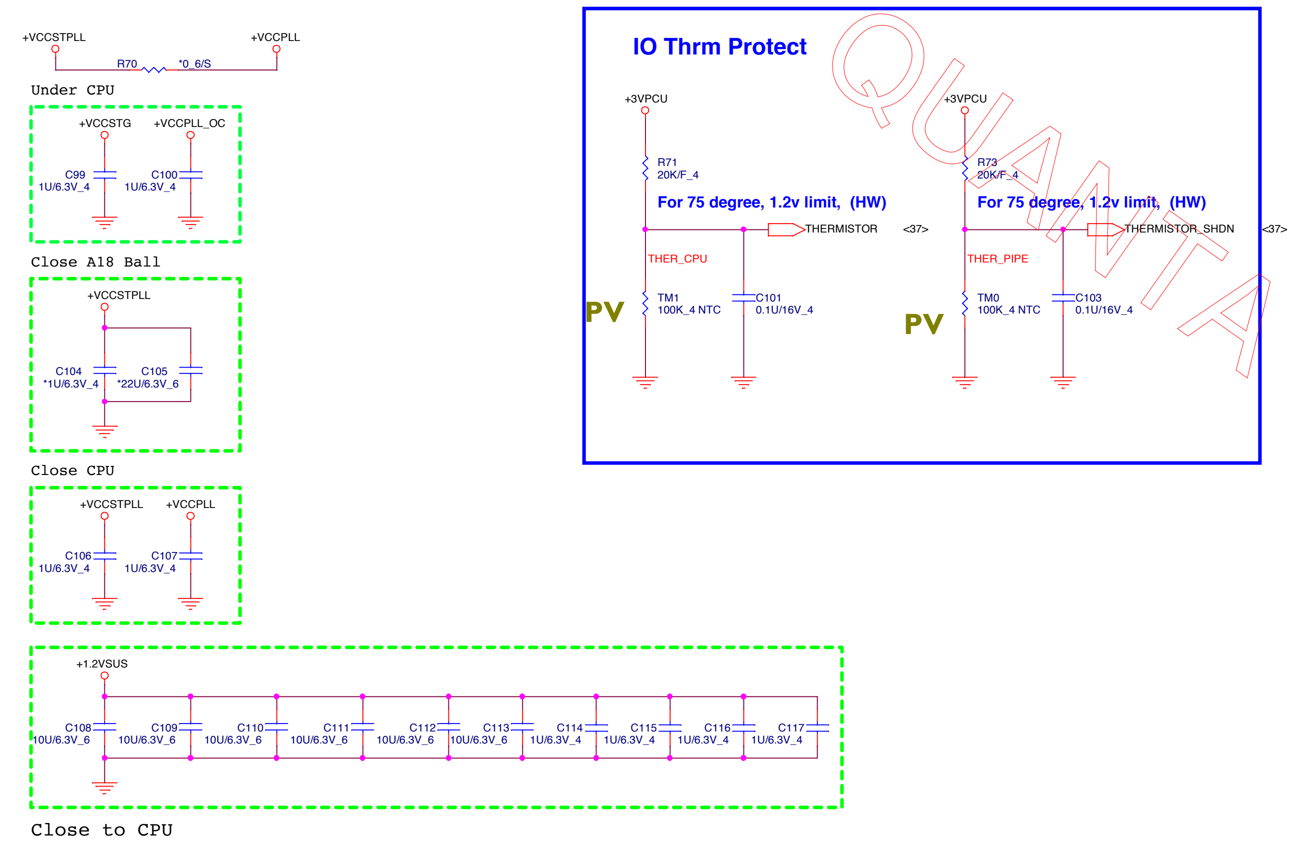

Close to CPU

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size: Custom
Document Number: 06 -- SKYLAKE 5/15 (POWER-2)
Rev: 1A
Date: Wednesday, March 08, 2017
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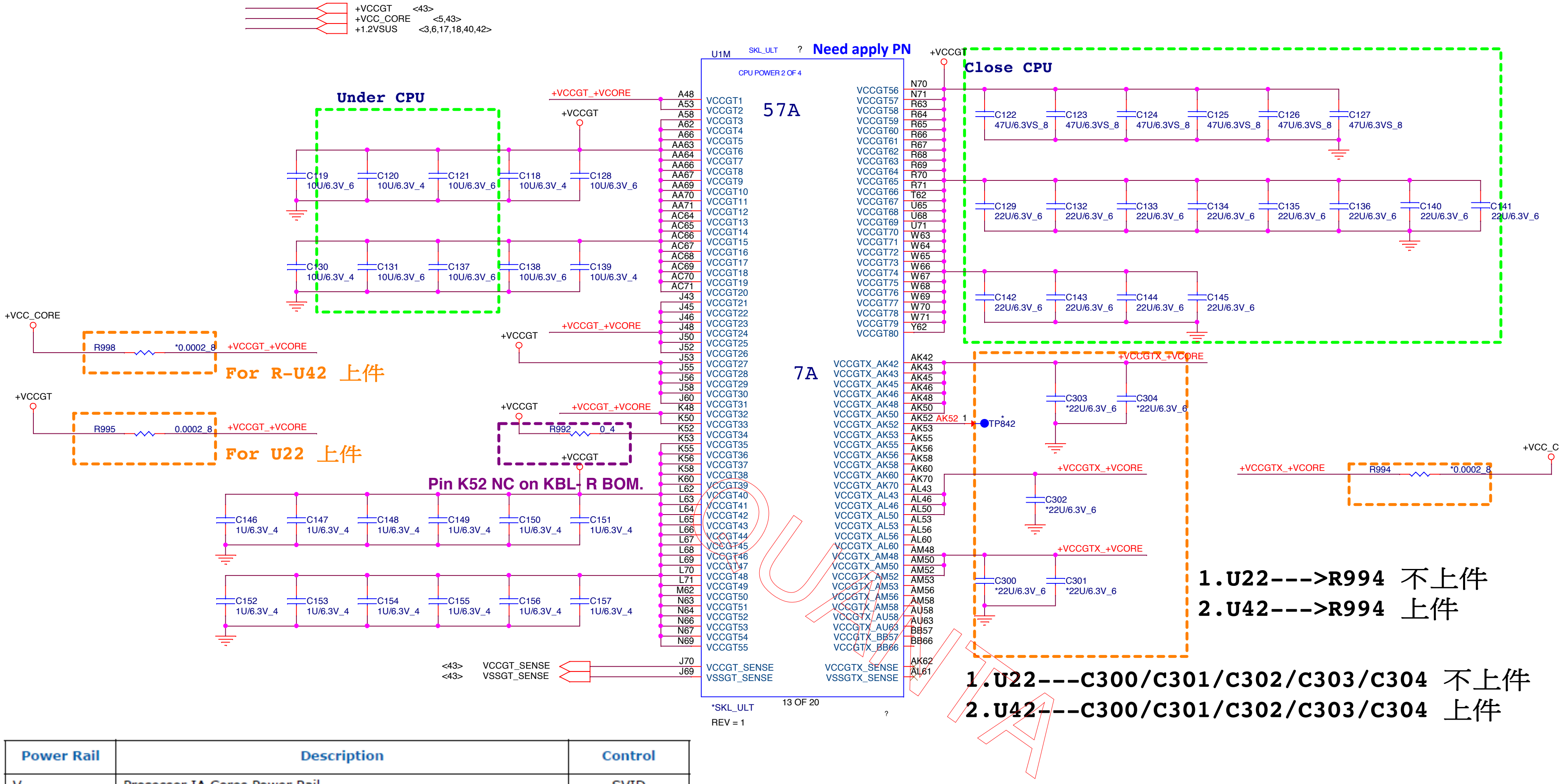

Need apply PN

For R-U42 上件

For U22 上件

Pin K52 NC on KBL- R BOM.

1.U22--->R994 不上件
2.U42--->R994 上件

1.U22---C300/C301/C302/C303/C304 不上件
2.U42---C300/C301/C302/C303/C304 上件

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size: Custom
Document Number: 07 -- SKYLAKE 6/15 (POWER-3)
Rev: 1A
Date: Wednesday, March 08, 2017
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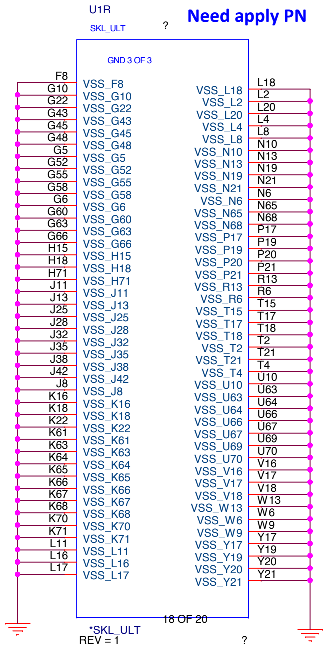

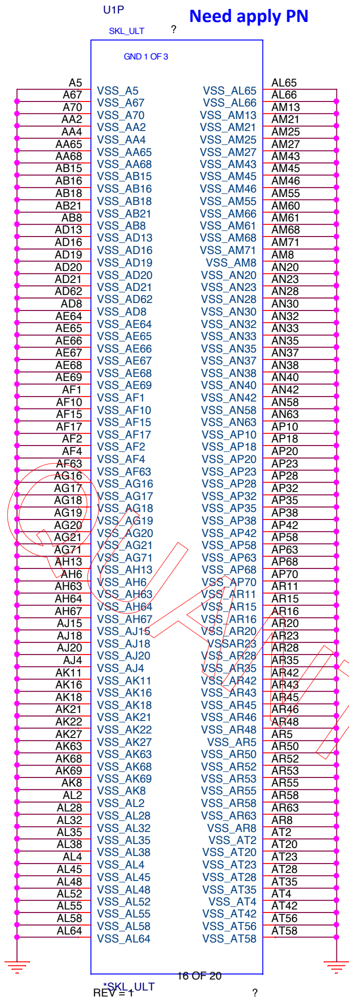

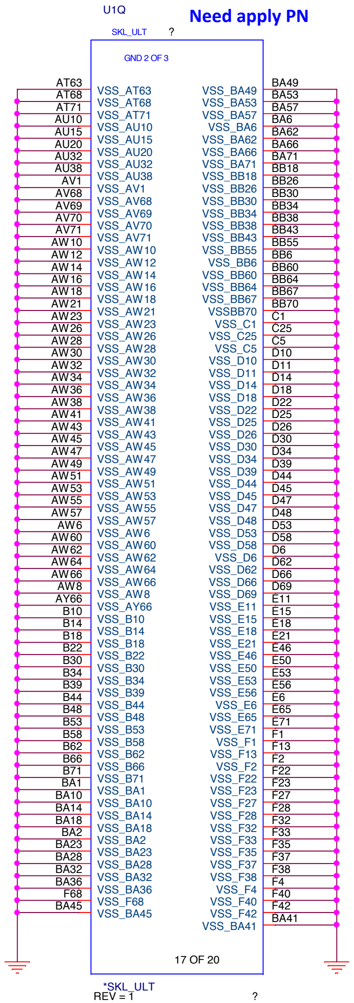

PROJECT : 0P1B
Quanta Computer Inc.

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Size	Document Number	Rev
Custom	**08 -- SKYLAKE 7/15 (GND)**	1A

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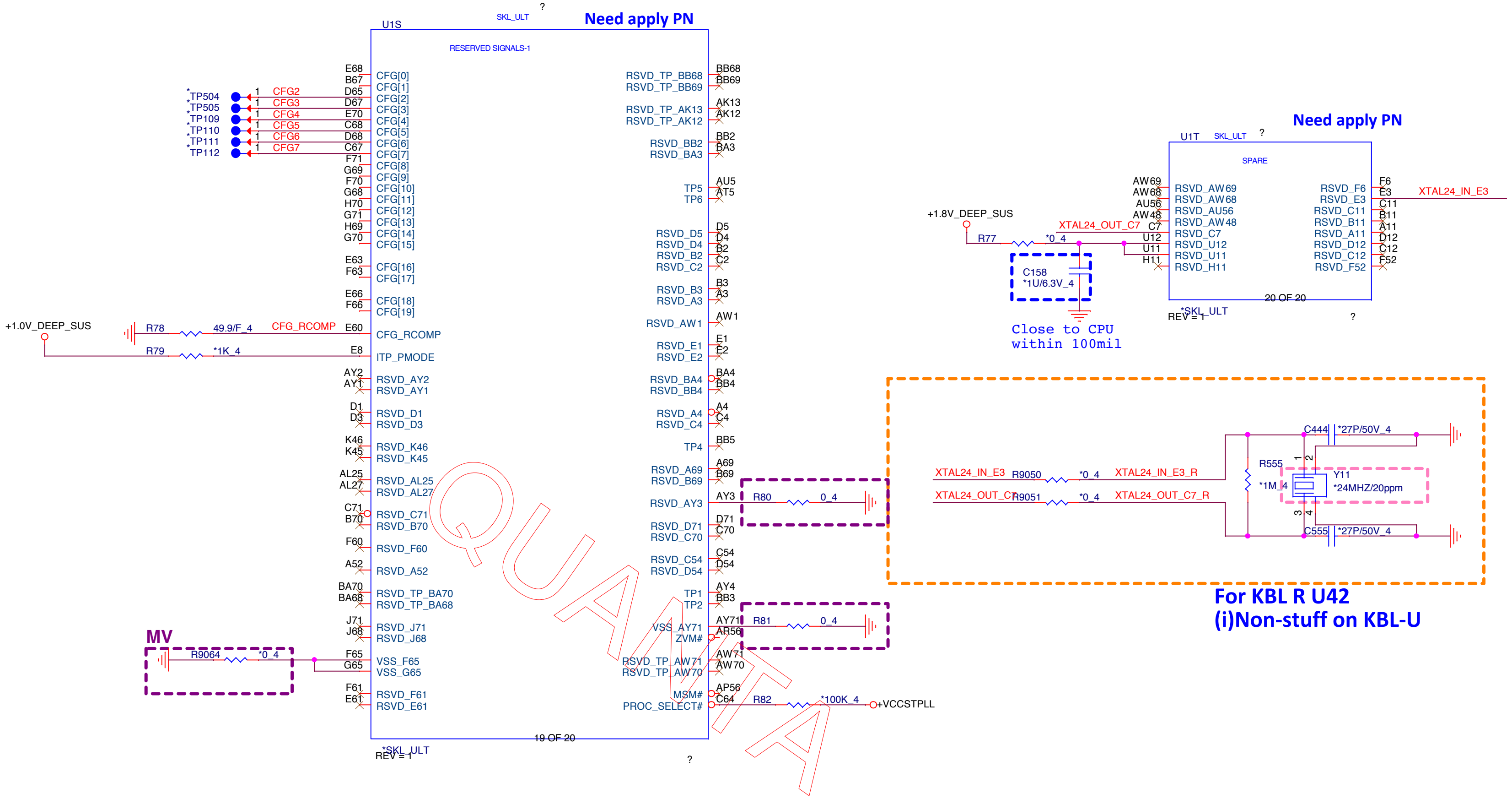

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

PROJECT : 0P1B
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

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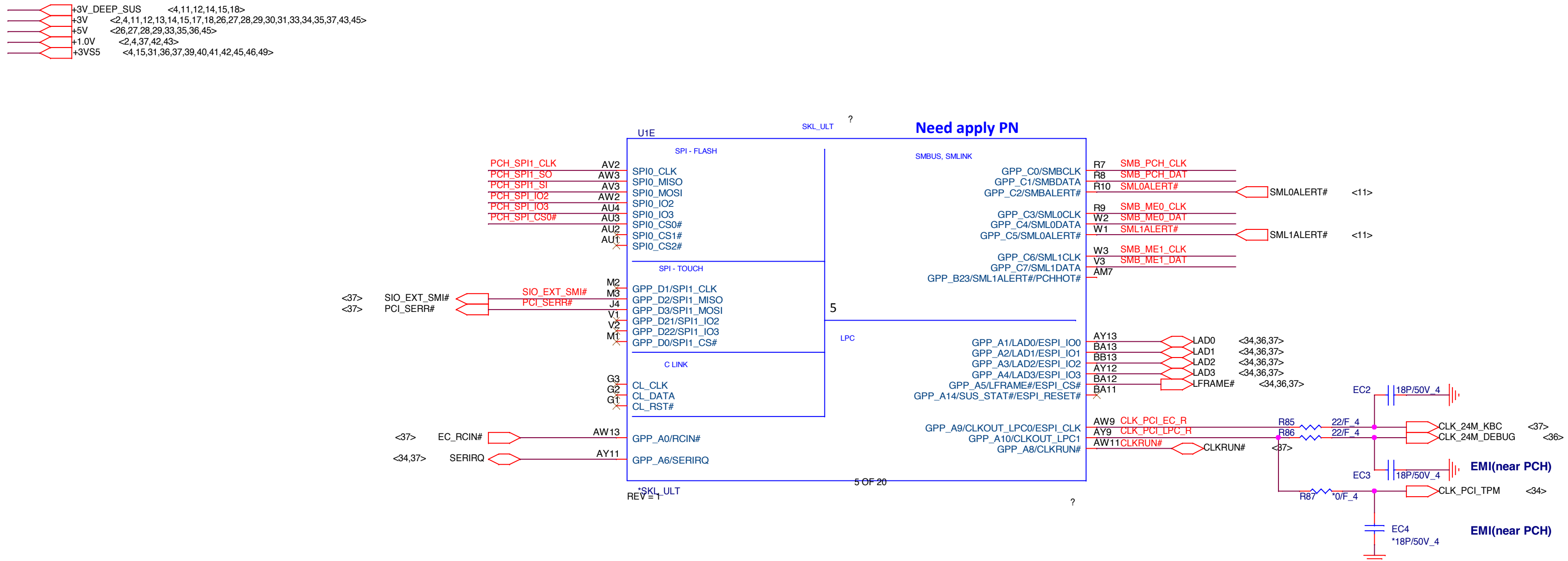
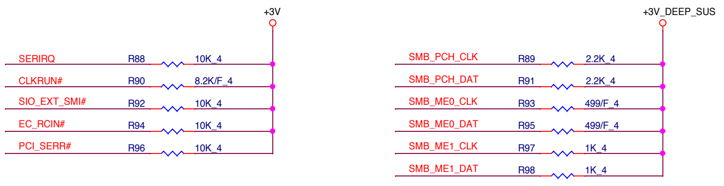
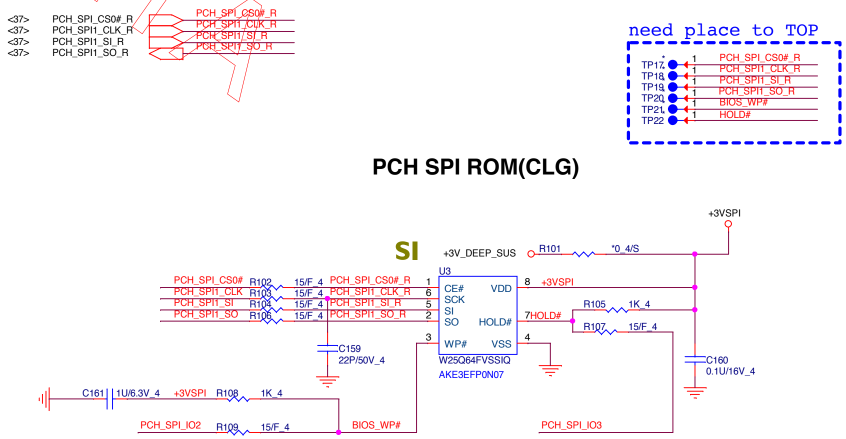

+3V_DEEP_SUS <4,11,12,14,15,18>
+3V <2,4,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
+5V <26,27,28,29,33,35,36,45>
+1.0V <2,4,37,42,43>
+3VS5 <4,15,31,36,37,39,40,41,42,45,46,49>
U1E
SKL_ULT
Need apply PN
SPI - FLASH
PCH_SPI1_CLK AV2 SPI0_CLK
PCH_SPI1_SO AW3 SPI0_MISO
PCH_SPI1_SI AV3 SPI0_MOSI
PCH_SPI_IO2 AW2 SPI0_IO2
PCH_SPI_IO3 AU4 SPI0_IO3
PCH_SPI_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#
SPI - TOUCH
M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#
<37> SIO_EXT_SMI#
<37> PCI_SERR#
C LINK
G3 CL_CLK
G2 CL_DATA
G1 CL_RST#
<37> EC_RCIN# AW13 GPP_A0/RCIN#
<34,37> SERIRQ AY11 GPP_A6/SERIRQ
SMBUS, SMLINK
GPP_C0/SMBCLK R7 SMB_PCH_CLK
GPP_C1/SMBDATA R8 SMB_PCH_DAT
GPP_C2/SMBALERT# R10 SMLOALERT# SMLOALERT# <11>
GPP_C3/SML0CLK R9 SMB_ME0_CLK
GPP_C4/SML0DATA W2 SMB_ME0_DAT
GPP_C5/SML0ALERT# W1 SML1ALERT# SML1ALERT# <11>
GPP_C6/SML1CLK W3 SMB_ME1_CLK
GPP_C7/SML1DATA V3 SMB_ME1_DAT
GPP_B23/SML1ALERT#/PCHHOT# AM7
LPC
GPP_A1/LAD0/ESPI_IO0 AY13 LAD0 <34,36,37>
GPP_A2/LAD1/ESPI_IO1 BA13 LAD1 <34,36,37>
GPP_A3/LAD2/ESPI_IO2 BB13 LAD2 <34,36,37>
GPP_A4/LAD3/ESPI_IO3 AY12 LAD3 <34,36,37>
GPP_A5/LFRAME#/ESPI_CS# BA12 LFRAME# <34,36,37>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11
GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI_EC_R R85 22/F_4 CLK_24M_KBC <37>
GPP_A10/CLKOUT_LPC1 AY9 CLK_PCI_LPC_R R86 22/F_4 CLK_24M_DEBUG <36>
GPP_A8/CLKRUN# AW11 CLKRUN# CLKRUN# <37>
EC2 18P/50V_4
EC3 18P/50V_4
EMI(near PCH)
R87 *0/F_4 CLK_PCI_TPM <34>
EC4 *18P/50V_4
EMI(near PCH)
5 OF 20
*SKL_ULT
REV = 1

GPIO Pull UP

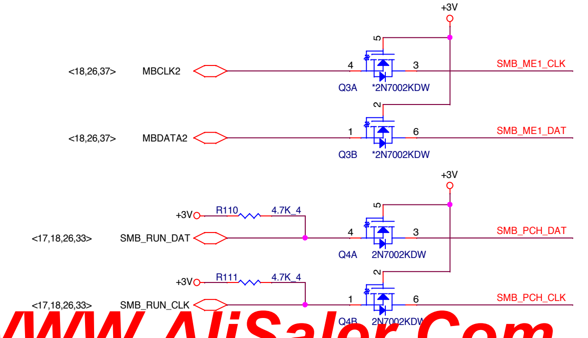


PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023



SMBus/Pull-up(CLG)



CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

NB5
PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE 09/15(SPI/LPC/SM)	1A

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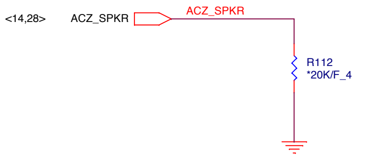
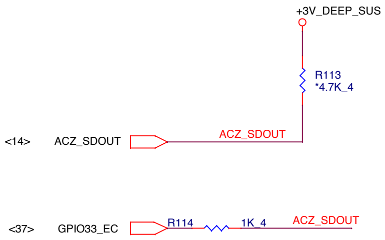
Functional Strap Definitions

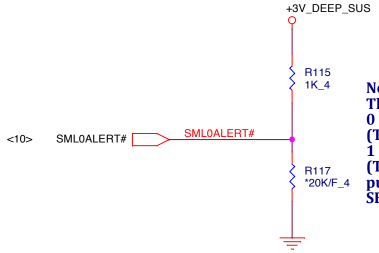
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



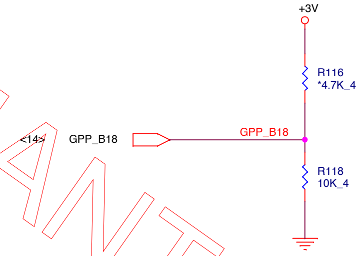
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



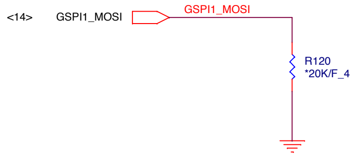
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

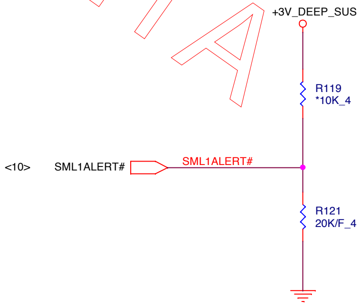


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.



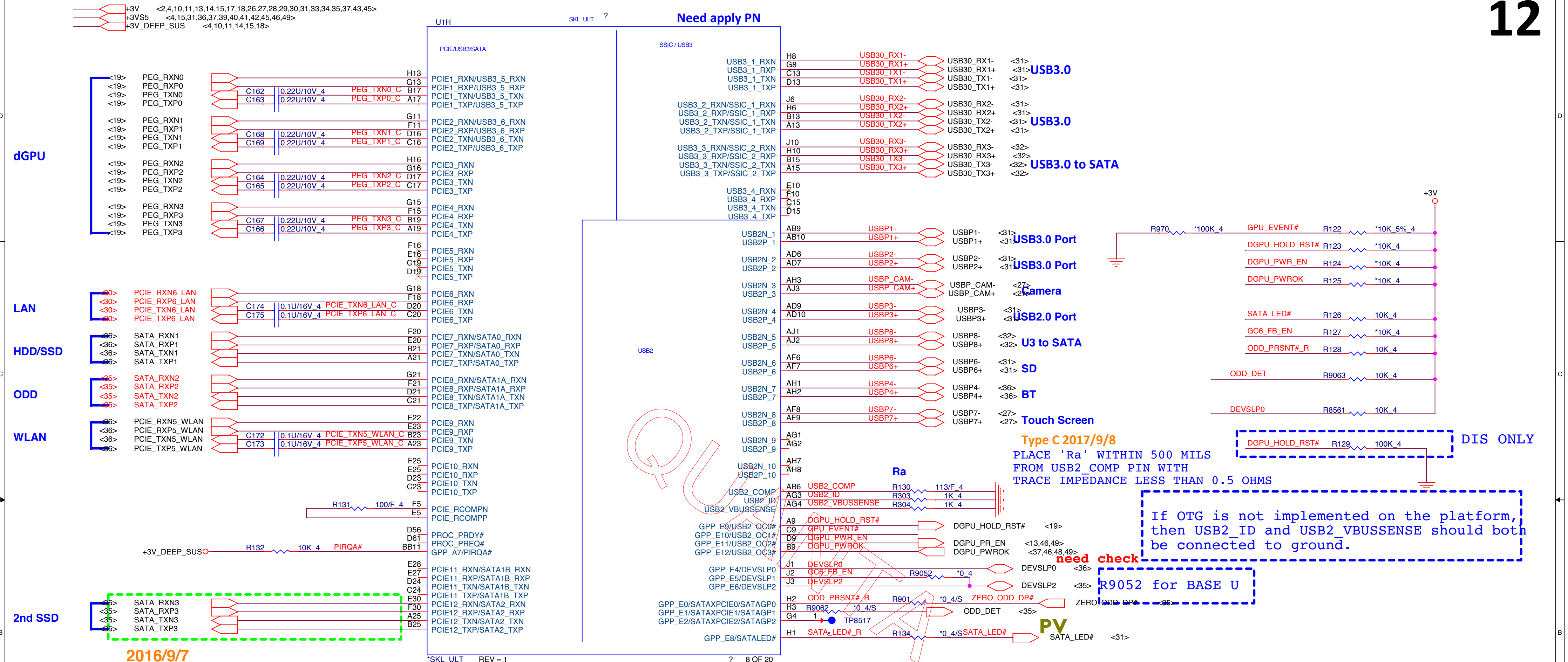
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	**Boot BIOS Destination**
0	**SPI**
1	**LPC**



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

NB5
PROJECT : 0P1B
Quanta Computer Inc.
Size Custom
Document Number **11 -- SKYLAKE 10/15(HDA)**
Rev 1A
Date: Wednesday, March 08, 2017



2016/9/7
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	Un-used
Port3	dGPU	Port2	Un-used
Port4	dGPU	Port3	WLAN
Port5		Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD/SSD		
Port8	ODD		
Port9	WLAN		
Port10			
Port11			
Port12	2nd SSD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB
PORT-2	USB3.0 MB
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB
PORT-2	Cobime USB3.0 MB
PORT-3	Webcam
PORT-4	USB2.0 Small Board
PORT-5	USB3.0 to SATA
PORT-6	SD Card
PORT-7	WLAN (BT)
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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PROJECT : 0P1B
Quanta Computer Inc.
Size Custom
Document Number 11 -- SKYLAKE 10/15(HDA)
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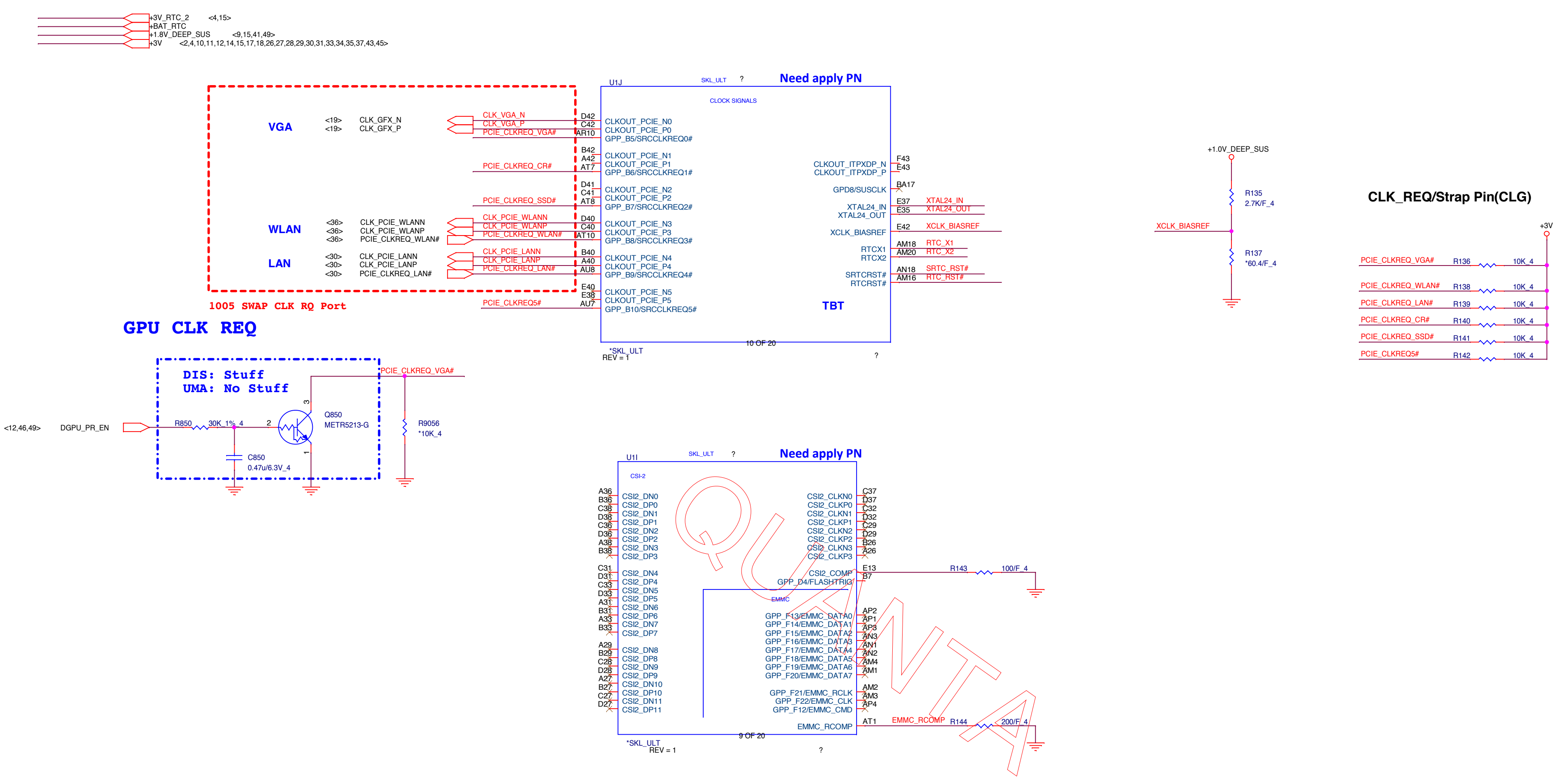
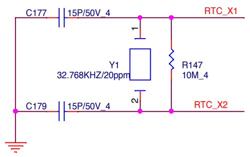
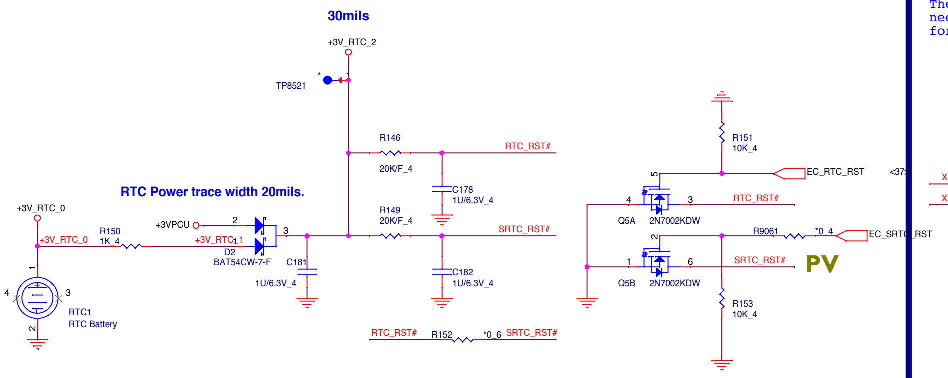


RTC Clock 32.768KHz

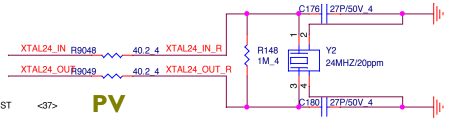


RTC Circuitry(RTC)



External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.


XTAL24_IN R9048 40.2_4 XTAL24_IN_R
XTAL24_OUT R9049 40.2_4 XTAL24_OUT_R
R148 1M_4
C176 27P/50V_4
Y2 24MHZ/20ppm
C180 27P/50V_4
PV

NB5

PROJECT : 0P1B
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Size	Document Number	Rev
Custom	13 -- SKYLAKE 12/15 (CLK/EMMC)	1A

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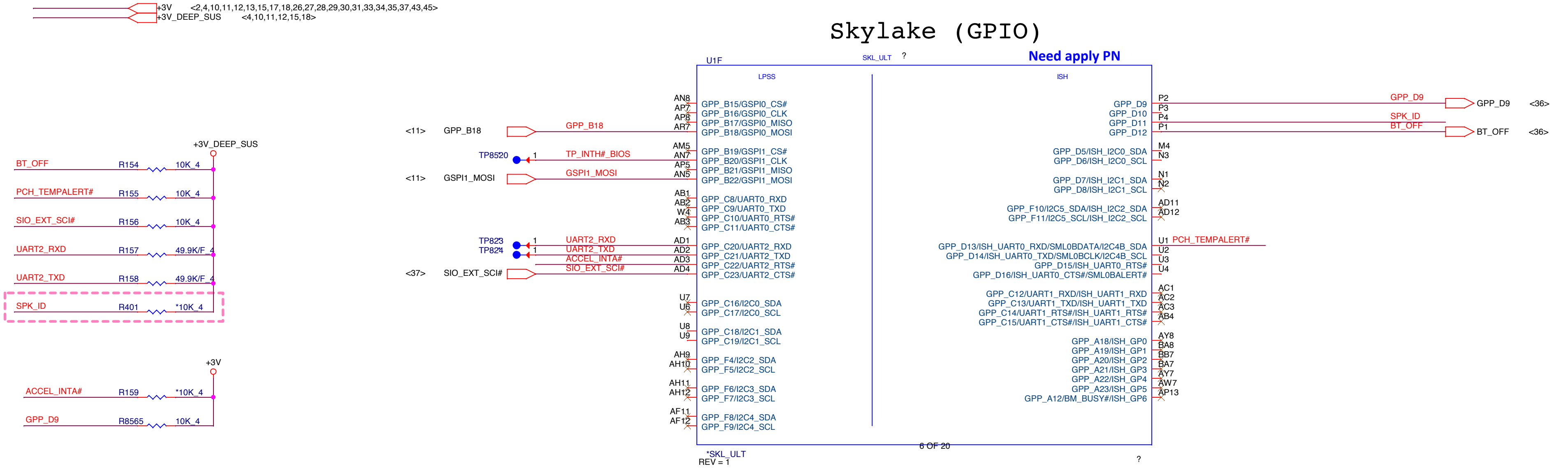
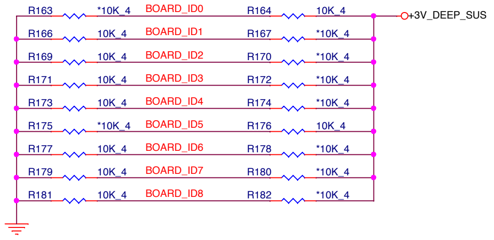
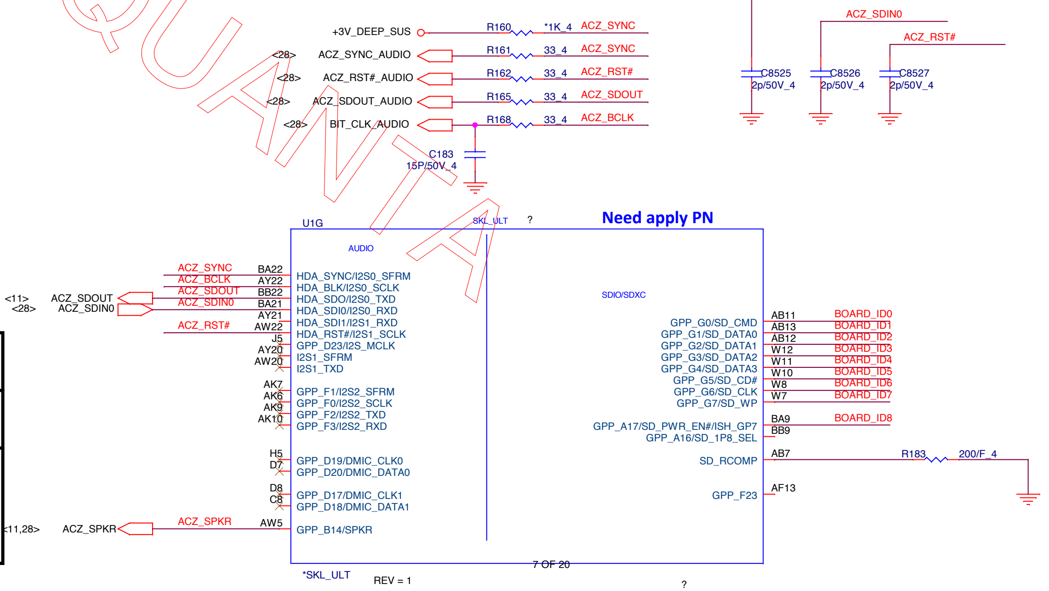
Skylake (GPIO)




R163 *10K_4 BOARD_ID0 R164 10K_4
+3V_DEEP_SUS
R166 10K_4 BOARD_ID1 R167 *10K_4
R169 10K_4 BOARD_ID2 R170 *10K_4
R171 10K_4 BOARD_ID3 R172 *10K_4
R173 10K_4 BOARD_ID4 R174 *10K_4
R175 *10K_4 BOARD_ID5 R176 10K_4
R177 10K_4 BOARD_ID6 R178 *10K_4
R179 10K_4 BOARD_ID7 R180 *10K_4
R181 10K_4 BOARD_ID8 R182 *10K_4

Skylake U	**BOARD_ID[8:7]**	**BOARD_ID[6:5]**	**Board ID [4:3]**	**BOARD_ID[2:1]**	**BOARD_ID0**
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	**Reserve** **(Default = 00)**	**00 SKL U** **01 KBL U** **10 Base U** **11 KBL R(4+2)**	**Reserve** **(Default = 00)**	**00 14"** **01 15"** **10 Reserve** **11 Reserve**	**0 : UMA** **1 : DIS**

HDA Bus(CLG)


+3V_DEEP_SUS R160 *1K_4 ACZ_SYNC
<28> ACZ_SYNC_AUDIO R161 33_4 ACZ_SYNC
<28> ACZ_RST#_AUDIO R162 33_4 ACZ_RST#
<28> ACZ_SDOUT_AUDIO R165 33_4 ACZ_SDOUT
<28> BIT_CLK_AUDIO R168 33_4 ACZ_BCLK
C183 15P/50V_4
ACZ_SDOUT
ACZ_SDIN0
ACZ_RST#
C8525 2p/50V_4
C8526 2p/50V_4
C8527 2p/50V_4
U1G
SKL_ULT ?
Need apply PN
AUDIO
SDIO/SDXC
ACZ_SYNC BA22 HDA_SYNC/I2S0_SFRM
ACZ_BCLK AY22 HDA_BLK/I2S0_SCLK
ACZ_SDOUT BB22 HDA_SDO/I2S0_TXD
ACZ_SDIN0 BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
ACZ_RST# AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD
H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1
ACZ_SPKR AW5 GPP_B14/SPKR
<11> ACZ_SDOUT
<28> ACZ_SDIN0
<11,28> ACZ_SPKR
GPP_G0/SD_CMD AB11 BOARD_ID0
GPP_G1/SD_DATA0 AB13 BOARD_ID1
GPP_G2/SD_DATA1 AB12 BOARD_ID2
GPP_G3/SD_DATA2 W12 BOARD_ID3
GPP_G4/SD_DATA3 W11 BOARD_ID4
GPP_G5/SD_CD# W10 BOARD_ID5
GPP_G6/SD_CLK W8 BOARD_ID6
GPP_G7/SD_WP W7 BOARD_ID7
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9 BOARD_ID8
GPP_A16/SD_1P8_SEL BB9
SD_RCOMP AB7 R183 200/F_4
GPP_F23 AF13
7 OF 20
*SKL_ULT
REV = 1
?

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Quanta Computer Inc.

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Size	Document Number	Rev
Custom	14 -- SKYLAKE 13/15 (GPIO)	1A

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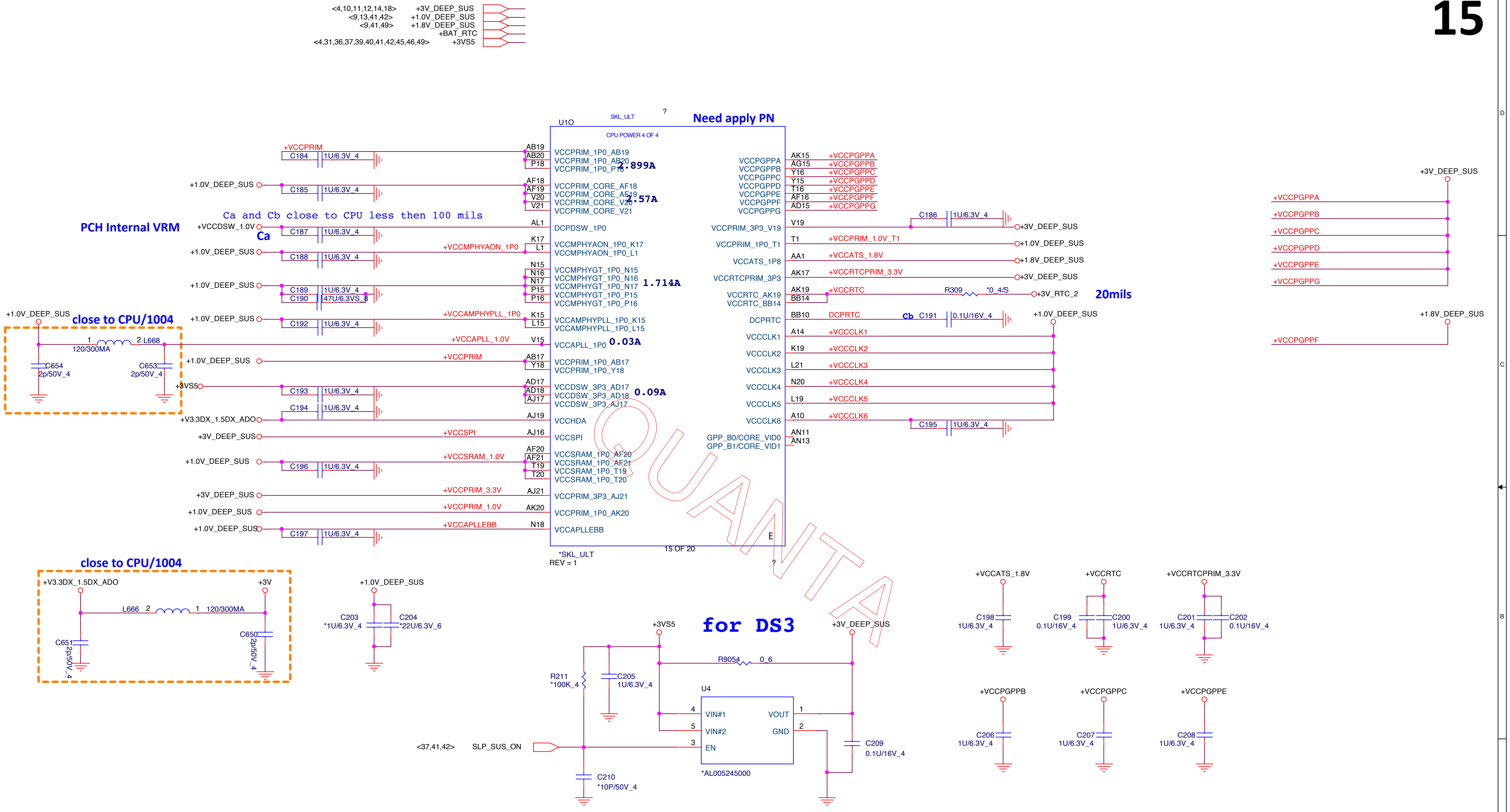

PROJECT : 0P1B
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NB5

Size	Document Number	Rev
Custom	**15 -- SKYLAKE 14/15(PCH POWER)**	1A

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del XDP

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	16 -- SKYLAKE 15/15 XDP&APS *	1A

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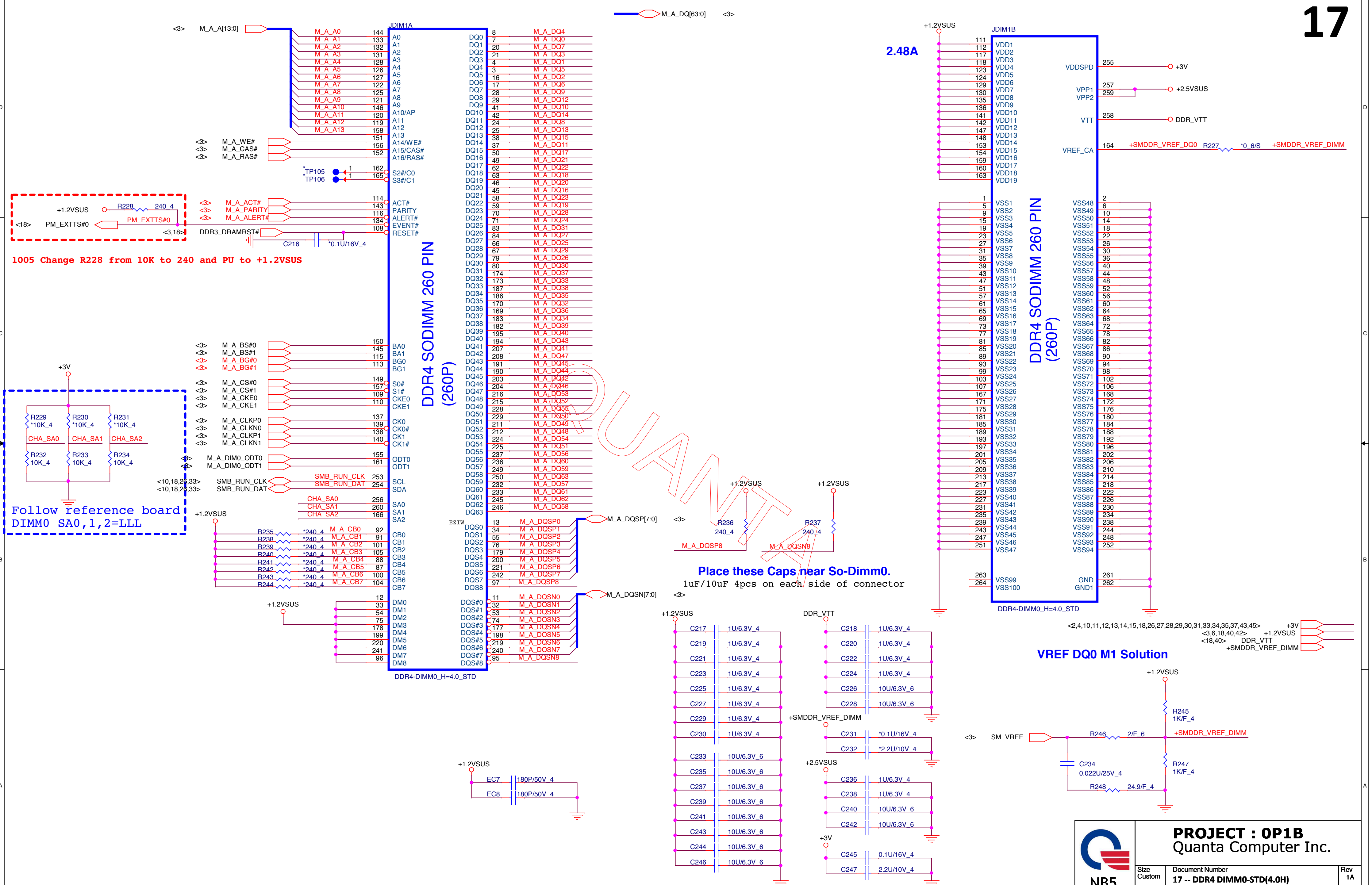

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	17 -- DDR4 DIMM0-STD(4.0H)	1A

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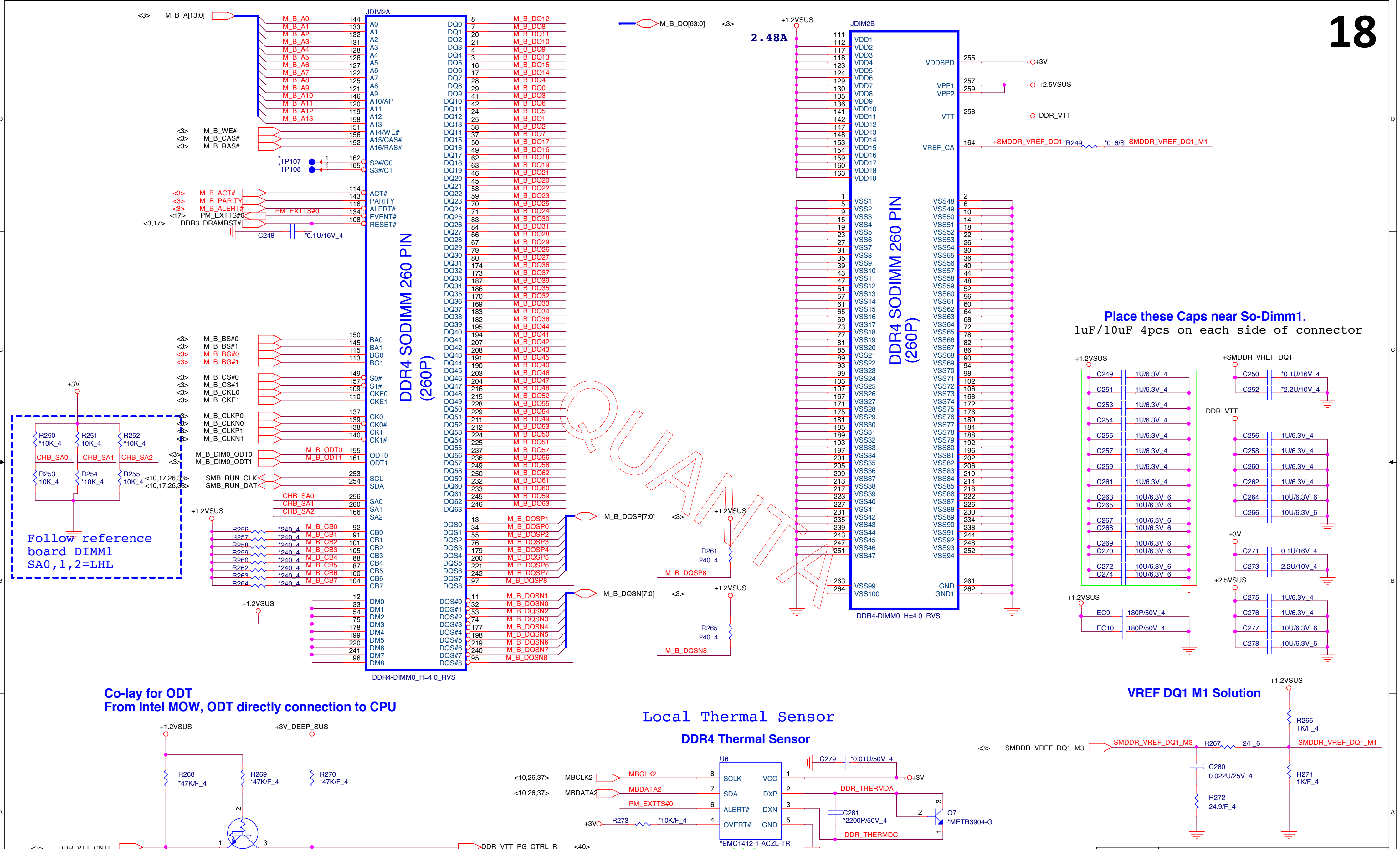

Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector

C249, C251, C253, C254, C255, C257, C259, C261 1U/6.3V_4
C263, C265, C267, C268, C269, C270, C272, C274 10U/6.3V_6
EC9, EC10 180P/50V_4
C250 *0.1U/16V_4
C252 *2.2U/10V_4
C256, C258, C260, C262 1U/6.3V_4
C264, C266 10U/6.3V_6
C271 0.1U/16V_4
C273 2.2U/10V_4
C275, C276 1U/6.3V_4
C277, C278 10U/6.3V_6

Co-lay for ODT
From Intel MOW, ODT directly connection to CPU

Local Thermal Sensor

DDR4 Thermal Sensor

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

VREF DQ1 M1 Solution

<38,39,45,49> +5VPCU
<3,6,17,40,42> +1.2VSUS
<17,40> DDR_VTT
<4,31,32,39,40,41,42,43,44,45,46,48> +5VS5
<2,4,10,11,12,13,14,15,17,26,27,28,29,30,31,33,34,35,37,43,45> +3V

NB5

PROJECT : 0P1B
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Size	Document Number	Rev
Custom	18 -- DDR4 DIMM1-RVS(4.0H)	1A

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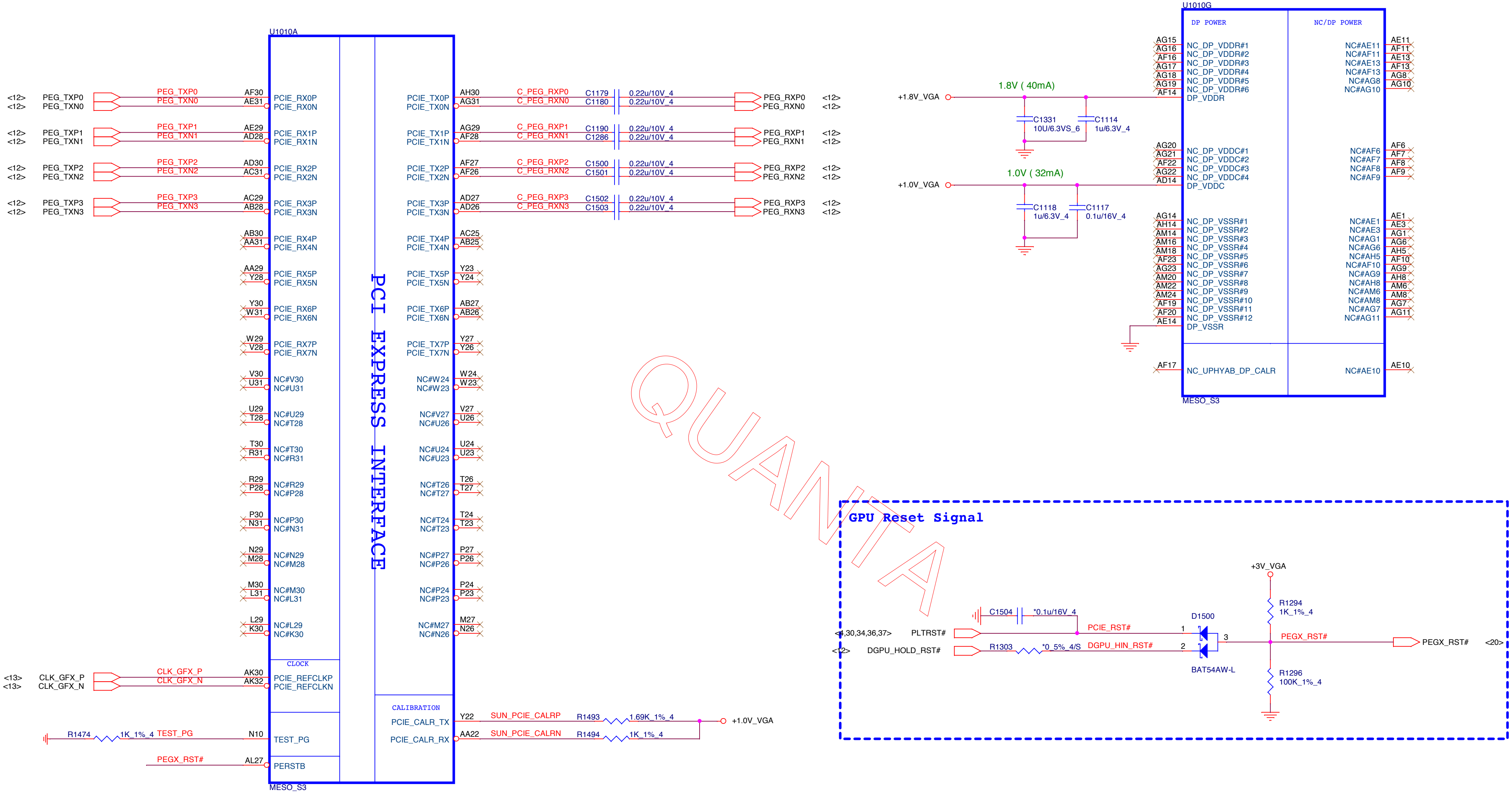

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
1A	**M1-70_S3_PCIE/DP POWER**	1A

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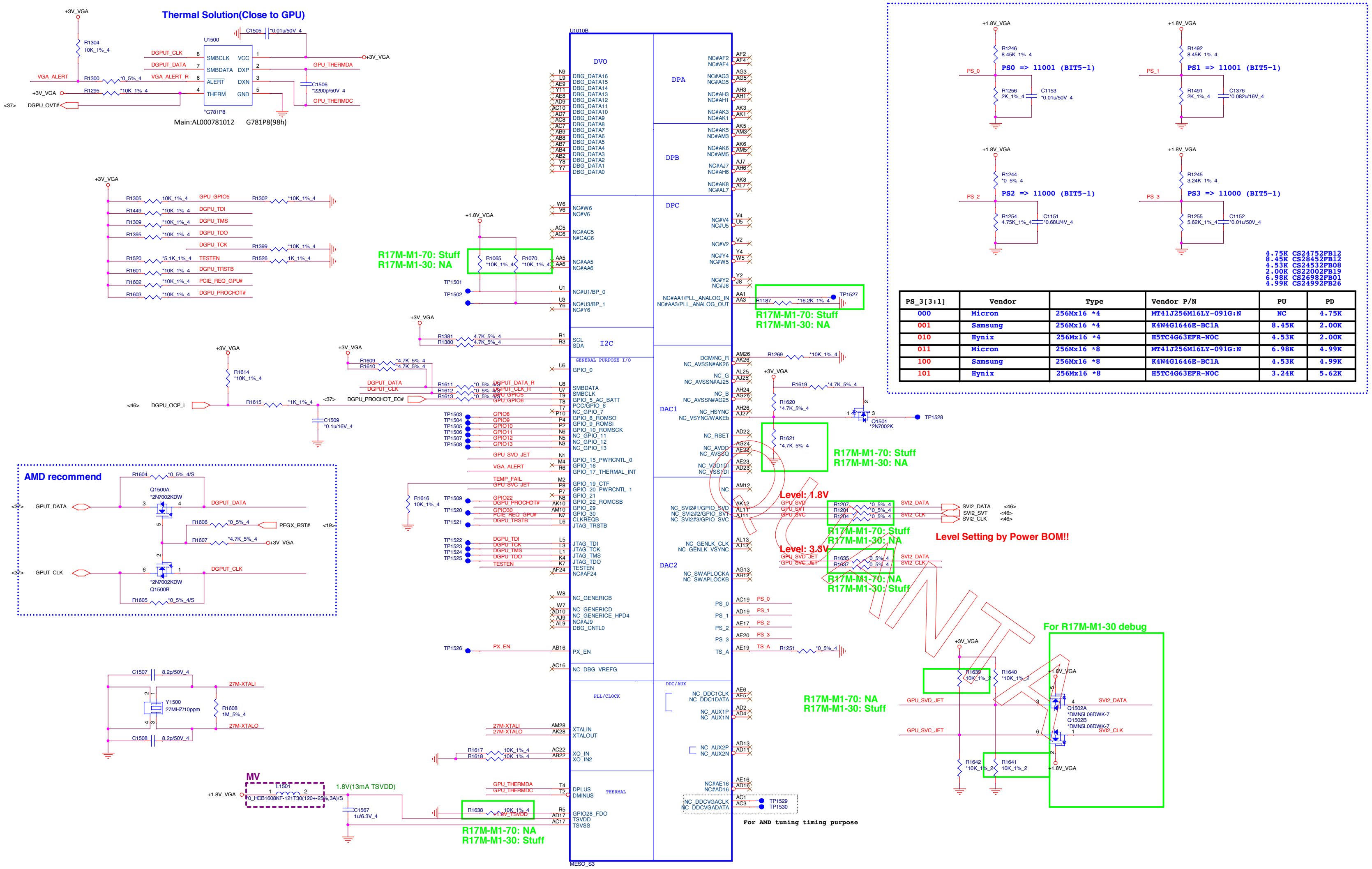
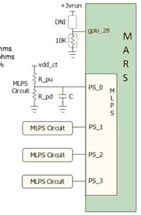


4.75K CS24752FB12
8.45K CS28452FB12
4.53K CS24532FB08
2.00K CS22002FB19
6.98K CS26982FB01
4.99K CS24992FB26

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Micron	256Mx16 *4	MT41J256M16LY-091G:N	NC	4.75K
001	Samsung	256Mx16 *4	K4W4G1646E-BC1A	8.45K	2.00K
010	Hynix	256Mx16 *4	H5TC4G63EFR-N0C	4.53K	2.00K
011	Micron	256Mx16 *8	MT41J256M16LY-091G:N	6.98K	4.99K
100	Samsung	256Mx16 *8	K4W4G1646E-BC1A	4.53K	4.99K
101	Hynix	256Mx16 *8	H5TC4G63EFR-N0C	3.24K	5.62K

MLPS Implementation
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

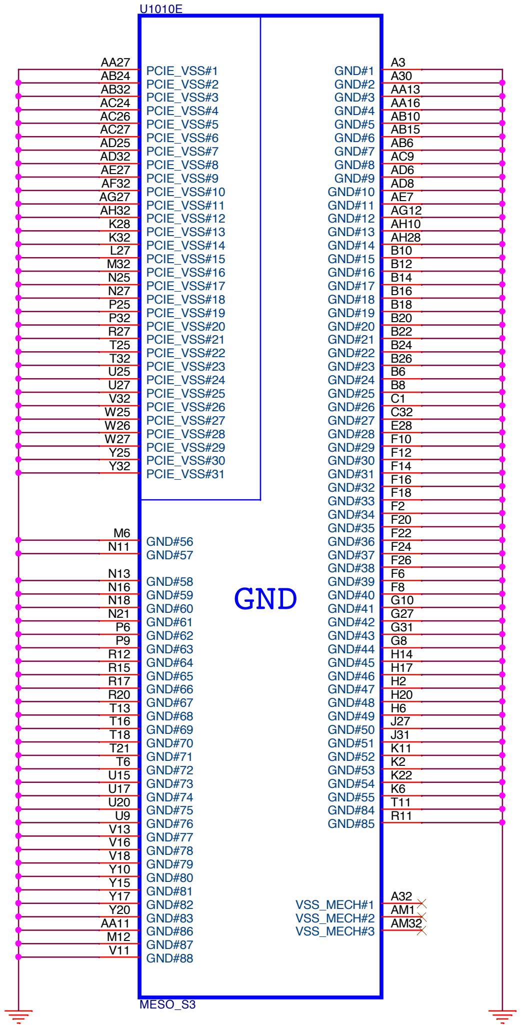
R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Table 3–24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

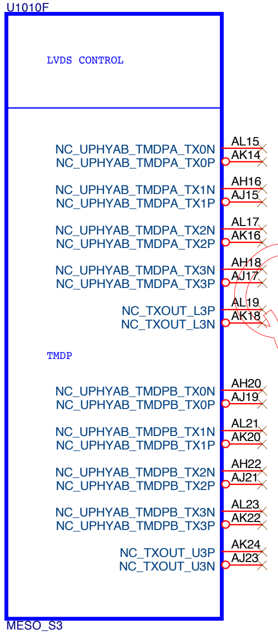
MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

U1010E



MESO_S3

U1010F


LVDS CONTROL
NC_UPHYAB_TMDPA_TX0N AL15
NC_UPHYAB_TMDPA_TX0P AK14
NC_UPHYAB_TMDPA_TX1N AH16
NC_UPHYAB_TMDPA_TX1P AJ15
NC_UPHYAB_TMDPA_TX2N AL17
NC_UPHYAB_TMDPA_TX2P AK16
NC_UPHYAB_TMDPA_TX3N AH18
NC_UPHYAB_TMDPA_TX3P AJ17
NC_TXOUT_L3P AL19
NC_TXOUT_L3N AK18
TMDP
NC_UPHYAB_TMDPB_TX0N AH20
NC_UPHYAB_TMDPB_TX0P AJ19
NC_UPHYAB_TMDPB_TX1N AL21
NC_UPHYAB_TMDPB_TX1P AK20
NC_UPHYAB_TMDPB_TX2N AH22
NC_UPHYAB_TMDPB_TX2P AJ21
NC_UPHYAB_TMDPB_TX3N AL23
NC_UPHYAB_TMDPB_TX3P AK22
NC_TXOUT_U3P AK24
NC_TXOUT_U3N AJ23

MESO_S3

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

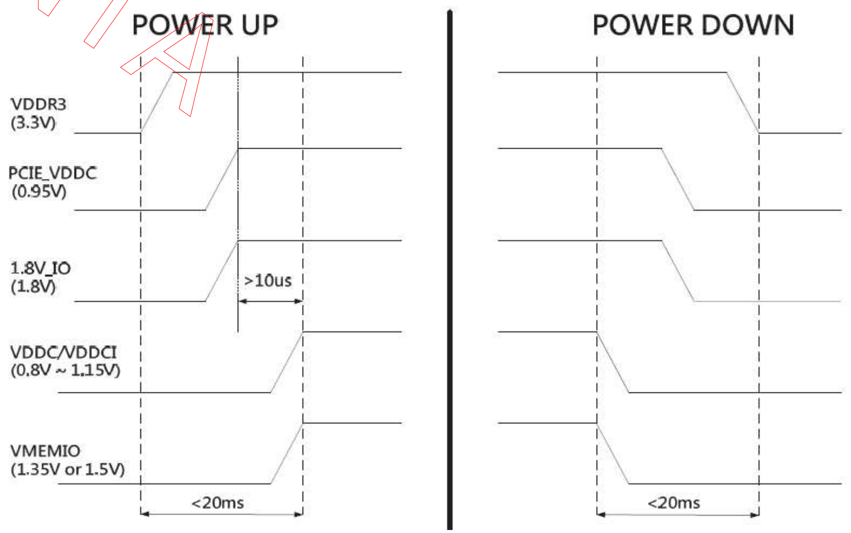
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2

POWER UP / POWER DOWN SEQUENCE



PROJECT : 0P1B
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NB5

Size	Document Number	Rev
	M1-70_S3_GND/LVDS/Strap	1A
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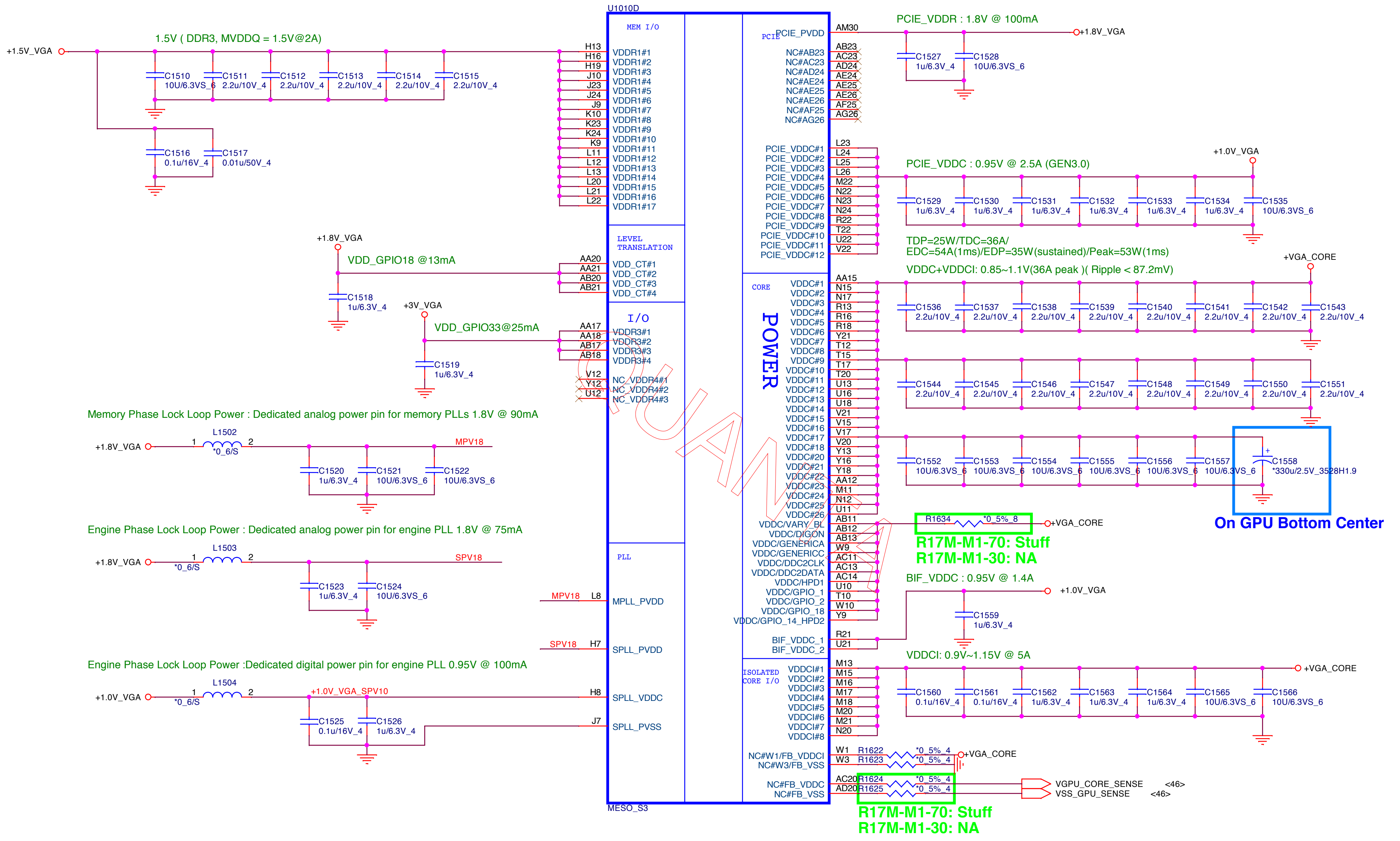
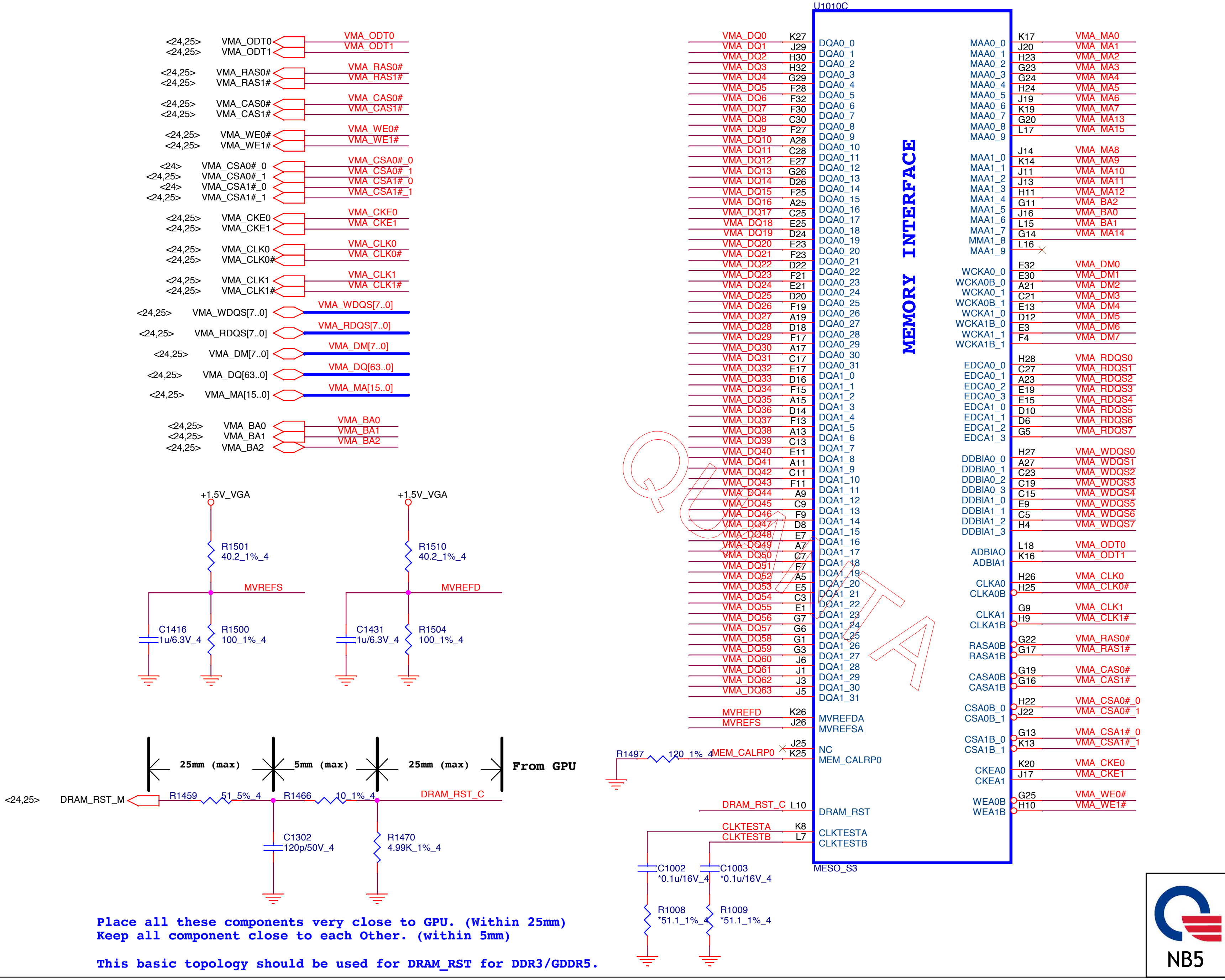

U1010D
MEM I/O
1.5V (DDR3, MVDDQ = 1.5V@2A)
+1.5V_VGA
C1510 10U/6.3VS_6
C1511 2.2u/10V_4
C1512 2.2u/10V_4
C1513 2.2u/10V_4
C1514 2.2u/10V_4
C1515 2.2u/10V_4
C1516 0.1u/16V_4
C1517 0.01u/50V_4
H13 H16 H19 J10 J23 J24 J9 K10 K23 K24 K9 L11 L12 L13 L20 L21 L22
VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17
LEVEL TRANSLATION
+1.8V_VGA
VDD_GPIO18 @13mA
C1518 1u/6.3V_4
AA20 AA21 AB20 AB21
VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4
+3V_VGA
VDD_GPIO33@25mA
C1519 1u/6.3V_4
I/O
AA17 AA18 AB17 AB18
VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4
V12 Y12 U12
NC_VDDR4#1 NC_VDDR4#2 NC_VDDR4#3
Memory Phase Lock Loop Power : Dedicated analog power pin for memory PLLs 1.8V @ 90mA
+1.8V_VGA
L1502 *0_6/S
MPV18
C1520 1u/6.3V_4
C1521 10U/6.3VS_6
C1522 10U/6.3VS_6
Engine Phase Lock Loop Power : Dedicated analog power pin for engine PLL 1.8V @ 75mA
+1.8V_VGA
L1503 *0_6/S
SPV18
C1523 1u/6.3V_4
C1524 10U/6.3VS_6
PLL
MPV18 L8 MPLL_PVDD
SPV18 H7 SPLL_PVDD
Engine Phase Lock Loop Power :Dedicated digital power pin for engine PLL 0.95V @ 100mA
+1.0V_VGA
L1504 *0_6/S
+1.0V_VGA_SPV10
H8 SPLL_VDDC
J7 SPLL_PVSS
C1525 0.1u/16V_4
C1526 1u/6.3V_4
MESO_S3
PCIE
PCIE_PVDD AM30
PCIE_VDDR : 1.8V @ 100mA
+1.8V_VGA
C1527 1u/6.3V_4
C1528 10U/6.3VS_6
NC#AB23 NC#AC23 NC#AD24 NC#AE24 NC#AE25 NC#AE26 NC#AF25 NC#AG26
AB23 AC23 AD24 AE24 AE25 AE26 AF25 AG26
PCIE_VDDC#1 … PCIE_VDDC#12
L23 L24 L25 L26 M22 N22 N23 N24 R22 T22 U22 V22
+1.0V_VGA
PCIE_VDDC : 0.95V @ 2.5A (GEN3.0)
C1529 1u/6.3V_4
C1530 1u/6.3V_4
C1531 1u/6.3V_4
C1532 1u/6.3V_4
C1533 1u/6.3V_4
C1534 1u/6.3V_4
C1535 10U/6.3VS_6
TDP=25W/TDC=36A/
EDC=54A(1ms)/EDP=35W(sustained)/Peak=53W(1ms)
VDDC+VDDCI: 0.85~1.1V(36A peak)(Ripple < 87.2mV)
+VGA_CORE
CORE
POWER
VDDC#1 … VDDC#26
AA15 N15 N17 R13 R16 R18 Y21 T12 T15 T17 T20 U13 U16 U18 V21 V15 V17 V20 Y13 Y16 Y18 AA12 M11 N12 U11
C1536 … C1543 2.2u/10V_4
C1544 … C1551 2.2u/10V_4
C1552 … C1557 10U/6.3VS_6
C1558 *330u/2.5V_3528H1.9
On GPU Bottom Center
VDDC/VARY_BL VDDC/DIGON VDDC/GENERICA VDDC/GENERICC VDDC/DDC2CLK VDDC/DDC2DATA VDDC/HPD1 VDDC/GPIO_1 VDDC/GPIO_2 VDDC/GPIO_18 VDDC/GPIO_14_HPD2
AB11 AB12 AB13 W9 AC11 AC13 AC14 U10 T10 W10 Y9
R1634 *0_5%_8
+VGA_CORE
R17M-M1-70: Stuff
R17M-M1-30: NA
BIF_VDDC : 0.95V @ 1.4A
+1.0V_VGA
C1559 1u/6.3V_4
BIF_VDDC_1 R21
BIF_VDDC_2 U21
VDDCI: 0.9V~1.15V @ 5A
ISOLATED CORE I/O
VDDCI#1 … VDDCI#8
M13 M15 M16 M17 M18 M20 M21 N20
+VGA_CORE
C1560 0.1u/16V_4
C1561 0.1u/16V_4
C1562 1u/6.3V_4
C1563 1u/6.3V_4
C1564 1u/6.3V_4
C1565 10U/6.3VS_6
C1566 10U/6.3VS_6
NC#W1/FB_VDDCI W1 R1622 *0_5%_4
NC#W3/FB_VSS W3 R1623 *0_5%_4
+VGA_CORE
NC#FB_VDDC AC20 R1624 *0_5%_4
NC#FB_VSS AD20 R1625 *0_5%_4
VGPU_CORE_SENSE <46>
VSS_GPU_SENSE <46>
R17M-M1-70: Stuff
R17M-M1-30: NA

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_POWER	1A

Date: Wednesday, March 08, 2017 Sheet 22 of 51



Place all these components very close to GPU. (Within 25mm)
Keep all component close to each Other. (within 5mm)

This basic topology should be used for DRAM_RST for DDR3/GDDR5.

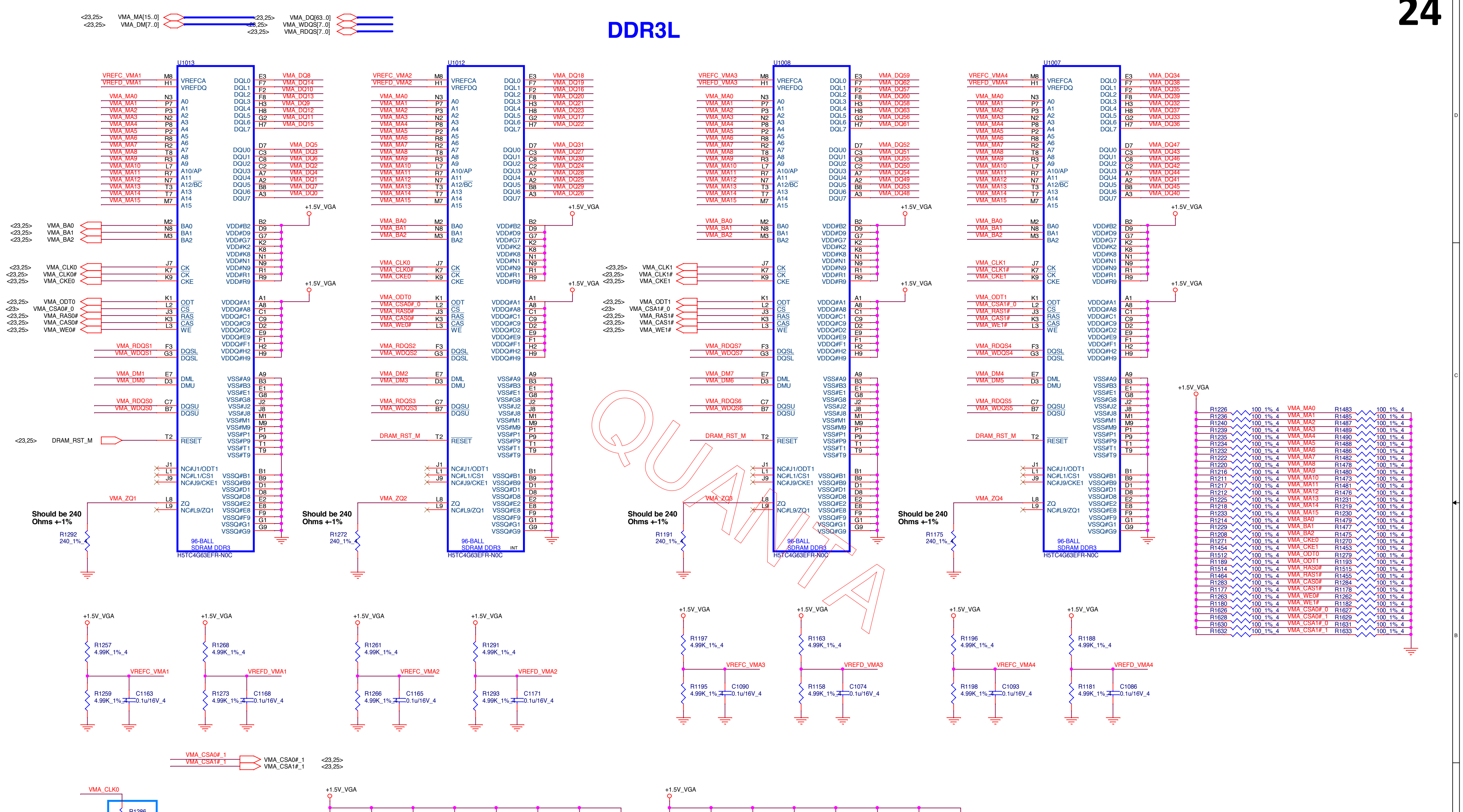
NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_MEM	1A

Date: Wednesday, March 08, 2017 | Sheet 23 of 51

DDR3L

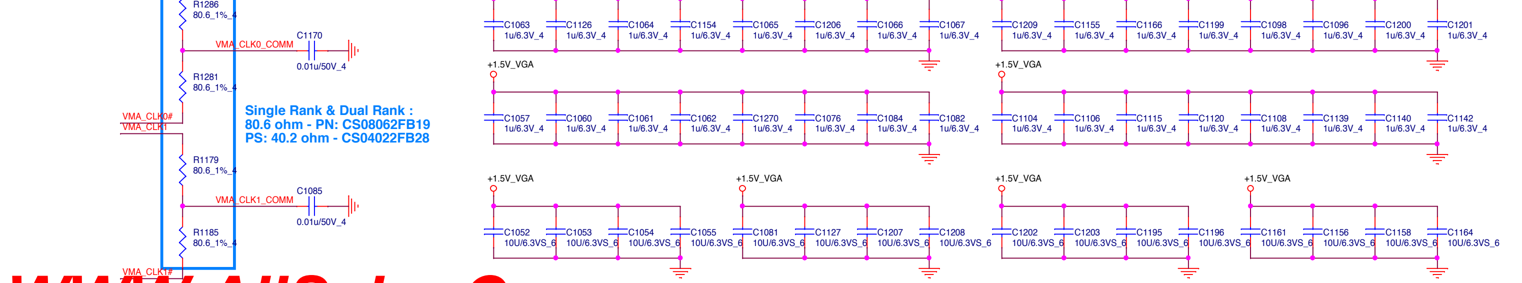


Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%



Single Rank & Dual Rank :
80.6 ohm - PN: CS08062FB19
PS: 40.2 ohm - CS04022FB28

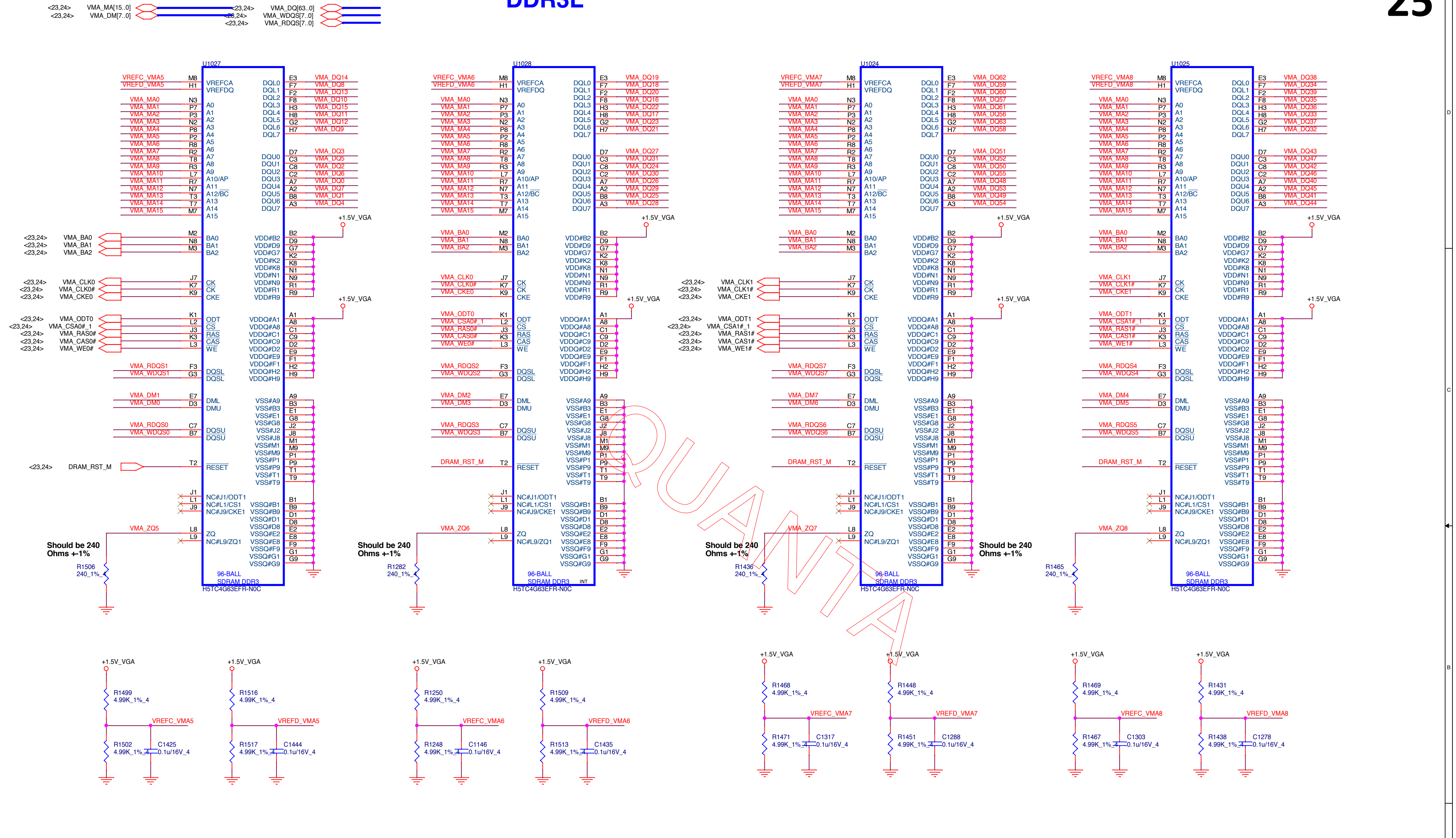
	QBCON PN	TOP BSQ
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01

PROJECT : 0P1B
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	M1-70_S3_VRAM_DDR3L BGA96	1A

Date: Wednesday, March 08, 2017 Sheet 24of 51

DDR3L

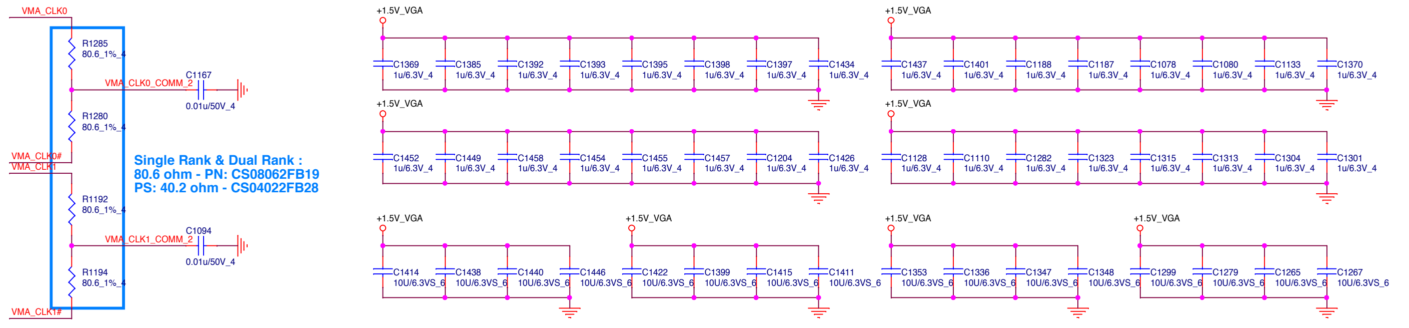


Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%


VMA_CLK0
R1285 80.6_1%_4
VMA_CLK0_COMM_2
C1167 0.01u/50V_4
R1280 80.6_1%_4
VMA_CLK0#
VMA_CLK1
R1192 80.6_1%_4
VMA_CLK1_COMM_2
C1094 0.01u/50V_4
R1194 80.6_1%_4
VMA_CLK1#
+1.5V_VGA
C1369 C1385 C1392 C1393 C1395 C1398 C1397 C1434 1u/6.3V_4
C1437 C1401 C1188 C1187 C1078 C1080 C1133 C1370 1u/6.3V_4
C1452 C1449 C1458 C1454 C1455 C1457 C1204 C1426 1u/6.3V_4
C1128 C1110 C1282 C1323 C1315 C1313 C1304 C1301 1u/6.3V_4
C1414 C1438 C1440 C1446 C1422 C1399 C1415 C1411 10U/6.3VS_6
C1353 C1336 C1347 C1348 C1299 C1279 C1265 C1267 10U/6.3VS_6

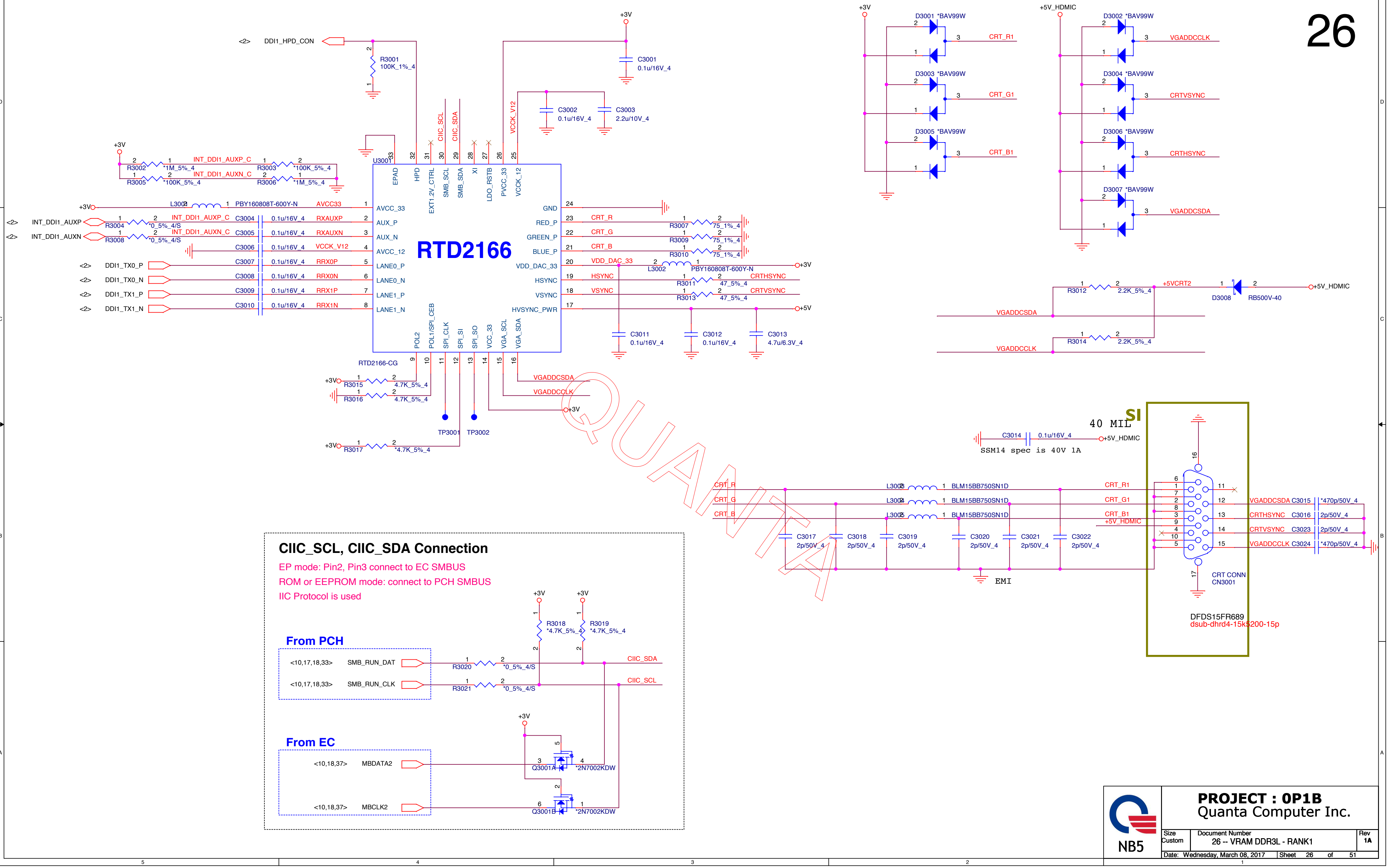
Single Rank & Dual Rank :
80.6 ohm - PN: CS08062FB19
PS: 40.2 ohm - CS04022FB28

	QBCON PN	TOP BSQ
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size C
Document Number **M1-70_S3_VRAM_DDR3L BGA96**
Rev 1A
Date: Wednesday, March 08, 2017



CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS

ROM or EEPROM mode: connect to PCH SMBUS

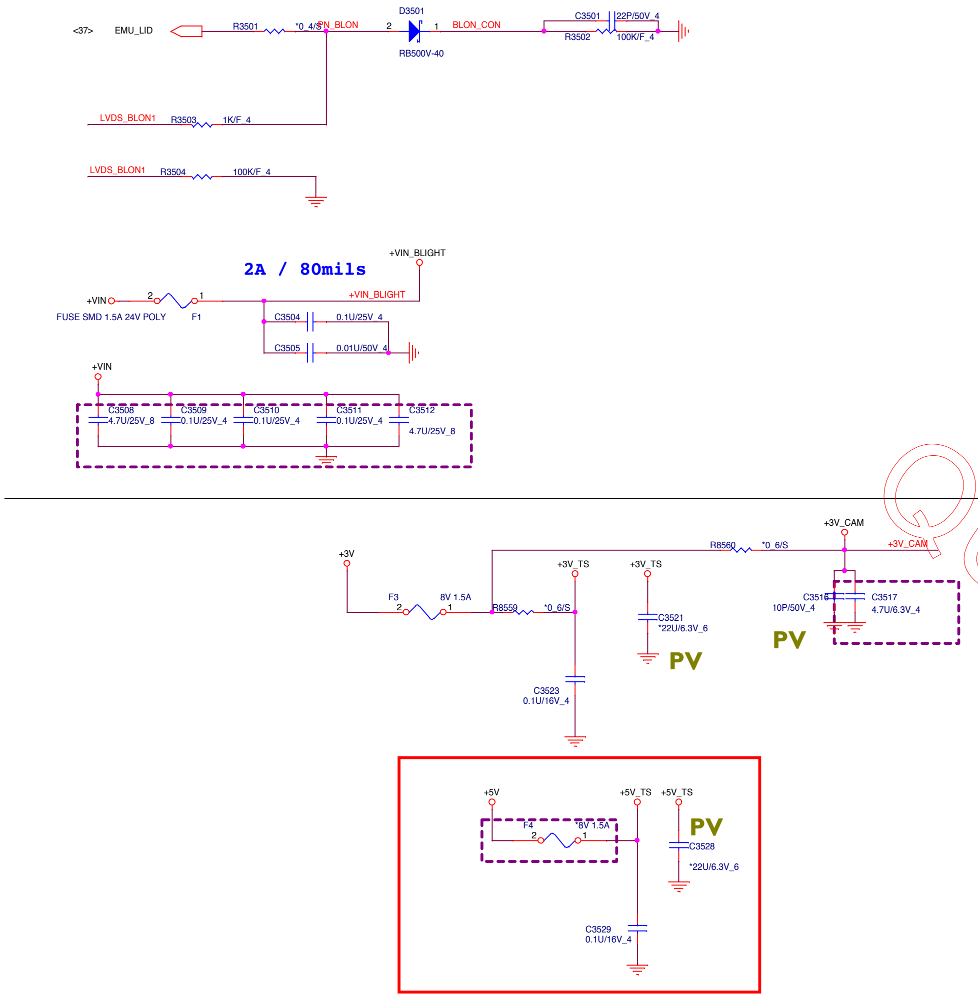
IIC Protocol is used

PROJECT : 0P1B
Quanta Computer Inc.
NB5

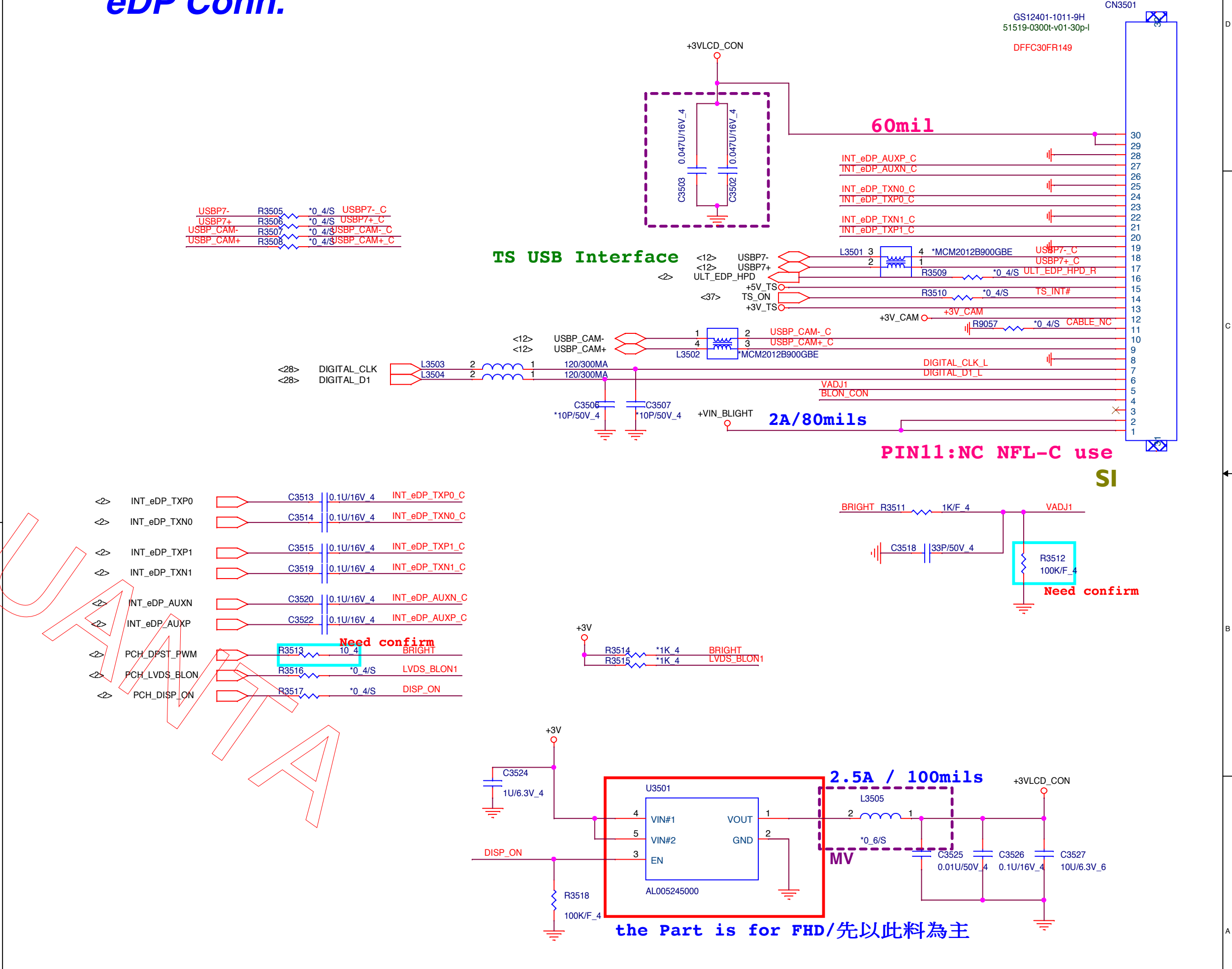
Size	Document Number	Rev
Custom	26 -- VRAM DDR3L - RANK1	1A

Date: Wednesday, March 08, 2017 Sheet 26 of 51

LID Switch



eDP Conn.



<2,4,10,11,12,13,14,15,17,18,26,28,29,30,31,33,34,35,37,43,45> +3V
<6,13,31,33,36,37,38,39> +3VPCU
<26,28,29,33,35,36,45> +5V
<35,38,39,40,41,43,44,46,47,48,50> +VIN

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	27 -- eDP CONN/LID/CAM/D-MIC/TS	1A

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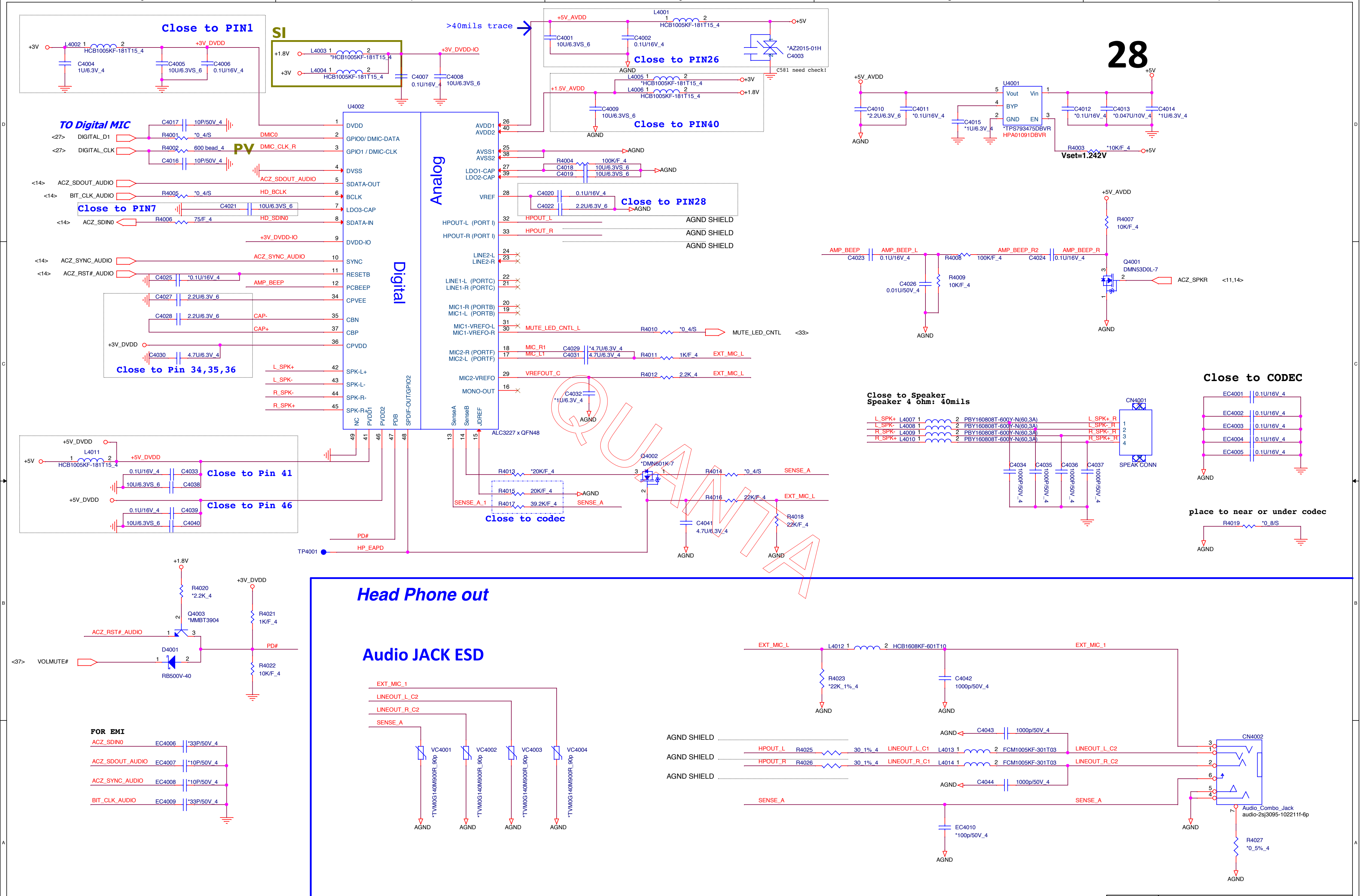

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	28 -- Codec ALC3227-CG	1A

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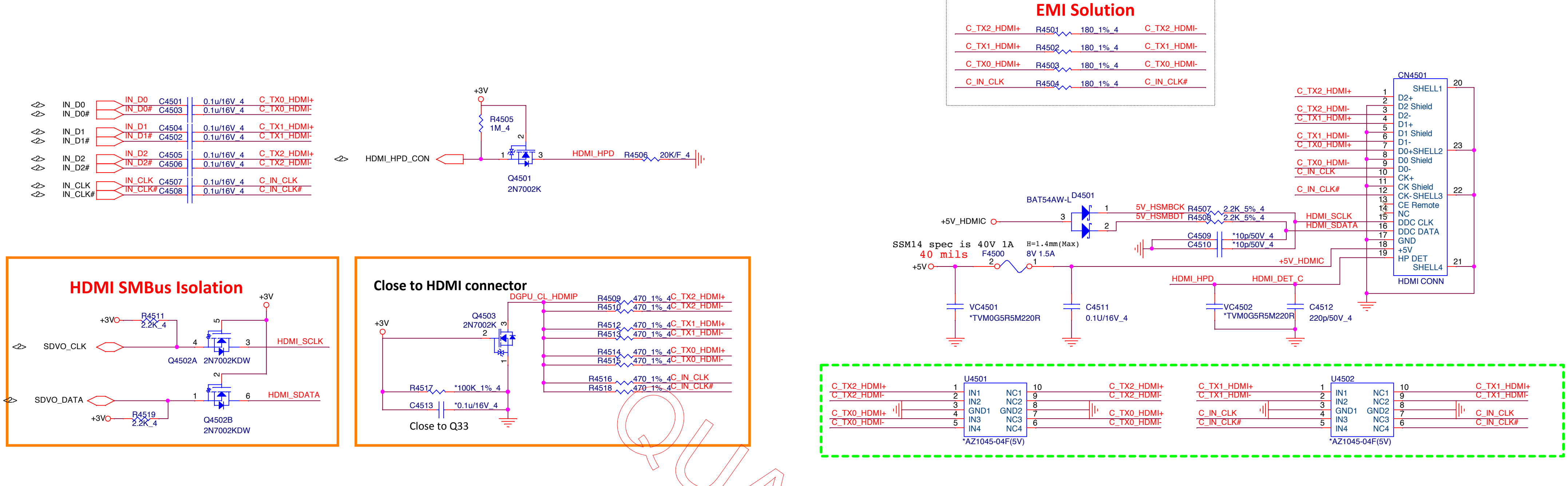
HDMI CONN


EMI Solution
C_TX2_HDMI+ R4501 180_1%_4 C_TX2_HDMI-
C_TX1_HDMI+ R4502 180_1%_4 C_TX1_HDMI-
C_TX0_HDMI+ R4503 180_1%_4 C_TX0_HDMI-
C_IN_CLK R4504 180_1%_4 C_IN_CLK#
<2> IN_D0 IN_D0 C4501 0.1u/16V_4 C_TX0_HDMI+
<2> IN_D0# IN_D0# C4503 0.1u/16V_4 C_TX0_HDMI-
<2> IN_D1 IN_D1 C4504 0.1u/16V_4 C_TX1_HDMI+
<2> IN_D1# IN_D1# C4502 0.1u/16V_4 C_TX1_HDMI-
<2> IN_D2 IN_D2 C4505 0.1u/16V_4 C_TX2_HDMI+
<2> IN_D2# IN_D2# C4506 0.1u/16V_4 C_TX2_HDMI-
<2> IN_CLK IN_CLK C4507 0.1u/16V_4 C_IN_CLK
<2> IN_CLK# IN_CLK# C4508 0.1u/16V_4 C_IN_CLK#
+3V
R4505 1M_4
<2> HDMI_HPD_CON
Q4501 2N7002K
HDMI_HPD R4506 20K/F_4
CN4501
SHELL1 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+SHELL2 D0 Shield D0- CK+ CK Shield CK-SHELL3 CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL4
HDMI CONN
C_TX2_HDMI+ C_TX2_HDMI- C_TX1_HDMI+ C_TX1_HDMI- C_TX0_HDMI+ C_TX0_HDMI- C_IN_CLK C_IN_CLK#
BAT54AW-L D4501
+5V_HDMIC
5V_HSMBCK R4507 2.2K_5%_4
5V_HSMBDT R4508 2.2K_5%_4
HDMI_SCLK HDMI_SDATA
C4509 *10p/50V_4
C4510 *10p/50V_4
SSM14 spec is 40V 1A
40 mils
F4500
H=1.4mm(Max)
8V 1.5A
+5V
+5V_HDMIC
HDMI_HPD HDMI_DET_C
VC4501 *TVM0G5R5M220R
C4511 0.1U/16V_4
VC4502 *TVM0G5R5M220R
C4512 220p/50V_4
HDMI SMBus Isolation
+3V R4511 2.2K_4
<2> SDVO_CLK
Q4502A 2N7002KDW
HDMI_SCLK
<2> SDVO_DATA
+3V R4519 2.2K_4
Q4502B 2N7002KDW
HDMI_SDATA
Close to HDMI connector
DGPU_CL_HDMIP
Q4503 2N7002K
+3V
R4509 470_1%_4 C_TX2_HDMI+
R4510 470_1%_4 C_TX2_HDMI-
R4512 470_1%_4 C_TX1_HDMI+
R4513 470_1%_4 C_TX1_HDMI-
R4514 470_1%_4 C_TX0_HDMI+
R4515 470_1%_4 C_TX0_HDMI-
R4516 470_1%_4 C_IN_CLK
R4518 470_1%_4 C_IN_CLK#
R4517 *100K_1%_4
C4513 *0.1u/16V_4
Close to Q33
U4501
IN1 IN2 GND1 IN3 IN4 NC1 NC2 GND2 NC3 NC4
*AZ1045-04F(5V)
U4502
*AZ1045-04F(5V)
C_TX1_HDMI+ C_TX1_HDMI- C_IN_CLK C_IN_CLK#

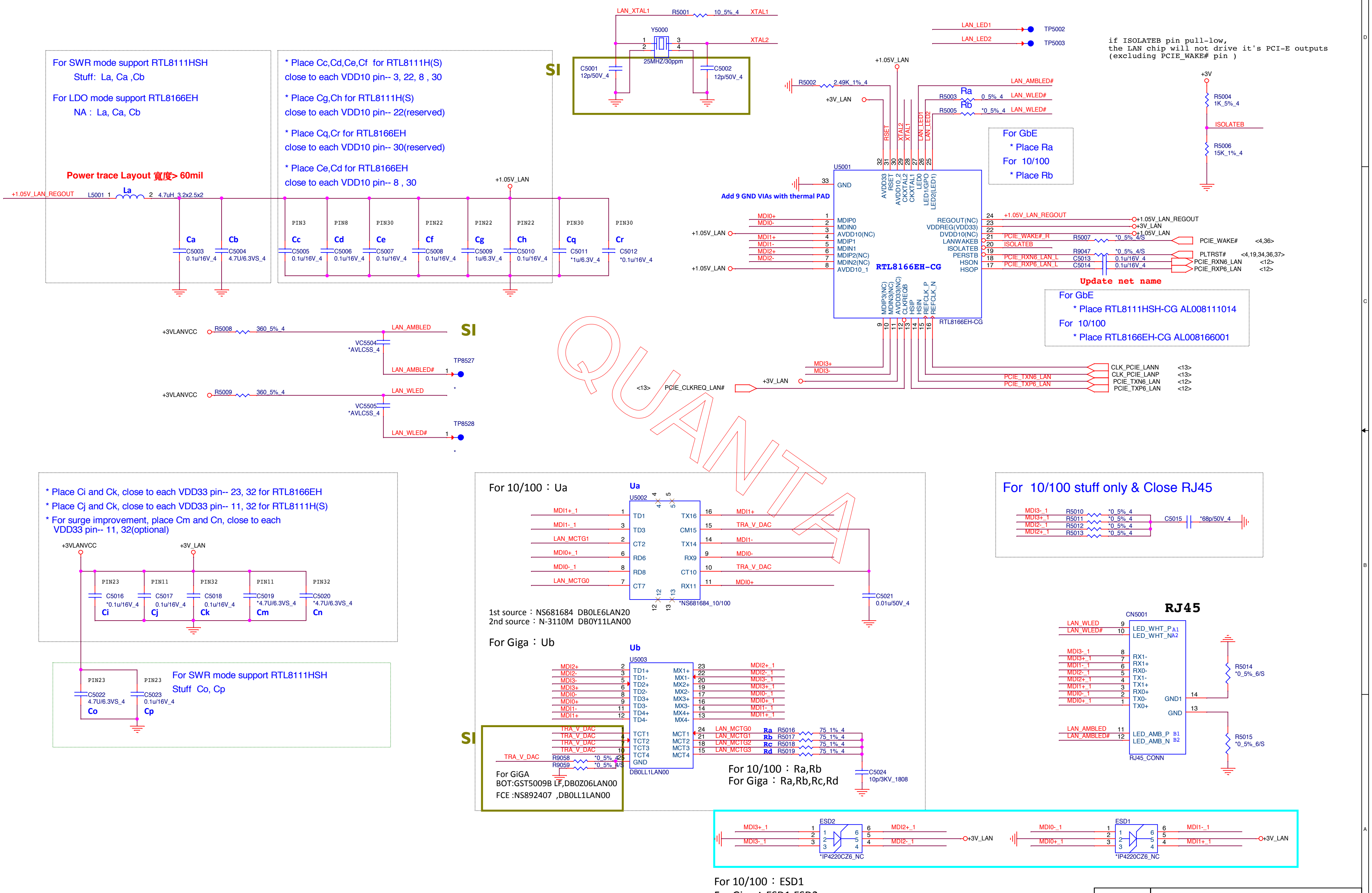
NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29 -- HDMI/AMP HPA022642RTJR	1A

Date: Wednesday, March 08, 2017 Sheet 29 of 51

LAN RTL8166EH/RTL8111HSH



For SWR mode support RTL8111HSH
Stuff: La, Ca ,Cb

For LDO mode support RTL8166EH
NA : La, Ca, Cb

Power trace Layout 寬度> 60mil

* Place Cc,Cd,Ce,Cf for RTL8111H(S) close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) close to each VDD10 pin-- 22(reserved)

* Place Cq,Cr for RTL8166EH close to each VDD10 pin-- 30(reserved)

* Place Ce,Cd for RTL8166EH close to each VDD10 pin-- 8 , 30

Add 9 GND VIAs with thermal PAD

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

For GbE
* Place Ra
For 10/100
* Place Rb

For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8166EH-CG AL008166001

* Place Ci and Ck, close to each VDD33 pin-- 23, 32 for RTL8166EH
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S)
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

For SWR mode support RTL8111HSH
Stuff Co, Cp

For 10/100 : Ua

1st source : NS681684 DB0LE6LAN20
2nd source : N-3110M DB0Y11LAN00

For Giga : Ub

For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100 : Ra,Rb
For Giga : Ra,Rb,Rc,Rd

For 10/100 stuff only & Close RJ45

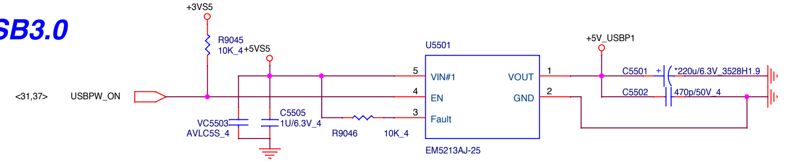
For 10/100 : ESD1
For Giga : ESD1,ESD2

PROJECT : 0P1B
Quanta Computer Inc.
NB5

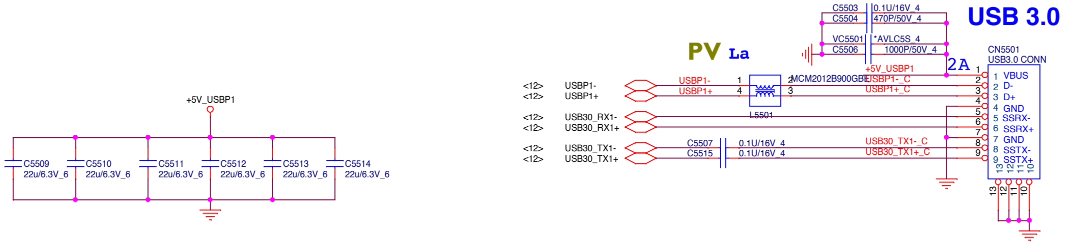
Size	Document Number	Rev
C	30 -- LAN RTL8166EH/RTL8111HSH	1A

Date: Wednesday, March 08, 2017 Sheet 30 of 51

USB3.0

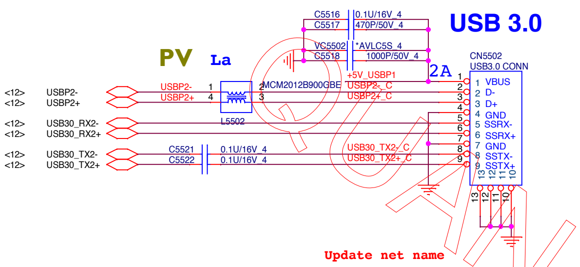


USB 2.0/3.0 Combo

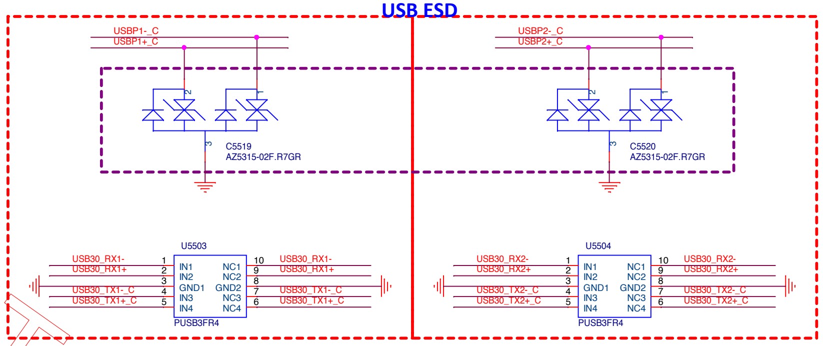


UART for Win7 WHQL DEBUG

USB 2.0/3.0 Combo

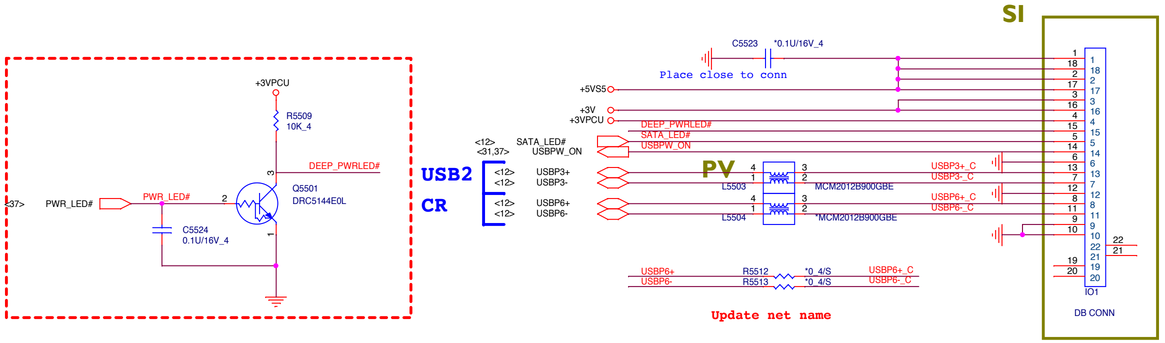


Update net name



Update net name

Daughter Board



Update net name

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	31 -- USB SW & TYPE-C -TPS25810	1A

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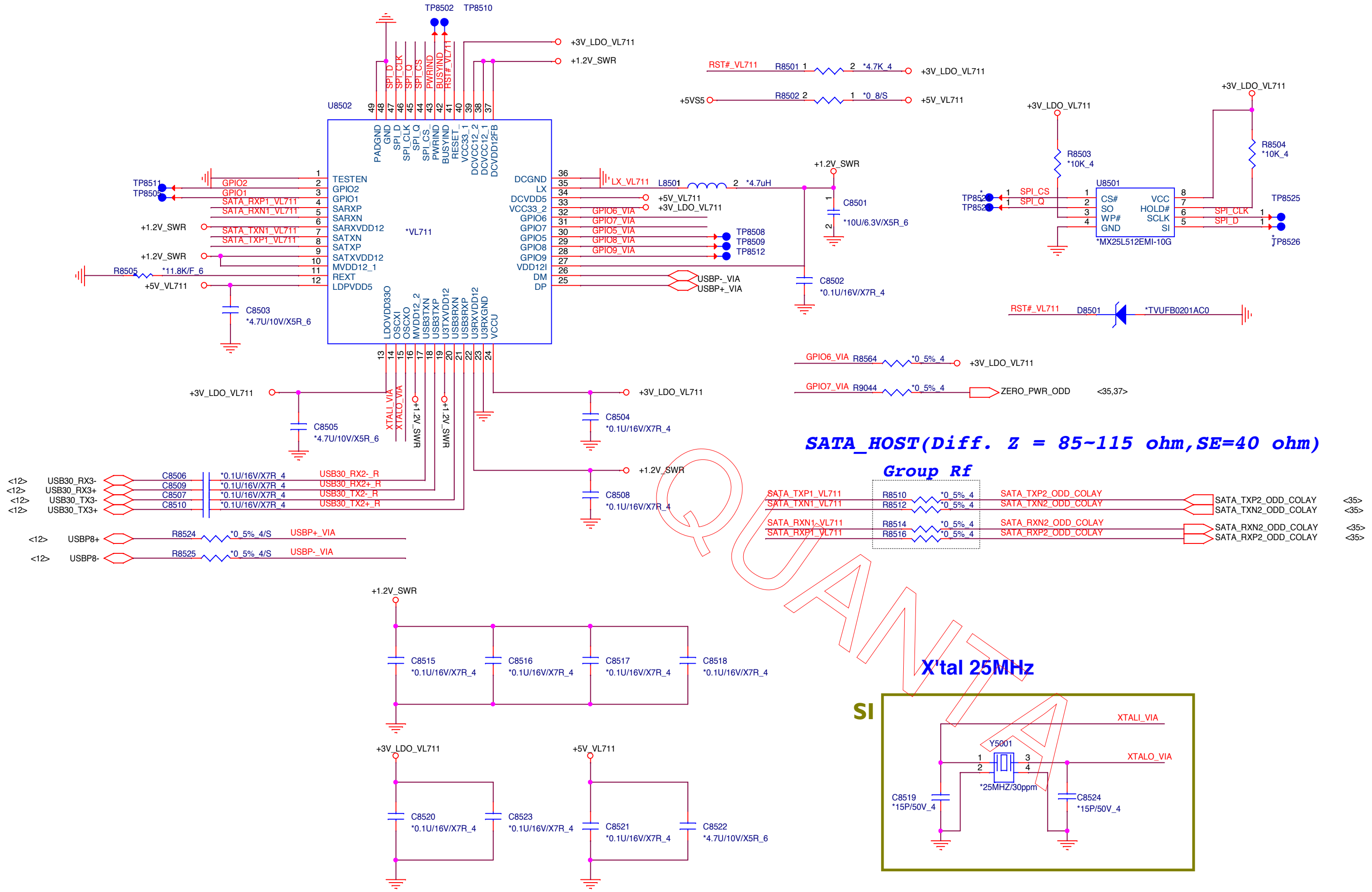
USB3 to SATA VL711



PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	32 -- USB SW & TYPE-C -TPS25810	1A

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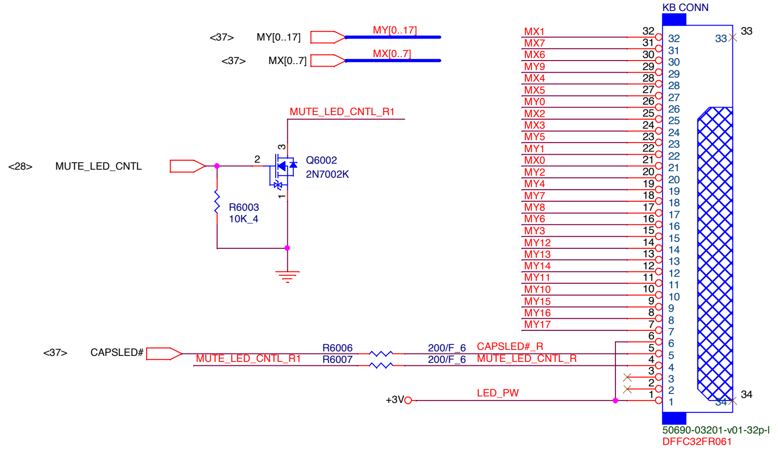
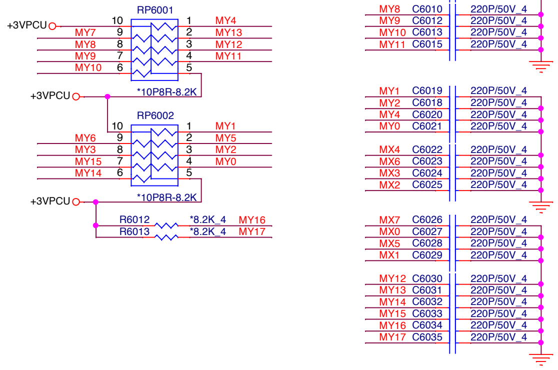
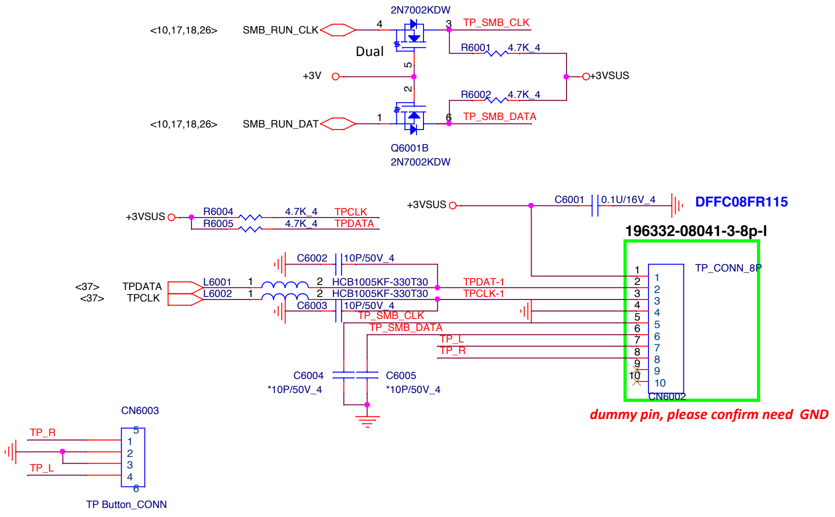
KEYBOARD Con.



KEYBOARD PULL-UP

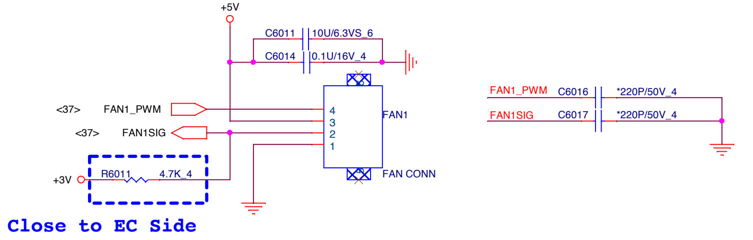


Touch Pad Connector



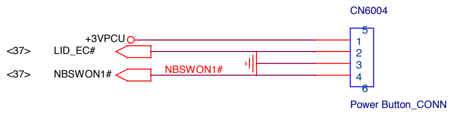
dummy pin, please confirm need GND

FAN



Close to EC Side

Power Button



NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- KB/TP/FAN	1A

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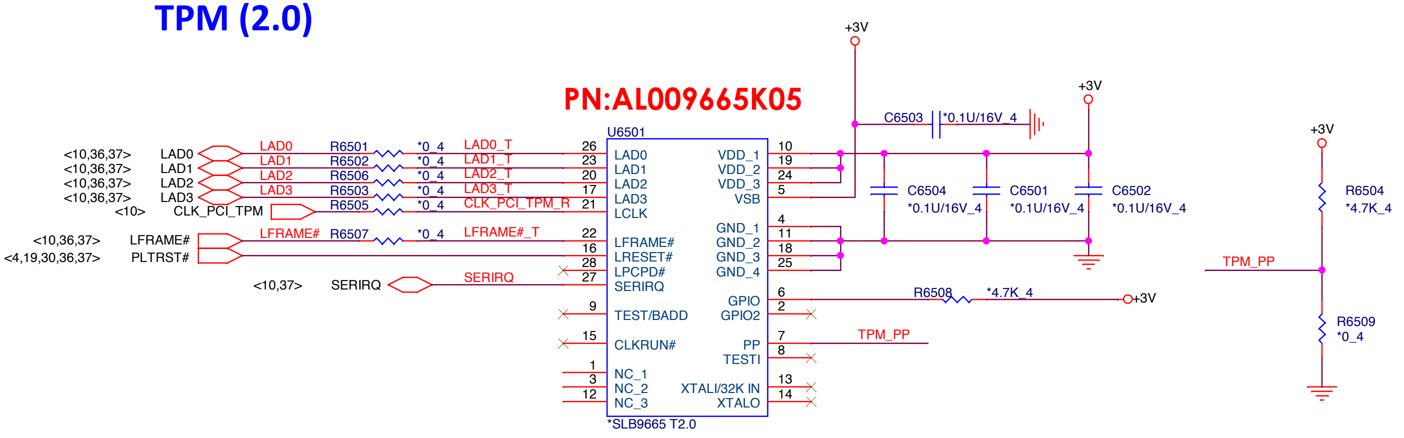
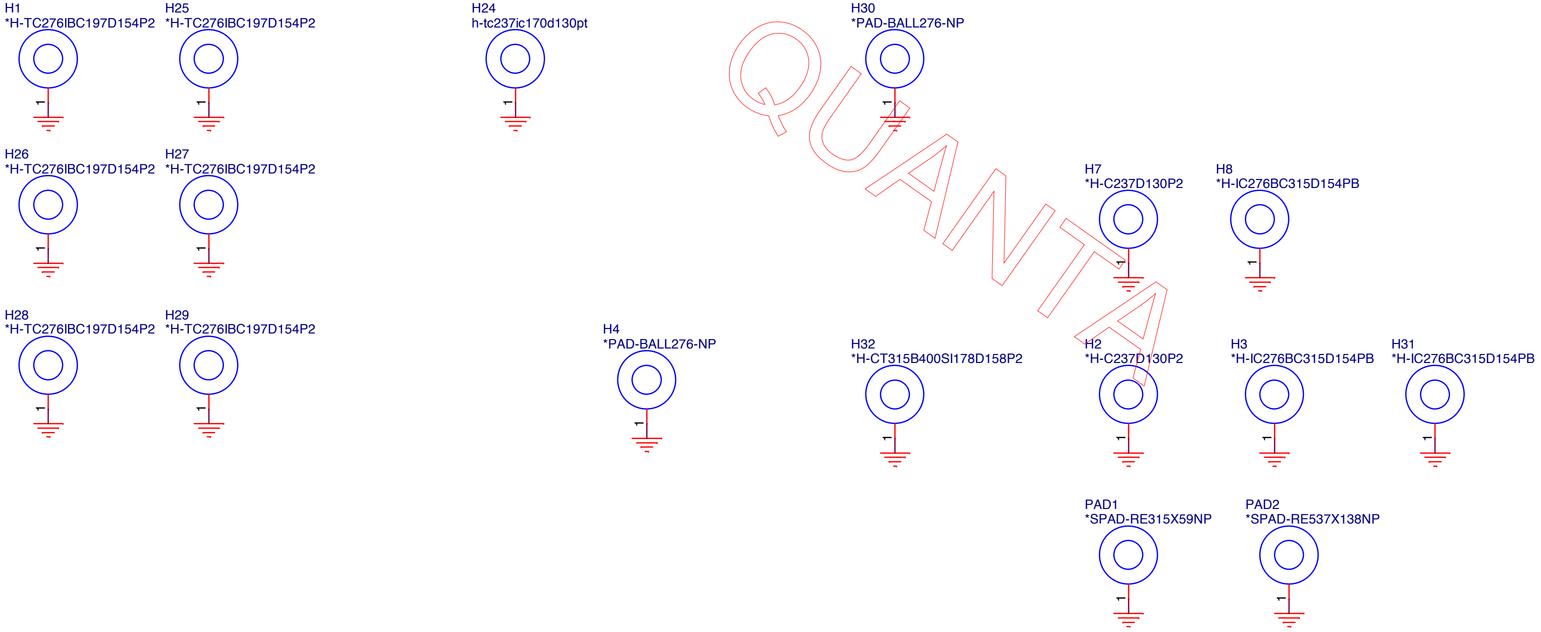
TPM (2.0)





NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
B	34 -- TPM/G-Sensor/IR CAM	1A

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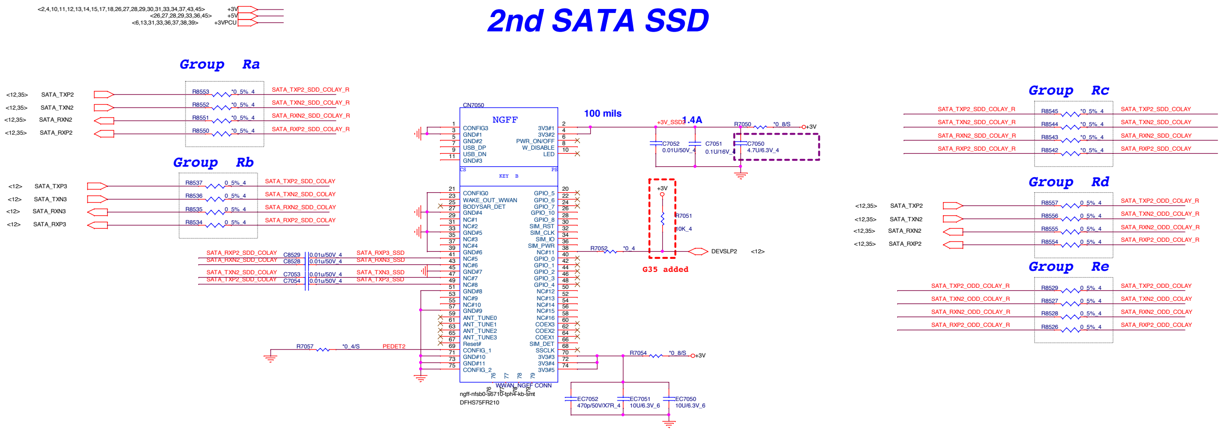
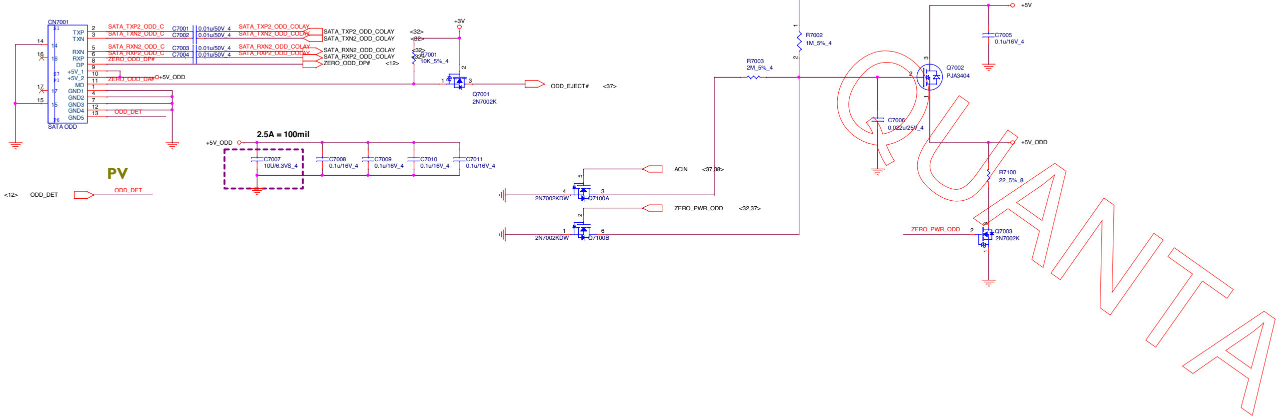
2nd SATA SSD



<2,4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,37,43,45> +3V
<26,27,28,29,33,36,45> +5V
<6,13,31,33,36,37,38,39> +3VPCU
Group Ra
<12,35> SATA_TXP2 R8553 *0_5%_4 SATA_TXP2_SDD_COLAY_R
<12,35> SATA_TXN2 R8552 *0_5%_4 SATA_TXN2_SDD_COLAY_R
<12,35> SATA_RXN2 R8551 *0_5%_4 SATA_RXN2_SDD_COLAY_R
<12,35> SATA_RXP2 R8550 *0_5%_4 SATA_RXP2_SDD_COLAY_R
Group Rb
<12> SATA_TXP3 R8537 0_5%_4 SATA_TXP2_SDD_COLAY
<12> SATA_TXN3 R8536 0_5%_4 SATA_TXN2_SDD_COLAY
<12> SATA_RXN3 R8535 0_5%_4 SATA_RXN2_SDD_COLAY
<12> SATA_RXP3 R8534 0_5%_4 SATA_RXP2_SDD_COLAY
SATA_RXP2_SDD_COLAY C8529 0.01u/50V_4 SATA_RXP3_SSD
SATA_RXN2_SDD_COLAY C8528 0.01u/50V_4 SATA_RXN3_SSD
SATA_TXN2_SDD_COLAY C7053 0.01u/50V_4 SATA_TXN3_SSD
SATA_TXP2_SDD_COLAY C7054 0.01u/50V_4 SATA_TXP3_SSD
R7057 *0_4/S PEDET2
CN7050
NGFF
CONFIG3 GND#1 GND#2 USB_DP USB_DN GND#3
3V3#1 3V3#2 PWR_ON/OFF W_DISABLE LED
CS KEY B PS
CONFIG0 WAKE_OUT_WWAN BODYSAR_DET GND#4 NC#1 NC#2 GND#5 NC#3 NC#4 GND#6 NC#5 NC#6 GND#7 NC#7 NC#8 GND#8 NC#9 NC#10 GND#9 ANT_TUNE0 ANT_TUNE1 ANT_TUNE2 ANT_TUNE3 Reset# CONFIG_1 GND#10 GND#11 CONFIG_2
GPIO_5 GPIO_6 GPIO_7 GPIO_10 GPIO_8 SIM_RST SIM_CLK SIM_IO SIM_PWR NC#11 GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 NC#12 NC#13 NC#14 NC#15 NC#16 COEX3 COEX2 COEX1 SIM_DET SSCLK 3V3#3 3V3#4 3V3#5
76 77 78 79
WWAN_NGFF CONN
ngff-nfsb0-s6710-tph4-kb-smt
DFHS75FR210
100 mils
+3V_SSD2 1.4A
R7050 *0_8/S +3V
C7052 0.01U/50V_4
C7051 0.1U/16V_4
C7050 4.7U/6.3V_4
+3V
R7051 10K_4
R7052 *0_4
DEVSLP2 <12>
G35 added
R7054 *0_8/S +3V
EC7052 470p/50V/X7R_4
EC7051 10U/6.3V_6
EC7050 10U/6.3V_6
Group Rc
SATA_TXP2_SDD_COLAY_R R8545 *0_5%_4 SATA_TXP2_SDD_COLAY
SATA_TXN2_SDD_COLAY_R R8544 *0_5%_4 SATA_TXN2_SDD_COLAY
SATA_RXN2_SDD_COLAY_R R8543 *0_5%_4 SATA_RXN2_SDD_COLAY
SATA_RXP2_SDD_COLAY_R R8542 *0_5%_4 SATA_RXP2_SDD_COLAY
Group Rd
<12,35> SATA_TXP2 R8557 0_5%_4 SATA_TXP2_ODD_COLAY_R
<12,35> SATA_TXN2 R8556 0_5%_4 SATA_TXN2_ODD_COLAY_R
<12,35> SATA_RXN2 R8555 0_5%_4 SATA_RXN2_ODD_COLAY_R
<12,35> SATA_RXP2 R8554 0_5%_4 SATA_RXP2_ODD_COLAY_R
Group Re
SATA_TXP2_ODD_COLAY_R R8529 0_5%_4 SATA_TXP2_ODD_COLAY
SATA_TXN2_ODD_COLAY_R R8527 0_5%_4 SATA_TXN2_ODD_COLAY
SATA_RXN2_ODD_COLAY_R R8528 0_5%_4 SATA_RXN2_ODD_COLAY
SATA_RXP2_ODD_COLAY_R R8526 0_5%_4 SATA_RXP2_ODD_COLAY

SATA ODD



NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 -- SSD_ODD_EMMC_ASM1153	1A

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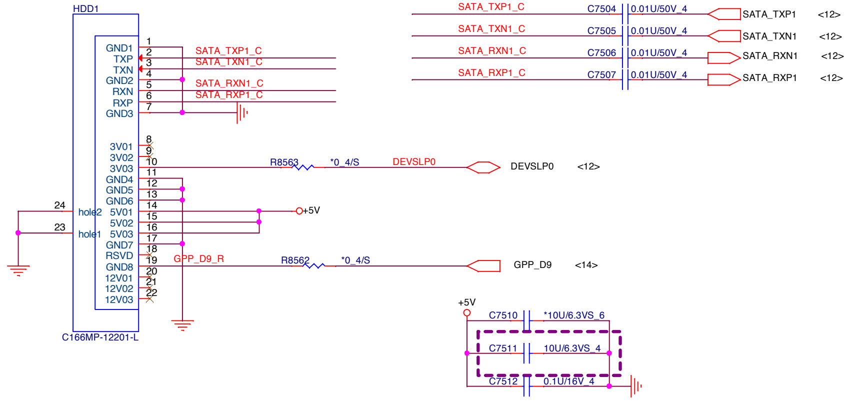
HDD

SATA HDD



WLAN

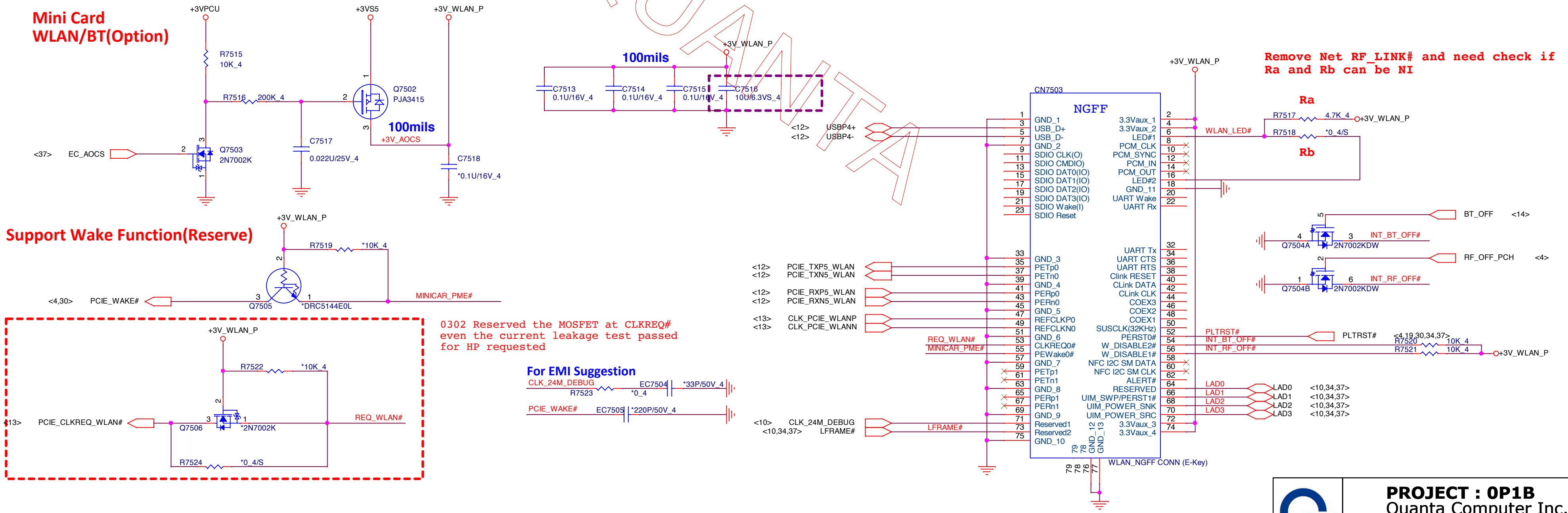
Mini Card
WLAN/BT(Option)

Support Wake Function(Reserve)

0302 Reserved the MOSFET at CLKREQ#
even the current leakage test passed
for HP requested

For EMI Suggestion

Remove Net RF_LINK# and need check if
Ra and Rb can be NI



NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 -- HDD/WLAN(NGFF)	1A

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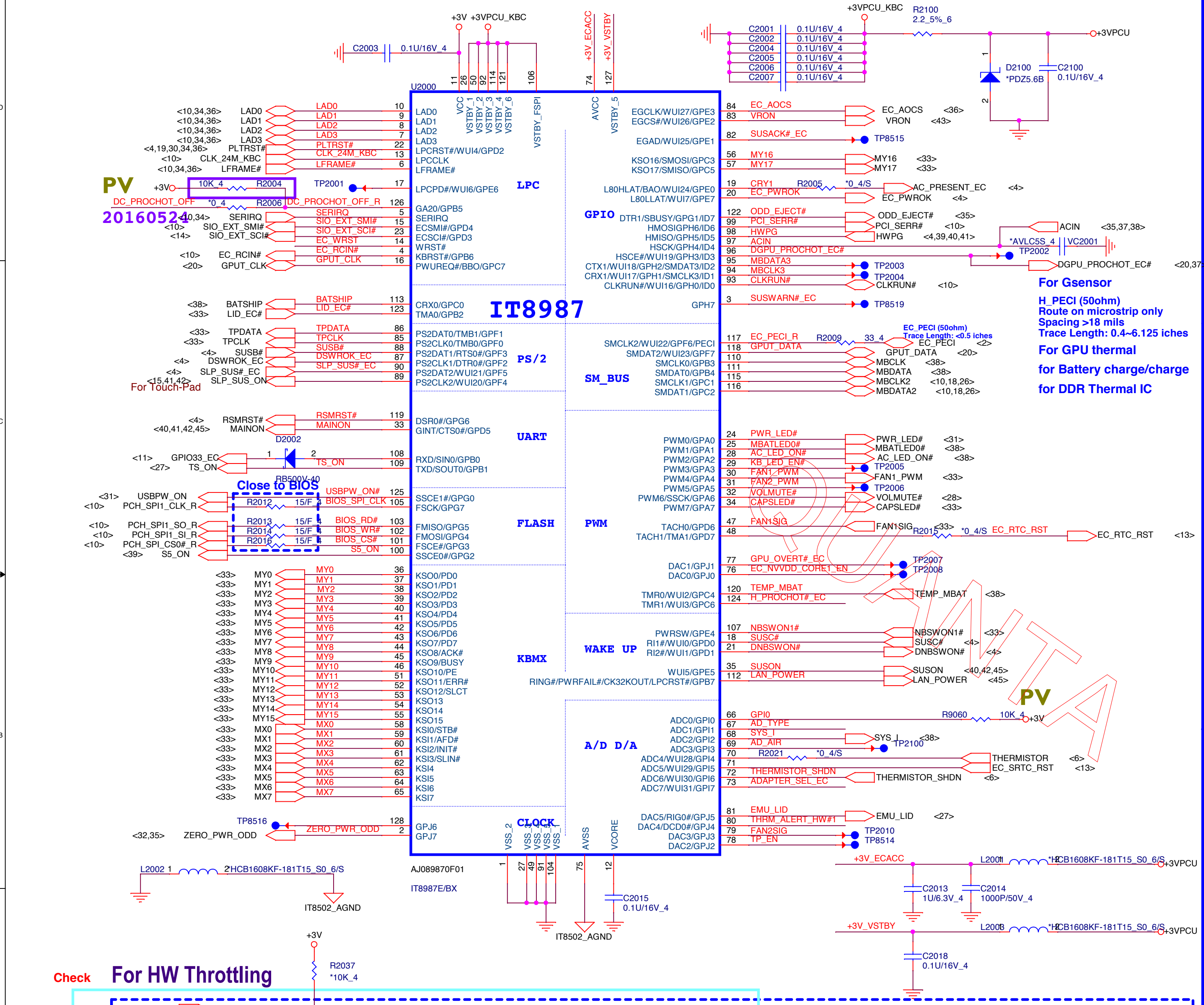
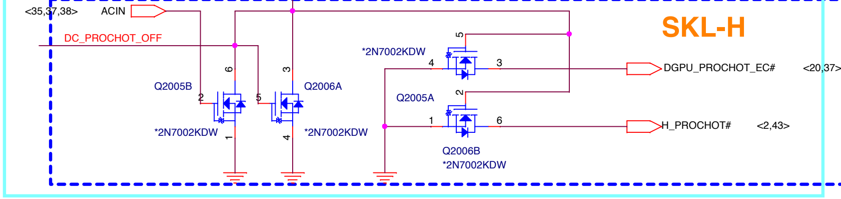
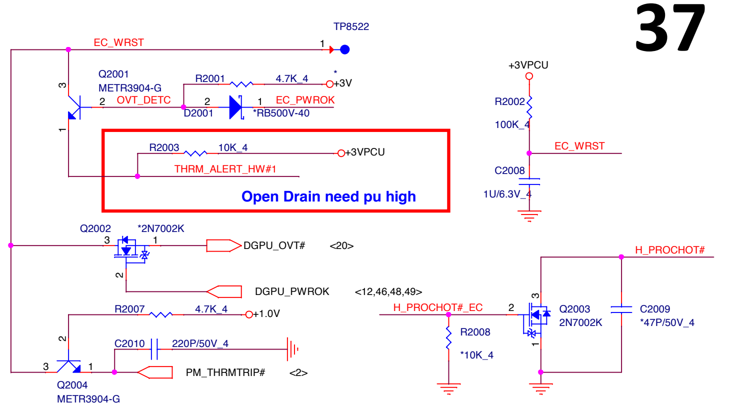
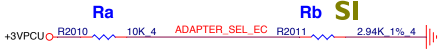




	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	**H**
AC remove: AC mode to DC mode	L	L	**L**
DC mode recover from PROCHOT	L	H	**H**

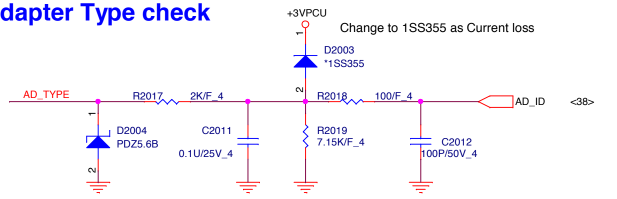


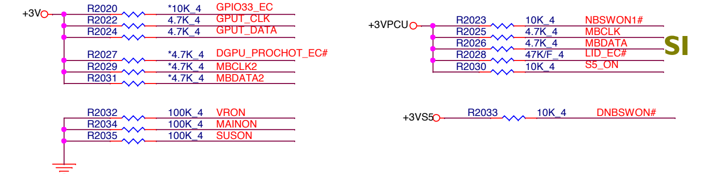
Adapter select for EC

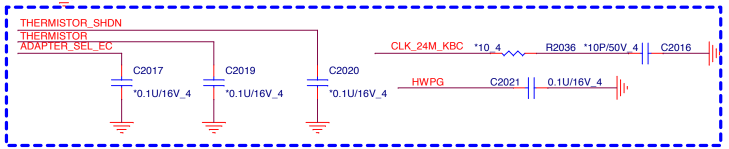


	Ra	Rb	ADAPTER_SEL_EC	BOM
150W	10K(CS31002FB26)	100K(CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K	2.25V	
90W	10K(CS31002FB26)	8.33K	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

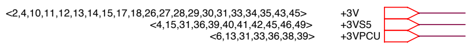
Adapter Type check







CLOSE to EC Pin


<2,4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,43,45> +3V
<4,15,31,36,39,40,41,42,45,46,49> +3VS5
<6,13,31,33,36,38,39> +3VPCU

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Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A

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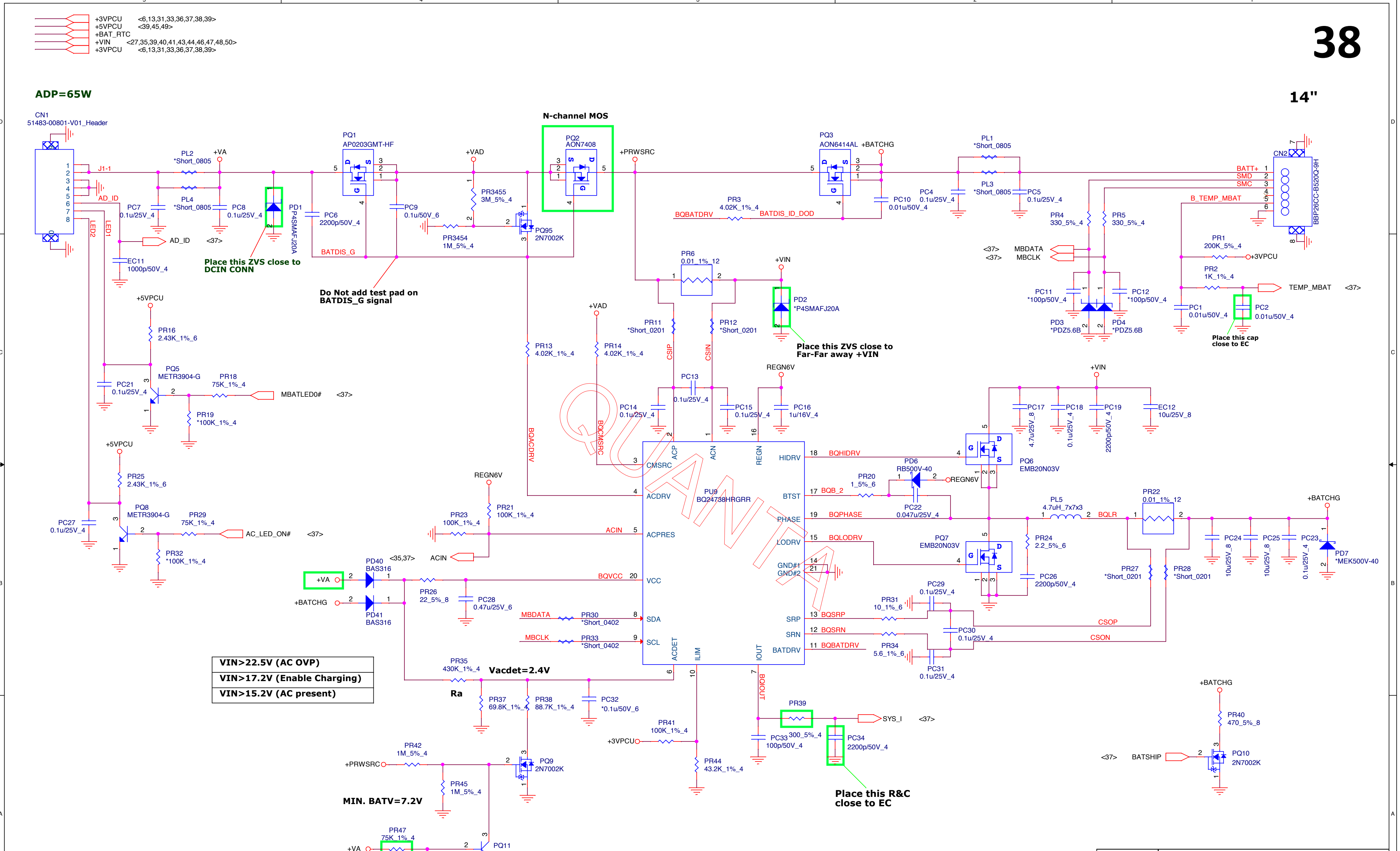
14"

ADP=65W



Place this ZVS close to DCIN CONN

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this R&C close to EC

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

MIN. BATV=7.2V

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Charger (BQ24738H)	1A

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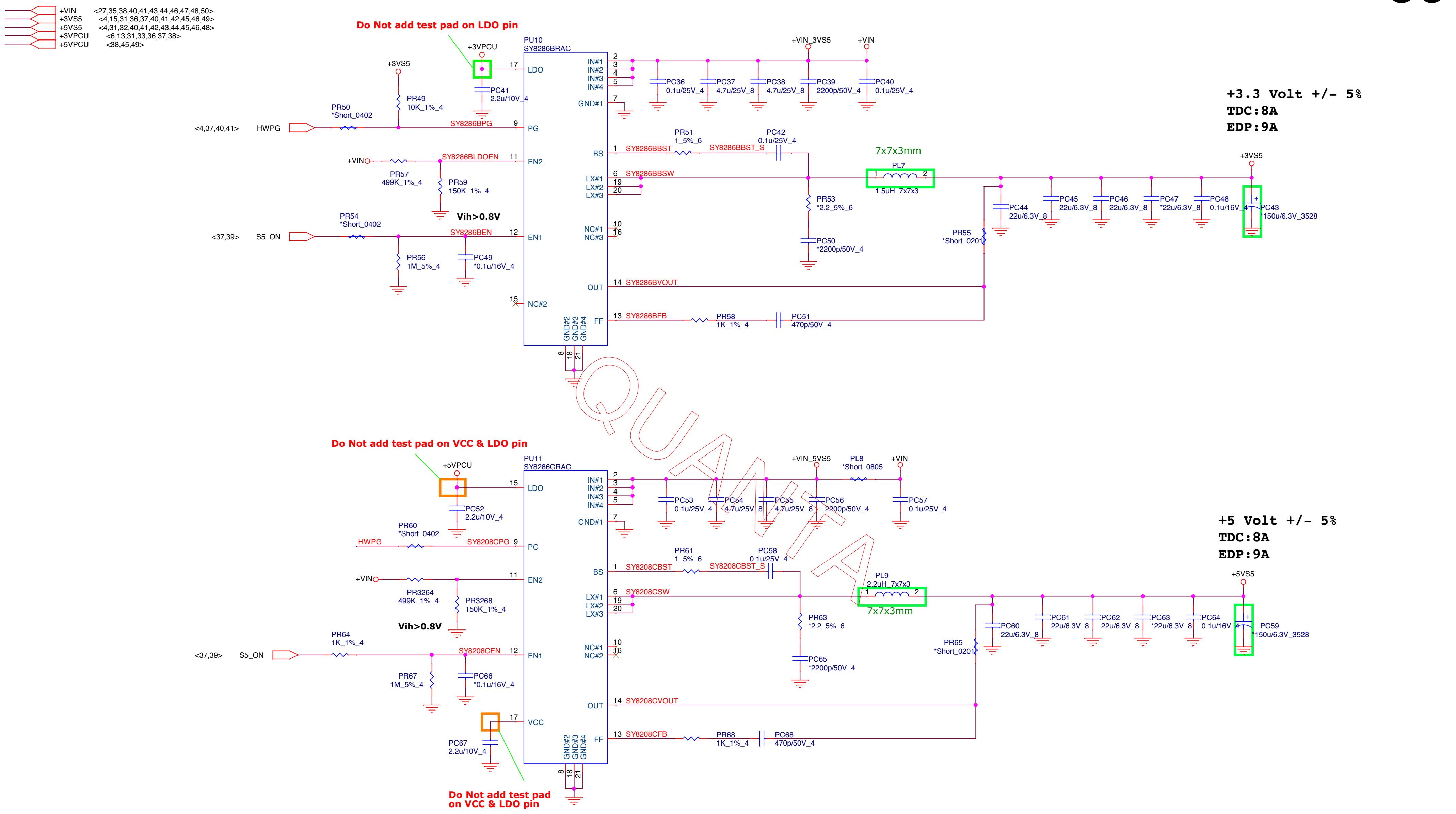
DC/DC +3VS5/+5VS5



NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A

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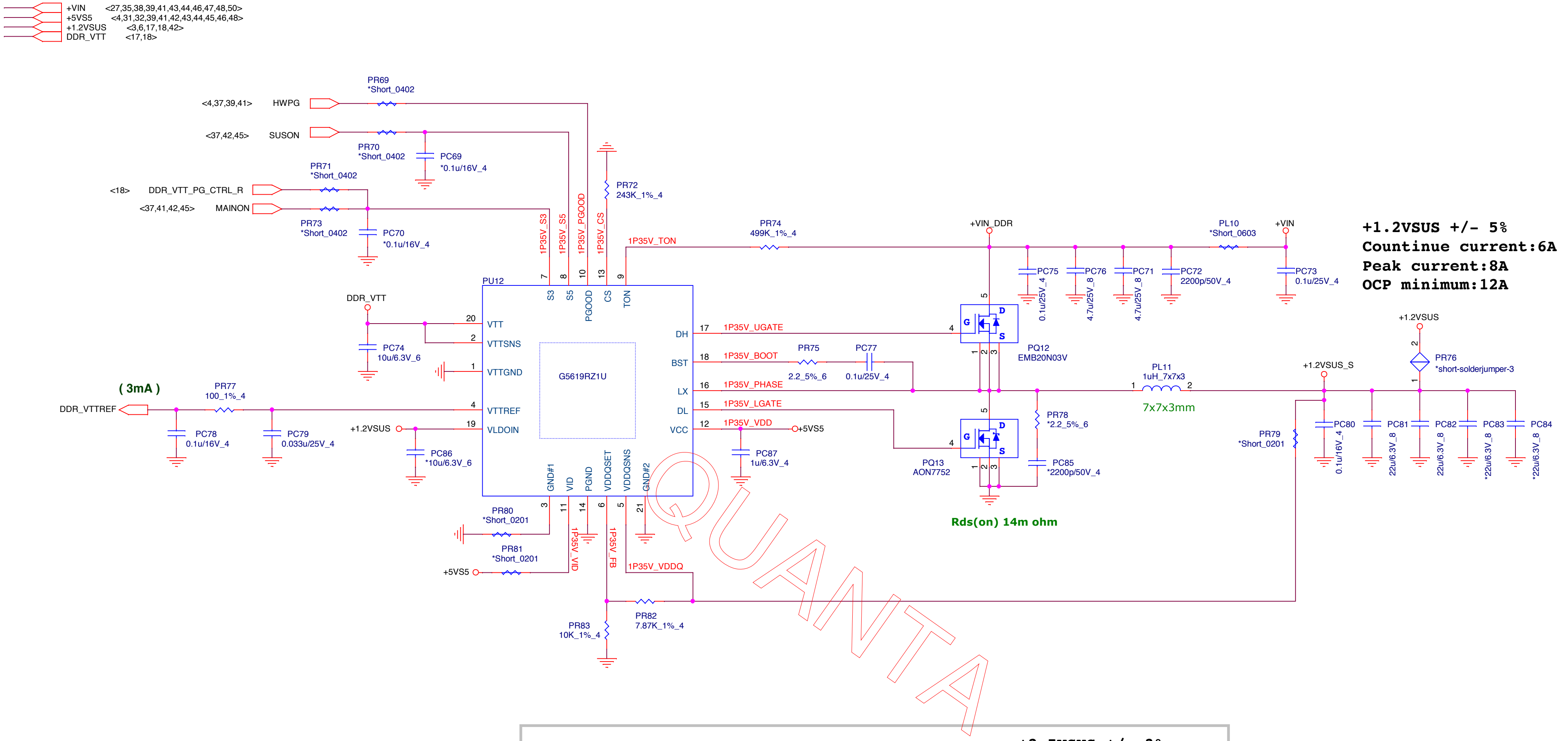
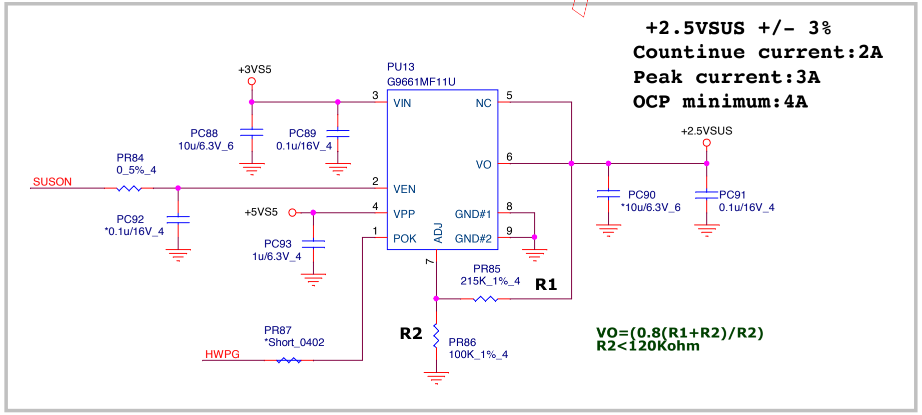


+1.2VSUS +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



+2.5VSUS +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

VO=(0.8(R1+R2)/R2)
R2<120Kohm

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
	DDR4 (G5619RZ1U)	1A

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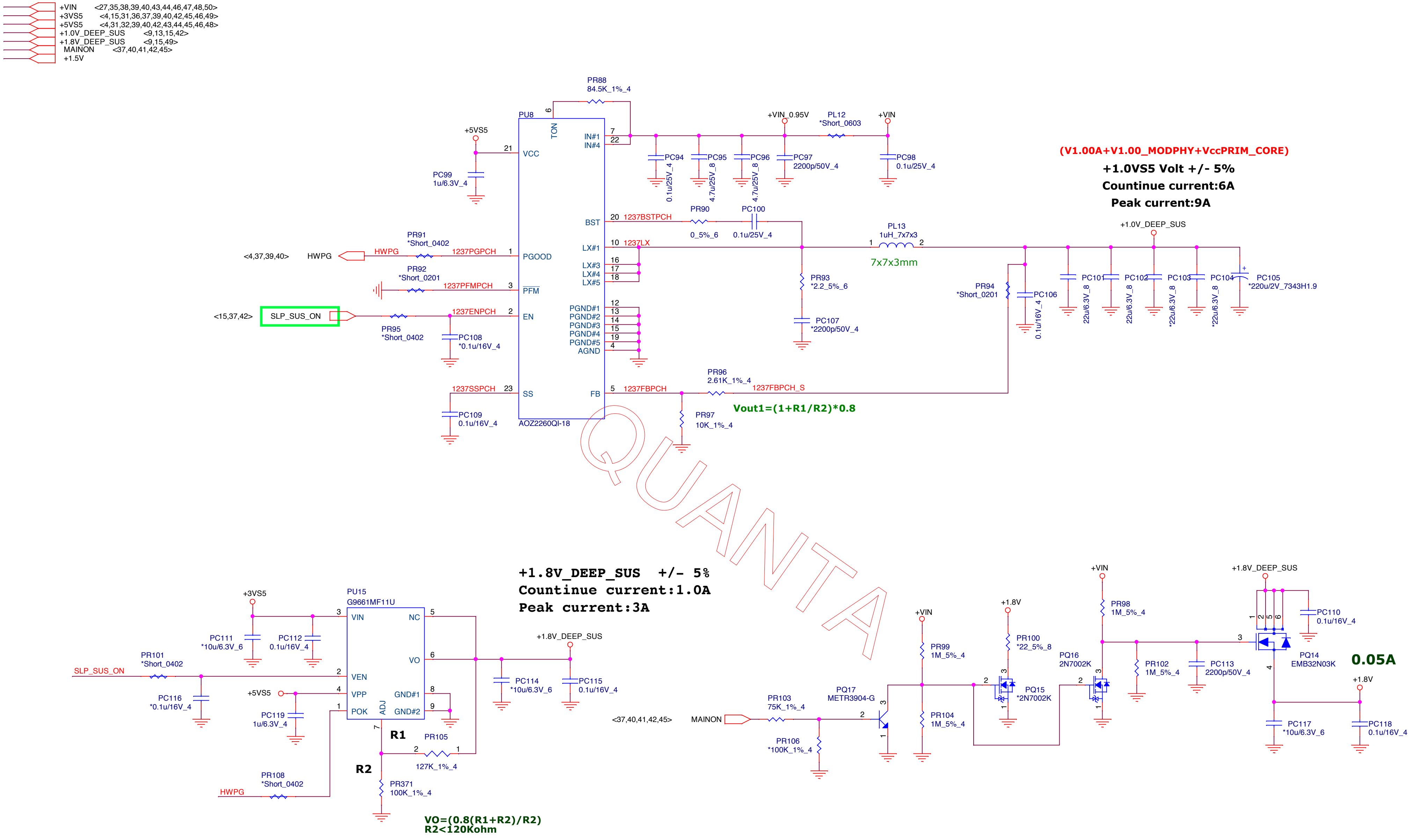

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)

+1.0VS5 Volt +/- 5%

Countinue current:6A

Peak current:9A

+1.8V_DEEP_SUS +/- 5%

Countinue current:1.0A

Peak current:3A

NB5

PROJECT : 0P1B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+1.8V_DEEP_SUS	1A

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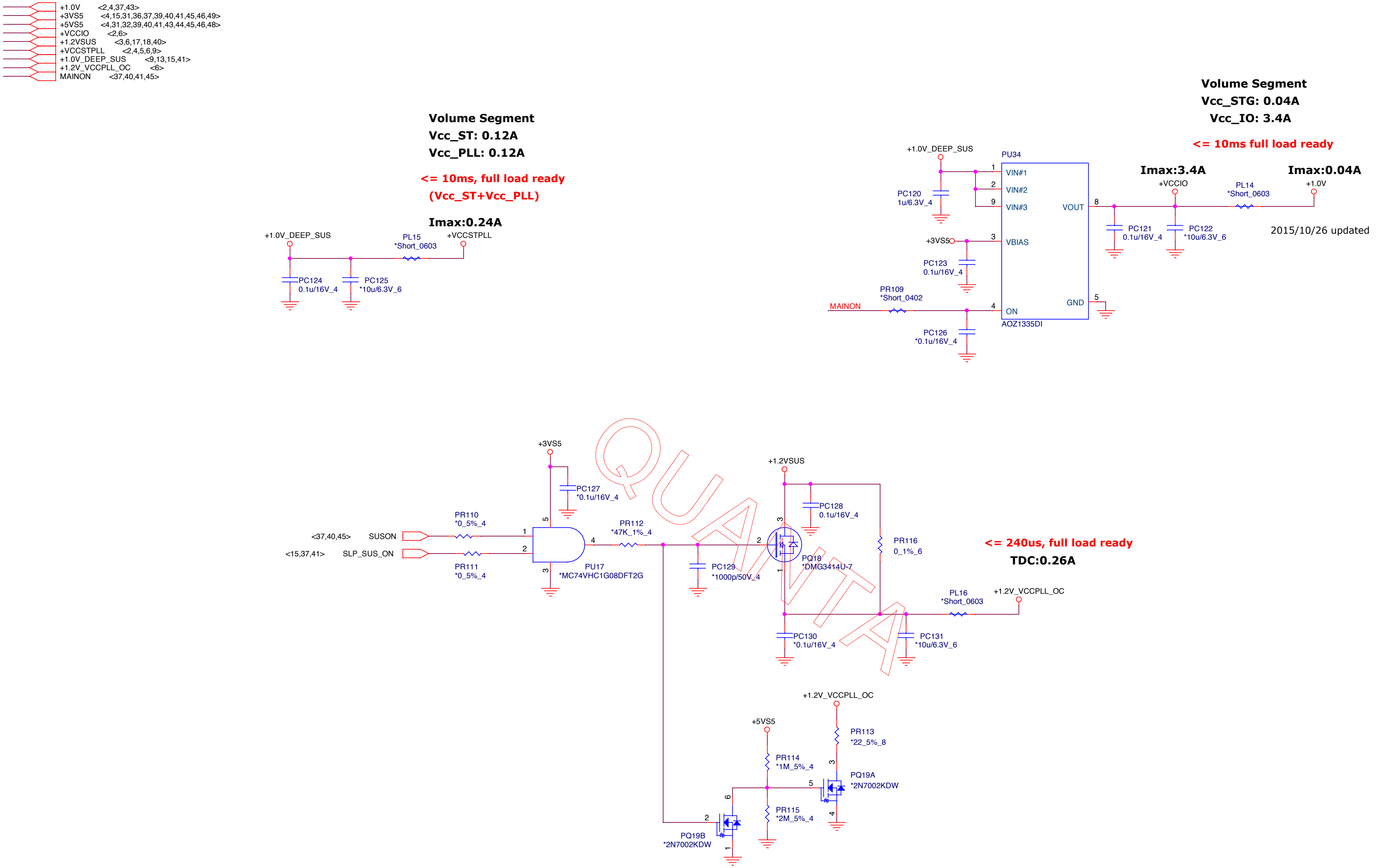

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

Imax:0.24A

Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A

Imax:0.04A

2015/10/26 updated

<= 240us, full load ready
TDC:0.26A

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A

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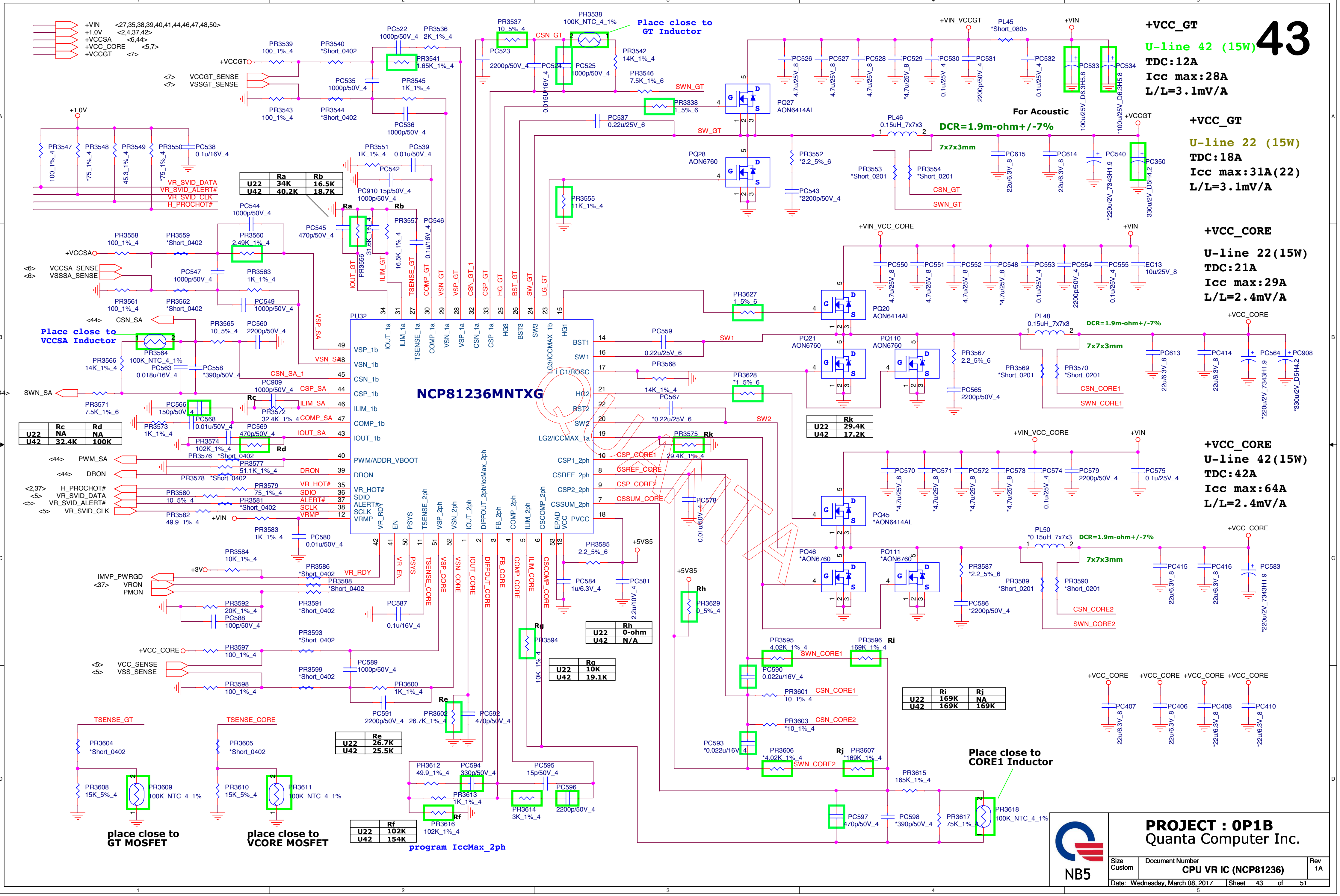

+VCC_GT
U-line 42 (15W)
TDC:12A
Icc max:28A
L/L=3.1mV/A

+VCC_GT
U-line 22 (15W)
TDC:18A
Icc max:31A(22)
L/L=3.1mV/A

+VCC_CORE
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

+VCC_CORE
U-line 42(15W)
TDC:42A
Icc max:64A
L/L=2.4mV/A

	Ra	Rb
U22	34K	16.5K
U42	40.2K	18.7K

	Rc	Rd
U22	NA	NA
U42	32.4K	100K

	Rk
U22	29.4K
U42	17.2K

	Rh
U22	0-ohm
U42	N/A

	Rg
U22	10K
U42	19.1K

	Re
U22	26.7K
U42	25.5K

	Rf
U22	102K
U42	154K

	Ri	Rj
U22	169K	NA
U42	169K	169K

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Quanta Computer Inc.

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Size	Document Number	Rev
Custom	CPU VR IC (NCP81236)	1A

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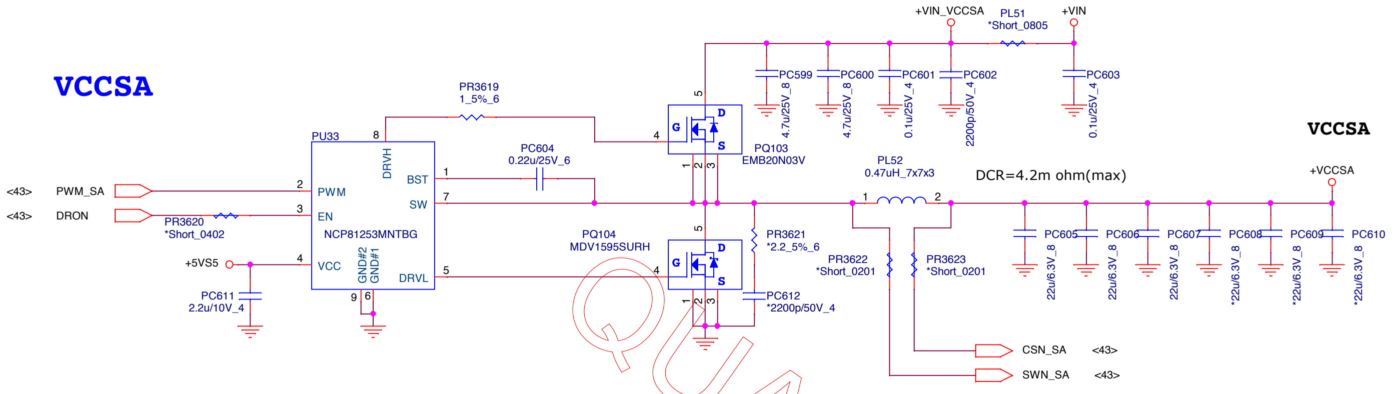

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	1A

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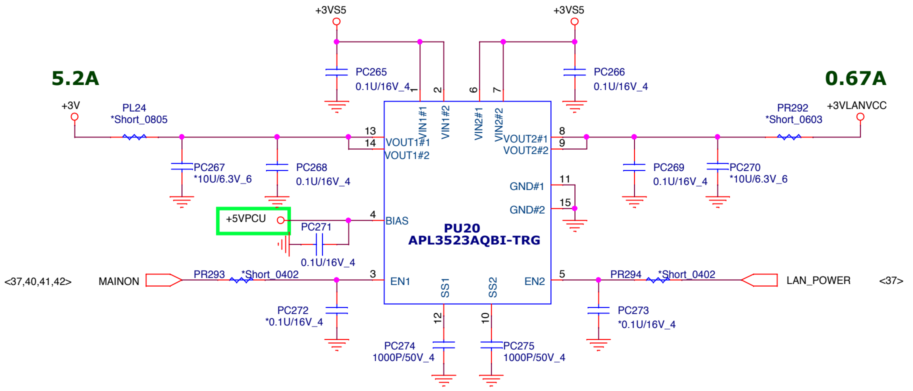
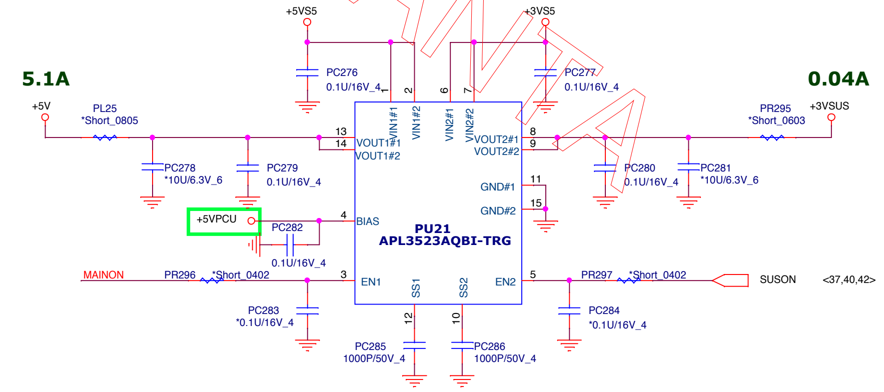
+3V <2,4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43>
+5V <26,27,28,29,33,35,36>
+VIN <27,35,38,39,40,41,43,44,46,47,48,50>
+3VS5 <4,15,31,36,37,39,40,41,42,46,49>
+5VS5 <4,31,32,39,40,41,42,43,44,46,48>
+3VSUS <33>
+5VPCU <38,39,49>
+3VLANVCC <30>





NB5

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Size	Document Number	Rev
Custom	**Load switch IC (APL3523A)**	1A

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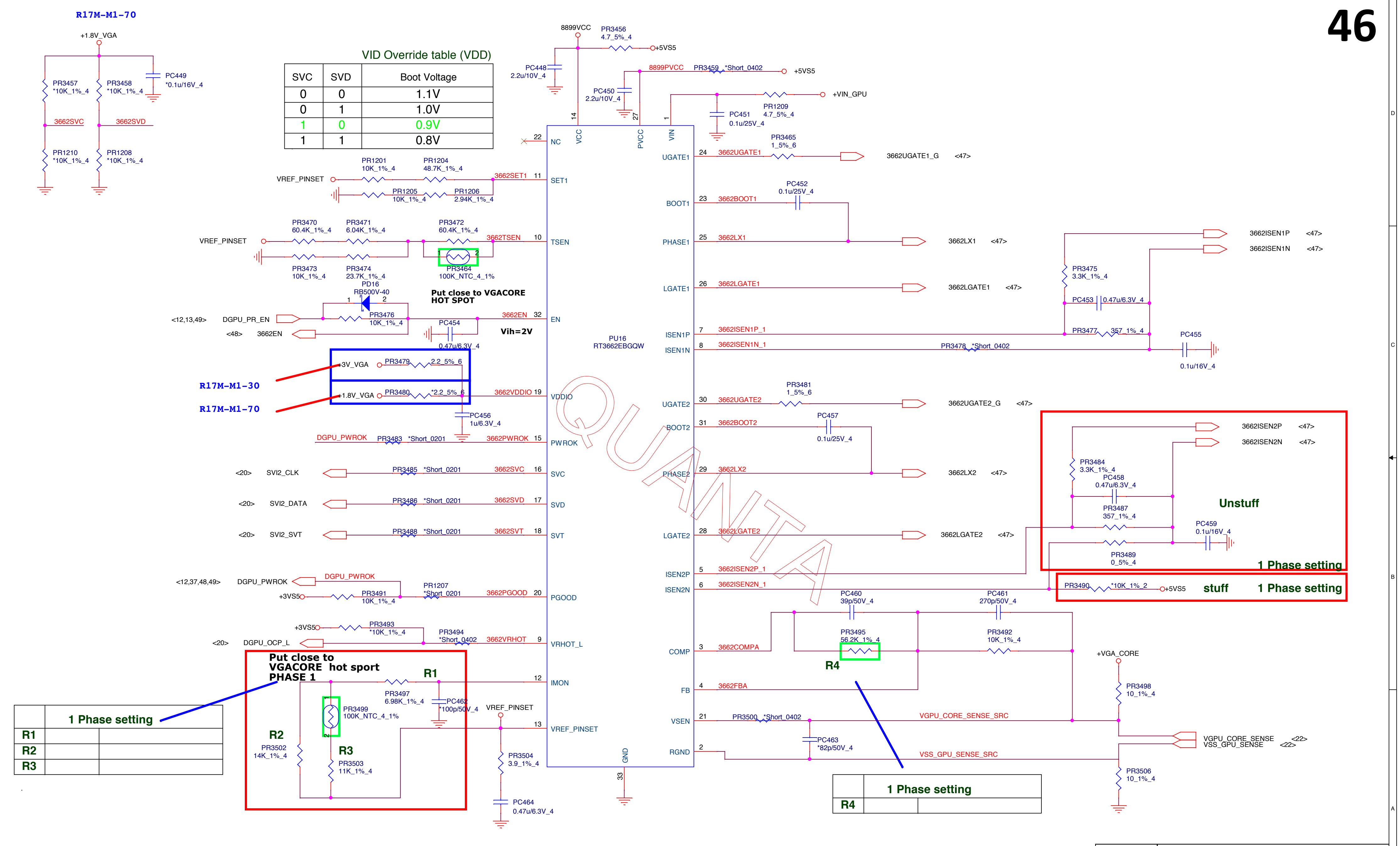

VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

	1 Phase setting	
R1		
R2		
R3		

	1 Phase setting	
R4		

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Quanta Computer Inc.

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Size	Document Number	Rev
Custom	EC ENE KB9027B	1A

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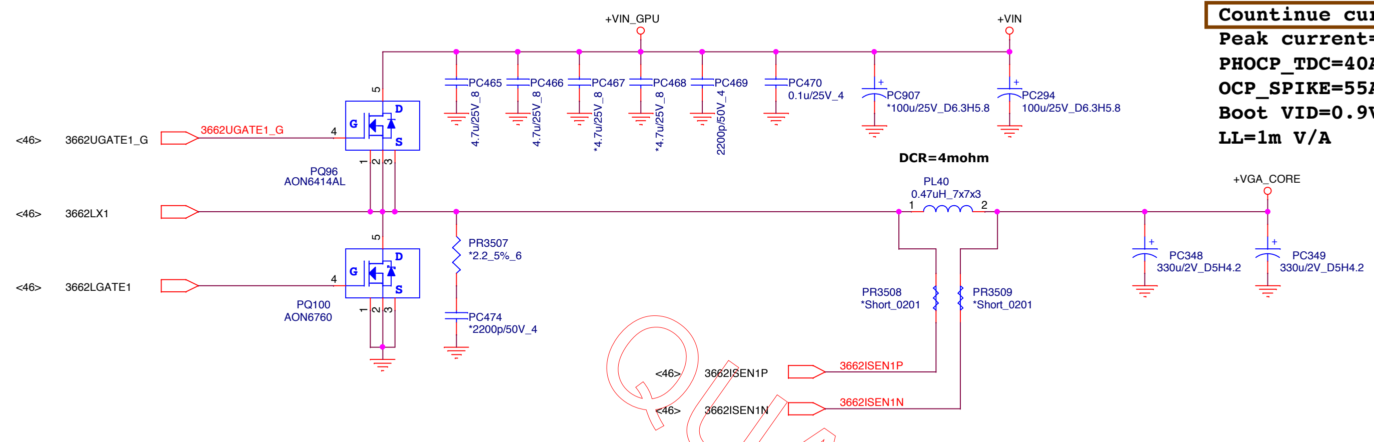


VGACORE (R17M-M1-30_ 25W/38W(1ms))

Countinue current:28A

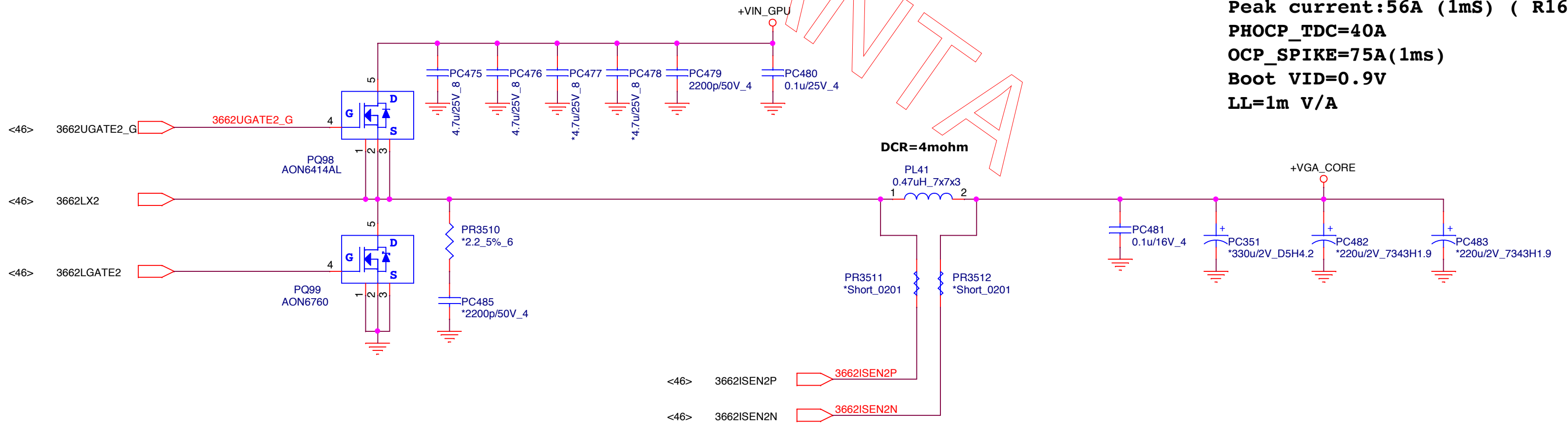
Peak current=38A (1ms)

PHOCP_TDC=40A (soft-start only)

OCP_SPIKE=55A(1ms)

Boot VID=0.9V

LL=1m V/A



VGACORE (R16M-M2-50_ 37W/56W(1ms))

Countinue current:40A (R16M-M2-50)

Peak current:56A (1mS) (R16M-M2-50)

PHOCP_TDC=40A

OCP_SPIKE=75A(1ms)

Boot VID=0.9V

LL=1m V/A

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Custom	EC ENE KB9027B	1A

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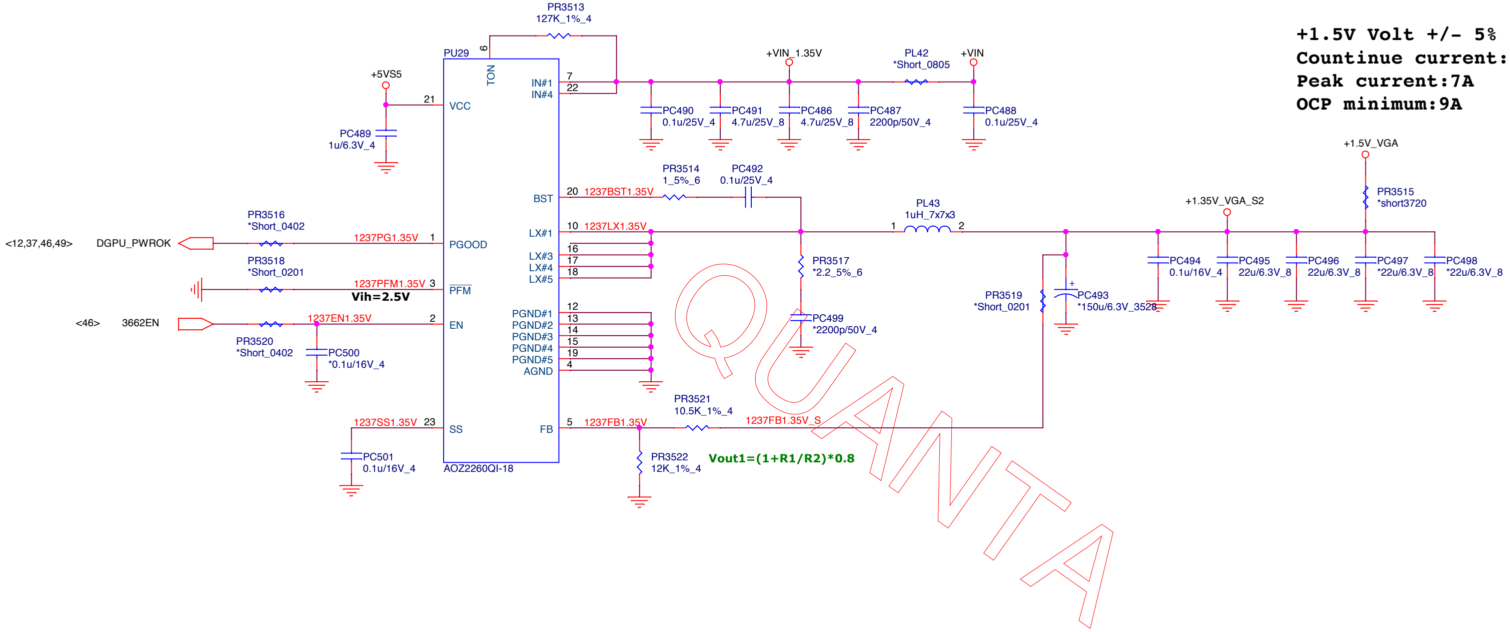

+1.5V Volt +/- 5%
Countinue current:6A
Peak current:7A
OCP minimum:9A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

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1A
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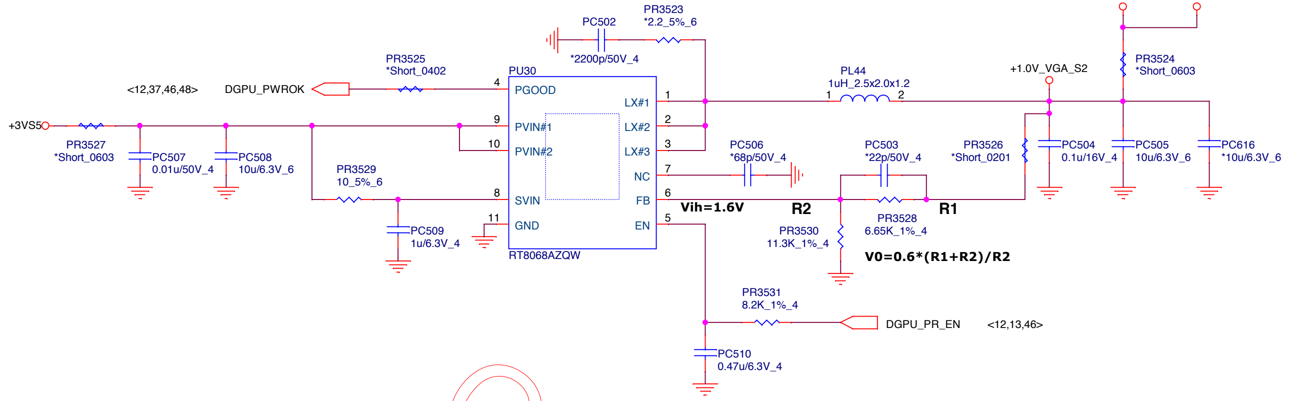
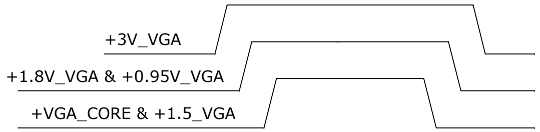
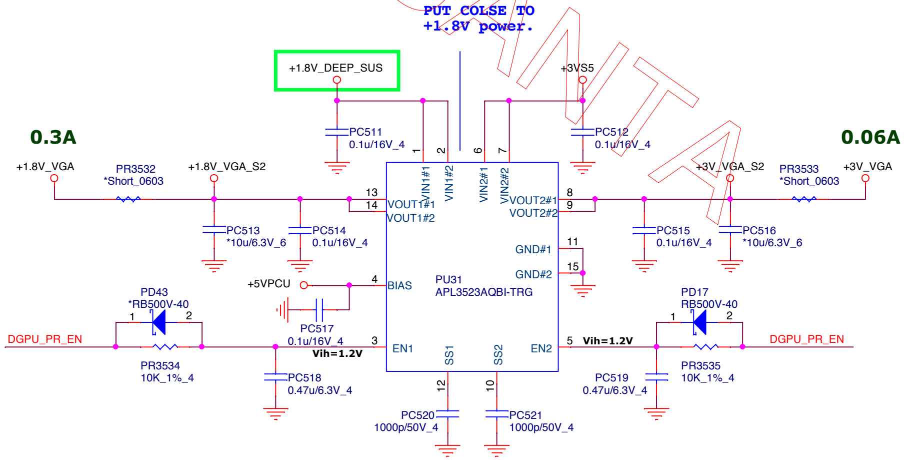
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A







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Quanta Computer Inc.

Size	Document Number	Rev
Custom	**EC ENE KB9027B**	1A

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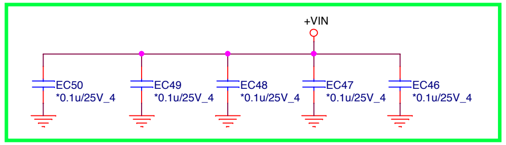
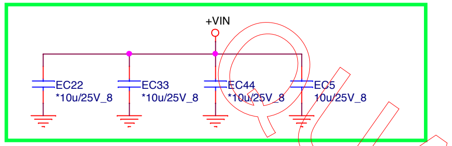
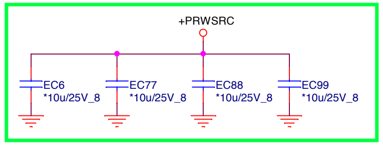


EMI request for ISN



EMI request for ISN



NB5

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Size Custom	Document Number **EMI solution**	Rev 1A 1A
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NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**EC ENE KB9027B**	1A

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