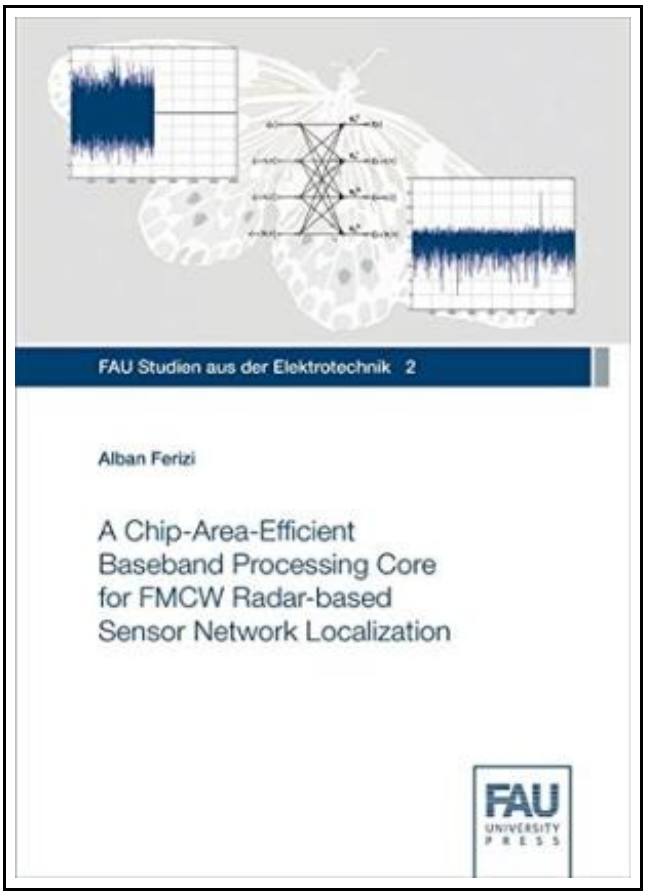
A Chip-Area-Efficient Baseband Processing Core for FMCW Radar-based Sensor Network Localization



Filesize: 1.42 MB

Reviews

Very good e-book and helpful one. It is among the most awesome publication we have read. Its been developed in an remarkably simple way in fact it is simply right after i finished reading this book through which basically transformed me, affect the way i really believe.

(Prof. Kacey O'Hara)

A CHIP-AREA-EFFICIENT BASEBAND PROCESSING CORE FOR FMCW RADAR-BASED SENSOR NETWORK LOCALIZATION

To download **A Chip-Area-Efficient Baseband Processing Core for FMCW Radar-based Sensor Network Localization** eBook, you should refer to the hyperlink below and download the document or have access to other information which are relevant to A CHIP-AREA-EFFICIENT BASEBAND PROCESSING CORE FOR FMCW RADAR-BASED SENSOR NETWORK LOCALIZATION ebook.

FAU University Press Jan 2015, 2015. Taschenbuch. Book Condition: Neu. 241x172x12 mm. Neuware - There exists a variety of industrial applications in local environments, with an increasing demand for low-power and high-precision local positioning solutions based on wireless sensor networks. The focus of developing autonomous and cooperative sensor nodes with localization functionality is on the localization accuracy and range, energy efficiency and the size of the sensor nodes. In this context special attention is paid to the sensor digital signal processing, where the main task is to perform a Fast Fourier Transform (FFT). In this work the design of the radix-4 DIF FFT algorithm and its optimization with respect to hardware implementation for low-power local positioning systems is introduced. Furthermore, an area-efficient digital implementation of a baseband processing core for autonomous wireless sensor nodes with localization functionality is presented. The challenge for designing the digital system was to reduce memory requirements towards a low cost hardware design in general, and particularly for an ASIC design. Reducing chip area implies lower energy consumption and helps saving implementation and production costs. The presented novel baseband processing system concept has been implemented and verified on an FPGA. For the application scenario of a two-sweep-measurement system, an ASIC layout is designed based on the IBM 130 nm CMOS technology. 130 pp. Englisch.

See Also