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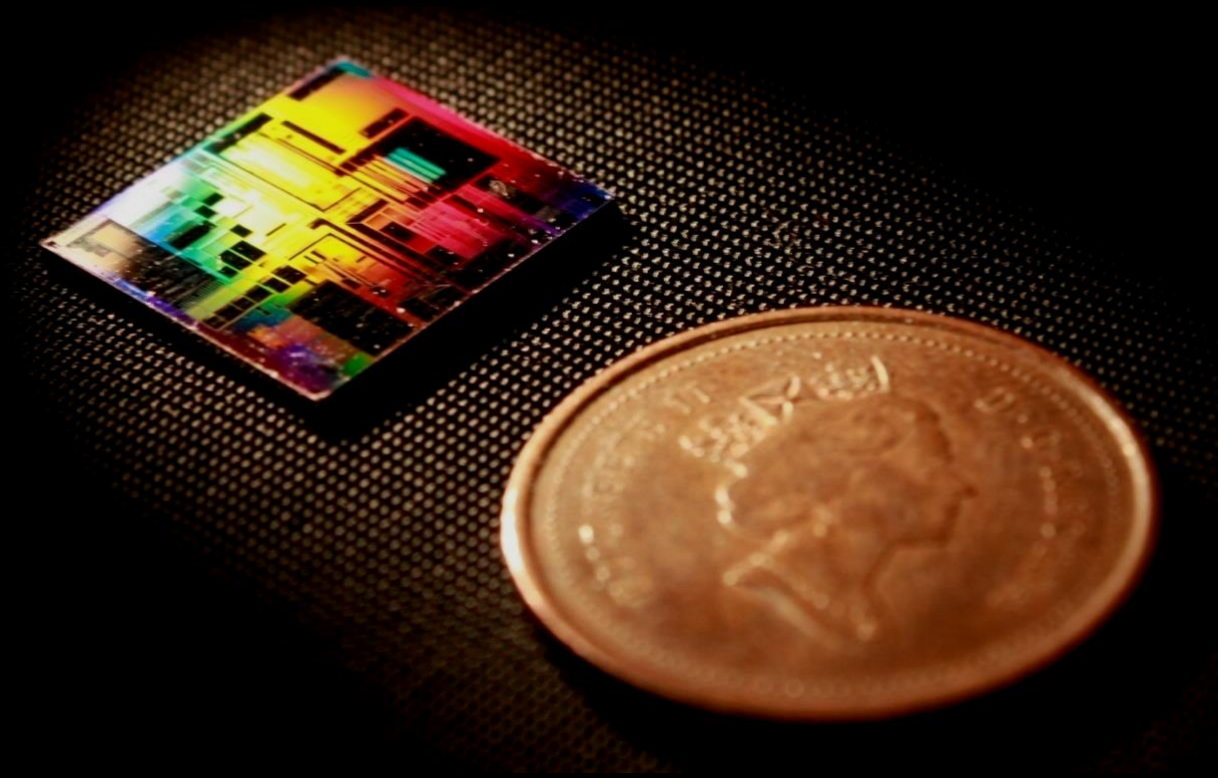
Designing and Planning Layouts

2019 SiEPIC Passive Silicon Photonics Workshop, Vancouver, Canada



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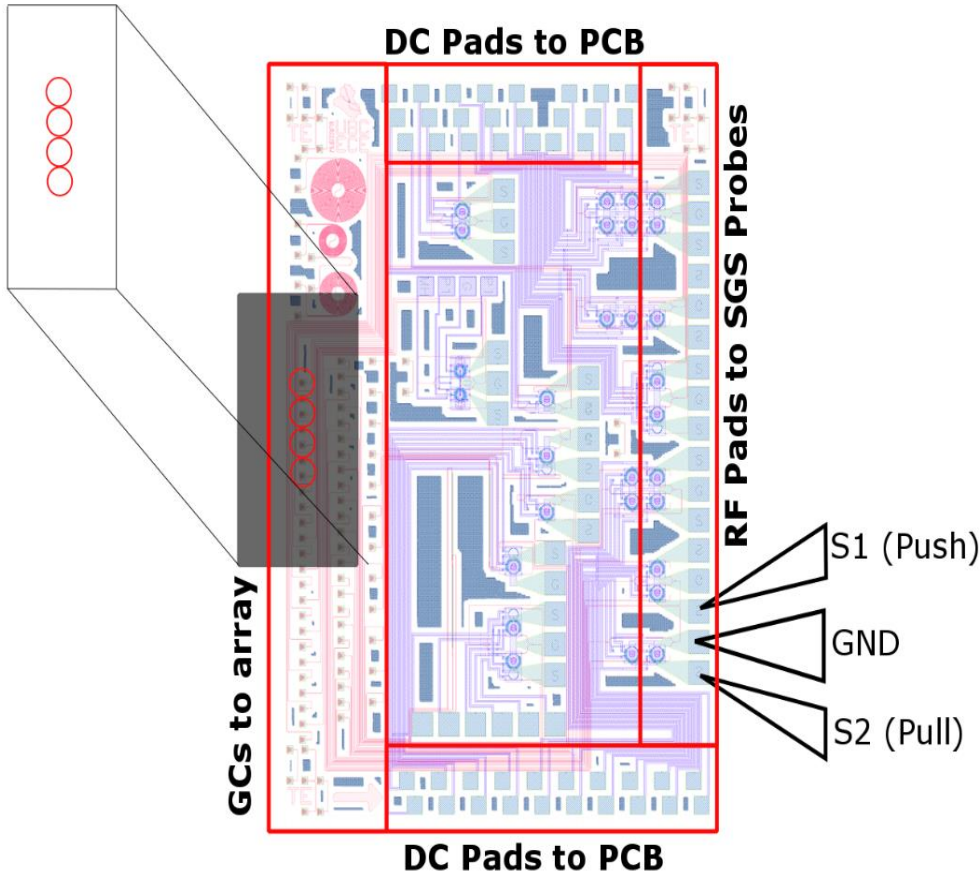
Keep your layout hierarchal

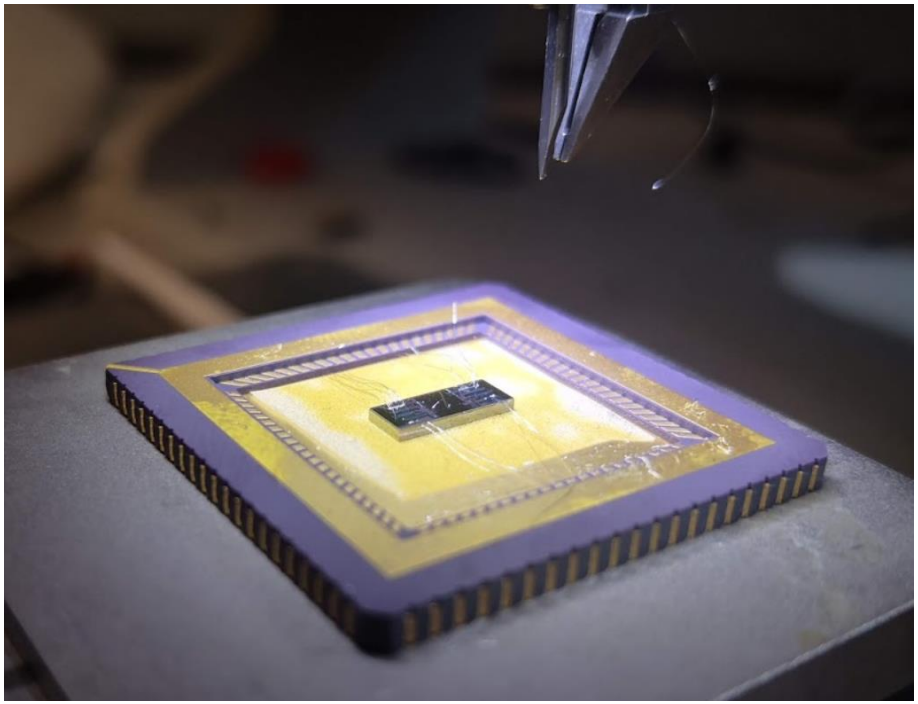
- **Don’t flatten your layout (or at least save the flattened as a separate version)**
- **Maintains your Pcell properties**

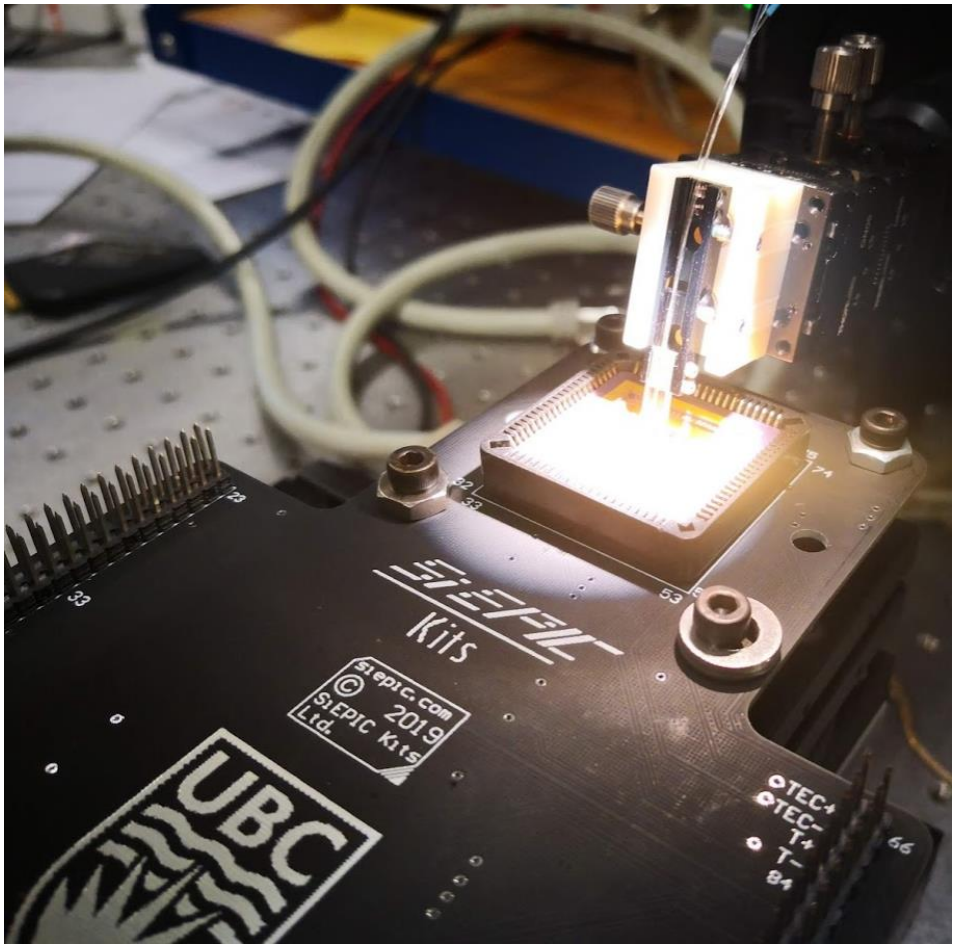
Design for testing

- Think of all the off-chip interfaces
  - Optical fiber array(s)
  - DC Probing needles
  - DC wire bonds
  - RF Probing
    - Microwave traces
    - Impedance matching
      - On-chip termination?
        - Sheet resistance /sq.
    - Which probe are you using?
      - Pad pitch
      - GS/GSG (single drive)
      - SGS/ GSGSG (push-pull)



Design for packaging





Alignment

- **Alignment and automated testing is not easy, unless you design for it**
- **Keep all your GCs in the same orientation**