

FIGURE 3-2. P/O POWER SUPPLY PCB

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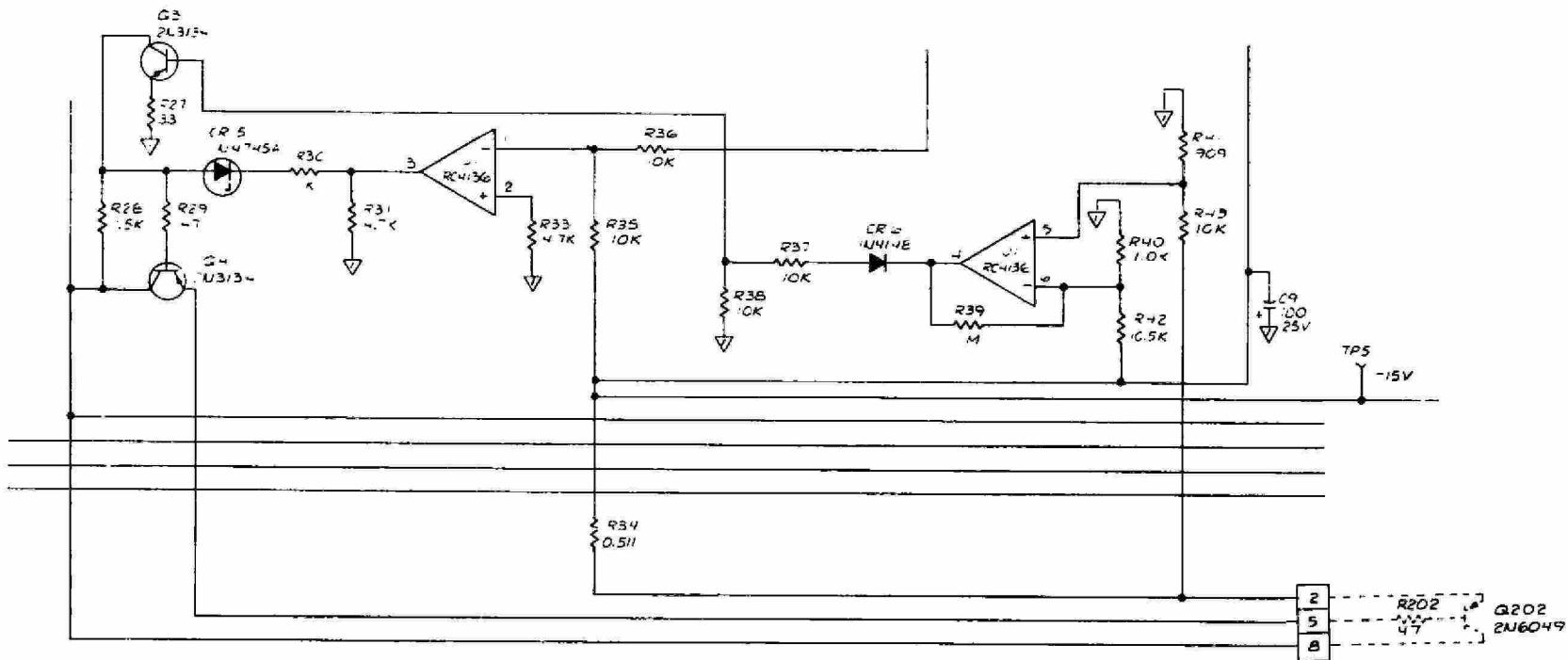


FIGURE 3-3. P/O POWER SUPPLY PCB

is filtered by C6 with bleeder R25 which produces $-24 \text{ volts} \pm 1.5 \text{ volts}$ with a typical ripple of 2.0 volts peak-to-peak to be used as the System Unregulated -24 volts.

The various operational amplifier circuits on the power supply card require both + and -15 volts for their operation. The +15 volts is obtained with zener diode CR10 with filter C4 and series dropping resistor R4. The -15 volts is obtained with zener diode CR14 with filter C7 and series dropping resistor R26.

The +24 volts is applied to the regulator driver Q1 and pass-gate Q201 to produce the regulated +15 volts for the system. The emitter of Q201 (nominal +15 volts) through current sense resistor R7 is applied to a voltage divider network consisting of R13, potentiometer R14, and R15. The wiper of R14 is about +3.0 volts when the output is exactly +15 volts. This +3.0 volts is applied to the inverting input of U1D operational amplifier. The non-inverting input of U1D has a reference potential from zener diode CR12 of 8.8 volts DC. This 8.8 volts is dropped by a voltage divider R10 and R11 to produce about 3.0 volts at the non-inverting input at U1D. The resulting output of U1D is applied through forward biased zener diode CR11 to the pass-gate driver Q1 which maintains the output at +15 volts DC as set by R14 (+15 volts $\pm 0.1V$). Current limiting is accomplished by U1C with current sensing in R7. On the input of R7 (emitter of Q201) there is a voltage divider consisting of R18 and R19. With exactly 15 volts from Q201 emitter, the voltage from the divider to the non-inverting input of U1C is about +1.241 volts DC. With no current flow the voltage at the junction of R7 and R12 would also be +15 volts which would produce +1.304 volts DC from the voltage divider R17 and R16 to the inverting input of U1C. The output of U1C is then negative and Q2 is cut off allowing the regulator to function. At about 1.5 amperes current flow however, the junction of R17 and R16 drops below the output of R18 and R19 and the polarity of the U1C output goes positive. This will turn on Q2 which will reduce the voltage in the output to keep total current less than 1.5 amperes.

The negative regulator functions in a similar manner. The -24 volt system supply is applied to the regulator driver Q4 and pass-gate Q202 to produce the regulated -15 volts for the system. The emitter of Q202 (nominal -15 volts) through current sense resistor R23 is applied to a voltage divider network consisting of R35 and R36 to +15 volts. Since these resistance values are equal, their junction output to U1A inverting input is 0 if the + and - supplies are correct. The non-inverting input of U1A is referenced to ground (0 volts). The output of U1A is applied through forward biased zener diode CR15 to the pass-gate driver Q4 which maintains the output at -15 volts DC if the +15 volts has been properly set. Current limiting is accomplished by U1B with current sensing in R34. On the input of R34 (emitter of Q202) there is a voltage divider consisting of R41 and R43 which places -1.241 volts DC on the non-inverting input of U1B. With no current flow the voltage divider R40 and R42 place a -1.304 volts DC on the inverting input of U1B.

The output of U1B then is positive and Q3 is cut off allowing the regulator driver Q4 to function. At about 1.5 ampere current flow the junction of R40 and R42 goes more positive than the non-inverting input and U1B output goes negative. This will turn on Q3 which will reduce the voltage in the output to keep the current less than 1.5 amperes.

Crowbar IC's (U2 and U3, not shown) which toggle at 17 volts have been added to the power supply between TP4 and ground and at TP5 and ground. These crowbars protect the output in the event of a regulator failure. The effective serial number of insertion was 138 in November of 1975. All units shipped after this time have been so modified.

3.3 TESTS AND ADJUSTMENTS

See Figure 3-4 for component location.

1. **± 24 Volt Unregulated System Supply**
 - a. Measure the value of the voltage on the electrolytic capacitor C3, + end.
 - b. This voltage is a nominal $+24$ volt DC ± 1.5 volts with a typical ripple of 2.0 volts peak-to-peak.
 - c. Measure the value of the voltage on the electrolytic capacitor C6, - end.
 - d. This voltage is a nominal -24 volts DC with a typical ripple of 2.0 volts peak-to-peak.
2. **± 15 Volt Regulated System Supply**
 - a. Measure the value of the voltage on TP4 (TP4 to TP6).
 - b. This voltage is $+15 \pm 0.1$ volts with a typical ripple of 1 millivolt.
 - c. Adjust the voltage within these specifications with R14 which is the only potentiometer on the card.
 - d. The output is protected with a 17 volt crowbar P/N 78-590-200 on Serial 138 (December 1975) and higher. This crowbar is designated U2 and is located as shown in Figure 3-4.
 - e. Measure the value of the voltage on TP5 (TP5 to TP6).
 - f. This voltage is -15 ± 0.4 volts with a typical ripple of 1 millivolt.

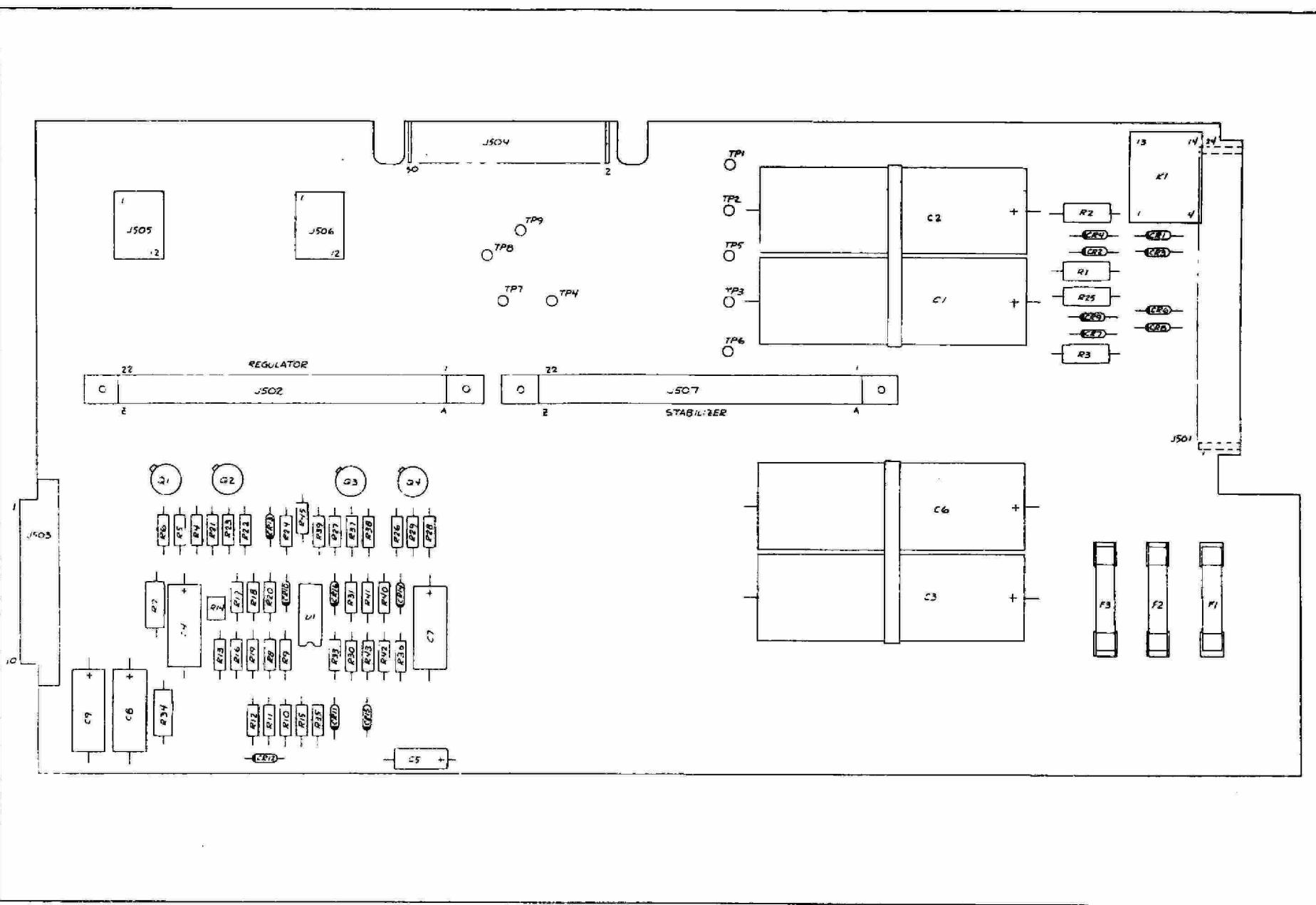


FIGURE 3-4. COMPONENT LOCATION

- g. The output again is protected with a 17 volt crowbar P/N 78-590-200 on Serial 138 (December 1975) and higher. This crowbar is designated U3 and is located as shown in Figure 3-4.
- 3. **±24 Volt Unregulated Recorder Supply**
 - a. Measure the value of the voltage at TP1 (TP1 to TP3).
 - b. This voltage is $+24 \pm 1.5$ VDC with a typical ripple of 1.8 volts peak-to-peak.
 - c. Measure the value of the voltage at TP2 (TP2 to TP3).
 - d. This voltage is -24 ± 1.5 VDC with a typical ripple of 1.8 volts peak-to-peak.
- 4. **+24 Volt Unregulated Magnet Heater Supply**
 - a. Measure the value of the voltage at TP8 (TP8 to TP6).
 - b. This value is $+25$ volts ± 1.5 VDC with a typical ripple of 1.2 volts peak-to-peak.
- 5. **+10.5 Volt Regulated Variable Temperature and Digital Circuitry Supply**
 - a. Measure the value of the voltage at TP7 (TP7 to TP6).
 - b. This voltage is 11.5 VDC $\pm 1.2V$ with a typical ripple of 15 millivolts peak-to-peak.

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SECTION 4.0
FIELD CONTROL PCB

4.1 FUNCTION

DC current from various front panel sources and controls and the recorder sweep potentiometer must flow through the magnet sweep coil in order to sweep the permanent magnet field to search for the NMR resonance.

This card receives those signals, appropriately sums, amplifies, and then uses the resultant current to drive the magnet PC sweep coil.

4.2 THEORY OF OPERATION

1. POWER SOURCES

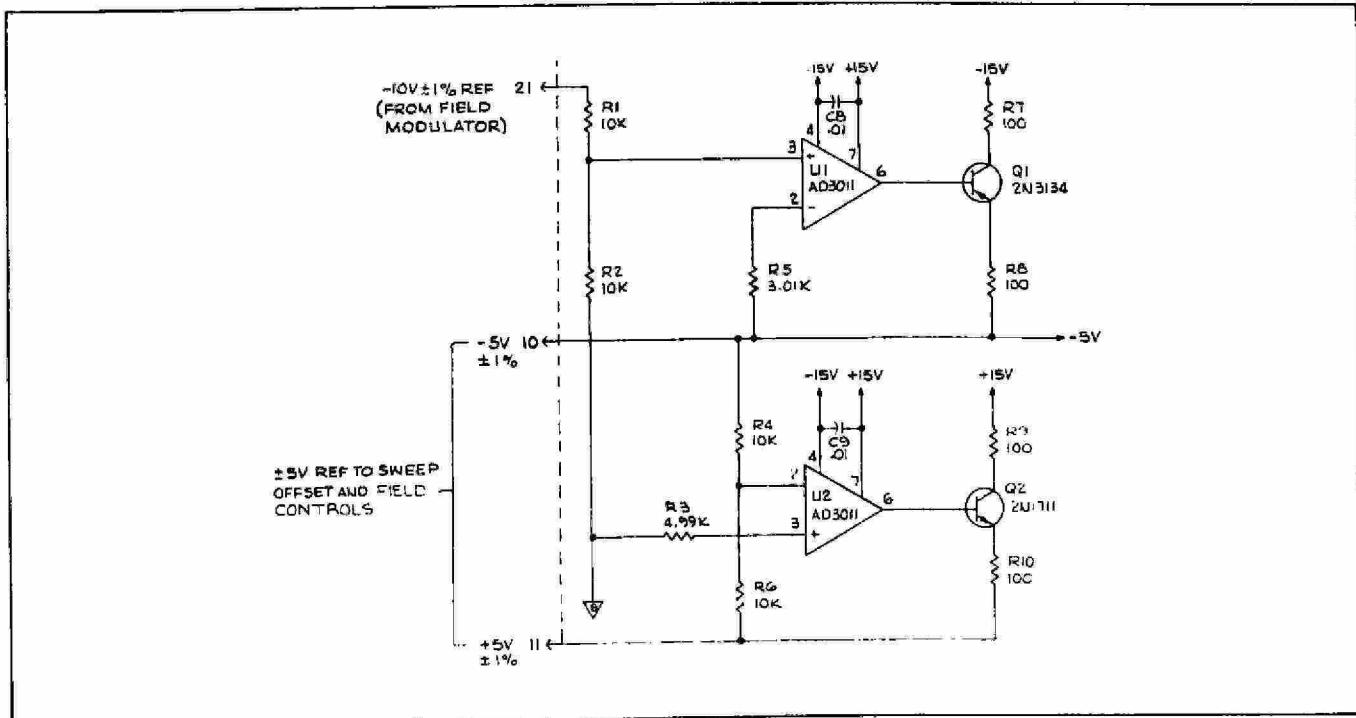


FIGURE 4-1. POWER SOURCES

The -10 volt precision voltage reference from the Field Modulator is applied to a voltage divider network R1 and R2 which applies a -5 volts to operational amplifier U1 non-inverting input. The output of U1 drives emitter follower Q1 whose emitter output is a highly regulated -5 volts to the Recorder Sweep Potentiometer and the SWEEP OFFSET and COARSE and FINE FIELD CONTROLS. The SWEEP OFFSET is the thumbwheel switch also called END OF SWEEP. This -5 volt output is applied to the inverting differential input of U1 to maintain the output at -5 volts.

A voltage divider network of R4 and R6 between -5 VDC and the +5 VDC places 0V into U2 inverting input. The output drives emitter follower Q2 until the output is exactly +5 volts. The non-inverting input of U2 is referenced to ground (0 volts).

2. SWEEP AND OFFSET CIRCUITS

A 3K 3 Turn potentiometer is driven with the X-Axis carriage of the recorder. The wiper of this potentiometer which varies from 0V to -5 volts as the recorder moves from chart zero to the left limit is connected to operational amplifier U3 non-inverting input. A trim potentiometer R15 sets the output to zero with zero input.

The output of U3 is applied to the voltage divider network of the SWEEP WIDTH control. A portion of U3 output is returned to buffer operational amplifier U4 non-inverting input. In the NORMAL (not INDOR) mode the output of U4 is applied to the inverting input of U7 through the contacts of K1 and Scan Calibration potentiometer R22.

The output of the thumbwheel END OF SWEEP switch between -5 VDC and +5 VDC is applied to U5 non-inverting input. The output is set to zero for zero volt input with R19. The output of U5 is applied to U7 inverting input with the sweep.

The combined sweep and offset are amplified in U7 and applied to the summing junction in the inverting input of U8 and to VCO TRACKING. Other inputs to this junction are the COARSE and FINE FIELD potentiometer wipers. Also applied is the lock correction signal from the Lock Channel PCB.

Operational amplifier U8 drives the output power amplifiers Q3 and Q4. The complementary emitter followers drives the sweep coil with R35 controlling the gain of DC amplifier U8, Q3, and Q4.

K1 energizes in the INDOR Mode which places the recorder sweep input to U6 which amplifies it and applies it to the decoupler to sweep its frequency through the same width as the SWEEP WIDTH selected. END OF SWEEP, COARSE and FINE FIELD, Tracking output, and Lock Correction inputs operate as before. The field no longer varies with the recorder sweep.

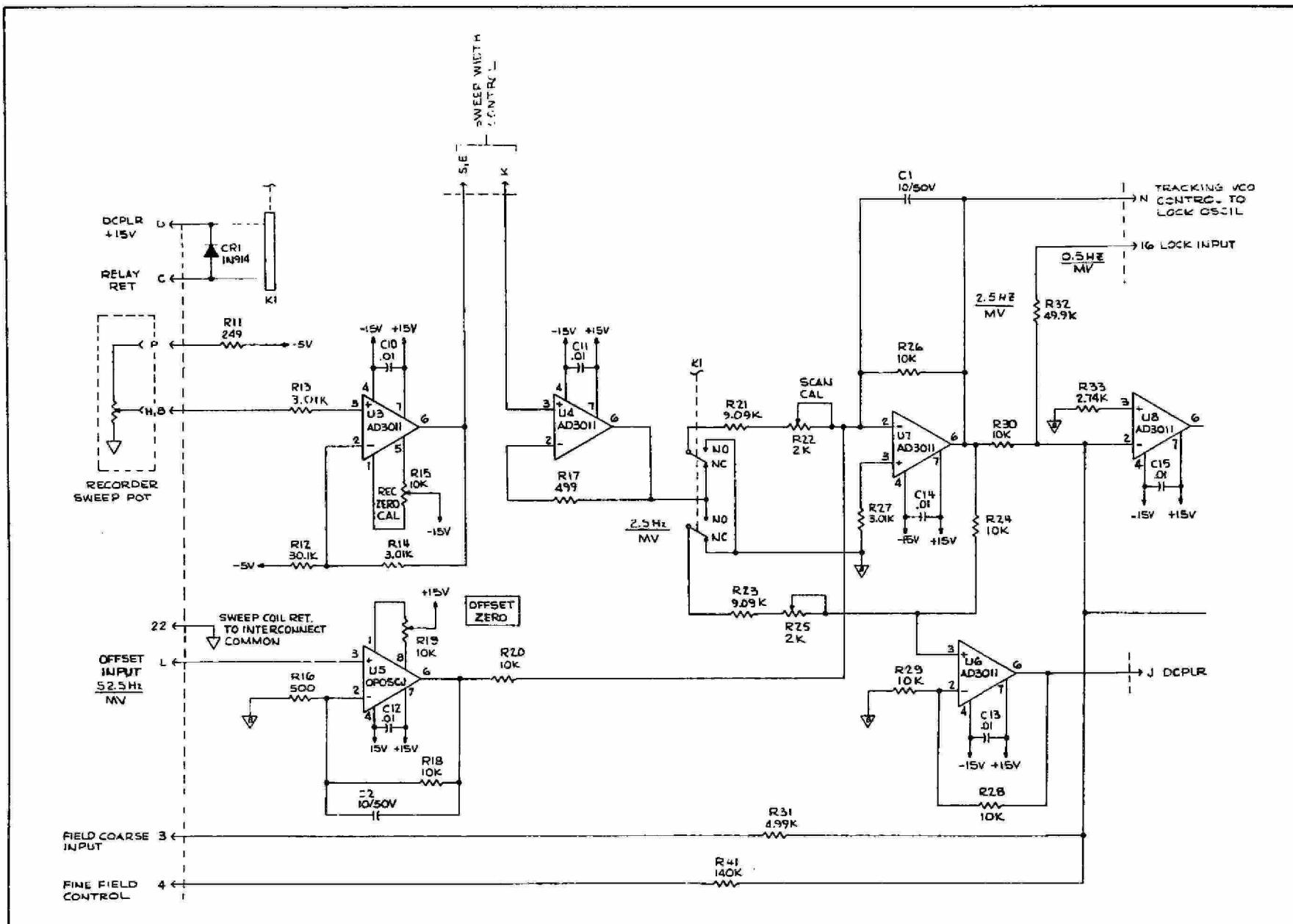


FIGURE 4-2. P/O FIELD CONTROLLER

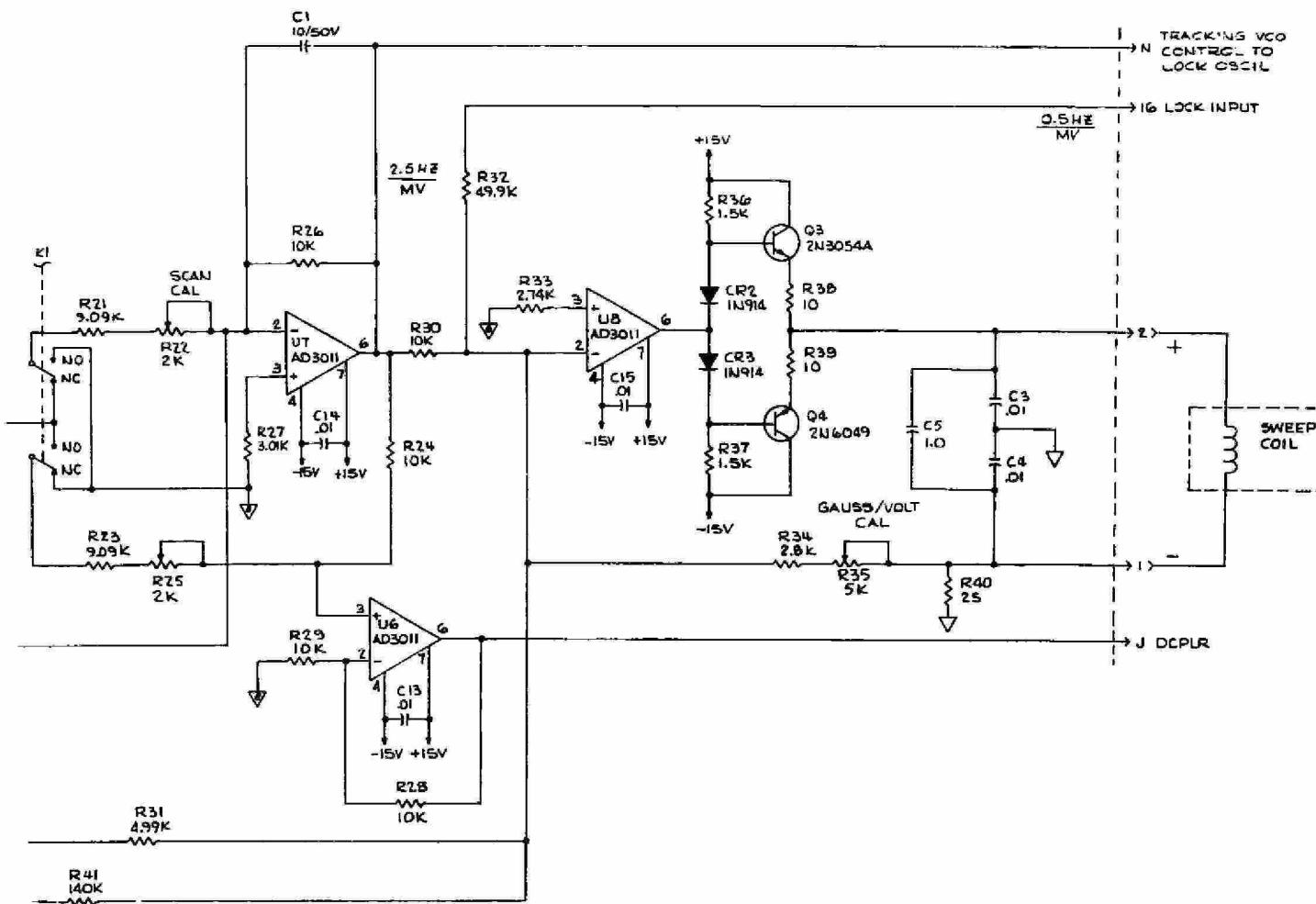


FIGURE 4-3. P/O FIELD CONTROLLER

4.3 ADJUSTMENTS AND CALIBRATIONS

1. POWER SOURCES

- a. Locate all components on Figure 4-4.

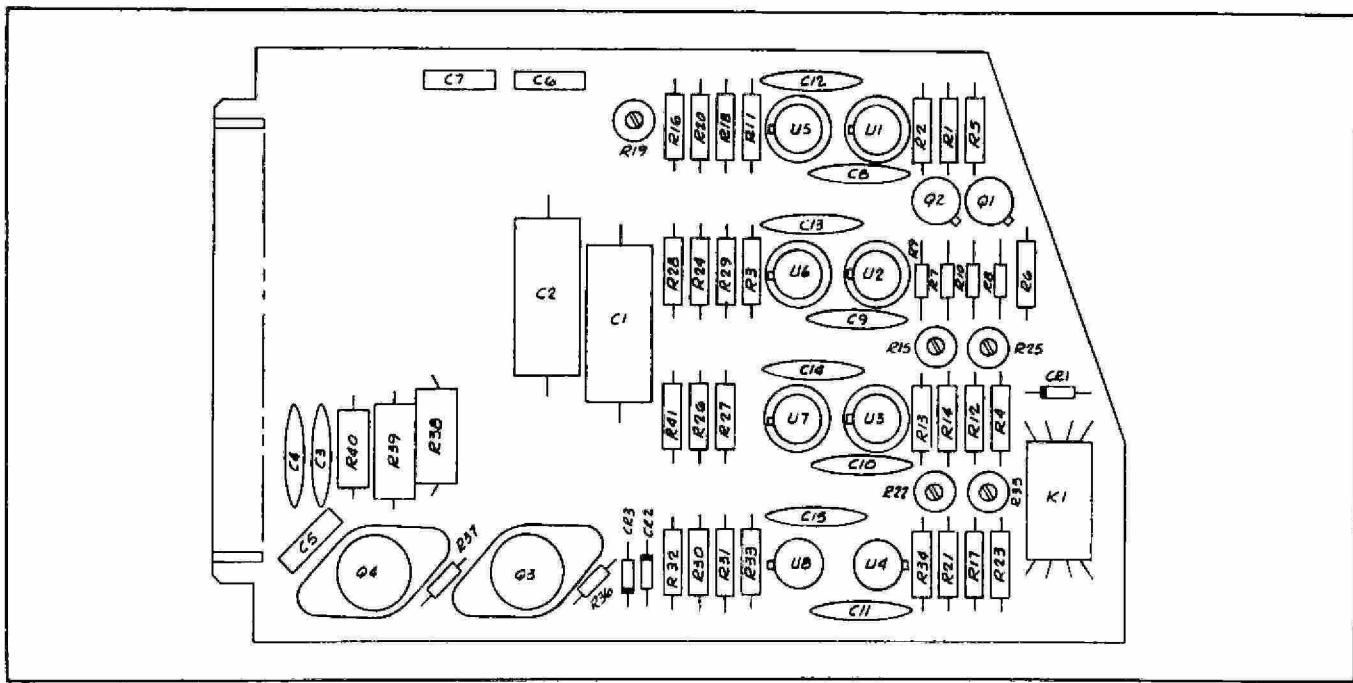


FIGURE 4-4. COMPONENT LAYOUT

- b. Measure and record the value of voltage at pin 21. It must be -10 ± 0.1 volts DC. The source of this voltage is the Field Modulator PCB.
- c. Measure and record the value of voltage at pin 10. It must be -5 ± 0.05 volts DC. The source of this voltage is U1.
- d. Measure and record the value of voltage at pin 11. It must be $+5 \pm 0.05$ volts DC. The source of this voltage is U2.
- e. Measure and record the value of voltage at pins W,19. It must be -15 ± 0.4 V from the Power Supply.
- f. Measure and record the value of voltage at pins X,20. It must be $+15 \pm 0.1$ V from the Power Supply.

2. SWEEP AND OFFSET CALIBRATION

The order of the following adjustments is critical. If any adjustment is made, the remaining steps must be accomplished.

a. OFFSET ZERO

- 1) Set the thumbwheel END OF SWEEP control to zero.**
- 2) Adjust R19 for zero volts measured at pin 6 of U5 (junction R18 and R20).**
- 3) Normal range is +0.065 to -0.055V DC.**

b. RECORDER ZERO

- 1) Position the paper at the "hash mark" and the pen directly over zero (pen down on the paper) on the right hand side of the chart.**
- 2) Center R15 in its range.**
- 3) Adjust the pulley on the X-Axis slidewire potentiometer for zero volts \pm 0.01 volt DC at pin 6 of U3 (junction R14 and pin 5 of the PCB).
 - a) Hold the pen stationary over chart zero during this adjustment.**
 - b) Tighten the pulley and ensure the pulley does not drag on the frame after tightening.****
- 4) Readjust R15 for 0 volts \pm 0.01 volt at pin 6 of U3 (junction R14 and PCB pin 5).**

c. SWEEP WIDTH

- 1) Set the thumbwheel END OF SWEEP control to -0.000.**
- 2) Select SWEEP WIDTH of 20 PPM.**
- 3) Accurately position the recorder pen at zero on the chart.**
- 4) Measure the voltage at pin 6 of U7 (junction C1, R26, R30, and R24).**

- 5) It should be about zero but a slight offset is unimportant.
- 6) Move the recorder pen to 20 PPM (Start of Sweep Line) on the chart paper.
- 7) Move the END OF SWEEP thumbwheel to -20 PPM.
- 8) Measure the voltage at pin 6 of U7 (junction C1, R26, R24, and R30).
- 9) Adjust R22 until the voltage is the same within 0.5 millivolts at chart left (20 PPM) as it was at chart right (0).
- 10) An iterative process is necessary to make this adjustment.

d. DECOUPLER SWEEP WIDTH

- 1) Set the thumbwheel END OF SWEEP switch to +000.0 PPM.
- 2) Set SWEEP WIDTH to 20 PPM.
- 3) Select INDOR operation of the Spin Decoupler module.
- 4) Accurately position the recorder pen at chart zero.
- 5) Measure and record the voltage at pin 6 of U6 (junction R28 and pin J of the card).
- 6) Set END OF SWEEP to +20 PPM.
- 7) Move recorder arm to the 20 PPM position (start of sweep).
- 8) Adjust R25 so that the voltage at 20 PPM is the same as at 0 PPM within 0.5 millivolt.
- 9) Repeat the process as necessary to make this adjustment.
- 10) Turn the Spin Decoupler OFF.

e. LOCK VCO

- 1) Set END OF SWEEP thumbwheel switch to -0.000 PPM.

- 2) Accurately position the recorder pen at 0.
- 3) Monitor TP2 on the Field Modulator card with a high resolution frequency counter and record the frequency.
- 4) Set END OF SWEEP thumbwheel switch to -20.0 PPM.
- 5) Measure the frequency at TP2 of the Field Modulator for a frequency shift of $+1800 \pm 2$ Hz.
- 6) If the frequency change is other than $+1800 \pm 2$ Hz, adjust R127 on the Field Modulator (in oven closest to the edge) until it is within tolerance.
- 7) Repeat the process until no further adjustment is required.
- 8) Set the END OF SWEEP thumbwheel switch to +000.0.
- 9) Measure and record the frequency at TP2 of the Field Modulator.
- 10) Set the END OF SWEEP thumbwheel switch to +20.0 PPM.
- 11) Measure the frequency at TP2 of the Field Modulator for a frequency shift of -1800 ± 4 Hz.
- 12) Repeat this entire step (e) if the frequency shift is outside tolerance.
- 13) Set END OF SWEEP thumbwheel switch to +000.0.
- 14) Select 19 F (if installed) by depressing OTHER NUCLEI Switch.
- 15) Measure and record the frequency at TP2 of the Field Modulator PCB.
- 16) Set END OF SWEEP thumbwheel switch to +20 PPM.
- 17) Measure and record the frequency at TP2 of the Field Modulator PCB for a difference frequency of $+1694 \pm 2$ Hz.
- 18) Adjust R129 in the Field Modulator oven (next to R127) until this condition is met.
- 19) Repeat steps 13) through 19) as often as required.

20) Return to NORMAL (proton) operation.

f. DECOUPLER VCO

- 1) Set END OF SWEEP thumbwheel switch to -0.000 PPM.
- 2) Turn the Spin Decoupler to DECOUPLE Mode.
- 3) Accurately position the pen at 0.
- 4) Monitor J1103 on the Spin Decoupler rear panel and record the frequency using a high resolution frequency counter.
- 5) Set END OF SWEEP thumbwheel switch to -20.0 PPM.
- 6) Measure the frequency from J1103 for a frequency shift of $+1800 \pm 8$ Hz.
- 7) If the frequency shift is other than $+1800 \pm 8$ Hz, adjust R17 in the Spin Decoupler until this condition is met.
- 8) Repeat the process until no further adjustment is required.
- 9) Set END OF SWEEP thumbwheel switch to +000.0.
- 10) Select 19F (if installed) by depressing OTHER NUCLEI Switch.
- 11) Measure and record the frequency from J1103 of the Spin Decoupler.
- 12) Set END OF SWEEP thumbwheel switch to +20 PPM.
- 13) Measure and record the frequency from J1103 for a frequency difference of $+1694 \pm 10$ Hz.
- 14) Adjust R19 in the Spin Decoupler oven until this condition is met.
- 15) Repeat steps 9) through 15) as often as required.
- 16) Return to NORMAL (proton) operation.
- 17) Turn Spin Decoupler OFF.

g. FIELD CALIBRATION

1) Procedure A

- a) Set the spectrometer to observe a methanol line in the unlocked mode.
- b) Adjust **LOCK POWER**, **LOCK FREQUENCY**, and **LOCK GAIN** for a stable reading in the **LOCK METER** position.
- c) Shift the **END OF SWEEP** thumbwheel switch slowly through 20 PPM.
- d) Move the **FINE FREQUENCY** control to re-establish resonance when it is lost. Each division of the **FINE FREQUENCY** control is about 1 Hz.
- e) Adjust R35 so the lock channel remains on the resonance within 4 Hz in 20 PPM.

2) Procedure B (alternate)

- a) Place the recorder arm on chart zero and find the methanol resonance.
- b) Set **SWEEP WIDTH** to 20 PPM.
- c) Adjust **LOCK FREQUENCY**, **LOCK POWER** and **LOCK GAIN** for a stable indication in the **LOCK METER**.
- d) Slowly move the recorder arm to the left and adjust the **FINE FIELD** control to maintain resonance.
- e) Adjust R35 slightly and repeat these steps noting whether more or less correction of the **FINE FIELD** is required.
 - 1)) If less, continue adjusting R35 in this direction until no **FINE FIELD** correction is required.
 - 2)) If more, reverse the direction of adjustment of R35.
- f) Continue until less than 0.05 PPM change is required in 20 PPM.

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SECTION 5.0
FIELD MODULATOR/WIDE SWEEP ACCESSORY

5.1 FUNCTION

This PCB contains four principal functions:

1. A crystal controlled 25 KHz oscillator and a phase shifter chain providing the reference signal for the observe phase detector.
2. A temperature stabilized VCO tracking the recorder and field sweep with a stable voltage source supplying the front panel LOCK FREQUENCY potentiometers and a phase shifter chain providing the reference signals for the Lock Phase detectors.
3. A power amplifier section which drives the field modulation coils with a 25 KHz signal for observe and a 20 KHz to 30 KHz signal for lock.
4. A frequency-to-voltage converter to translate spinner speed to a front panel meter indication.

5.2 THEORY OF OPERATION

1. OBSERVE MODULATION

A temperature-stabilized crystal-controlled oscillator stage U1 generates 25 KHz for use as the observe modulation signal. The frequency is determined by Y1 with degenerative feedback through RT2, a negative temperature coefficient thermistor, stabilizing the output amplitude. This Wienbridge type circuit is used for its extreme spectral purity, stable frequency, and precise amplitude levels. The oscillator components are located in an oven for added frequency stability.

The output of the oscillator is through E1 and E3 to the modulation level and modulation phase control circuits. The modulation level input is through a voltage divider network with the maximum level set by R6. This is modified by the OBSERVE POWER

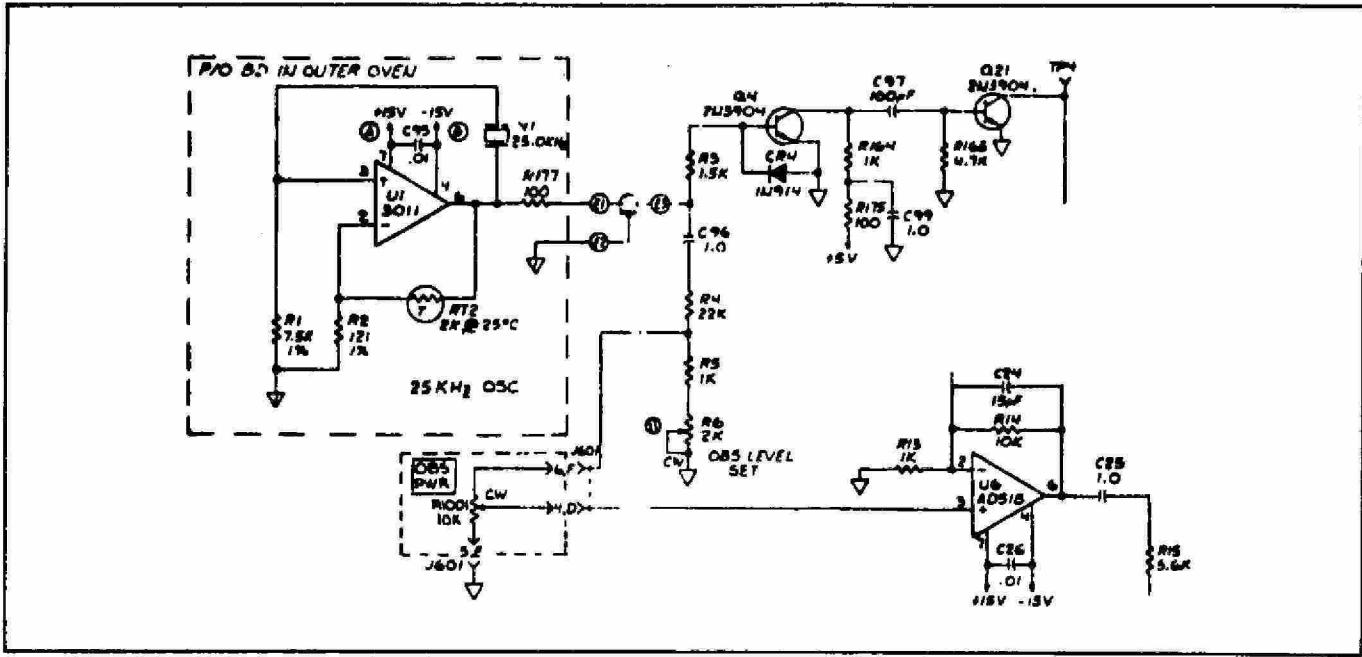


FIGURE 5-1. OBSERVE MODULATION GENERATION

potentiometer on the front panel and the modulation is applied through buffer amplifier U6 to the modulation power amplifier summing junction. The other output path from the oscillator output at E3 is to squaring amplifier Q4. On the negative excursion of the 25 KHz, the signal is limited to -0.6 volts peak by CR4. The positive signal excursion is limited to +0.6 volts peak by the base-emitter junction of Q4. A short RC circuit in Q4 collector differentiates the squarewave produced in Q4 producing alternate positive and negative spikes to Q21. Q21 conducts on the positive spikes producing a train of negative pulses at TP4 to the phase control circuits.

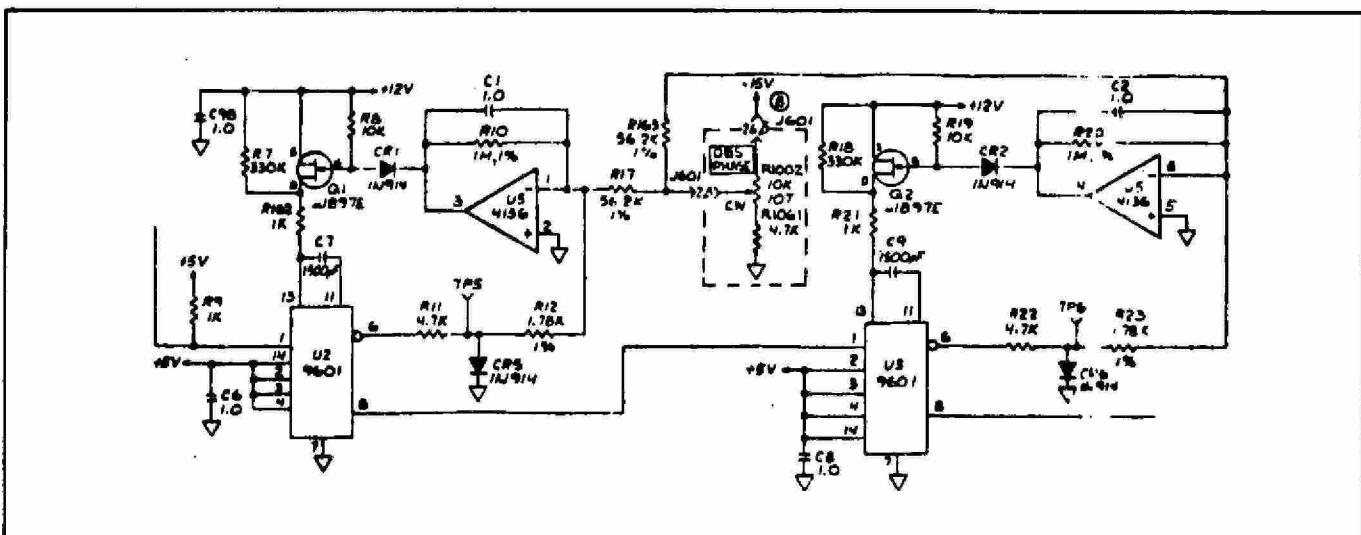


FIGURE 5-2. OBSERVE PHASE CONTROL

The negative pulses generated in Q21 trigger the resettable monostable multivibrator U2 on the leading edge of the negative pulse. The amount of time that U2 is "set" is determined by the RC network between pins 11 and 13 of the clip. Part of this RC is the impedance of the FET Q1. This impedance is proportional to the negative gate-source bias. At 0 volts bias (+12 volts on source and +12 volts on gate) the impedance is 47 ohms. At full cut-off (+12 volts on source and 0 volts on gate) the impedance is very high.

A front panel mounted 10 Turn potentiometer R1002 OBSERVE PHASE applies a negative voltage to the inverting input of U5A. This produces a positive voltage between 0 and +12 volts to the gate of Q1 to set the bias and hence the impedance in the RC network of U2. The Q-bar output of pin 8 of U2 is a positive pulse whose duration depends upon the setting of the OBSERVE PHASE control. The trailing or negative-going edge of this pulse triggers U3.

The RC time between pins 11 and 13 of U3 again determines the time of operation of U3. Part of this RC is the variable impedance of FET Q2. This impedance again is set by the value of the negative voltage from the OBSERVE PHASE inverted in U5B to the gate of Q2. The output of U3 is the positive pulse from the Q-bar output pin 8. The duration of this pulse plus the duration of the pulse from U2 is the total delay or phase shift. This range in phase shift as the OBSERVE PHASE is rotated from stop to stop is about 558°. The output of U3 is normally unbalanced and is next applied to the Observe Phase Reference Balance circuits.

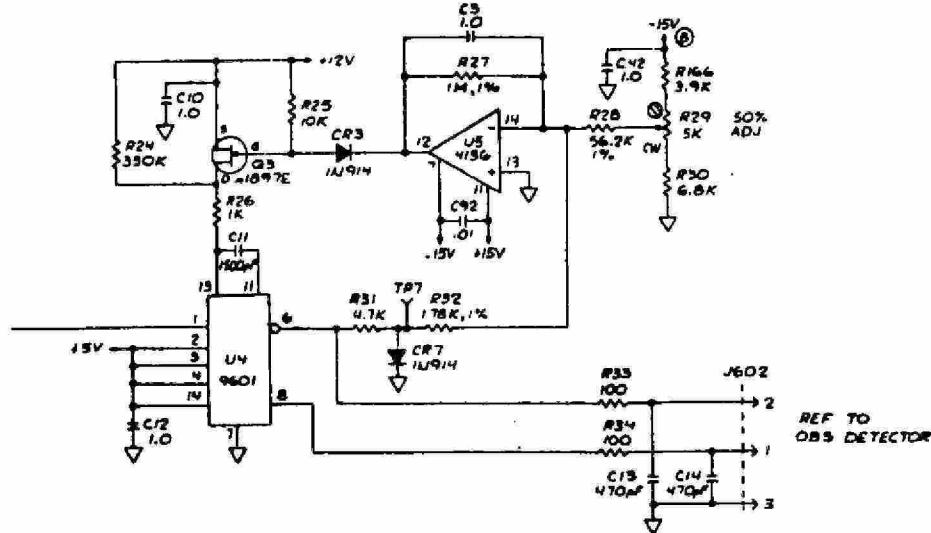


FIGURE 5-3. OBSERVE PHASE BALANCE

Retriggerable monostable multivibrator U4 is toggled on the trailing edge of the unbalanced rectangular waveform from U3. The RC time of the circuits between pins 11 and 13 determine the "on" time of the device. The impedance of the FET in this RC is set by the negative voltage level from the 50% ADJ control through U5D inverting operational amplifier. R29 50% ADJ is adjusted to produce an "on" time of 20 microseconds and an 'off' time also of 20 microseconds.

The Q output is output through pin 2 of J602 and the Q-bar output is applied to pin 1 of J602. The complementary outputs are used as the reference for the observe signal phase detection in the Observe Channel PCB.

2. LOCK MODULATION SIGNAL

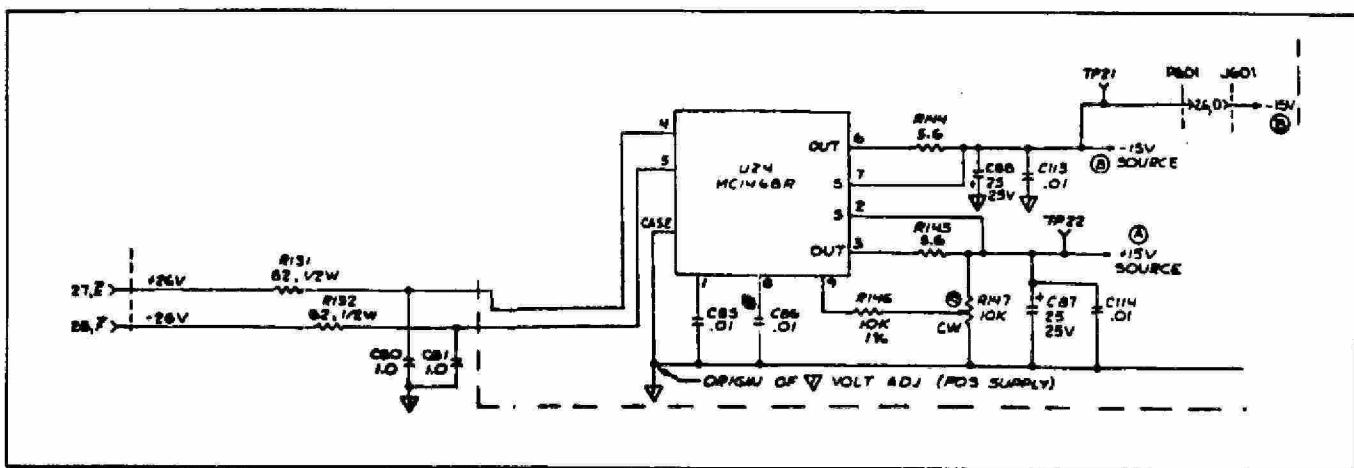


FIGURE 5-4. \pm 15 VOLT REGULATOR

The stability of the lock modulation is critical but it can be no better than the stability of the voltage sources. The stability of the various voltage regulator circuits is improved by placing the regulators in the temperature controlled oven.

The ± 24 Volt System Unregulated supply is applied to an integrated circuit voltage regulator U24, an MC1468R. The exact value of the regulated $+15$ volt output is set by R147. Since the $+15$ volt output is the reference for the -15 volt regulation, the adjustment of R147 actually sets both regulated outputs. The positive output is used only on the Field Modulator PCB but the -15 volts is used to drive various front panel controls as well as the electronics of this PCB.

U26 is the precision -10 volt regulator and is illustrated on Figure 5-5. The -15 volt regulated supply is applied to the base and collector of Q18. The input from U26 causes -10 volts to be present on the emitter of Q18. The -10 volts is applied to zener diode CR25 which produces a -8.8 volt reference. This is divided by voltage divider R139 and

R138 to produce -2.19 volts at the non-inverting input of U26. The -10 volt regulated is applied to a voltage divider network of R135, R136, and potentiometer R137 to apply between -1.84 volts to -2.38 volts on the inverting input of U26 depending upon the setting of R137. This potentiometer is set to provide exactly -10 volts from the circuit. A level shift zener diode CR24 (6.8 volt) places the output of U26 into the operating range of Q18.

The -10 volts is applied to the inverting input of operational amplifier U12 which has a gain of -1.27. The amplifier then has about +12.7 volts in its output to drive emitter follower Q11. The output of Q11 is the regulated +12 volts.

The -10 volts (TP19) is also applied to the two frequency-offset resistors R122 and R123 - only one of which will be in the circuit. On NORMAL (1H) the resistor R122 is used. For OTHER NUCLEI mode, the relay K2 is energized and R123 is used. For 19F, the value of R123 is the same as the proton path R122 but the value of R123 may change with future nuclei accessories. The current produced in this frequency-offset circuit is applied to the summing junction of U13.

The -10 VDC from TP19 is also applied through J601-24,b to the Field Control PCB as a precision voltage source.

The -10 VDC from TP19 is also applied through J601-23,a to the LOCK FREQUENCY COARSE and LOCK FREQUENCY FINE control potentiometers on the front panel. The outputs of the wipers of these two controls are applied to the summing junction of U13 through scaling resistors R124 and R125. Note that the effect of the COARSE control is about 136 times that of the FINE control due to the respective values of the scaling resistors.

Still another input to the summing junction in the inverting input of U13 is the VCO TRACKING from the Field Control. This DC signal is the summation of END OF SWEEP Offset and Recorder Sweep data. This signal is applied through one of two possible paths. For NORMAL or 1H the path is as shown through R127 and R126. For OTHER NUCLEI the path is through R129 and R128. R127 is adjusted in the TRACKING adjustment for protons and R129 is adjusted in the OTHER NUCLEI TRACKING adjustment of Section 4.0.

The total signal into U13 is the summation of VCO TRACKING, LOCK COARSE and FINE FREQUENCY control, and fixed offset. This combined signal is amplified in U13 and may be measured at TP18 as VCO CONTROL. The output of U13 is applied to the VCO and to the frequency compensation circuits.

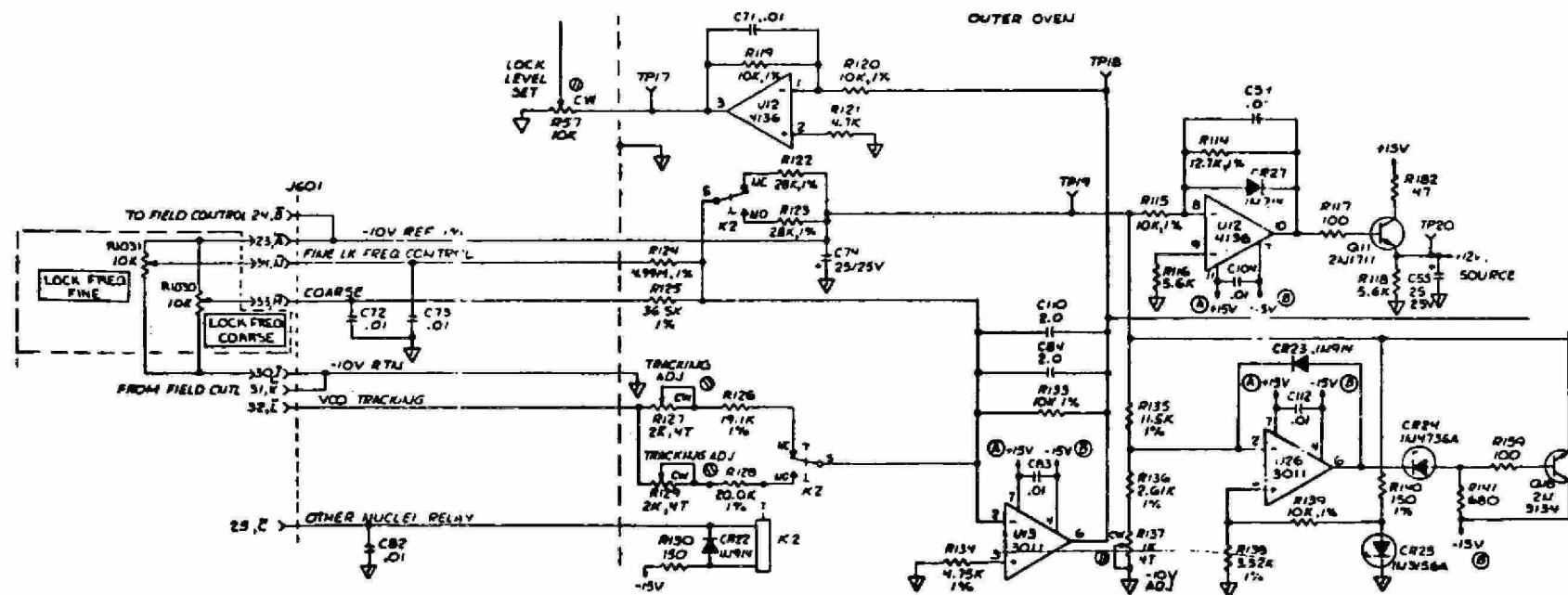


FIGURE 5-5. LOCK MODULATION INPUTS

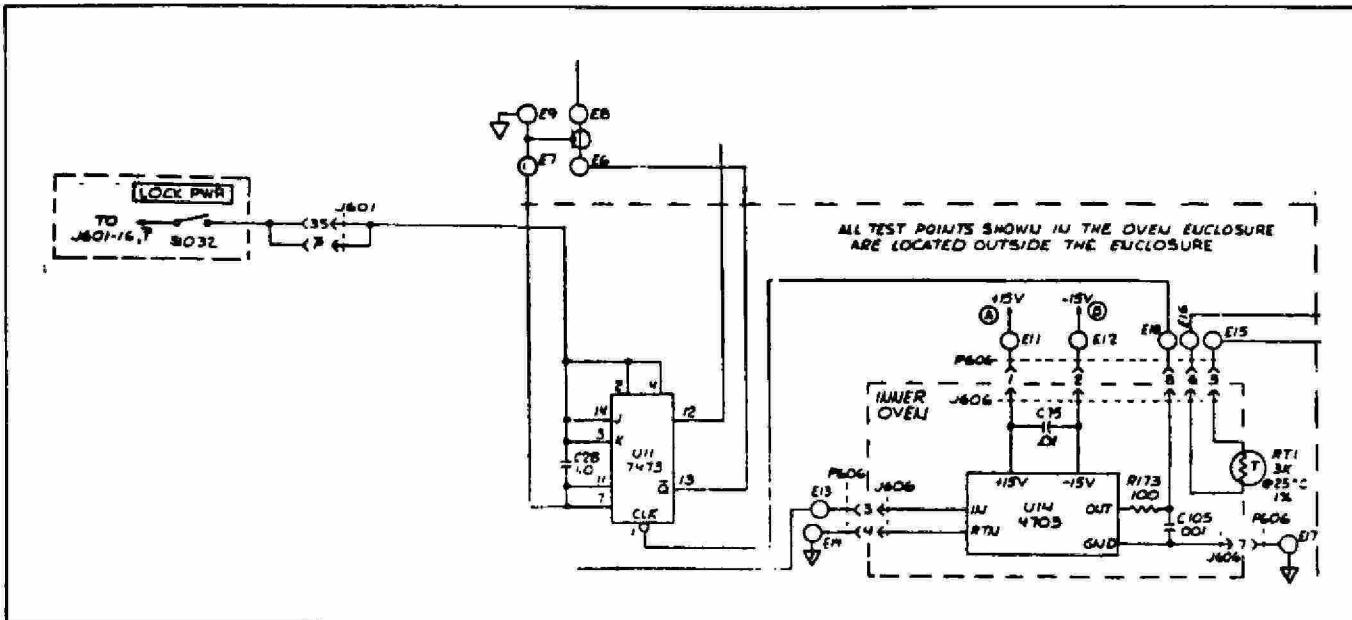


FIGURE 5-6. VCO CIRCUIT

The VCO Control voltage from U13 is applied to the VCO U14 to select one frequency from its range of 40 KHz to 60 KHz. For added stability, the VCO is in an inner oven. The total temperature control is also sensed at this point with RT1, a negative temperature coefficient thermistor. The output of U14 is divided-by-two in U11. The Q output of U11 is applied to the Lock Modulation Reference phase control and will be discussed later. The Q-bar output of U11 is applied through E6 and E8 to produce the lock modulation signal.

When the LOCK POWER control is turned fully counterclockwise, S1032 opens removing +5 volts from U11 which kills the 20-30 KHz lock signal. This is equivalent to turning the lock off completely.

The DC VCO CONTROL signal from U13 is present at TP18 as a positive DC level. This is buffered and inverted in U12A to a negative DC level at TP17. This is applied to a screwdriver adjustment R57 which sets the Lock Level maximum to U8 inverting input.

The circuit of U8, emitter-follower Q9, and switching transistor Q10 make up a saw-tooth or triangular wave generator. RC circuits in the feedback round the corners of this waveform until it resembles a sinusoid. The DC level amplified and inverted in U8 produces a sawtooth in the emitter of Q9 which is applied back to the non-inverting input of U8. The slope of the sawtooth depends upon the voltage level into U8. The higher the voltage level, the faster the ramp increases and the higher the level that will be attained. The sawtooth will increase in amplitude until the 20 KHz to 30 KHz signal from U11 to the base of Q10 goes positive dropping the emitter voltage of Q9 to ground. The ramp then

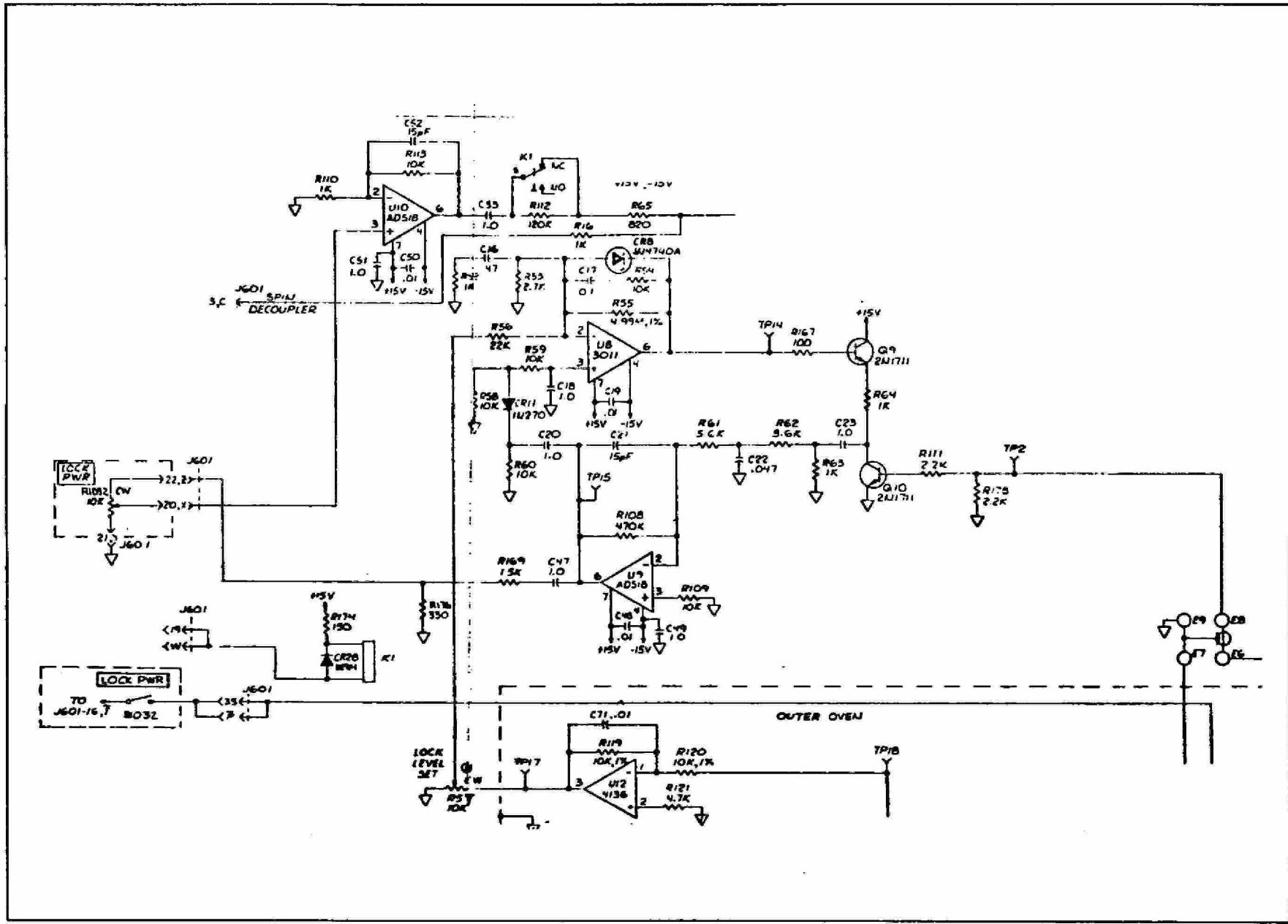


FIGURE 5-7. LOCK MODULATION

discharges toward zero until the negative portion of the 20 KHz to 30 KHz signal cuts off Q10 when the ramp starts positive again. The frequency of the ramp then is the same as the divided VCO output of 20 KHz to 30 KHz. The amplitude is determined by the level of the VCO control voltage which is also proportional to the VCO frequency. Therefore we can say that the amplitude of the sawtooth is also proportional to frequency in that with a change of frequency from 20 KHz to 30 KHz, the amplitude will increase by a factor of 1.5.

This pseudo-sinusoid is amplified and inverted in U9 and applied to the LOCK POWER control potentiometer. A portion of the signal is applied to the non-inverting input of the buffer amplifier U10. The output of U10 is applied through C53, R112, and R65 to the input of the modulation power amplifier.

Note that the spin decoupler input is also applied to the summing junction of the modulation power amplifier.

Relay K1 increases the amplitude of the lock signal about 150 times for use as a spin decoupler signal if required. At this time the relay K1 is not currently used and there is no provision for future use of this feature.

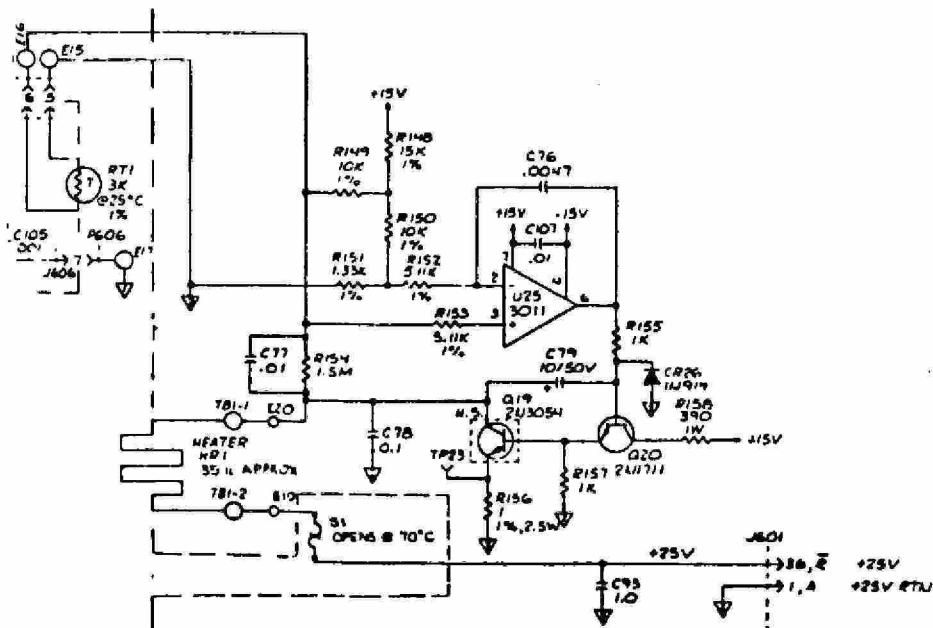


FIGURE 5-8. OVEN TEMPERATURE CONTROL

The lock signal is only as stable as the constant temperature of the VCO. Therefore, the thermal insulation integrity and temperature regulation must be maintained to a high degree of accuracy for repeatable results of the system.

A negative temperature coefficient thermistor RT1 is located in the inner oven with the VCO. This sensor is in a bridge circuit on the input to U25. Any imbalance in the bridge is amplified and controls the current flow through Q20, the pass-gate driver. This controls the current flow through the pass-gate Q19 which is in series with the heater. The circuit must stabilize between 43°C and 48°C and regulate at the point of stabilization within 0.1°C.

A thermal switch S1 in series with the heater opens if the temperature should reach 70°C. This switch is not resettable. The switch is of the fuseable link type and must be replaced should it ever open.

There are two types of Field Modulator circuit boards currently in use. The first type we shall discuss was used in systems below serial 147 without the 19F Accessory. This is the simplest type and we shall examine it to more fully understand the function of the second type; that is, all units serial 147 and higher and earlier units with the 19F Accessory. The second type was required to compensate for phase changes in the lock signal for SWEEP WIDTHS greater than 10 PPM which are normal in 19F spectra.

Figure 5-9 shows the Lock Reference Phase Control circuits. The 20 KHz to 30 KHz square wave from U11 is applied to the base of Q22 where it is inverted and applied to U15, a retriggerable monostable multivibrator. U15 "sets" on the negative going (+5V to 0V) waveform of the input and remains "set" for a time determined by the RC network between pins 11 and 13 of the IC. Part of this RC is the impedance of FET Q12 whose impedance value is proportional to the voltage on its gate. This voltage is set by the front panel control LOCK PHASE which applies a negative voltage to the inverting input of U20A which in turn drives Q12.

The Q-bar output then is a variable width positive pulse which triggers U16, another re-triggerable monostable multivibrator, on the negative going trailing edge. The pulse from the Q-bar output of U16 again has a width depending on the voltage from the LOCK PHASE front panel control inverted in U20D and applied to FET Q13 to vary the impedance between pins 11 and 13 of U16. The trailing edge of this output pulse may be delayed as much as 558° from the input at TP13.

The positive portion of the rectangular waveform from U16 operates U17 on the negative going trailing edge. A negative voltage from R87 50% ADJ sets the duty cycle of the monostable multivibrator U17 to 50 percent "on", 50 percent "off". This is accomplished

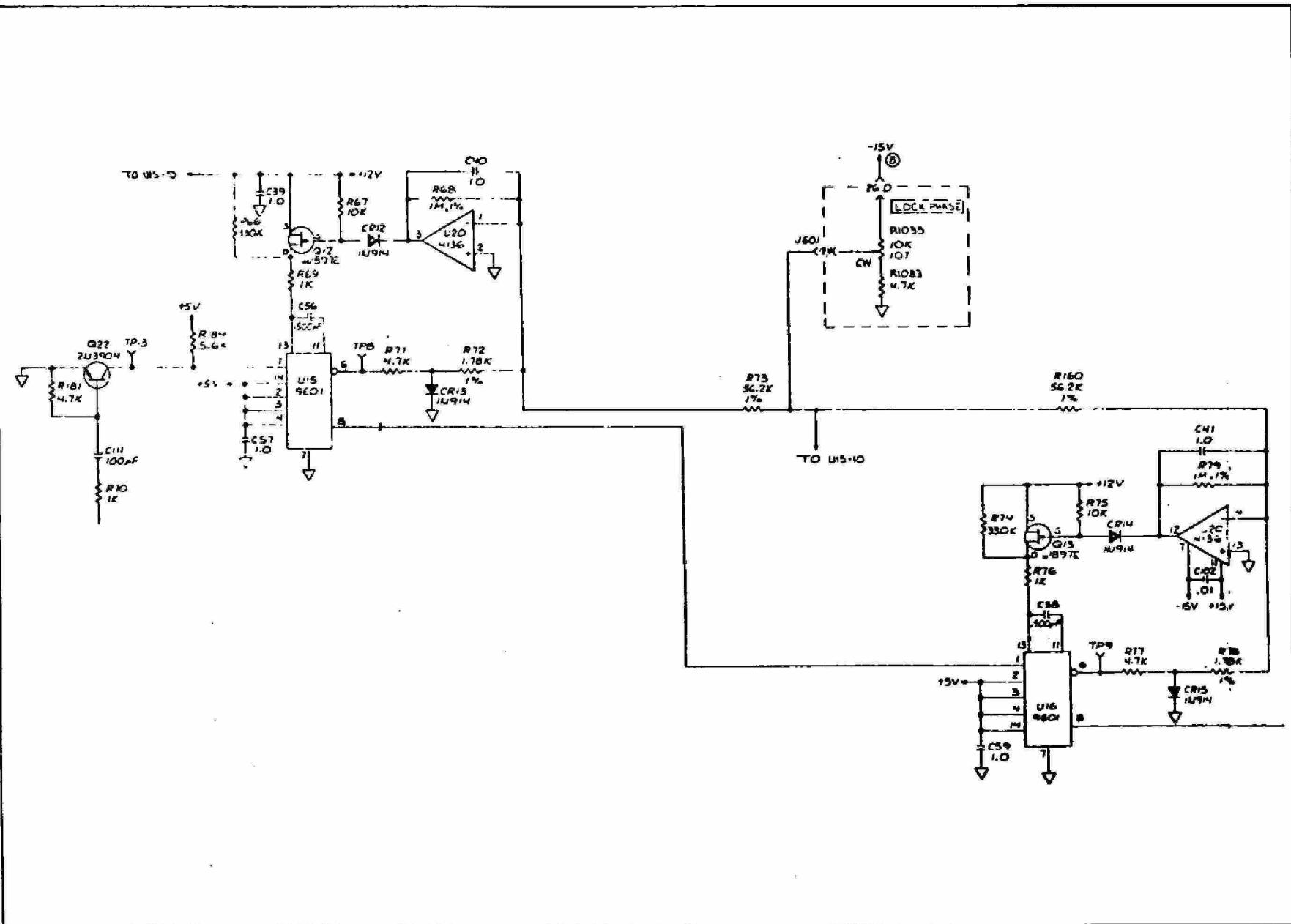


FIGURE 5-9. LOCK REFERENCE PHASE CONTROL

by applying the negative voltage from R87 through the inverting input of U21B to the gate of FET Q14 which in turn varies the RC between pins 11 and 13 of U17 to make the output pulse conform to a balance condition. This output is taken as Q and Q-bar to J604 pins 5 and 4 and the Q-bar output is also applied to U18.

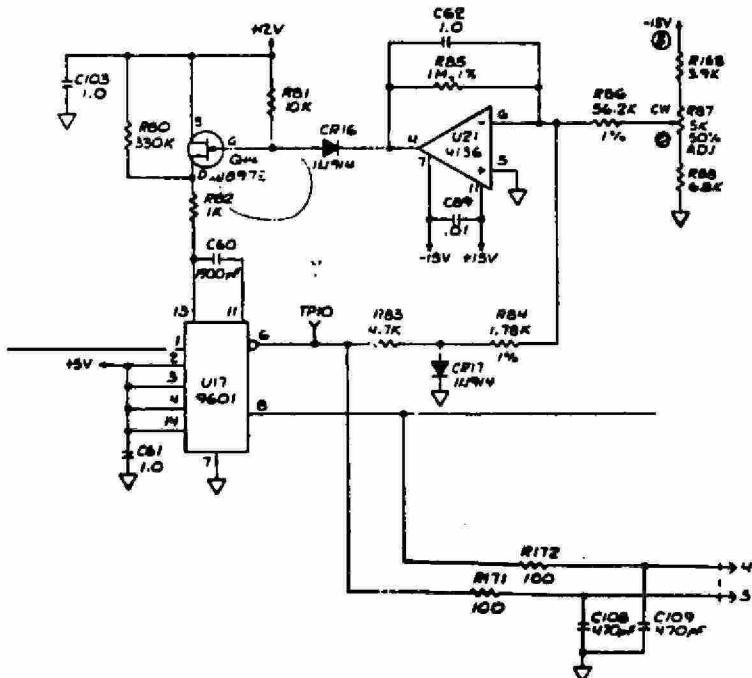


FIGURE 5-10. 0° REFERENCE BALANCE

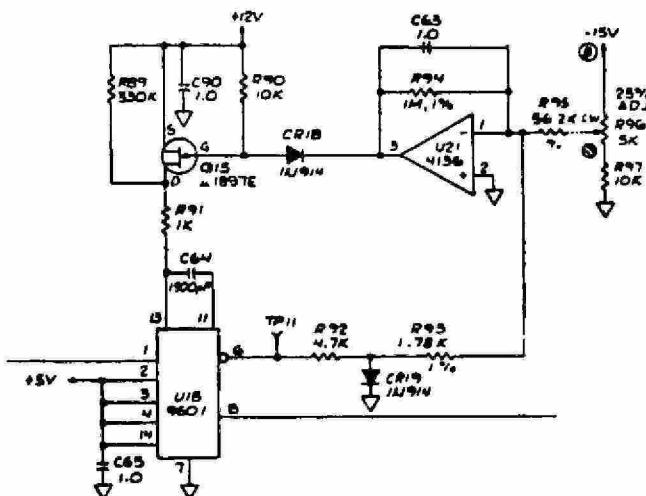


FIGURE 5-11. 90° PHASE SHIFT

The balanced input from U17 Q-bar output triggers the monostable multivibrator U18 on the input negative-going trailing edge. The time of operation is set by R96 25% ADJ such that the output of Q-bar is high 25 percent of the time and low for 75 percent of the time. This is accomplished by setting the level of negative voltage from R96 through the inverting input of U21A to the gate of FET Q15 which sets the impedance of the RC between pins 11 and 13 of U18 to the appropriate point. The Q-bar output of U18 is made to the 90° Lock Reference Balance circuit.

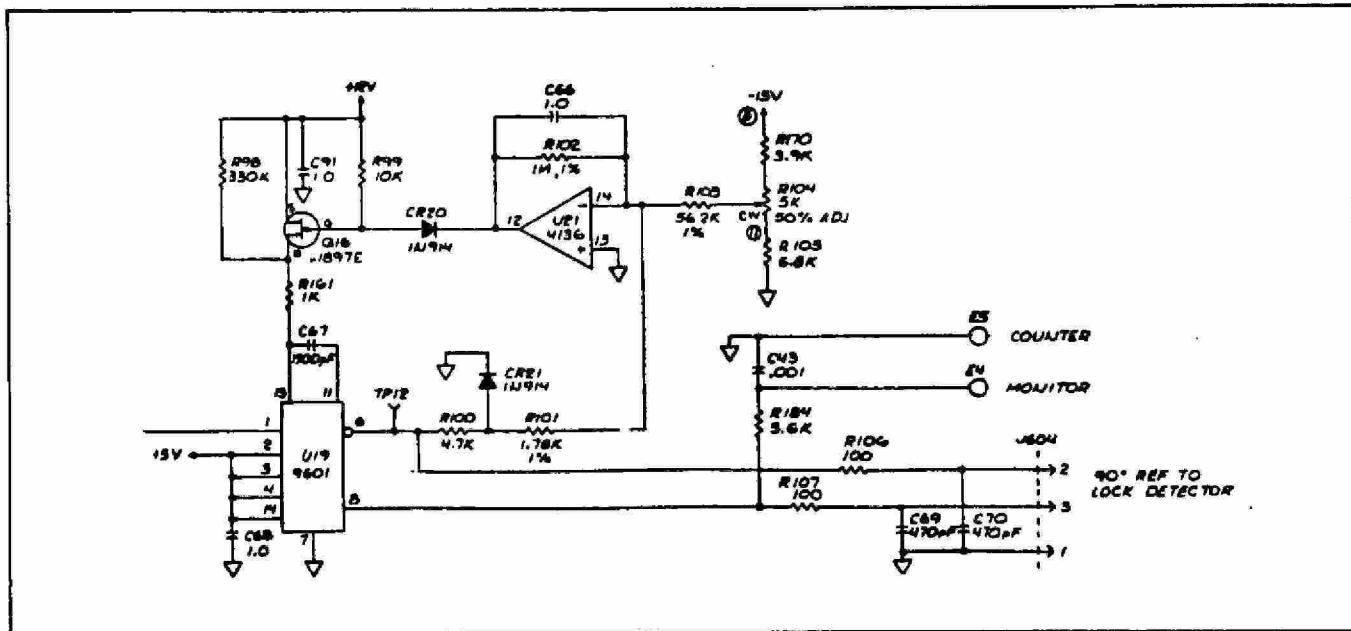


FIGURE 5-12. 90° LOCK BALANCE

The monostable multivibrator U19 again requires a negative going trailing edge of the positive 25% duty cycle pulse to trigger. The amount of "on" time compared to the total period of the output is set by R104 50% ADJ to the balanced square-wave point. This is accomplished by the amount of negative voltage from R104 inverted in U21D to a positive level on the gate of Q16 which determines the impedance between pins 11 and 13 of U19. The balanced complementary square-waves from the Q and Q-bar outputs of U19 are applied through J604 pins 2 and 3 to the 90° Lock Reference to the Lock Channel Phase Detector. Testpoints at E5 and E4 enable monitoring of the output frequency and voltage levels.

This completes the circuit description of the first type of Lock Reference used in the EM-390. With the addition of the Wide Sweep Accessory to the card the following description applies. Although some of the circuits remain in the same configuration, the IC designations change in some instances. The Wide Sweep Accessory replaces IC's U15 and U20 of the previous discussion.

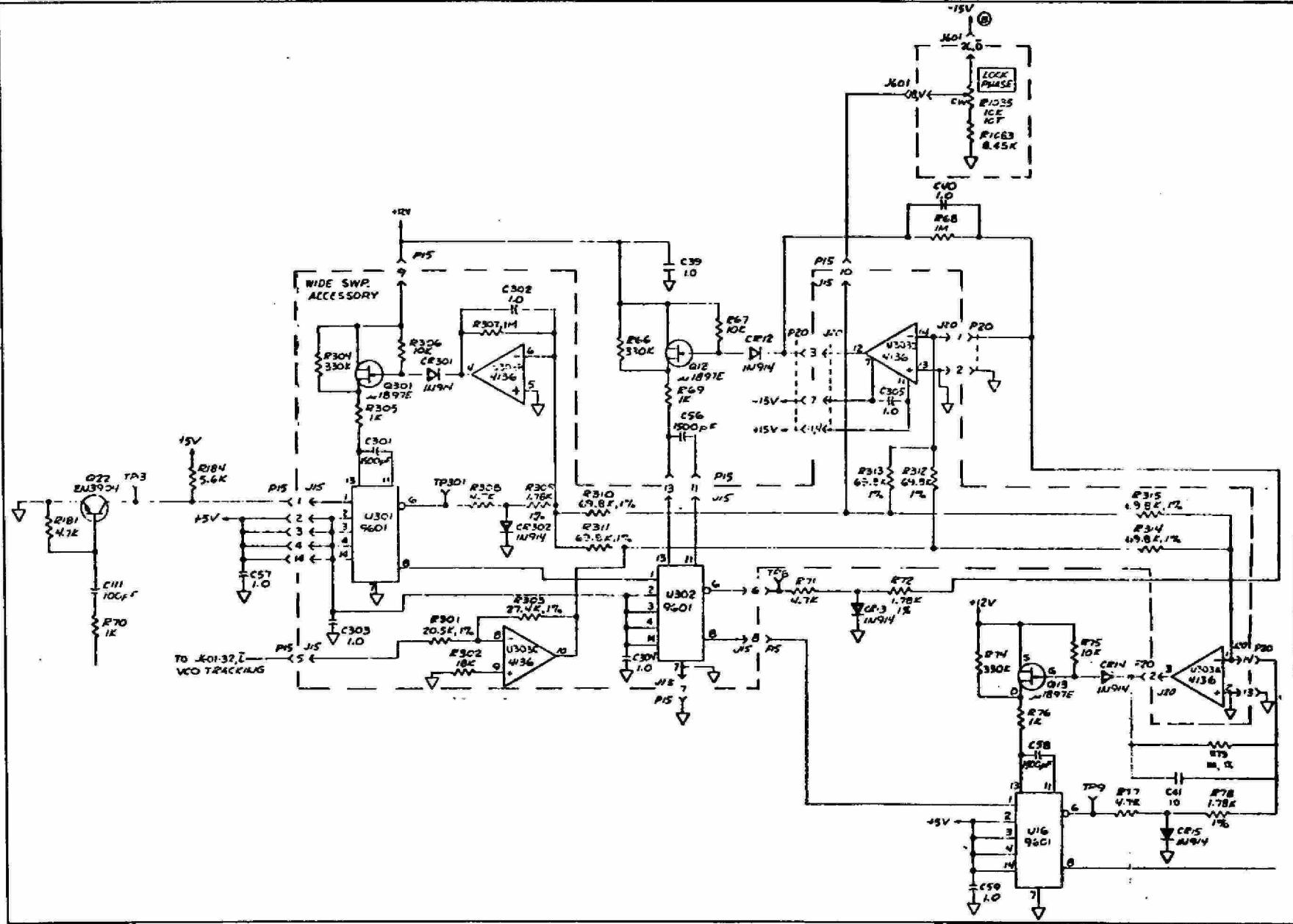


FIGURE 5-13. WIDE SWEEP ACCESSORY

The balanced squarewave from U11 is applied to Q22 as before. This square wave is inverted and applied to the first stage of the Wide Sweep Accessory, U301. IC U301 is a retriggerable monostable multivibrator which triggers on the negative going wavefront of the input and whose "on" time is governed by the RC between pins 11 and 13 of the IC.

There are two factors now which determine the voltage applied to the FET Q301 in the RC circuit of U301 thus determining the "on" time. One is the output of the LOCK PHASE front panel control applied to the inverting input of U303B. The other input is the VCO TRACKING signal from the Field Controller PCB buffered and inverted in U303C and applied to the inverting input of U303B with the LOCK PHASE input. This VCO TRACKING as you recall is the combined SWEEP and OFFSET data developed and summed in the Field Control PCB and its level is proportional to the frequency of the lock signal. The positive voltage from U303B to Q301 to set the "on" time of U301 is now the desired LOCK PHASE plus a frequency correction to account for phase shifts in the Receiver and Lock Channel due to frequency changes.

The compensated output positive pulse of U301 then toggles U302 on the negative going trailing edge. The "on" time of U302 is determined by the voltage on the gate of Q12. This voltage is determined by the values of the VCO TRACKING through U303C and LOCK PHASE control. Both levels are applied to the inverting input of U303D. The resulting positive pulse from U302 Q-bar output is applied to IC U16 input.

U16 operates as before with the "on" time now determined by the combined VCO TRACKING and LOCK PHASE levels applied to U303A. The total output then at Q-bar of U16 represents the phase shift due to the setting of the LOCK PHASE of up to 550° as modified by the frequency compensation to maintain lock over a 50 PPM range.

The rest of the circuits remain the same in both versions of the card; that is, 0° LOCK BALANCE, 90° PHASE SHIFT, and 90° LOCK BALANCE.

The +5 volt source for the logic ICs in the card is obtained from an integrated circuit regulated U23. The 10.5 volt Regulated digital circuit and Variable Temperature supply drives the regulator to produce the +5 volts.

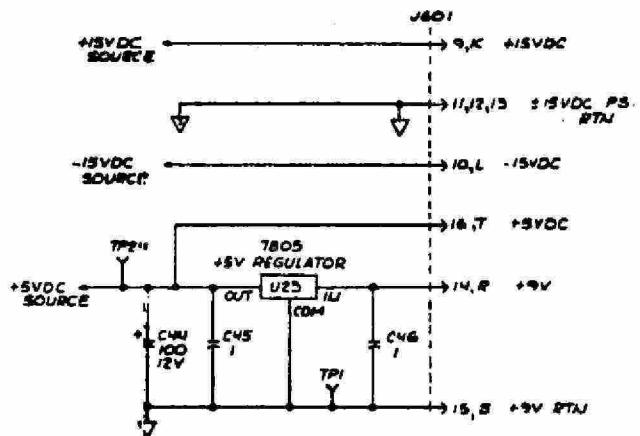


FIGURE 5-14. 5 VDC POWER SUPPLY

3. MODULATION AMPLIFIER

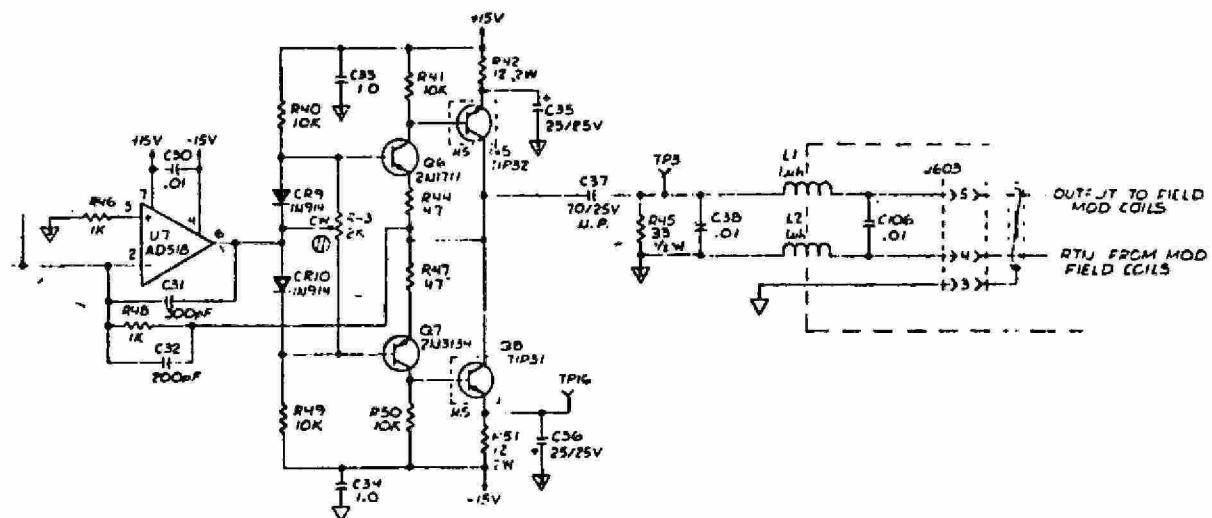


FIGURE 5-15. MODULATION POWER AMPLIFIER

The three possible modulation frequencies on the EM-390 are combined in the inverting input of U7. These are the 25 KHz Observe, the 20 KHz to 30 KHz Lock, and the 20 KHz to 30 KHz Spin Decoupler frequencies. The combined or resultant signal is amplified and applied to the power output drivers. The positive half-cycle drivers are Q5 and Q6 and the negative half-cycle drivers are Q7 and Q8. The output is balanced by the setting of R43 with the level shift and temperature compensation of CR9 and CR10. These diodes compensate for the fact that a transistor base-emitter junction requires a bias of 0.6 volt (silicon) to operate. Since the junctions of the diodes CR9 and CR10 are affected by

temperature in the same manner as the base-emitter junctions of the output transistors, the circuit is self-compensating for temperature variations.

The combined output is a sine wave of current to the modulation coils in the probe side-walls.

4. SPINNER SPEED TACHOMETER

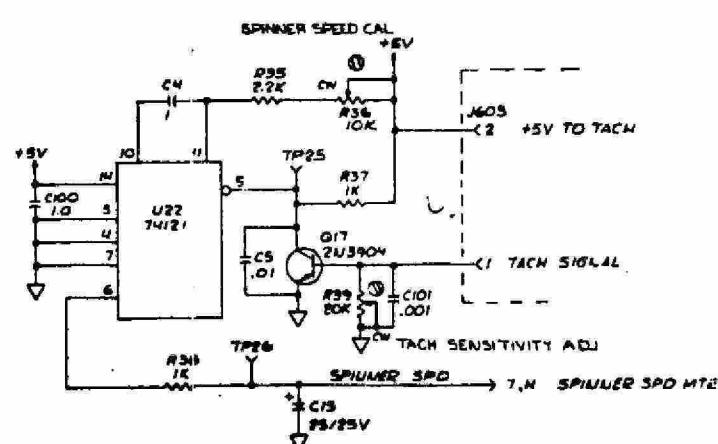


FIGURE 5-16. SPINNER SPEED

The pulses from the solid state tachometer in the probe are applied at J603-1 to squaring amplifier Q17. R39 is adjusted for the input sensitivity for reliable operation. The output of Q17 triggers monostable multivibrator U22 whose period is determined by the RC between pins 10 and 11 of the chip. R36 is used to set the "on" time of operation for the correct meter indication of spinner speed. An RC circuit on the output allows the DC level of the pulses to be displayed on a meter.

This circuit makes up a frequency-to-voltage converter whose DC output is proportional to one-half the input frequency.

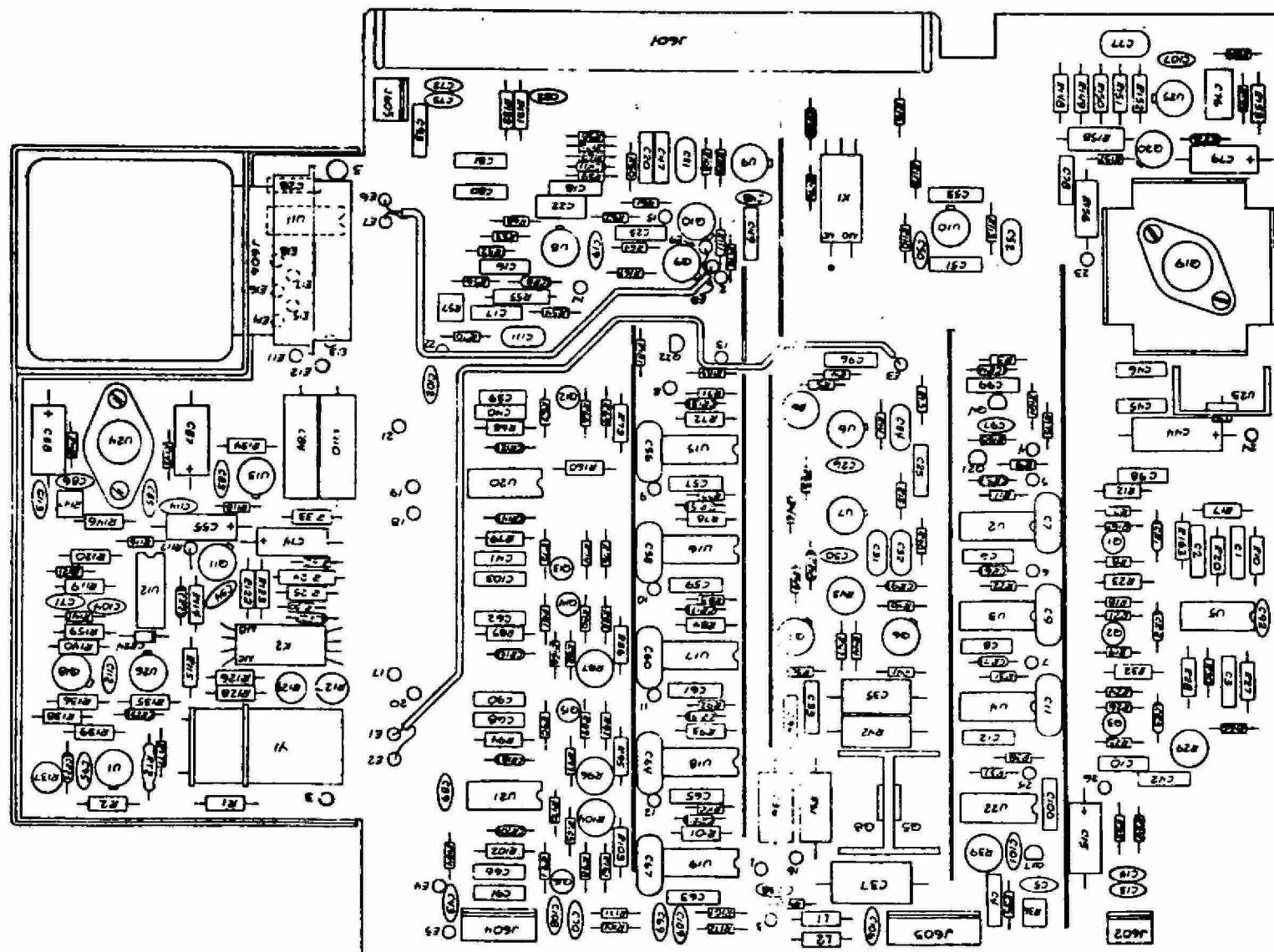
5.3 TESTS AND ADJUSTMENTS

1. REGULATED POWER SUPPLY ADJUSTMENT

a. Check the voltage at TP22.

1) The value should be +15 volts $\pm 0.1V$.

FIGURE 5-17. FIELD MODULATOR PART LAYOUT



- 2) Set the voltage to this value with R147 (under the oven cover).
 - b. The voltage at TP21 should be $-15V \pm 0.2V$.
 - c. Set the voltage at TP19 to $-10V \pm 0.2V$.
 - d. The voltage at TP20 should be $+12V \pm 0.2V$.
 - e. The voltage at TP24 should be $5V \pm 0.25V$.
2. OBSERVE 25 KHz PHASE SHIFT AND MODULATION SECTION
 - a. Set the LOCK POWER to OFF.
 - b. Observe the signal at E1 with an oscilloscope.
 - 1) The signal is a very clean sinewave.
 - 2) The amplitude is 4 to 6 volts peak-to-peak.
 - 3) The frequency is 25.0 KHz ± 1.5 Hz as measured on a high resolution counter.
 - c. Connect the oscilloscope to TP3.
 - 1) Set the OBSERVE POWER control fully clockwise.
 - 2) Set R43 approximately to mid-range.
 - 3) Adjust R6 for an 0.5 volt peak-to-peak 25 KHz sinewave at TP3.
 - 4) Adjust R43 for minimum crossover distortion.
 - d. Check that the signal on pin 5 of J603 is the same as that of TP3.
 - e. Set the OBSERVE POWER control fully counterclockwise.
 - 1) Measure the voltage drop across R51.
 - 2) This drop should be 0.26V to 0.35V DC.
 - f. Observe the following waveforms triggering the oscilloscope negative with TP4 signal.

- 1) Set the OBSERVE PHASE control fully counterclockwise. Observe TP4, TP5, and TP6 relationships

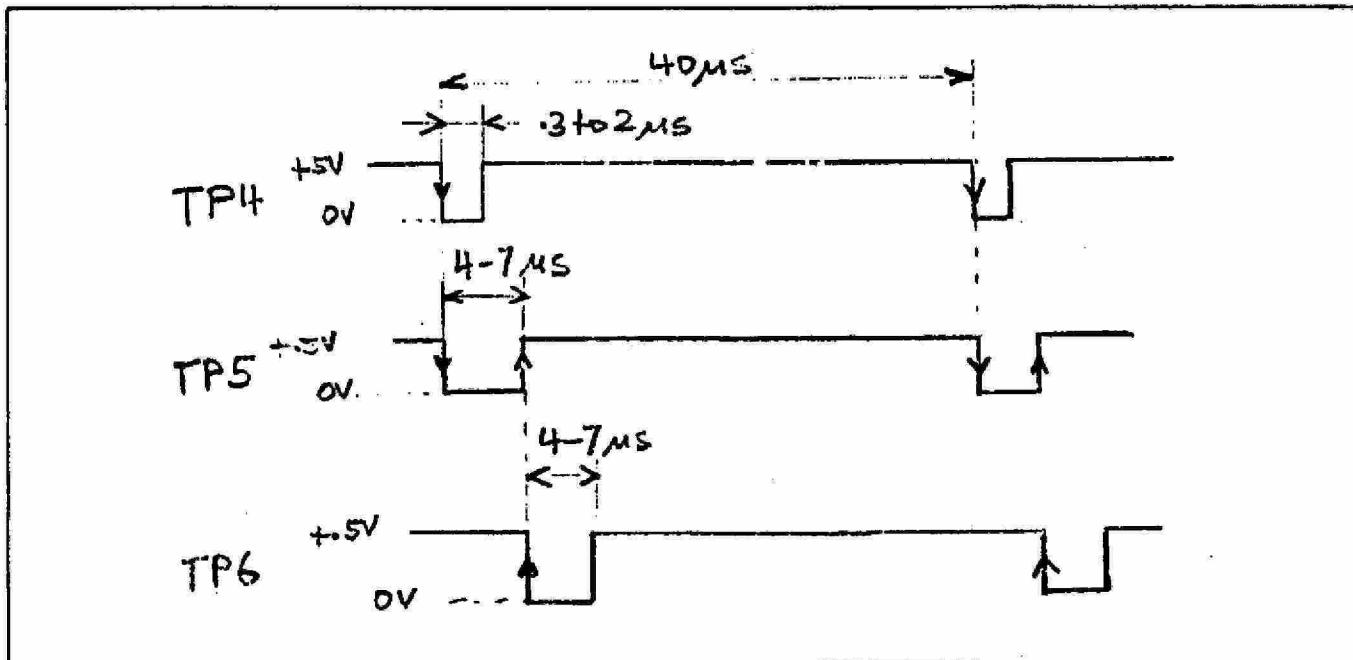


FIGURE 5-18. OBSERVE PHASE CCW

- 2) The voltage at U5 pin 3 and U5 pin 4 should be more than -1V DC in magnitude.
- 3) Set the OBSERVE PHASE control fully clockwise. Observe TP4, TP5, and TP6 relationships.

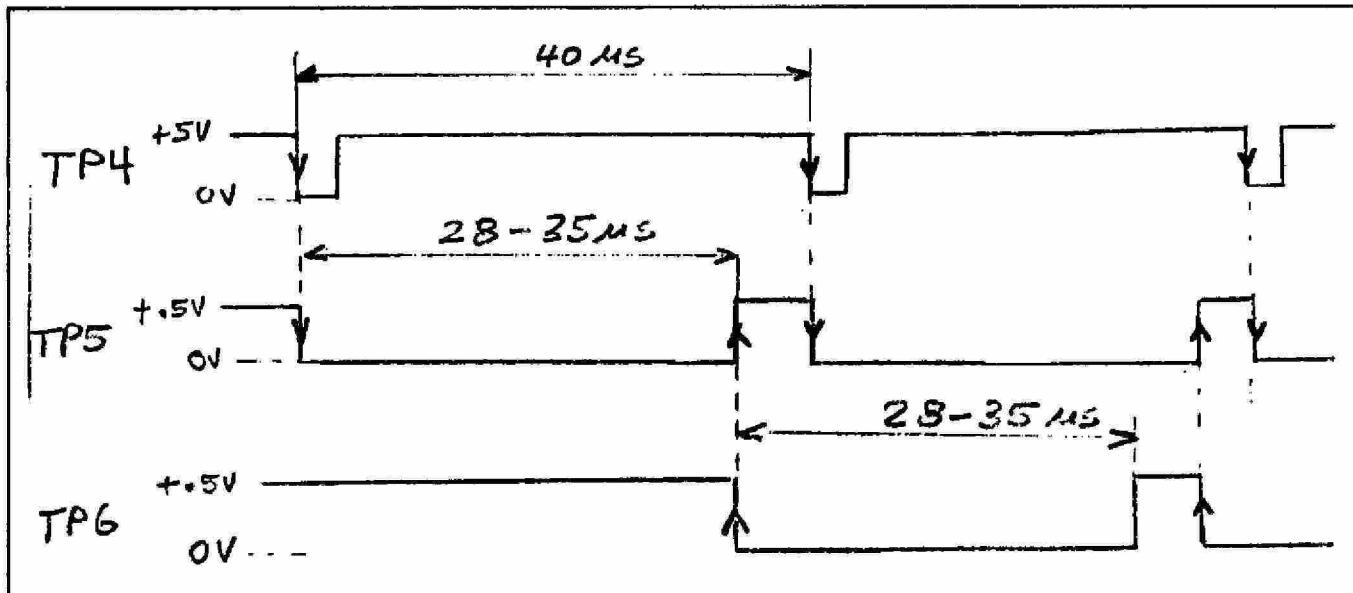


FIGURE 5-19. OBSERVE PHASE CCW

- 4) The voltage at U5-3 and U5-4 should be less than -10V DC in magnitude.
- g. Trigger the scope positive with the signal at TP6 and observe the signal at TP7.
- 1) Set R29 for a 50 percent duty cycle as shown in Figure 5-20.

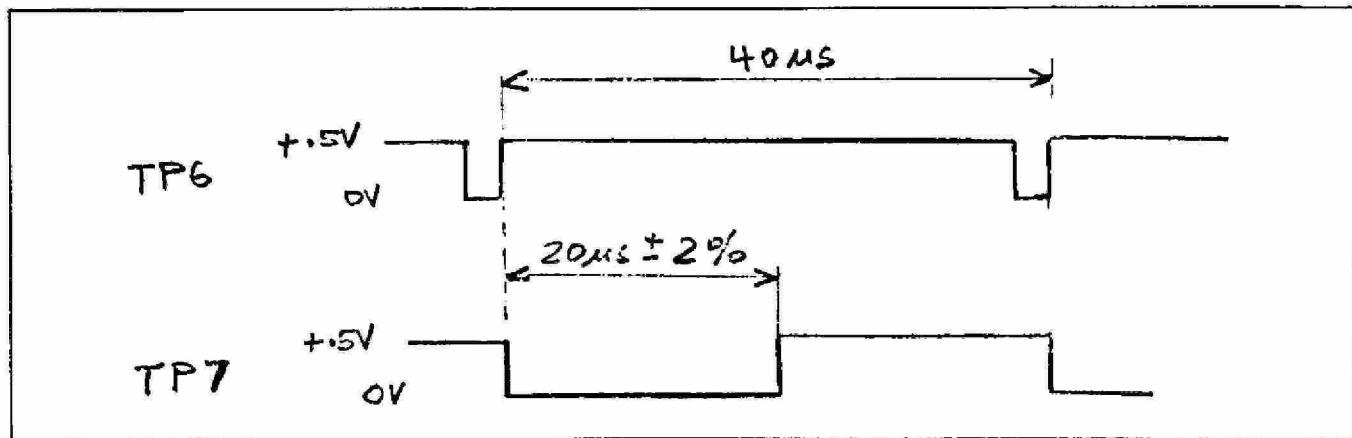


FIGURE 5-20. OBSERVE DUTY CYCLE SETTING

- 2) The voltage at U5-12 should be within -1 volt to -10 volts DC.
- h. Check that the TP7 signal is present at J602 pin 2 with an amplitude of 3 to 4 volts peak-to-peak.
- i. Check that the TP7 signal is present at J602 pin 1, 180° out of phase with J602-2, with an amplitude of 3 to 4 volts peak-to-peak.
- j. Trigger the oscilloscope negative with TP4.
- 1) Observe the signal at TP7.
- 2) Turn the OBSERVE PHASE through its entire range.
- 3) Check that the pulse width jitter on TP7 is less than 1 percent or 400 nanoseconds.

The most critical point of jitter is when the trailing edge of the TP5 signal and the leading edge of the TP6 signal coincide. This is due to input trigger signal leakage into the timing circuit within the monostable multivibrator IC's.

3. LOCK 20-30 KHz PHASE SHIFT AND MODULATION SECTION

- a. Turn the OBSERVE POWER control fully counterclockwise.**
- b. Set the LOCK POWER Switch to ON.**
- c. Set the COARSE and FINE FREQUENCY controls fully counterclockwise.**
- d. Jumper pin 32 of J601 to ground.**
- e. Monitor the signal at TP2 with oscilloscope and counter.**
 - 1) The signal amplitude is a square-wave of 3 to 4 volts peak-to-peak.**
 - 2) The frequency should be less than 19.0 KHz.**
- f. Turn the FINE FREQUENCY control fully clockwise.**
- g. The frequency of the signal at TP2 should increase by $100 \text{ Hz} \pm 15 \text{ Hz}$.**
- h. Turn the COARSE FREQUENCY control fully clockwise.**
- i. The frequency of the signal at TP2 should be higher than 31.5 KHz.**
- j. Remove the jumper from pin 32 to ground and place the recorder pen on chart zero.**
- k. Set the frequency at TP2 to exactly 25.0 KHz with the two frequency controls.**
- l. Select 10 PPM SWEEP WIDTH and move the recorder arm to the 900 Hz position of the chart.**
- m. Adjust R127 such that the signal frequency at TP2 changes by $900 \text{ Hz} \pm 10 \text{ Hz}$.**
- n. Move the recorder back to chart zero and adjust the frequency for exactly 25.0 KHz at TP2.**
- o. Observe the following waveforms triggering the oscilloscope negative with the TP13 signal.**
 - 1) Set the LOCK PHASE control fully counterclockwise.**

- 2) Observe the waveforms of TP13, TP8, and TP9 to be shown in Figure 5-21.

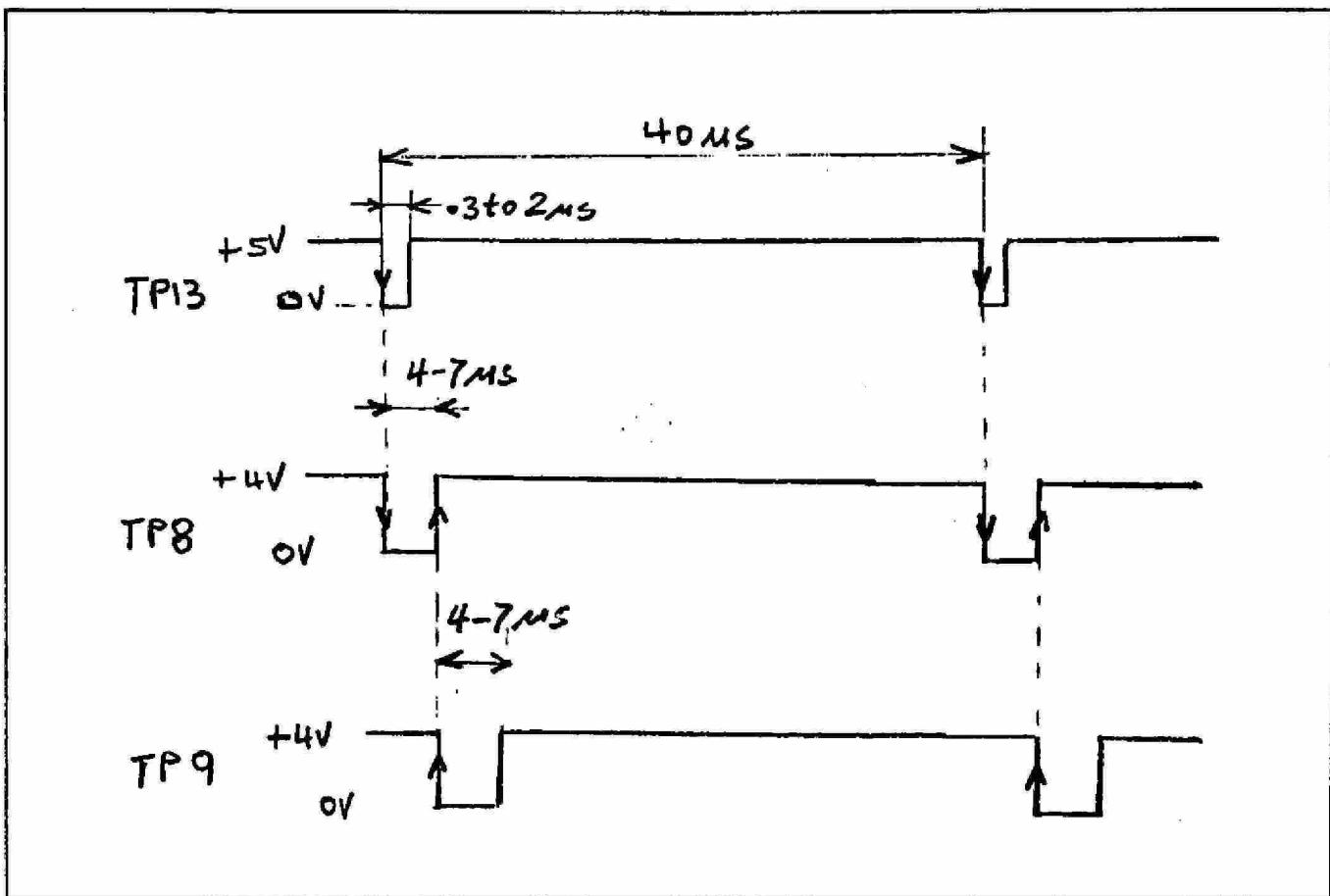


FIGURE 5-21. LOCK PHASE CCW

- 3) The voltage at U20 pin 12 should be more than -1 volt in magnitude.
- 4) Set the LOCK PHASE control fully clockwise.
- 5) Observe the waveforms at TP13, TP8, and TP9 to be as follows.

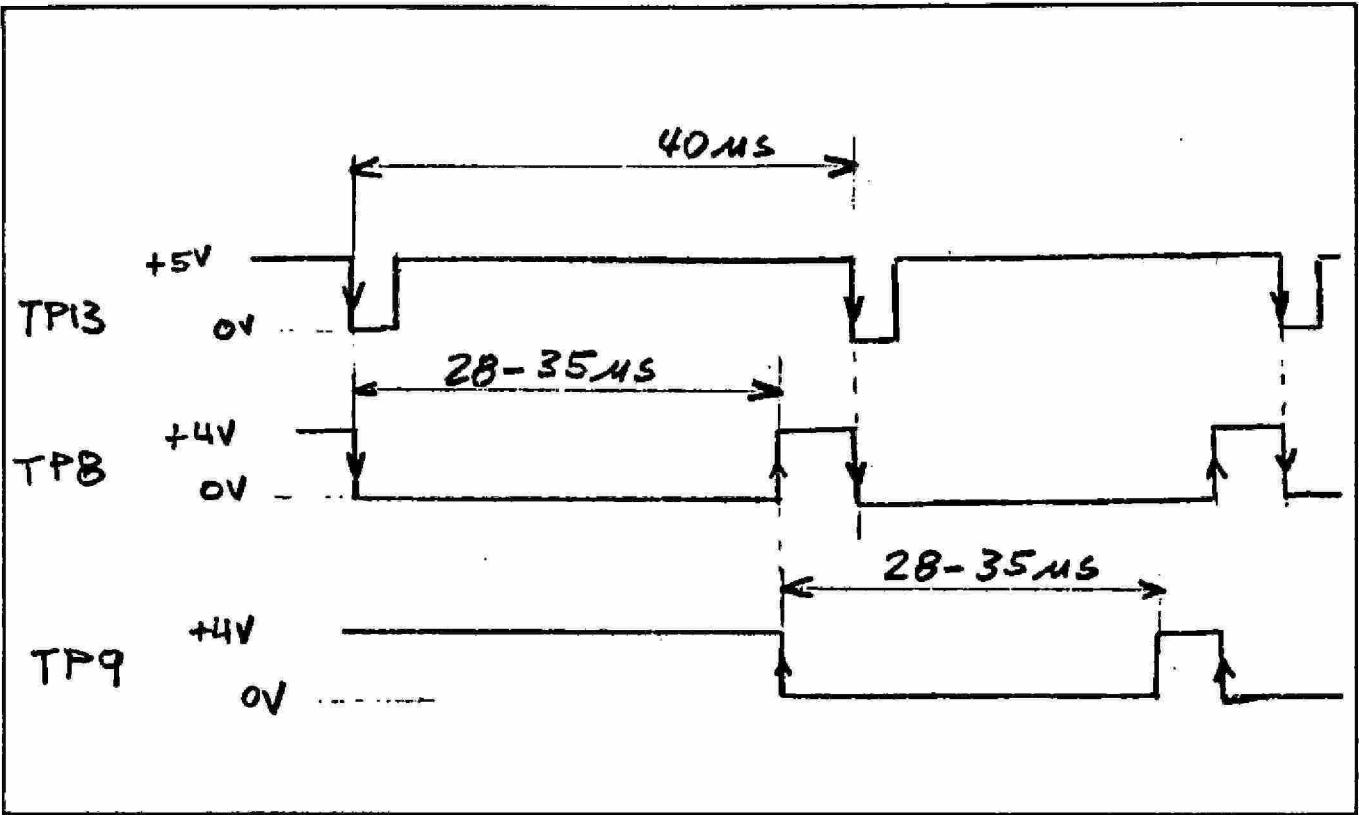


FIGURE 5-22. LOCK PHASE CCW

- 6) The voltage at U20 pin 3 and pin 12 should be less than -10 volts in magnitude.
- p. Trigger the oscilloscope positive with the signal at TP9.
- 1) Set the signal at TP10 with R87 to obtain a 50 percent duty cycle as shown in Figure 5-23.

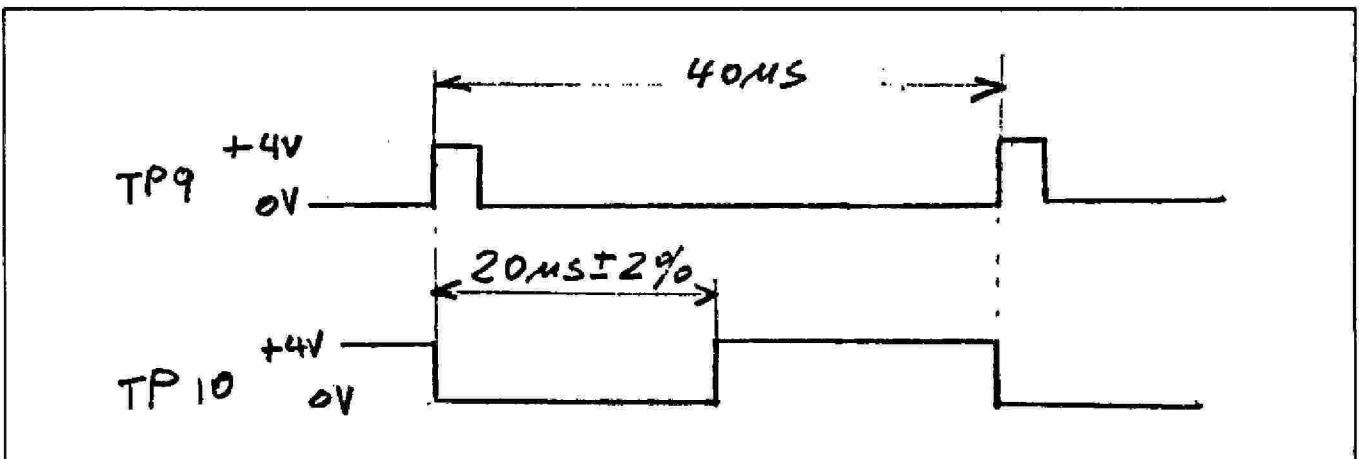


FIGURE 5-23. 0° LOCK DUTY CYCLE SETTING

- 2) The voltage at U21 pin 4 should be within -1V DC to -10V DC.
 - 3) Check that the TP10 signal is present at J604 pin 4 at 3 to 4 volts peak-to-peak.
 - 4) Check that the TP10 signal is present 180° out of phase at J604 pin 5 at 3 to 4 volts peak-to-peak.
- q. Trigger the oscilloscope positive with the signal at TP10.
- 1) Set the signal at TP11 with R96 to obtain a 25 percent duty cycle as follows in Figure 5-24.

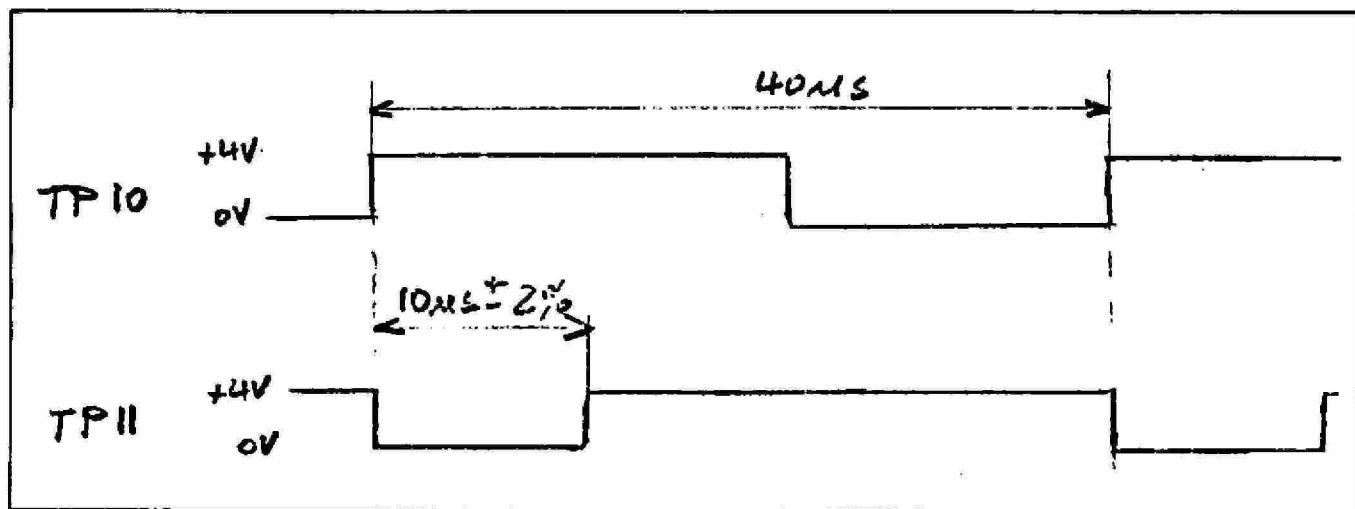


FIGURE 5-24. 90° PHASE SHIFT

- 2) The voltage at U21 pin 3 should be within -1 volt to -10 volts DC.
 - r. Trigger the oscilloscope positive with the signal at TP11.
- 1) Set the signal at TP12 with R104 to obtain a 50 percent duty cycle as follows in Figure 5-25.
 - 2) The voltage at U21 pin 12 should be within -1 volt to -10 volts DC.
 - 3) Check that the TP12 signal is present at an amplitude of 3 to 4 volts peak-to-peak at J604 pin 2.
 - 4) Check that the TP12 signal with 180° phase shift is present at an amplitude of 3 to 4 volts peak-to-peak at J604 pin 3.

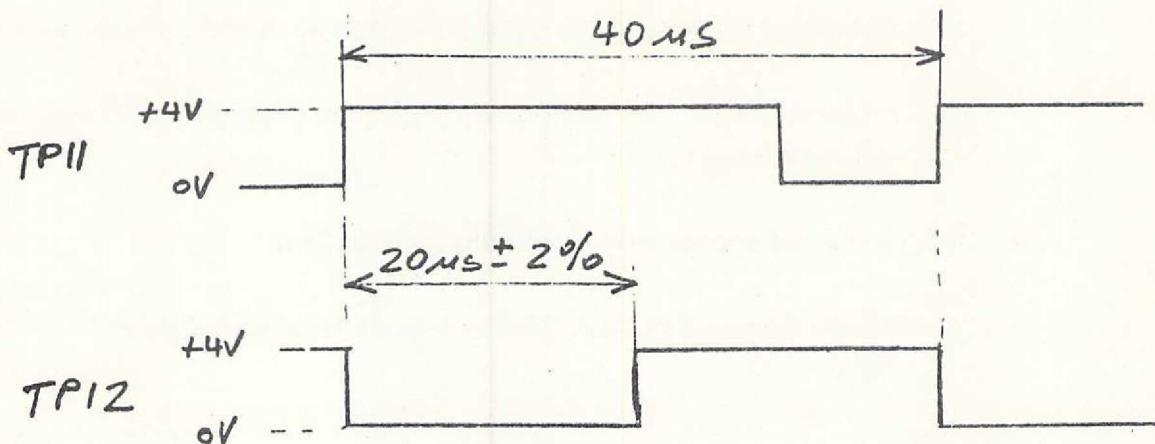


FIGURE 5-25. 90° LOCK DUTY CYCLE SETTING

- s. Trigger the oscilloscope negative with the TP13 signal and observe TP10.
 - 1) Slowly turn the LOCK PHASE control over its entire range.
 - 2) Check that the pulse width jitter is less than 1 percent or 400 nanoseconds.
 - 3) The most critical point of jitter is when the trailing edge of the TP8 signal and the leading edge of the TP9 signal coincide.
- t. Observe the signal at TP12 and rotate the COARSE FREQUENCY control from fully counterclockwise to fully clockwise.
 - 1) Check that the duty cycle of the signal at TP12 stays at 50 percent \pm 2 percent (800 nanoseconds) at the extreme positions of the control.
 - 2) Set the frequency back to 25 KHz.
- u. Turn the LOCK POWER control fully clockwise.
 - 1) Connect the oscilloscope to TP3 and adjust R57 to obtain a 50 millivolt peak-to-peak signal.

- 2) This waveform is a triangular type with rounded corners to approximate a sine-wave.
- v. Connect the oscilloscope to TP15 and set the signal frequency to 20.0 KHz.
 - 1) Measure and record the peak-to-peak amplitude.
 - 2) Check the DC voltage at TP14 – it should be more than +1 volt DC.
 - 3) Set the signal frequency to 30 KHz.
 - 4) The peak-to-peak amplitude of the signal should increase by a factor of $1.5 \pm 10\%$.
 - 5) Check the DC voltage at TP14 – it should be less than +9.2 volts DC.
- w. Connect the oscilloscope to TP14.
 - 1) Momentarily short the case of Q10 to ground.
 - 2) Observe the transmit response of the TP14 signal which should be well damped.

4. SPINNER SPEED TACHOMETER ADJUST

- a. Place the REFERENCE sample in the probe and spin at 40 rps.
- b. Run a trace of either chloroform or TMS and observe the spinning sidebands.
- c. The separation of the first spinning sideband from the main peak should be 40 Hz.
- d. Adjust R36 until the meter reading and spinning sideband separation from the main peak agree.

5. OVEN CONTROL SECTION

- a. Attach a heat sensor to the top of the U14 module in the inner oven and replace the covers without using the mounting screws.
- b. Wait 20 minutes for equilibration.

- c. Monitor the voltage at TP23 — it should be +0.25 to 0.35 volt.
- d. The temperature at U14 should be 43°C to 46°C.
- e. Observe TP23 and momentarily short CR26 to ground.
 - 1) Observe the voltage transient which should be well damped.
 - 2) Replace the oven covers after removing temperature sensor.

6. TRACKING ADJUST

See Section 4.0 Field Control PCB for tracking adjustments since any correction to that PCB affects VCO Tracking.

7. WIDE SWEEP ACCESSORY TEST

Trigger an oscilloscope with the pulse from TP13 and observe the delay at TP301 and TP9 as measured from the trailing edge of the pulse at TP13.

Table 5-1 shows the delay vs voltage characteristic at J15-10 and J15-5.

TABLE 5-1
Delay vs Voltage

Frequency	J15-5 Volts	J15-10 Volts	301,302, 16 μ s	TOTAL μ s
25 kHz	0	-15.0	13 ± 1.5	
25 kHz	0	-5.7	30 ± 2	
25 kHz	0	+Δ9.3	+Δ17 ± 2	+Δ51 ± 4
16200	+3.6	-15.0	6.0 ± 2.0	19 ± 3
33800	-3.6	-5.75	27 ± 2	

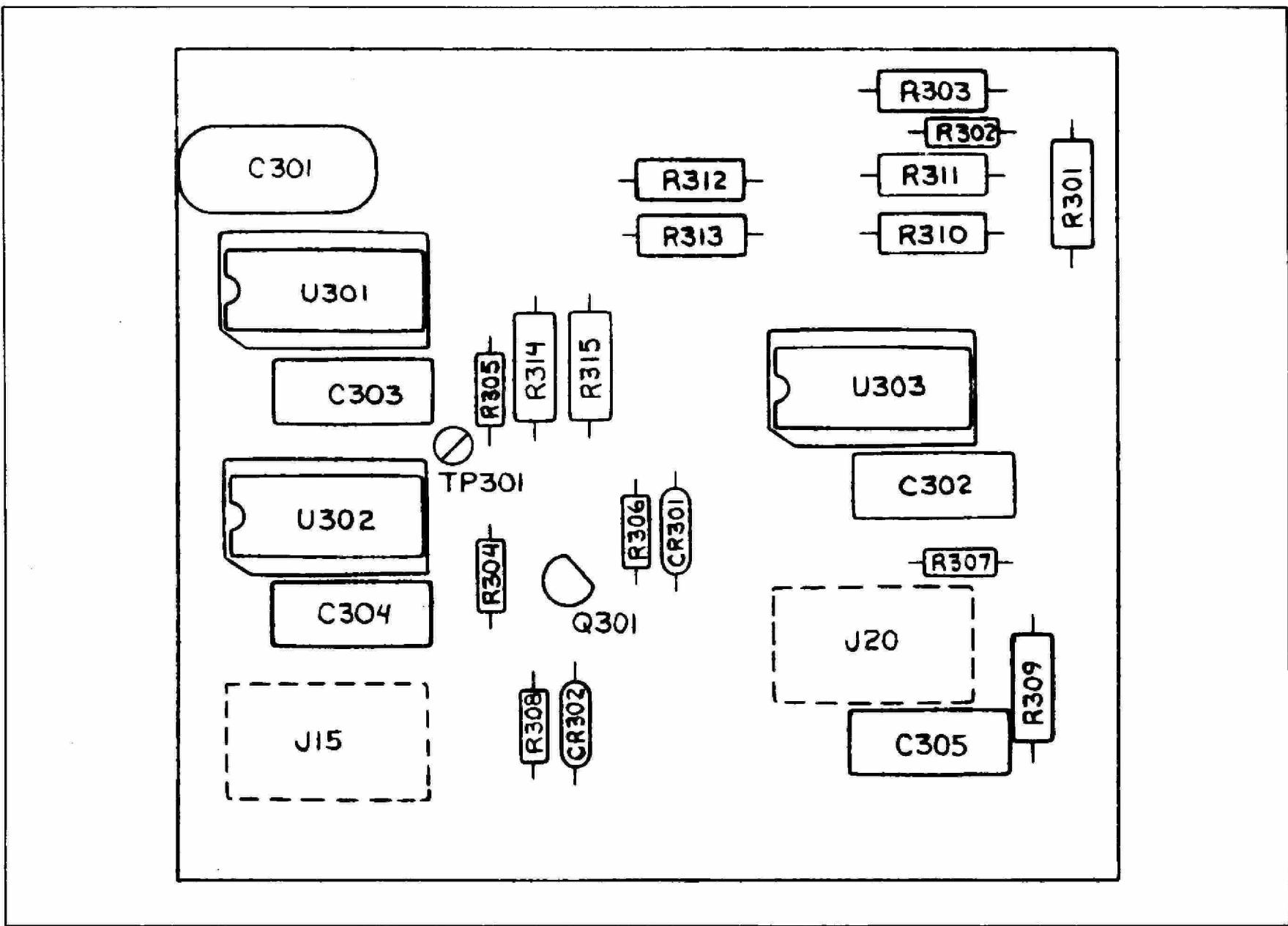


FIGURE 5-26. WIDE SWEEP COMPONENT LAYOUT

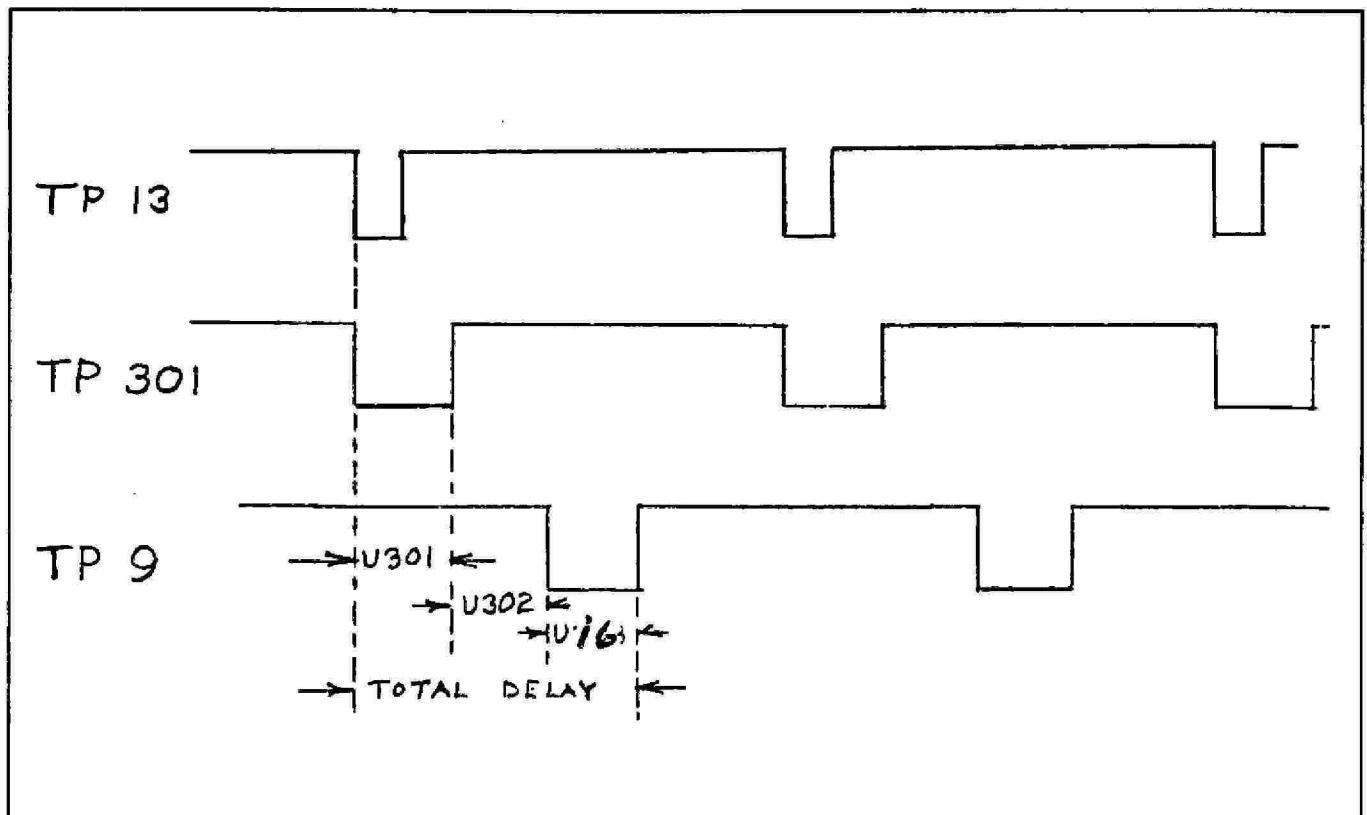


FIGURE 5-27. WIDE SWEEP WAVEFORMS

VARIAN ASSOCIATES
INSTRUMENT DIVISION
TECHNICAL SUPPORT
MAGNETICS GROUP

EM-390 TRAINING NOTES

SECTION 6.0
SHIM CONTROL

6.1 FUNCTION

The shim control circuits supply the various currents required to homogenize the magnetic field with various shim coils.

6.2 THEORY OF OPERATION

The circuits shown in Figures 6-1 through 6-4 are controlled by 12 front panel mounted potentiometers. Operational amplifiers with transistor drivers on the Shim Control PCB are used to control the shim currents for the shim coils mounted in the probe.

The circuits pictured should be sufficiently clear in their operation so that no further explanation is attempted here.

6.3 TESTS AND ADJUSTMENTS

1. Y² BALANCE

- a. A balance potentiometer (top right corner of the card) is provided for Y² homogeneity adjustments.
- b. With the system unlocked, observe a narrow line such as TMS on the chart paper.
- c. Optimize the homogeneity and trace the line.
- d. Rotate Y² Homogeneity Control one revolution.
- e. Adjust Y² BALANCE R64 to minimize the spectral shift of the line.
- f. Repeat the adjustment as often as required until no further improvement is possible.
- g. The shift must be less than 2 Hz for each revolution of Y² control.

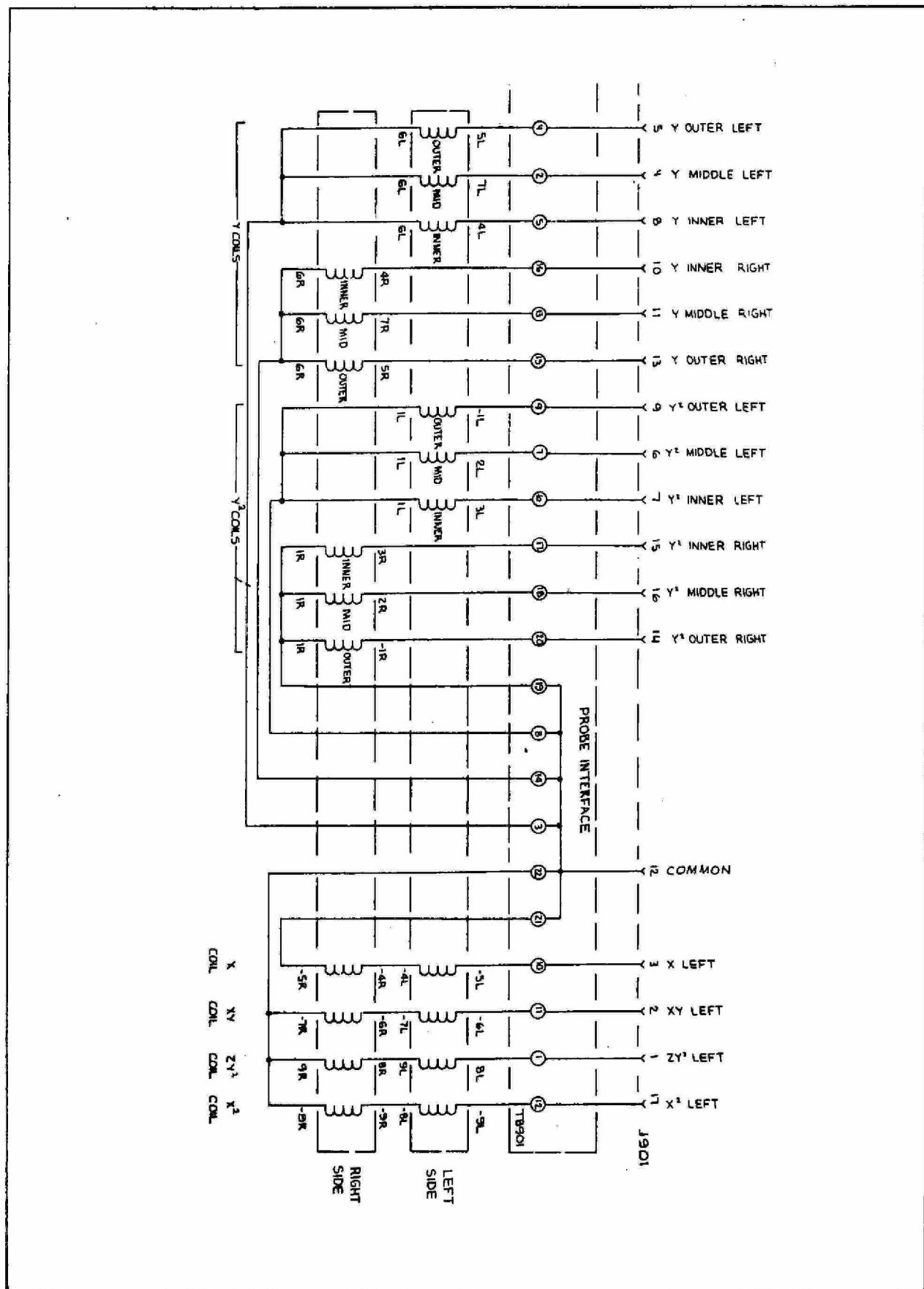


FIGURE 6-1. SHIM COILS IN PROBE

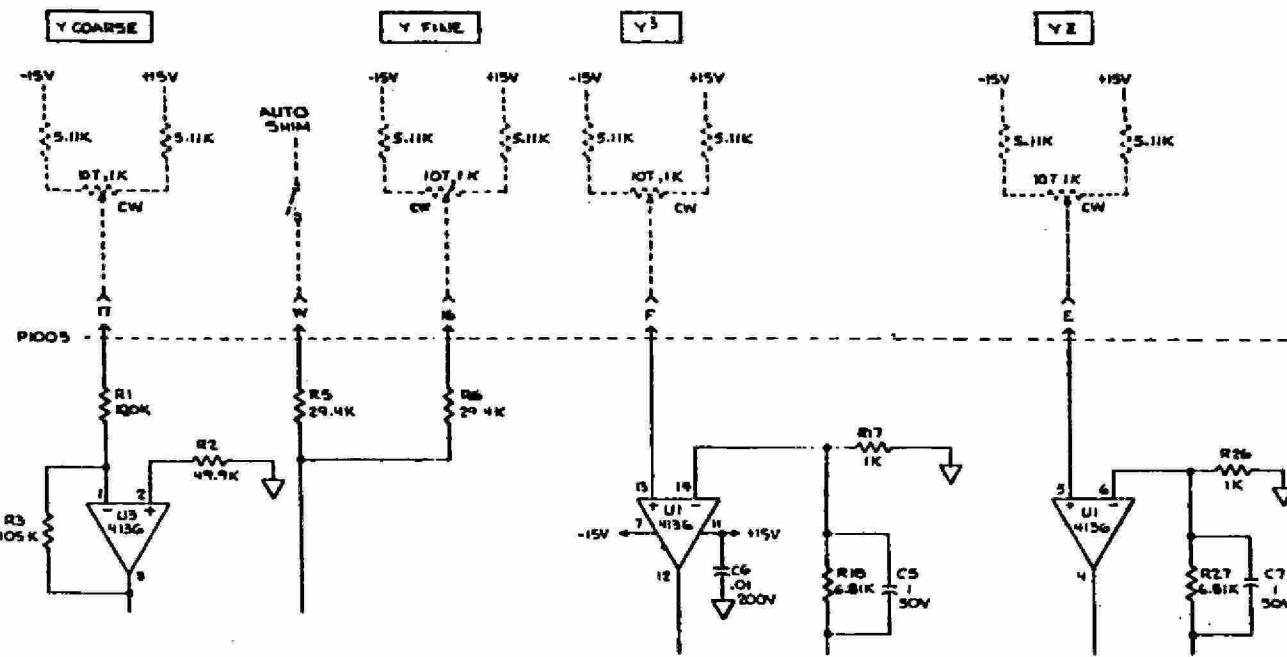


FIGURE 6-2. Y-SHIM CONTROLS

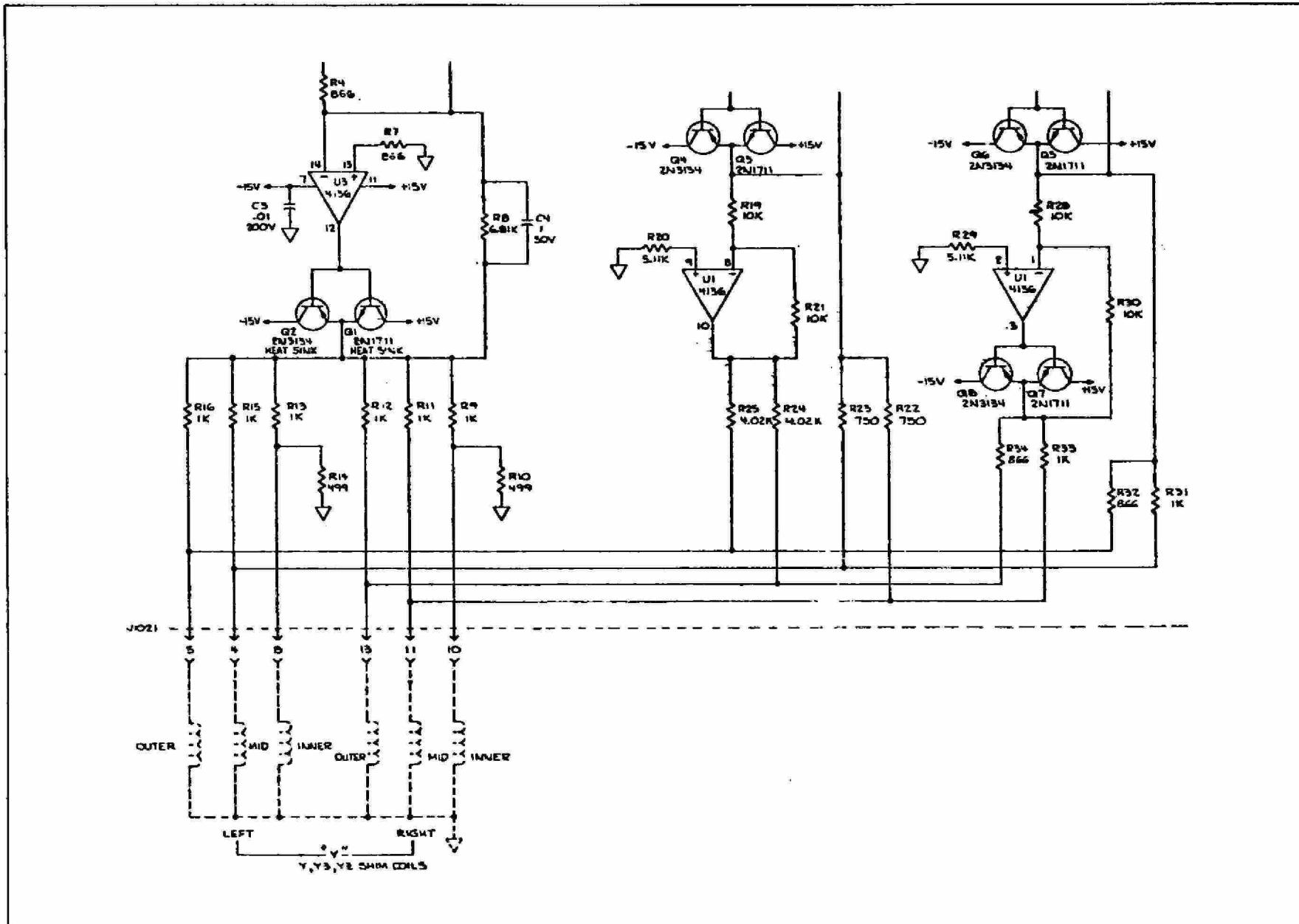


FIGURE 6-2. Y-SHIM CONTROLS (Continued)

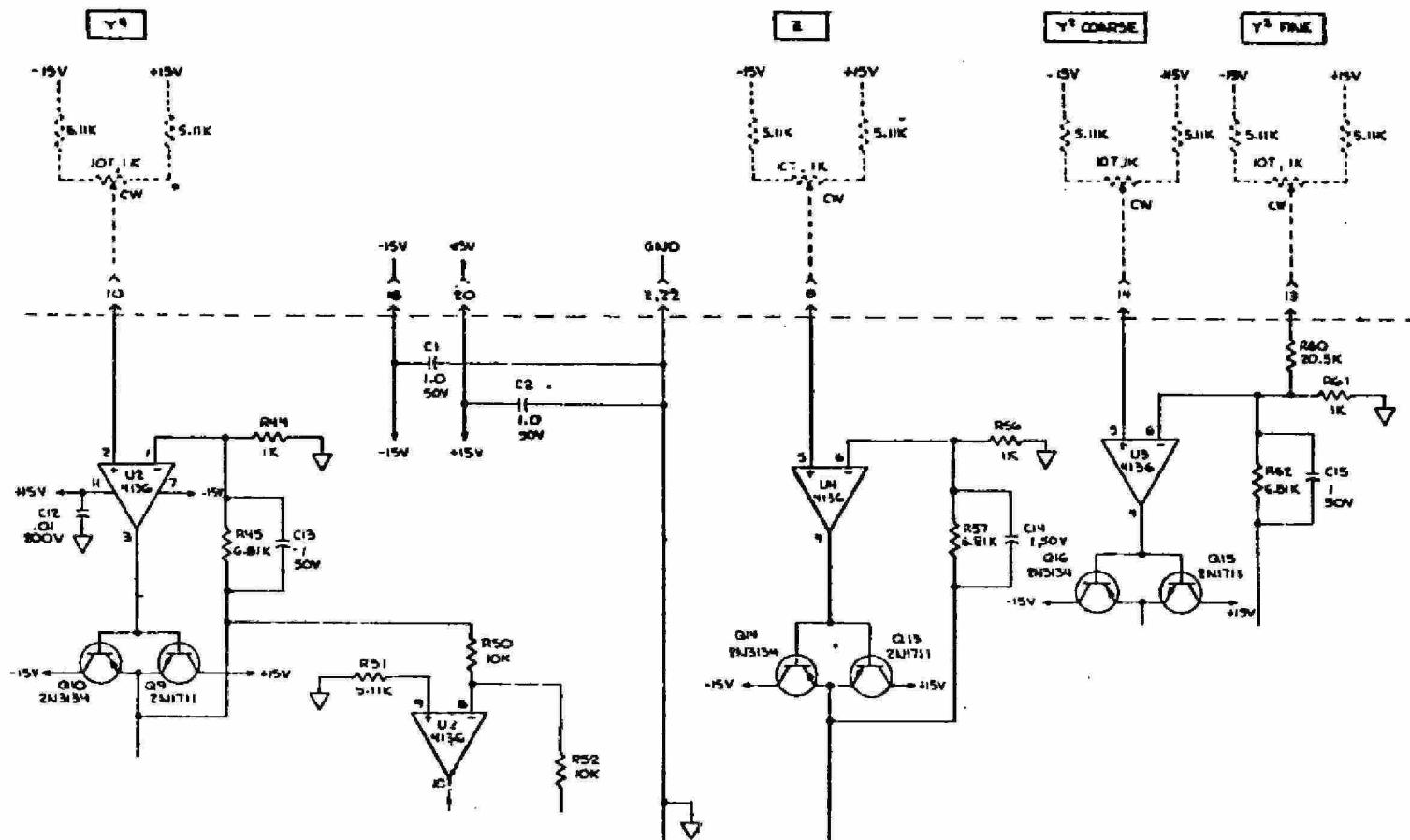


FIGURE 6-3. Y^2 SHIM CONTROLS

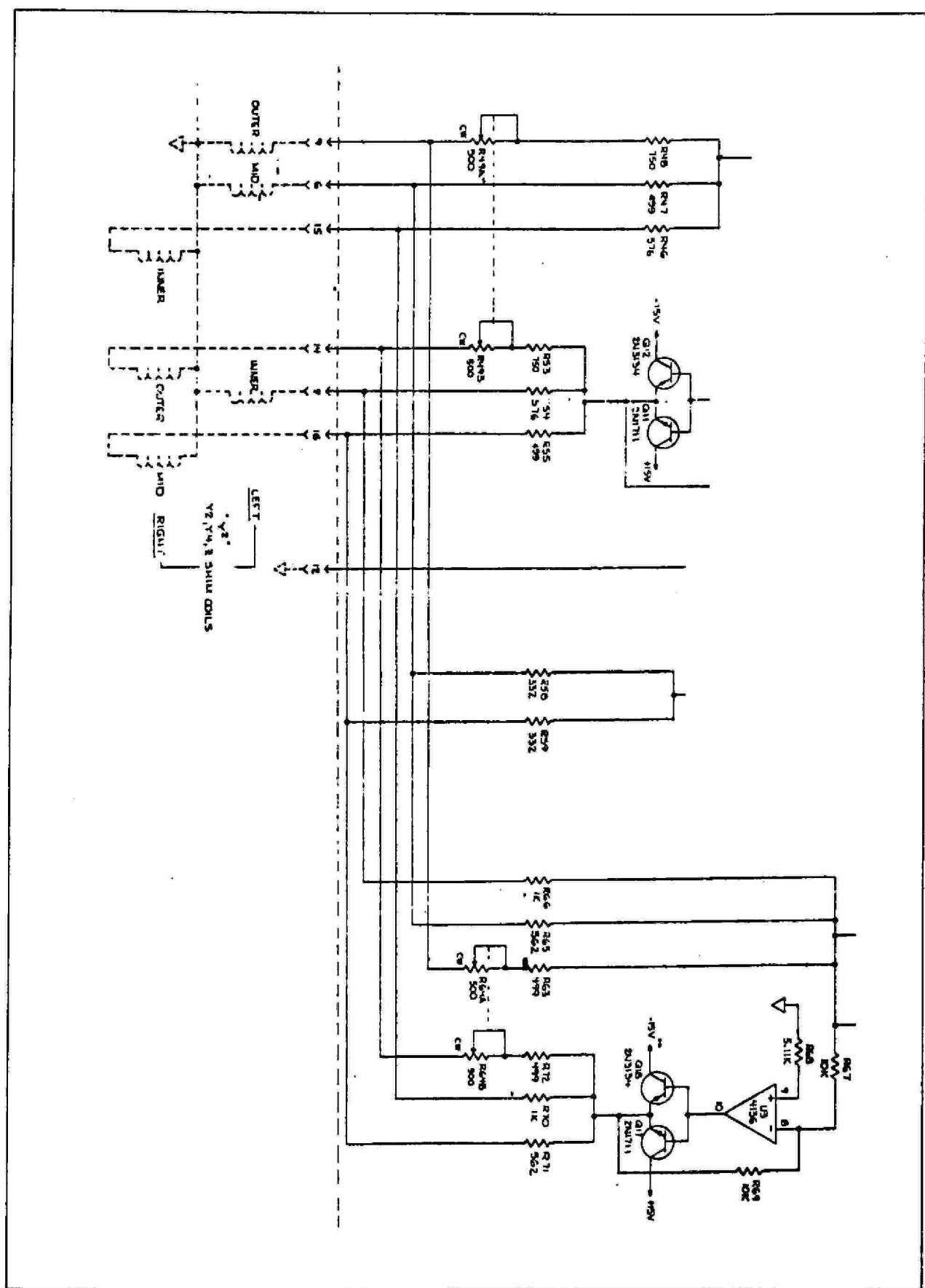


FIGURE 6-3. Y2 SHIM CONTROLS (continued)

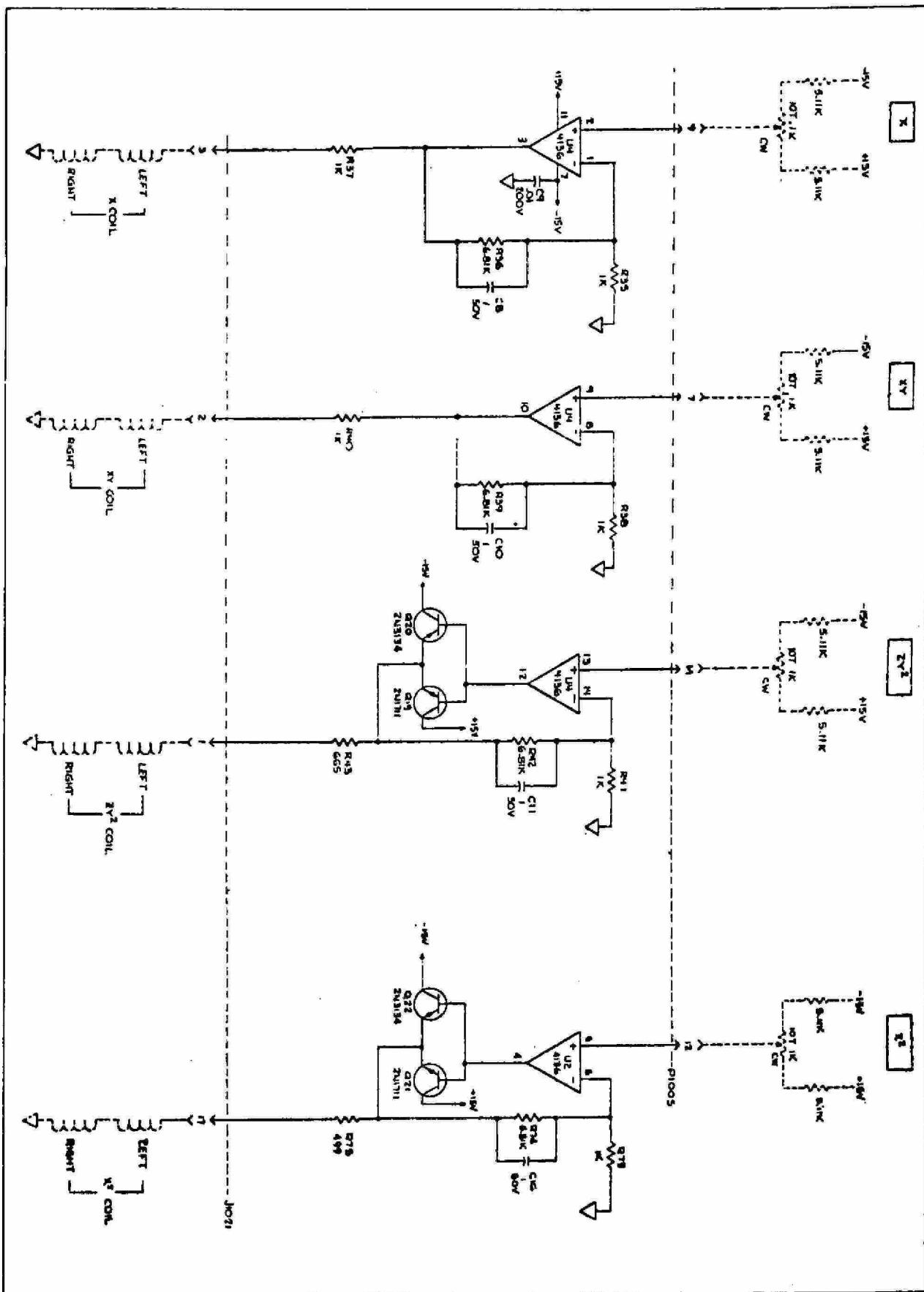


FIGURE 6-4. X, XY, ZY², AND X² SHIM COILS

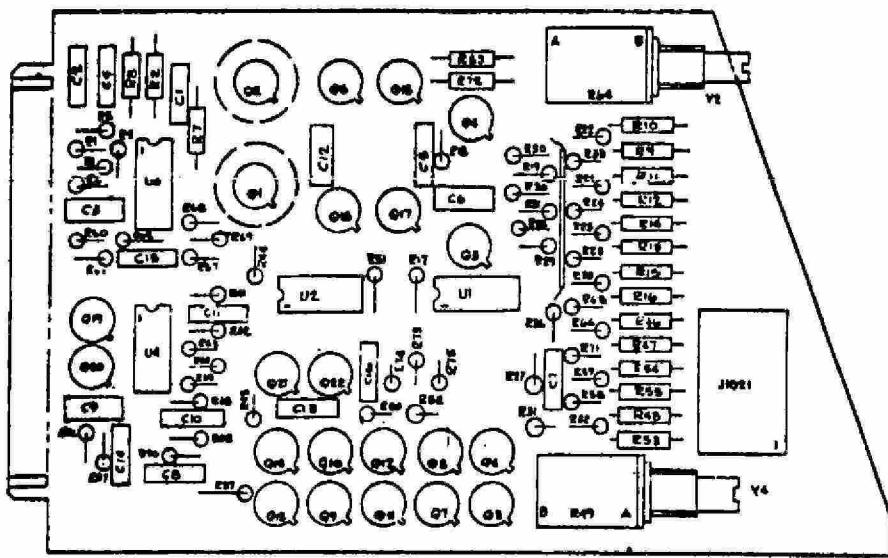


FIGURE 6-5. SHIFT COMPONENT LAYOUT

2. **Y^4 BALANCE**

- a. A balance potentiometer (lower right corner of the card) is provided for Y^4 homogeneity adjustments.
- b. With the system unlocked, observe a narrow line such as TMS on the chart paper.
- c. Optimize the homogeneity and trace the line.
- d. Rotate Y^4 Homogeneity control one revolution.
- e. Adjust Y^4 BALANCE R49 to minimize the spectral shift of the line.
- f. Repeat the adjustment as often as required until no further improvement is possible.
- g. The shift must be less than 2 Hz for each revolution of Y^4 control.

3. SHIM COIL RESISTANCE

The resistance tests are necessary since each coil may be driven by one or more IC/transistor combinations. Disconnect the ribbon cable with P1021 from the Shim Control PCB and measure the following using the X1 scale of the Ohm Meter. Since the individual coil resistances vary from probe to probe, test for continuity of a few ohms at each point to pin 12.

SHIM COIL	J1021 PIN NO.
ZY ²	1 to 12 10
XY	2 to 12 -15
X	3 to 12
Y-LEFT MIDDLE	4 to 12
Y-LEFT OUTER	5 to 12
Y ² -LEFT MIDDLE	6 to 12
Y ² -LEFT INNER	7 to 12
Y-LEFT INNER	8 to 12
Y ² -LEFT OUTER	9 to 12
Y-RIGHT INNER	10 to 12
Y-RIGHT MIDDLE	11 to 12
Y-RIGHT OUTER	13 to 12
Y ² -RIGHT OUTER	14 to 12
Y ² -RIGHT INNER	15 to 12
Y ² -RIGHT MIDDLE	16 to 12
x ²	17 to 12

4. VOLTAGE CHECKS

Using a DVM capable of 0.1 millivolt resolution, check the value of each pin enumerated in the table above to pin 12. P1021 is mated to J1021 at this time. During each measurement rotate the controls listed to check for variation of voltage. Each control listed will vary the voltage measured if the active elements associated with the control are operational.

J1021 PIN NUMBER

VARY CONTROL

1	ZY ²
2	XY
3	X
4	ZY, Y ³ , Y-COARSE, Y-FINE
5	ZY, Y ³ , Y-COARSE, Y-FINE
6	Z, Y ⁴ , Y ² -FINE, Y ² -COARSE
7	Y ⁴ , Y ² -FINE, Y ² -COARSE
8	Y-COARSE, Y-FINE
9	Y ⁴ , Y ² -FINE, Y ² -COARSE
10	Y-COARSE, Y-FINE
11	- ZY, Y ³ , Y-COARSE, Y-FINE
13	- ZY, Y ³ , Y-COARSE, Y-FINE
14	- Y ⁴ , Y ² -FINE, Y ² -COARSE
15	Y ⁴ , Y ² -FINE, <u>Y COARSE</u>
16	Z, Y ⁴ , Y ² -FINE, Y ² -COARSE
17	X ²

+ 10.732

10.545

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EM-390 TRAINING NOTES

SECTION 7.0
VARIABLE TEMPERATURE PROBE

7.1 FUNCTION

This unit is a single coil variable temperature probe having the following features.

1. The shim coils are mounted within the side plates of the probe.
2. The modulation coils are current sheet type using bobbin construction.
3. The cooling for variable temperature work uses a Joule-Thompson type of valve where high pressure nitrogen or argon gas is throttled through a small opening and cooling occurs.
4. A heater sensor is used to control the temperature of the sample.
5. A tachometer is used for monitoring turbine speed.
6. A matching network is used to step the insert impedance down to the 93 ohm transmission line.
7. An air eject system is used to retrieve the sample from the probe.

7.2 THEORY OF OPERATION

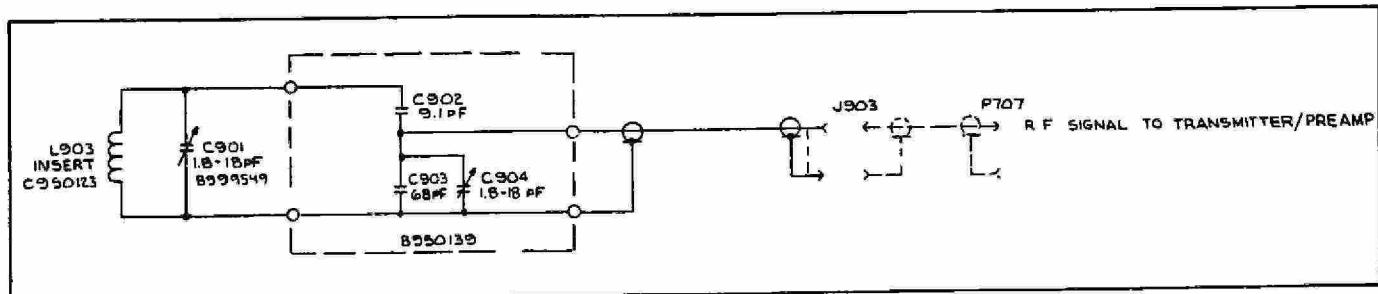


FIGURE 7-1. INSERT MATCHING NETWORK

An insert matching network is used to match the relatively high insert impedance to the 93 ohm transmission line. This network employs two trimming capacitors that are accessible from the top of the probe.

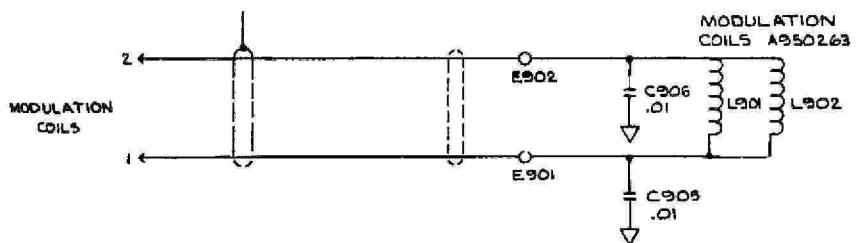


FIGURE 7-2. MODULATION COILS

The modulation coils are connected in parallel aiding and carry the combined Observe, Lock, and Spin Decoupler frequencies. These coils modulate the field at the specific driving frequencies.

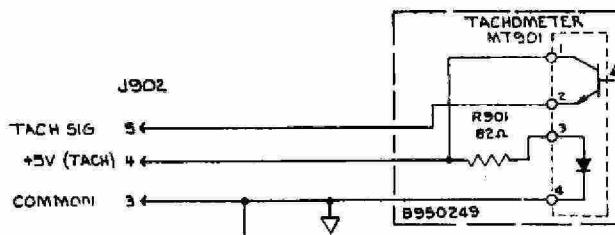


FIGURE 7-3. SPINNER SPEED TACHOMETER

The spinner speed tachometer contains a light emitting diode in the infra-red region. The emitted light is reflected back by the spinner to a light sensitive transistor which outputs two pulses per revolution of the sample. These pulses are routed to the Field Modulator PCB to generate a voltage proportional to the frequency of rotation.

The Shim Coils are pictured and their action discussed in Section 6.0.

A high pressure gas line carries dry nitrogen up to 1400 psi from the top of the probe to the inlet of the Joule-Thompson cryostat. The gas flows through a spiral heat exchanger. The gas then flows through a small opening past the heater sensor and the sample. The gas then flows through holes in the insert glass and down the space between the insert OD and the dewar ID. A pressure cap is used on the top of the turbine stack to keep the sample from lifting. The gas then counter flows past the heat exchanger cooling the incoming gas. The gas then exits at the bottom of the probe through a section of tubing to the top of the probe. A section of tubing can be connected to the exhaust hose barb for use in recirculating the gas in the air pump system.

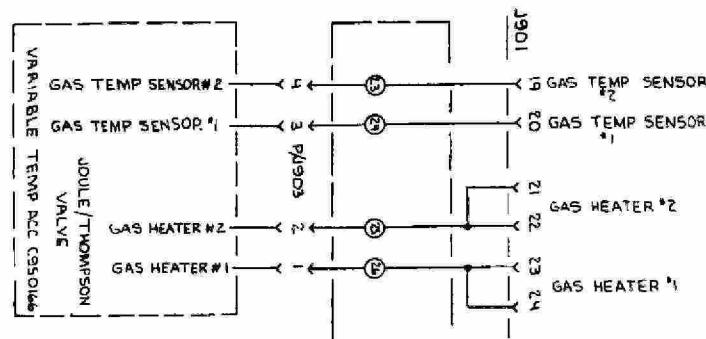


FIGURE 7-4. JOULE-THOMPSON VALVE

7.3 SAFETY PRECAUTIONS

High pressure gas lines are involved in this probe and injury can occur if the following precautions are not taken.

1. Check for correct procedure for installing fittings.
2. Double check all gas line fittings for tightness.
3. Never look for gas leaks in the high pressure lines using fingers or hands. Use a soap solution and look for bubbles.
4. Do not block the exhaust hose barb as internal pressures may build up.
5. Use only approved regulators and hardware that engineering has specified.
6. If a fitting is cross-threaded, replace it.

7.4 TESTS AND ADJUSTMENTS

- 1. Most probe failures are mechanical; that is, breakage of inserts, mis-alignment of the insert, build-up of dirt and sample residue in the probe, broken or un-wound modulation coils, loss of seal or vacuum in the dewar where insert wires come through, etc.**
- 2. A thorough visual inspection of the probe will detect any and all of these defects.**
- 3. After inspection, replace the probe in the gap and reconnect all hoses and connectors.**
- 4. Adjust C4 and C1 tuning wands for minimum leakage. If an impedance meter is available, C4 and C1 tune the probe to 93 ohms 0° at 90 MHz.**
- 5. Check for smooth, uniform spinning of the sample in the probe.**
- 6. Check for correct tachometer operation.**
- 7. Test for resolution and sensitivity as detailed in the basic system test.**

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EM-390 TRAINING NOTES

SECTION 8.0
 ^1H TRANSMITTER/PREAMPLIFIER

8.1 FUNCTION

A crystal controlled oscillator generates the basic frequency of 19.826250 MHz which is multiplied by 4 to produce the First Local Oscillator signal of 79.305 MHz.

This signal is mixed with 10.670 MHz (Second Local Oscillator signal from the Receiver) to produce the transmitted RF signal of 89.975 MHz.

A 90 MHz RF Preamplifier on this card amplifies the resonance signal and is converted to the probe through the directional coupler.

8.2 THEORY OF OPERATION

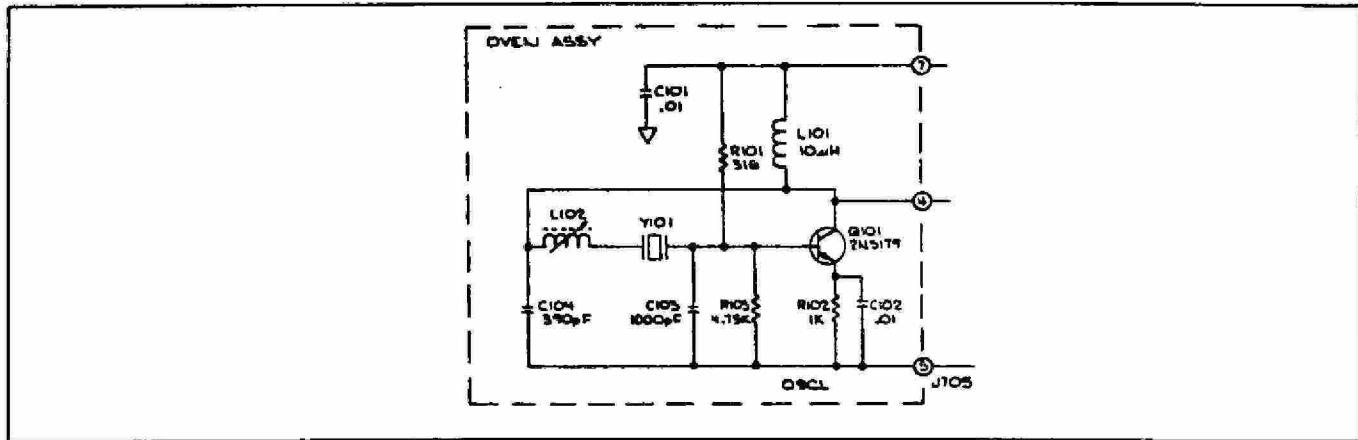


FIGURE 8-1. 19.826250 MHz OSCILLATOR

Vcc for the oscillator is the 7.6 volts DC produced on the Receiver PCB applied through P703-1 to J705-7. The oscillator is tuned by the selection of Y101 and the tuning of L102 for 19.826250 MHz. The oscillator is in an oven assembly to enhance frequency stability.

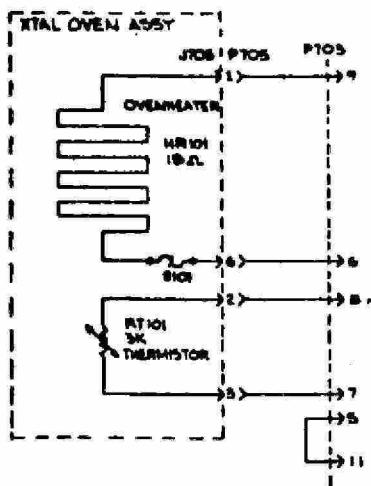


FIGURE 8-2. OSCILLATOR OVEN ASSY

The sensor for temperature control of both transmitter and receiver ovens is located on Transmitter No. 1 which is the designation of the transmitter in use. The oven heater is in series with the temperature controller output on the receiver, the receiver oven heater, and either the Second Transmitter (the one not in use, if installed) or a dummy load simulating the Second Transmitter. A fuseable link thermal switch is in series with the heater. If the temperature exceeds 70° C, the link opens and the switch must be replaced. The short circuit between J703 pins 5 and 11 is used when this card is in the Second Transmitter slot to disable the dummy load and replace it with the oven heater. If only one transmitter is used, the lack of this short enables the dummy load automatically.

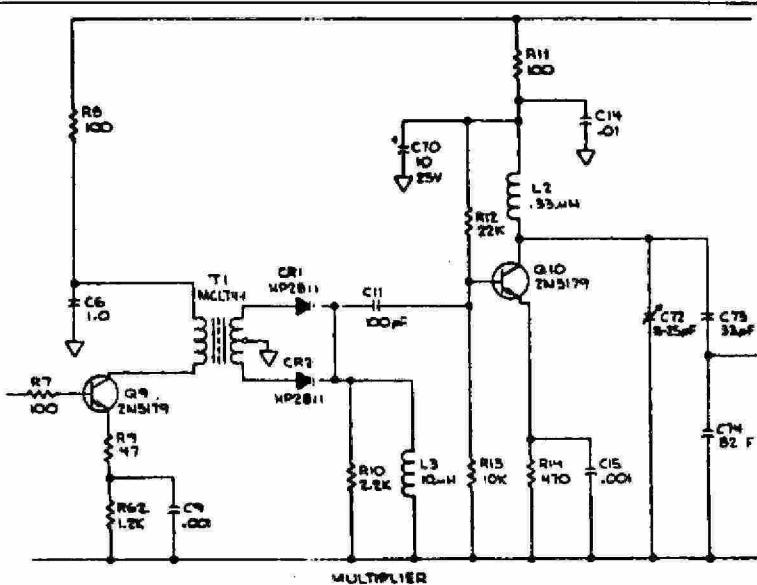


FIGURE 8-3. FIRST MULTIPLIER

The 19.826250 MHz is applied to buffer amplifier Q9 which drives the primary of interstage transformer T1. The secondary of T1 is centertapped with a negative limiter, hot-carrier diodes CR1 and CR2, in each leg of its output. The resulting signal is a full-wave rectified signal on the base of Q10 causing it to conduct twice for each cycle of the input. Q10 with its tuned output circuits then comprise a frequency doubler producing 39.6525 MHz through C73 to the second doubler stage. C72 is tuned for maximum amplitude of the 2X frequency.

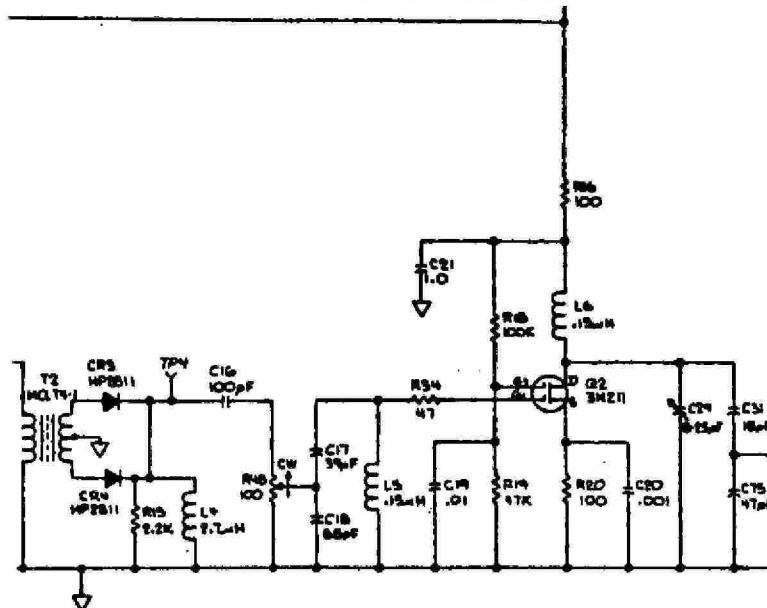


FIGURE 8-4. SECOND MULTIPLIER

The 39.6525 MHz from the first doubler is applied through T2 to the center-tapped secondary. Again there is a hot-carrier diode in each leg configured as a negative limiter. The resultant two positive half-cycles for each cycle of the input may be viewed at TP4 and is applied to the level control potentiometer R48 which is set for 3.5 to 4.5 volts peak-to-peak First Local Oscillator signal on the output of the card P704-1. The signal amplitude from R48 is applied to Q2. Q2 and its associated tuned circuits amplify and smooth the 79.305 MHz to a sinusoid. C24 is adjusted for maximum amplitude at 79.305 MHz.

The 79.305 MHz from the second doubler is applied past TP5 to an FET buffer amplifier. Gain in Q3 buffer stage is controlled by the potential on gate 2 which is set by a fixed voltage divider R21 and R22. The output of Q3 is maximized by C28 and the signal is applied to the high-level output stage Q11, a grounded base amplifier. The output of Q11 is peaked with C53 to the maximum 79.305 clean sine-wave output. This output is 3.5 to 4.5 volts peak-to-peak to the Receiver First Mixer. Notice in Figure 8-5 the extreme filtering of the input +15 volts regulated to minimize the noise in the output.

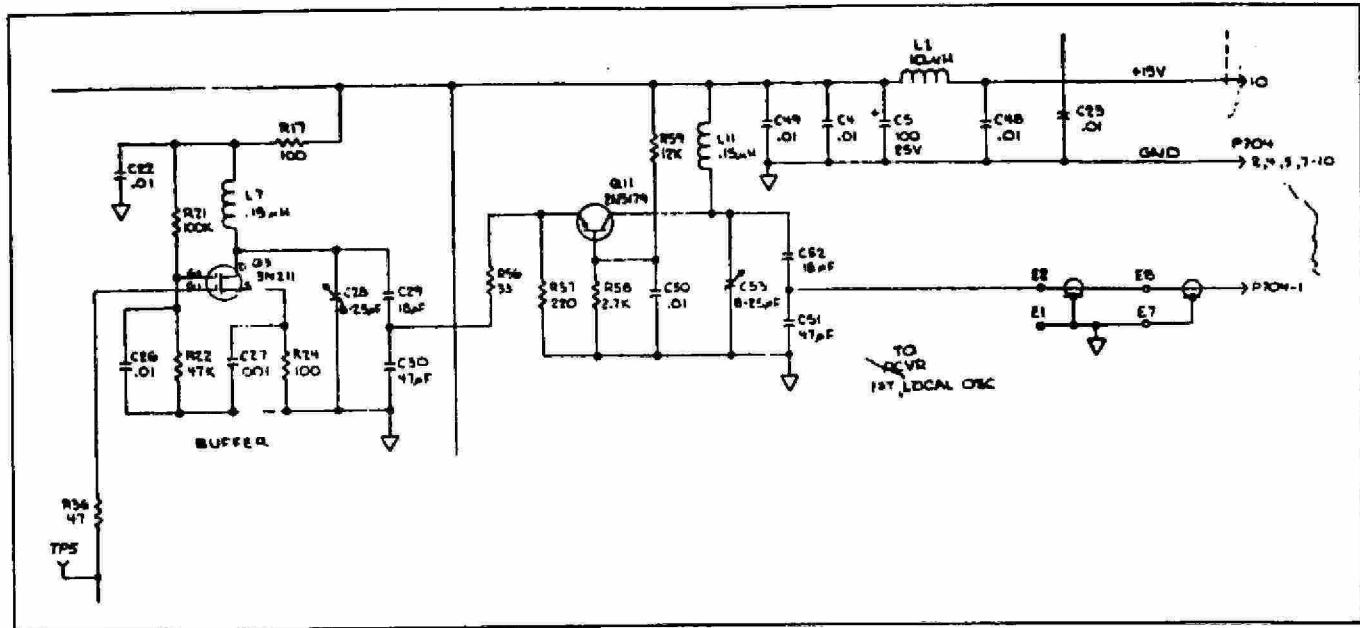


FIGURE 8-5. FIRST LOCAL OSCILLATOR OUTPUT

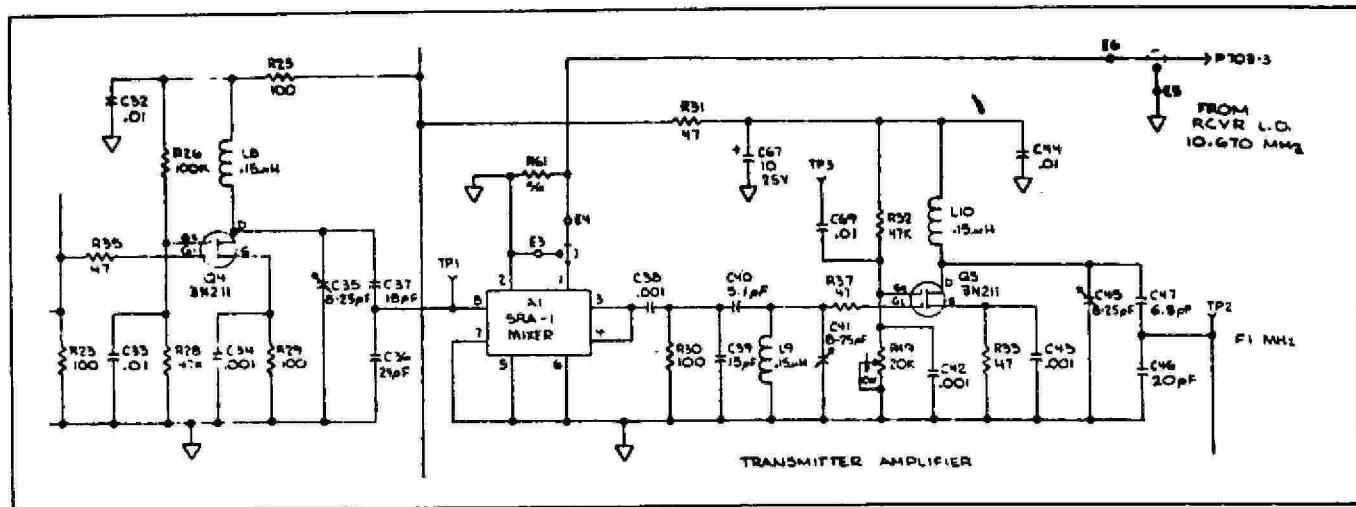


FIGURE 8-6. TRANSMITTER OUTPUT

The 79.305 MHz from the second doubler is also applied to buffer amplifier Q4. This stage's gain is fixed by the voltage on gate 2 which is determined by voltage divider R26 and R28. The output is maximized with C35 and applied to balanced mixer A1 and TP1.

The Second Local Oscillator signal generated on the Receiver PCB is applied at J703-3 to the other input of mixer A1. The amplitude of this input should be about 1.4 volts peak-to-peak.

The sum of these two frequencies, 89.975 MHz, is applied to output stage Q5. There are tuned circuits in both the input and output of Q5. Both C41 (input) and C45 (output) are tuned for maximum at TP2. R49 is the level set potentiometer which controls the gain of Q5 by varying the voltage on gate 2. This potentiometer is set to properly saturate the sample and its setting is

described in Section 8.3. The output is applied to the directional coupler for equal transmission to the probe receiver coil and to the 90 MHz RF preamplifier.

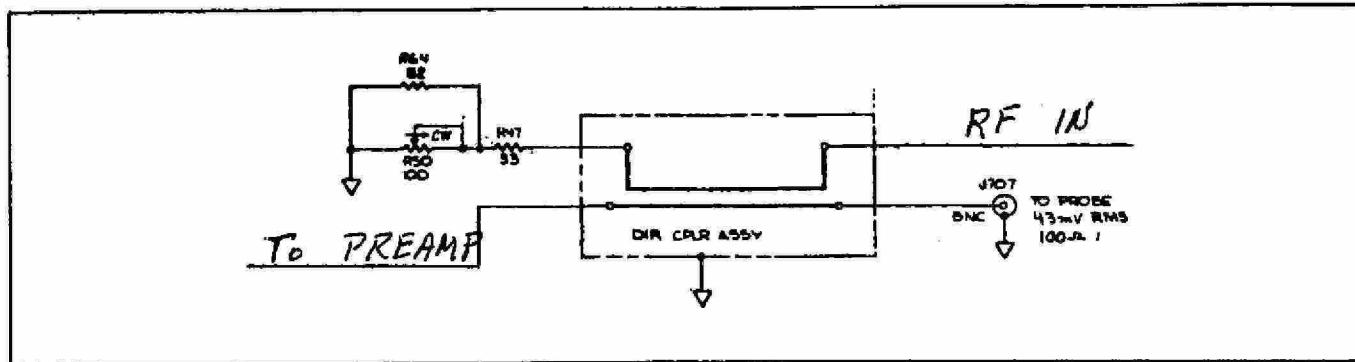


FIGURE 8-7. DIRECTIONAL COUPLER

The RF input is applied at 89.975 MHz to the directional coupler which is terminated in its characteristic impedance by the resistive network R47, R64, and potentiometer R50. When properly terminated, the coupler transmits equal amounts of signal to the probe through J707 and to the 90 MHz RF Preamplifier. NMR resonance is coupled from the probe to the RF Preamplifier at 90 MHz.

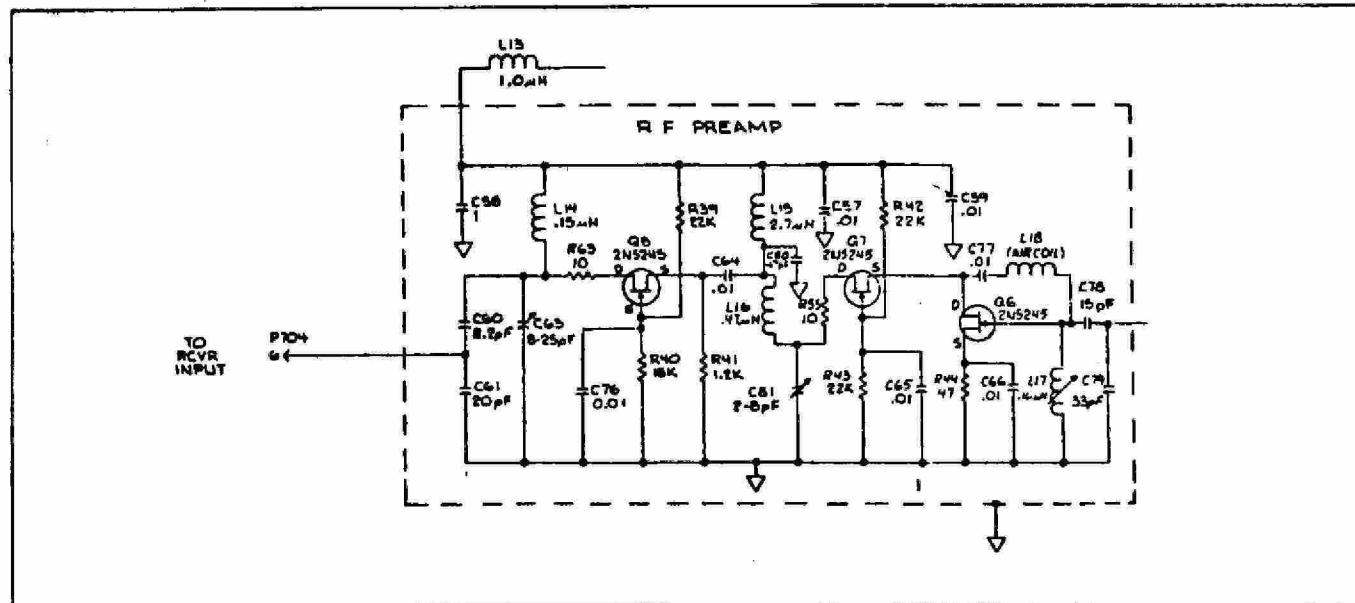


FIGURE 8-8. RF PREAMPLIFIER

The combined RF Transmitted signal and excited resonance signals are present in the input to Q6, the first element of a tuned cascode preamplifier stage. L17 tunes the input by matching the impedance of the incoming line from the directional coupler to the grounded source stage Q6. L17 tuning should not be attempted without a good vector impedance meter. Q6 and Q7 grounded gate stage make up the cascode amplifier with neutralization accomplished with C77 and L18. The output tank circuit of the cascode is tuned with C81 for maximum leakage on the front panel meter. Grounded gate stage Q8 provides further gain of the signals, both 89.975 MHz transmitted

and 90 MHz resonance, and is tuned by C63 for maximum signal on the LEAKAGE meter. The signals from the preamplifier are applied to the Receiver First Mixer.

8.3 TESTS AND ADJUSTMENTS

1. Connect a high frequency oscilloscope to TP4 and peak the signal for a maximum with C72.
2. Connect the oscilloscope to TP5 and peak the signal with C24.
3. Connect the oscilloscope to P704 pin 1.
 - a. Peak the signal with C28.
 - b. Peak the signal with C53.
 - c. Adjust R48 to obtain a 3.5 to 4.5 volts peak-to-peak signal amplitude.
4. Measure the frequency at P704 pin 1 with a high resolution frequency counter.
 - a. The frequency of this signal should be $79.305\text{ MHz} \pm 1\text{ KHz}$.
 - b. Adjust to this frequency with L102 in the crystal oscillator oven assembly.
5. Connect the oscilloscope to TP1 and peak the signal with C35.
 - a. The signal will be distorted and the tuning somewhat broad due to the non-linear input impedance of mixer A1.
 - b. The amplitude should be about 1.5 volts peak-to-peak.
6. Check the signal at pin 3 of J703 (E-6).
 - a. The frequency should be 10.670 MHz.
 - b. The amplitude is a minimum of 1.4 volts peak-to-peak.
7. Connect the oscilloscope to TP2.
 - a. Peak the signal with C41.
 - b. Peak the signal with C45.

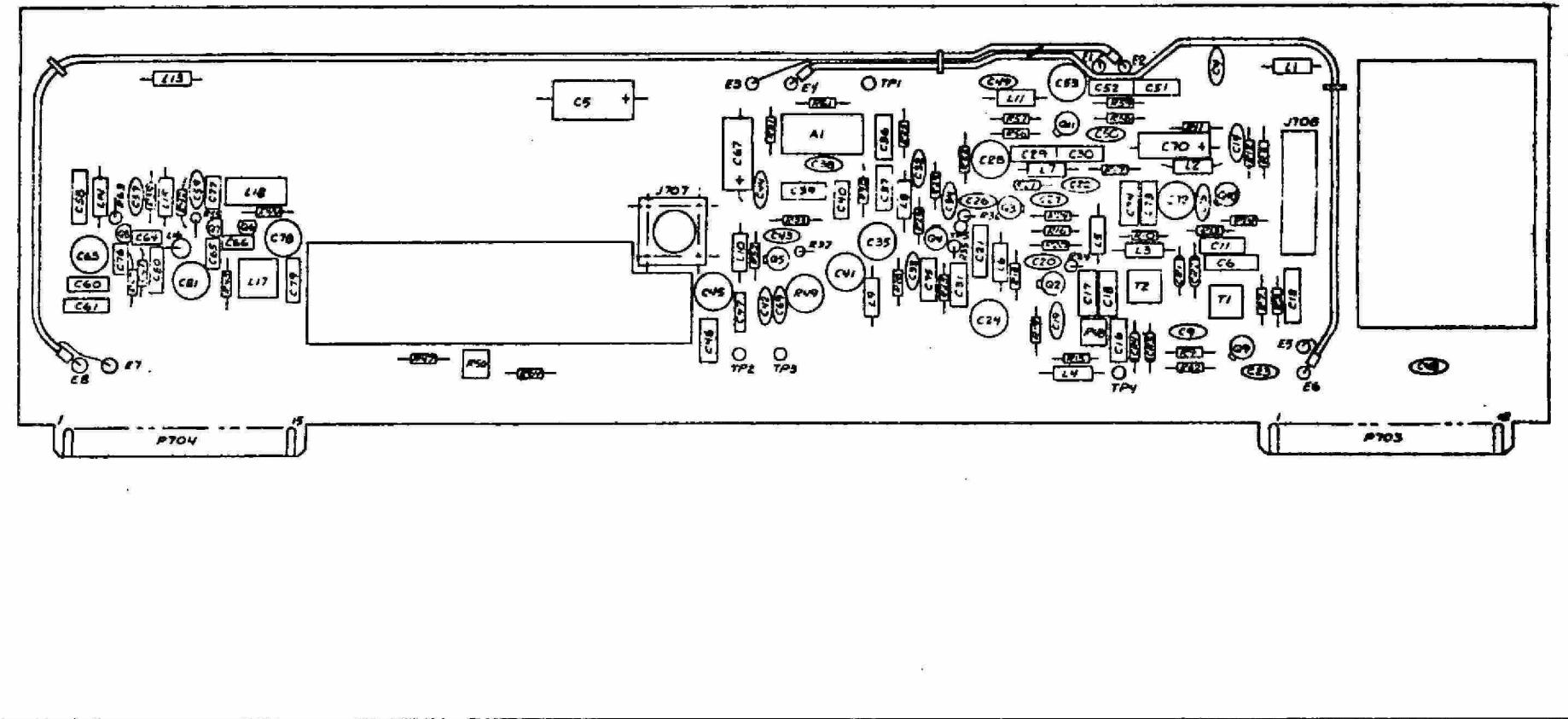


FIGURE 8-9. COMPONENT LAYOUT

- c. The signal should be 3 volts peak-to-peak or more with R49 fully clockwise.
8. Connect the oscilloscope to J707 and adjust R49 for 136 millivolts peak-to-peak.
- 8.4 PREAMPLIFIER TUNING**
- 1. Connect the oscilloscope to pin 6 of J704.
 - a. Peak the signal with C81.
 - b. Peak the signal with C63.
 - c. At the same time adjust R50 to keep the signal level below 0.5 volt RMS (1.4 volts peak-to-peak).
 - 2. L17 should not be touched without a vector impedance meter.
 - a. Remove the 7.6 volt supply from pin 1 of J703.
 - b. Connect the vector impedance meter to J707.
 - c. Set the vector impedance meter to 90 MHz.
 - d. Adjust L17 to obtain an impedance of 450 ohms \pm 200 ohms at 0° phase angle.
 - e. Remove the vector impedance meter and reconnect the +7.6 volts to pin 1 of J703.
 - 3. Observe the LEAKAGE Meter on the front panel (or P704 pin 6) and adjust R50 for minimum amplitude.
 - 4. Readjust R49 for the following.
 - a. Observe the 5 percent ethyl benzene sample quartet.
 - b. The sample quartet should saturate at an RF dial setting of 0.16 ± 0.4 mG.
 - 5. Repeat steps 3. and 4. as often as required.
 - 6. The temperature of the cover of the inner oven should be $45^\circ\text{C} \pm 3^\circ\text{C}$.

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SECTION 9.0

19 RF TRANSMITTER/RF PREAMPLIFIER

9.1 FUNCTION

A crystal controlled oscillator generates the basic frequency of 18.496320 MHz which is multiplied by 4 to produce the First Local Oscillator signal of 73.98528 MHz.

This signal is mixed with 10.670 MHz (Second Local Oscillator signal from the Receiver) to produce the transmitted signal of 84.655 MHz.

An 84.68 MHz RF Preamplifier on this card amplifies the resonance signal and is connected to the probe through the directional coupler.

9.2 THEORY OF OPERATION

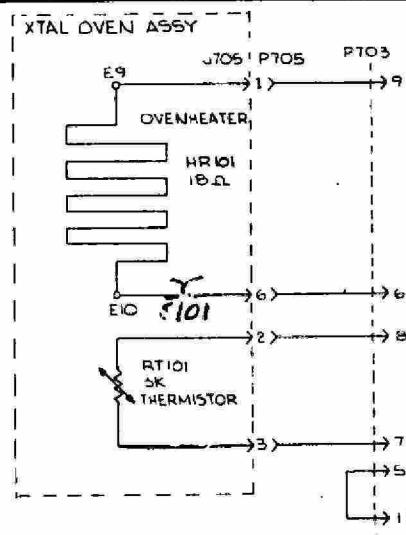


FIGURE 9-1. 18.496320 MHz OSCILLATOR

Vcc for the oscillator is the 7.6 volts DC produced on the Receiver PCB applied through P703-1 to J705-7. The oscillator is tuned by the selection of Y101 and the adjustment of L102 for 18.496320 MHz. The oscillator is in an oven assembly to enhance frequency stability.

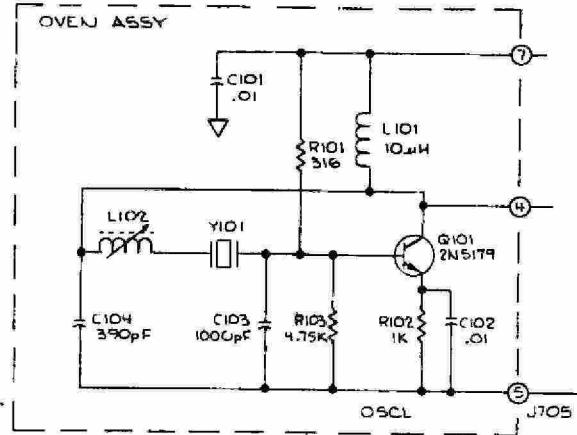


FIGURE 9-2. OSCILLATOR OVEN ASSEMBLY

The negative coefficient thermistor sensor for temperature control of both transmitter and receiver ovens is located on the First Transmitter which is the transmitter in use at any given time. The oven heater is in series with the temperature controller output on the Receiver, the receiver oven heater, and either the Second Transmitter (the one not in use, if installed) or a dummy load simulating the Second Transmitter. A fuseable link thermal switch is in series with the heater at P705-6. If the temperature exceeds 70°C, the link opens and the switch must be replaced. The short circuit between J703 pins 5 and 11 is used when this card is in the Second Transmitter slot to disable the dummy load and replace it with this oven heater. If only one transmitter is installed the lack of this short enables the dummy load automatically.

The 18.496320 MHz is applied to buffer amplifier Q9 which drives the primary of interstage transformer T1. The secondary of T1 is centertapped with a negative limiting hot-carrier diode CR1 and CR2 in each leg of its output. The resulting signal is a full-wave rectified signal on the base of Q10 causing it to conduct twice for each cycle of the input. Q10 with its tuned output circuits then comprise a frequency doubler producing 36.99264 MHz through C73 to the second doubler stage. C72 is tuned for maximum amplitude of the 2X frequency.

The 36.99264 MHz from the first doubler is applied through T2 to the center-tapped secondary. Again there is a hot-carrier diode CR3 and CR4 in each leg configured as a negative limiter. The resultant positive two half-cycles for each cycle of the input may be viewed at TP4 and is applied to the level control potentiometer R48 which is set for 3.5 to 4.5 volts peak-to-peak First Local Oscillator signal on the output of the card P704-1. The signal amplitude from R48 is applied to Q2. Q2 and the associated tuned circuits amplify and smooth the 73.985 MHz to a sinusoid. C24 is adjusted for maximum amplitude at 73.985 MHz.

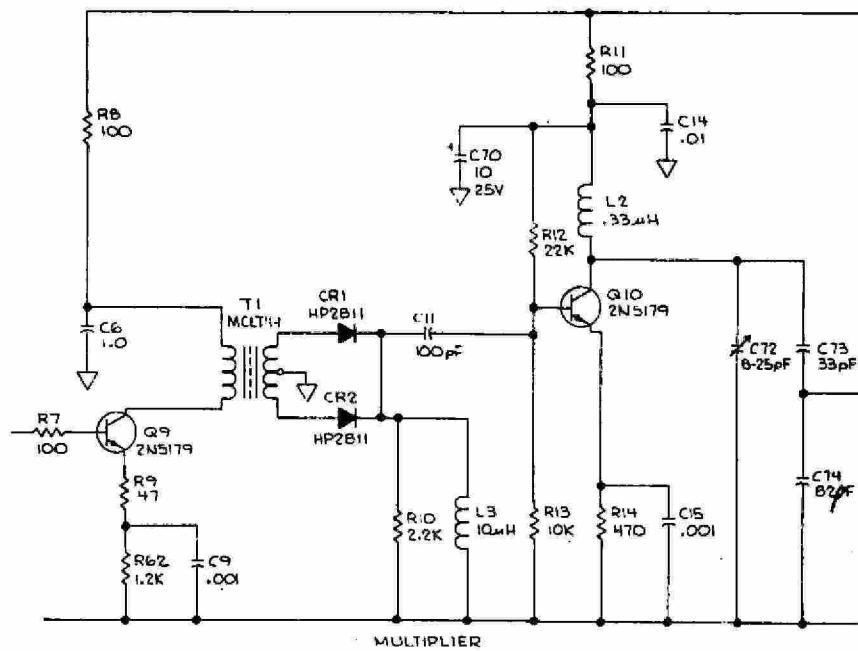


FIGURE 9-3. FIRST DOUBLER

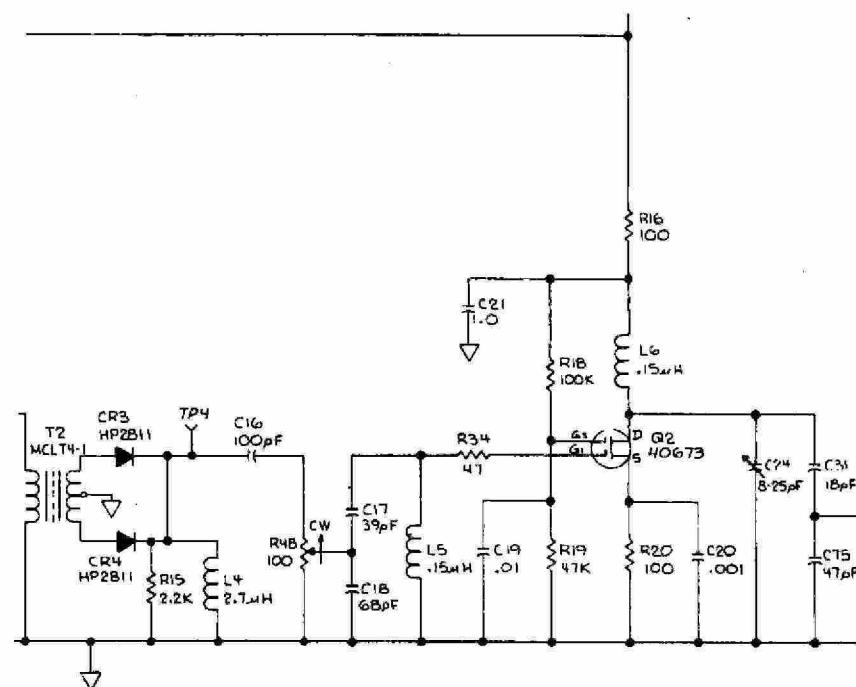


FIGURE 9-4. SECOND DOUBLER

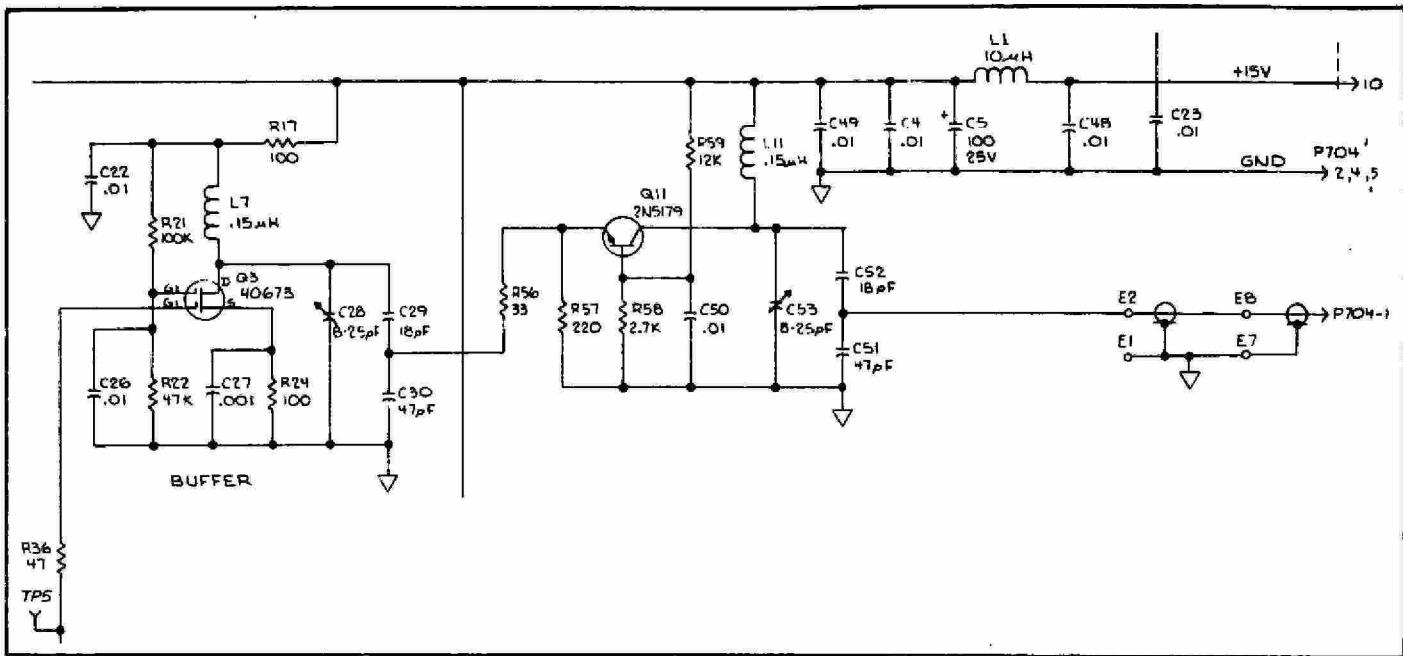


FIGURE 9-5. FIRST LOCAL OSCILLATOR OUTPUT

The 73.985 MHz from the second doubler is applied past TP5 to a FET buffer amplifier. Gain in Q3 buffer stage is controlled by the potential on gate 2 which is set by a fixed voltage divider R21 and R22. The output of Q3 is maximized by C28 and the signal is applied to the high-level output stage Q11, a grounded base amplifier. The output of Q11 is peaked with C53 to the maximum 73.985 MHz clean sine-wave output. This output is 3.5 to 4.5 volts peak-to-peak to the Receiver First Mixer. Notice in Figure 9-5 the extreme filtering of the input +15 volt regulated supply to minimize the noise in the output.

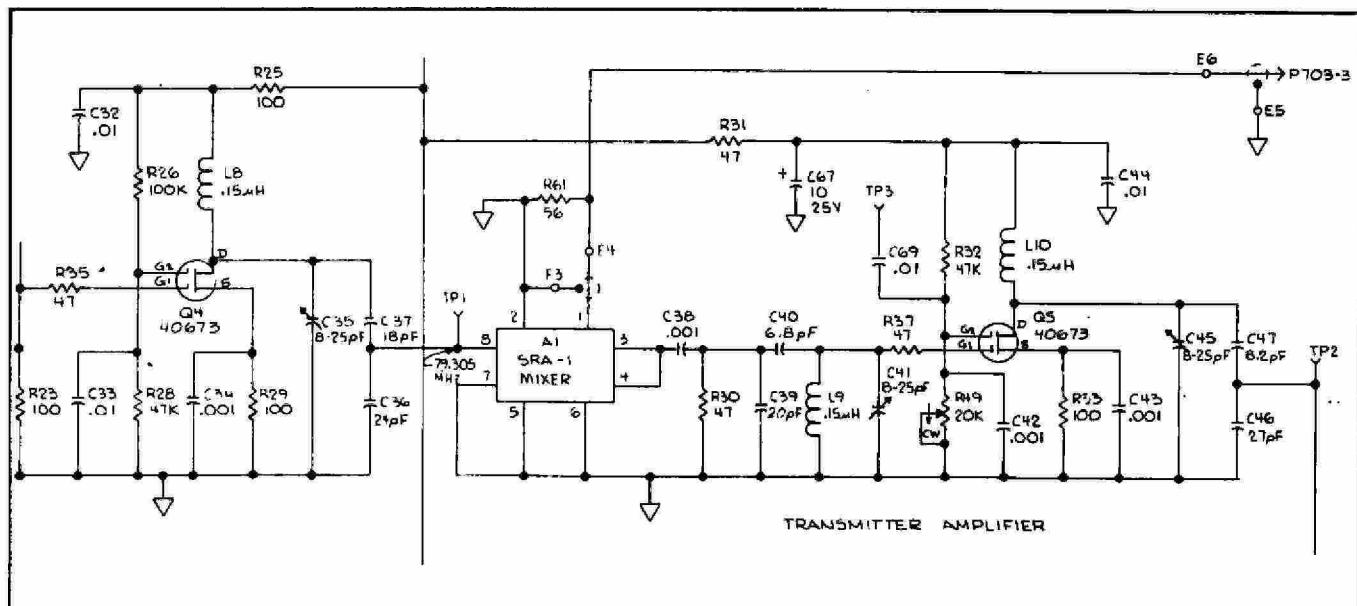


FIGURE 9-6. TRANSMITTER OUTPUT

The 73.985 MHz from the second doubler is also applied to buffer amplifier Q4. This stage's gain is also fixed by the voltage on gate 2 which is determined by voltage divider R26 and R28. The output is maximized with C35 and applied to balanced mixer A1 at TP1.

The Second Local Oscillator signal generated on the Receiver PCB is applied at J703-3 to the other input of mixer A1. The amplitude of this input should be about 1.4 volts peak-to-peak.

The sum of these two frequencies, 84.655 MHz, is applied to the output stage Q5. There are tuned circuits on both the input and output of Q5. Both C41 (input) and C45 (output) are tuned for maximum at TP2. R49 is the level set potentiometer which controls the gain of Q5 by varying the voltage on gate 2. This potentiometer is set to properly saturate the sample and the procedures for setting it is outlined in Section 9.3. The output is applied to the directional coupler for equal transmission to the probe receiver coil and to the 84.68 MHz RF Preamplifier.

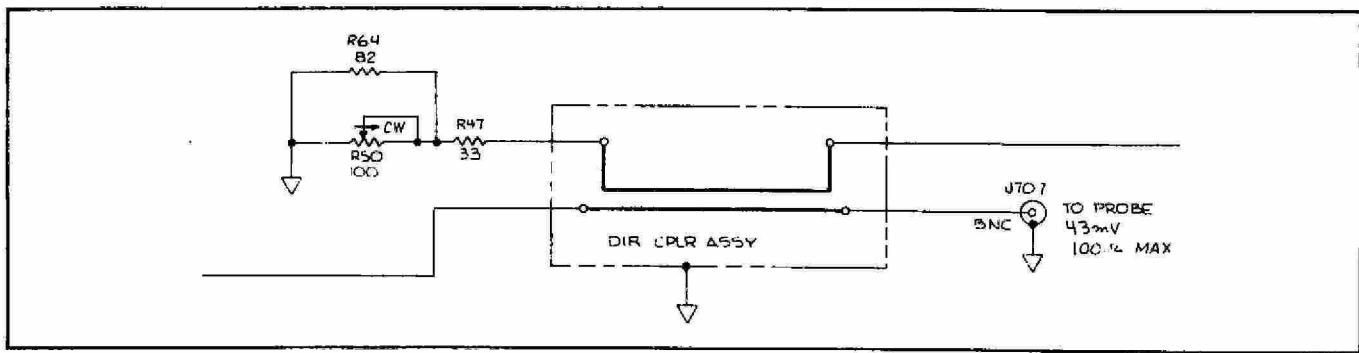


FIGURE 9-7. DIRECTIONAL COUPLER

The RF input is applied at 84.655 MHz to the directional coupler which is terminated in its characteristic impedance by the resistive network R47, R64, and potentiometer R50. When properly terminated, the coupler transmits equal amounts of signal to the probe through J707 and to the 84.68 MHz RF Preamplifier. NMR resonance at 84.68 MHz is coupled from the probe to the RF Preamplifier.

The combined RF Transmitted signal and the excited resonance signals are present in the input to Q6, the first element of a tuned cascode preamplifier stage. L17 tunes the input by matching the impedance of the incoming line from the directional coupler to the grounded source stage of Q6. Q6 and Q7 grounded gate stage make up the cascode amplifier with neutralization accomplished with C77 and L18. The output tank circuit of the cascode is tuned with C81 for maximum leakage on the front panel meter. Grounded gate stage Q8 provides further gain for the signals, both 84.655 MHz transmitted and 84.680 MHz resonance, and is tuned for maximum signal on the LEAKAGE meter. The signals from the preamplifier are applied to the Receiver First Mixer.

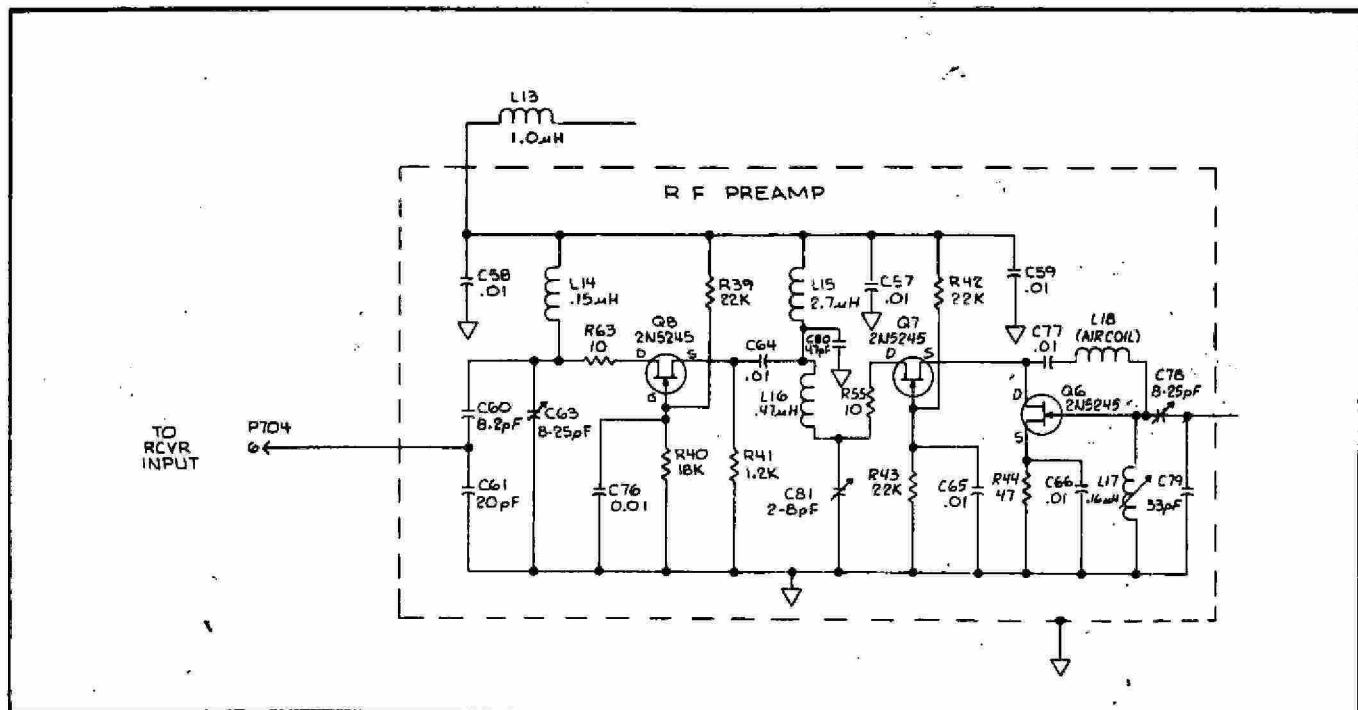


FIGURE 9-8. RF PREAMPLIFIER

9.3 TESTS AND ADJUSTMENTS

See Figure 9-9 for part locations.

1. Connect a high frequency oscilloscope to TP4 and peak the signal for a maximum with C72.
2. Connect the oscilloscope to TP5 and peak the signal with C24.
3. Connect the oscilloscope to P704 pin 1.
 - a. Peak the signal with C28.
 - b. Peak the signal with C53.
 - c. Adjust R48 to obtain a 3.5 to 4.5 volts peak-to-peak signal amplitude.
4. Measure the frequency at P704 pin 1 with a high resolution frequency counter.
 - a. The frequency of this signal should be 73.98528 MHz \pm 1 KHz.

L-6

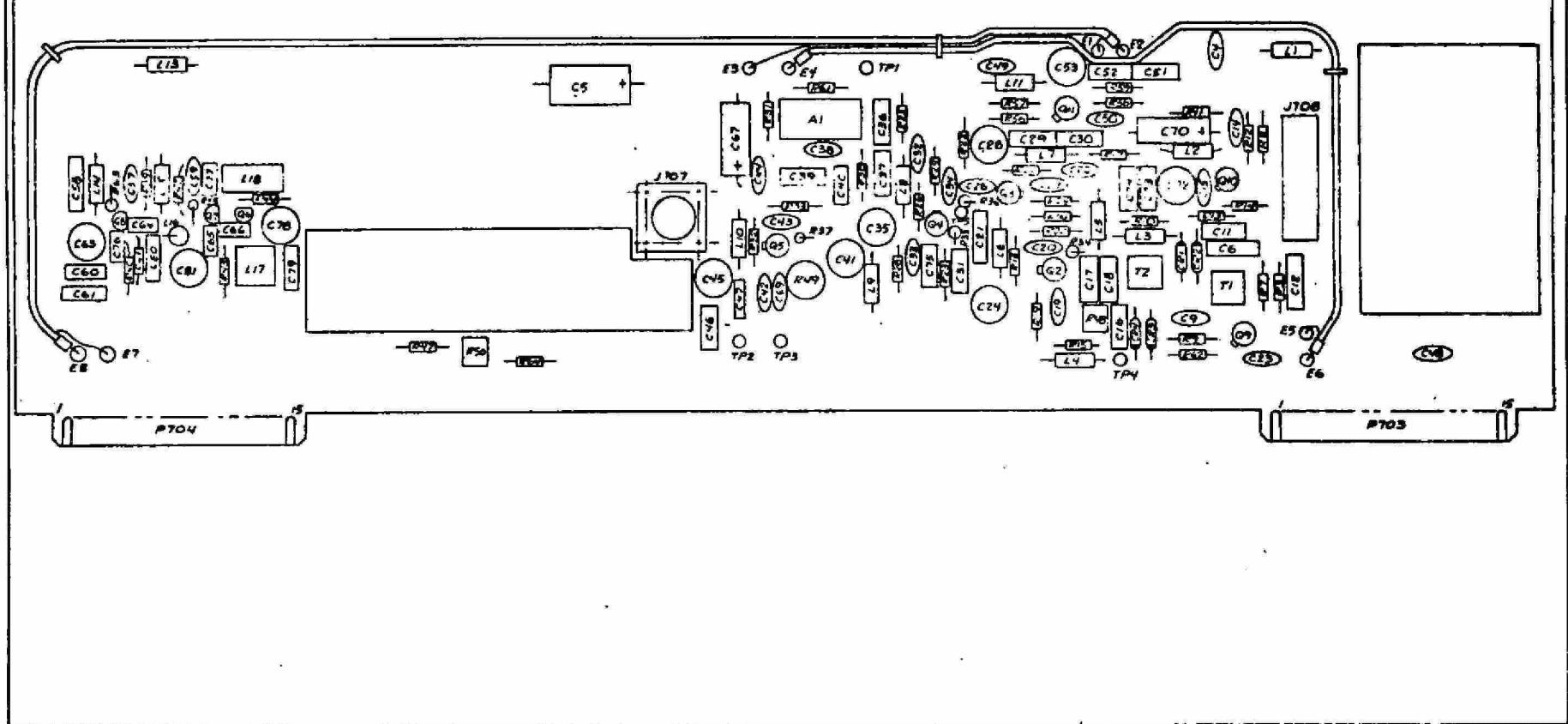


FIGURE 9-9. PARTS LAYOUT

- b. Adjust L102 in the crystal oscillator oven assembly for this frequency.
5. Connect the oscilloscope to TP1 and peak the signal with C35.
 - a. This signal will be distorted and the tuning somewhat broad due to the non-linear input impedance of mixer A1.
 - b. The amplitude should be about 1.5 volts peak-to-peak.
6. Check the signal at pin 3 of J703 (E-6).
 - a. The frequency should be 10.670 MHz.
 - b. The amplitude is a minimum of 1.4 volts peak-to-peak.
7. Connect the oscilloscope to TP2.
 - a. Peak the signal with C41.
 - b. Peak the signal with C45.
 - c. The signal should be 3 volts peak-to-peak or more with R49 fully clockwise.
8. Connect the oscilloscope to J707 and adjust R49 for 136 millivolts peak-to-peak.

9.4 PREAMPLIFIER TUNING

1. Connect the oscilloscope to pin 6 of J704.
 - a. Peak the signal with C81.
 - b. Peak the signal with C63.
 - c. At the same time adjust R50 to keep the signal level below 1.4 volts peak-to-peak.
2. L17 should not be touched without a vector impedance meter available.
 - a. Remove the 7.6 volt supply from pin 1 of J703.
 - b. Connect the vector impedance meter to J707.
 - c. Set the vector impedance meter to 84.7 MHz.

- d. Adjust L17 to obtain an impedance of 450 ohms \pm 200 ohms at 0° phase angle.
 - e. Remove the vector impedance meter and reconnect the +7.6 volts to pin 1 of J703.
- 3. Observe the LEAKAGE meter on the front panel (or monitor P704 pin 6) and adjust R50 for minimum amplitude.
- 4. Readjust R49 for the following:
 - a. Observe the 5 percent ethylbenzene sample quartet.
 - b. The sample quartet should saturate at an RF POWER setting of 0.16 \pm 0.4 mG.
- 5. Repeat steps 3. and 4. as often as required.
- 6. The temperature of the cover of the inner oven should be 45°C \pm 3°C.

SECTIONS 10-12 RESERVED FOR FUTURE ACCESSORIES WHICH ARE NOT NOW AVAILABLE.

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EM-390 TRAINING NOTES

SECTION 13.0
RECEIVER

13.1 FUNCTION

In order to fully understand the action of the receiver it is necessary to tie all frequencies generated in the EM-390 to the Frequency Consideration Diagram shown in Figure 13-1. This diagram was prepared by Walter Hofmann of VAG, ZUG, Switzerland for use in the European training program and is reprinted here with his permission.

In Section 5 we saw how the 25 KHz from the Field Modulator was generated and applied to the Modulation coils of the probe and the Observe Phase Detector as a reference.

10.670 MHz is generated in the Receiver as the Second Local Oscillator signal. This signal is applied to the transmitter for use in output frequency synthesis and to the Receiver Second Mixer for signal demodulation.

79.305 MHz (proton) is generated in the Transmitter as the First Local Oscillator signal. This signal is used in the transmitter output frequency synthesis and is applied to the Receiver First Mixer as the Local Oscillator input.

In the transmitter, the 10.670 and 79.305 MHz (proton) signals are mixed and the proton transmitted frequency becomes their sum or 89.975 MHz.

This signal irradiates a proton sample at the first lower frequency sideband of its resonance. The centerband of resonance f_0 is one modulation frequency above this point or 90.000 MHz which is also the Receiver tuned point. Also present is the first upper frequency sideband of 90.025 MHz which is centerband plus one modulation frequency. These three signals are present at the Receiver First Mixer signal input.

These frequencies mix with the First Local Oscillator signal and the difference frequency is taken to the output through a crystal filter. This filter is $10.7 \text{ MHz} \pm 15 \text{ KHz}$ for a 30 KHz band-pass. Only the 10.695 MHz is passed with no attenuation. 10.670 MHz (Transmitter-Local Oscillator) and 10.720 MHz (First Upper Sideband-Local Oscillator) are too far from the center of the filter to pass freely and are attenuated.

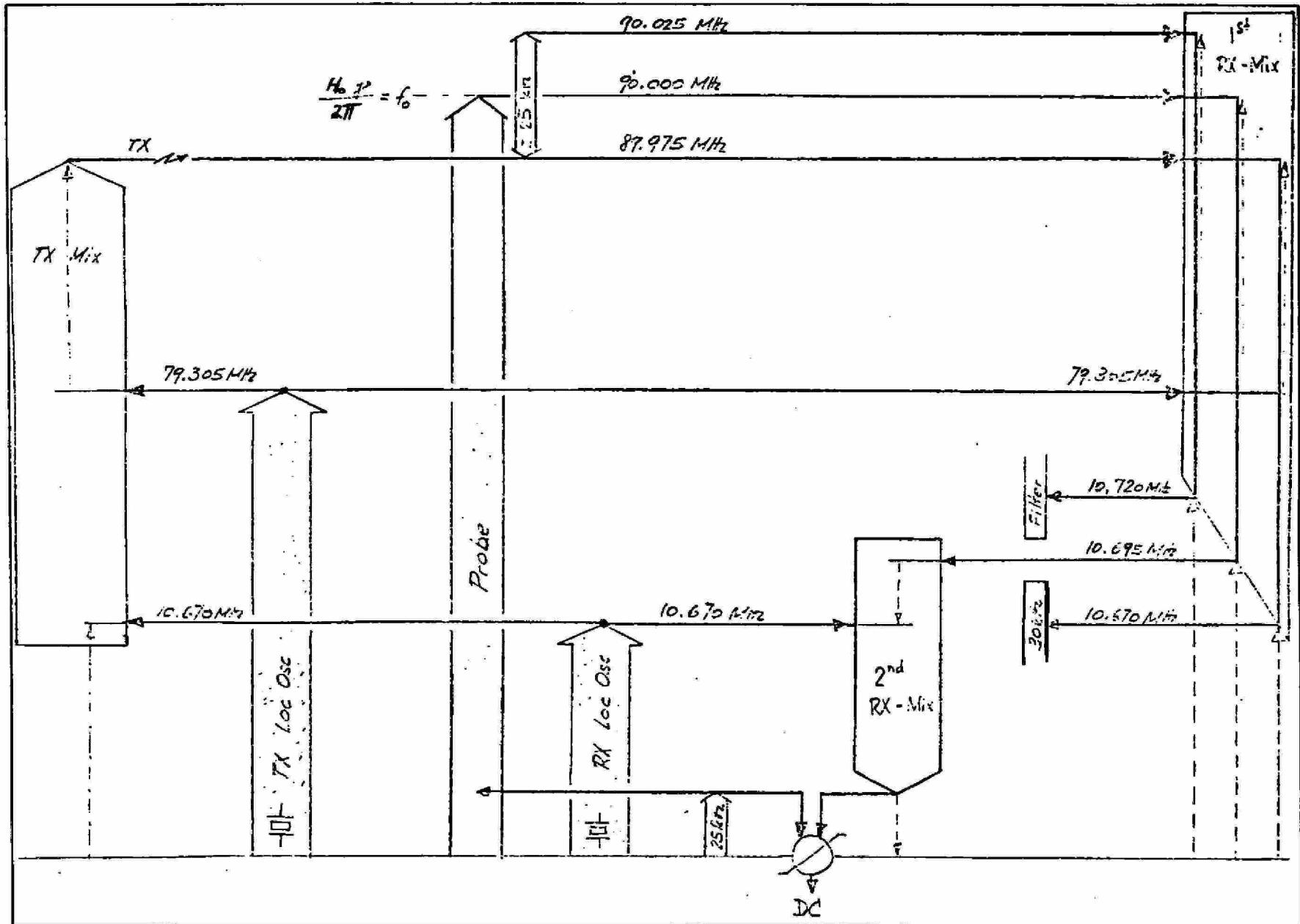


FIGURE 13-1. FREQUENCY CONSIDERATIONS

The 10.695 MHz is mixed with the 10.670 MHz to produce the 25 KHz audio for phase detection. The output of the phase detector is a varying DC level as the system sweeps through resonance.

13.2 THEORY OF OPERATION

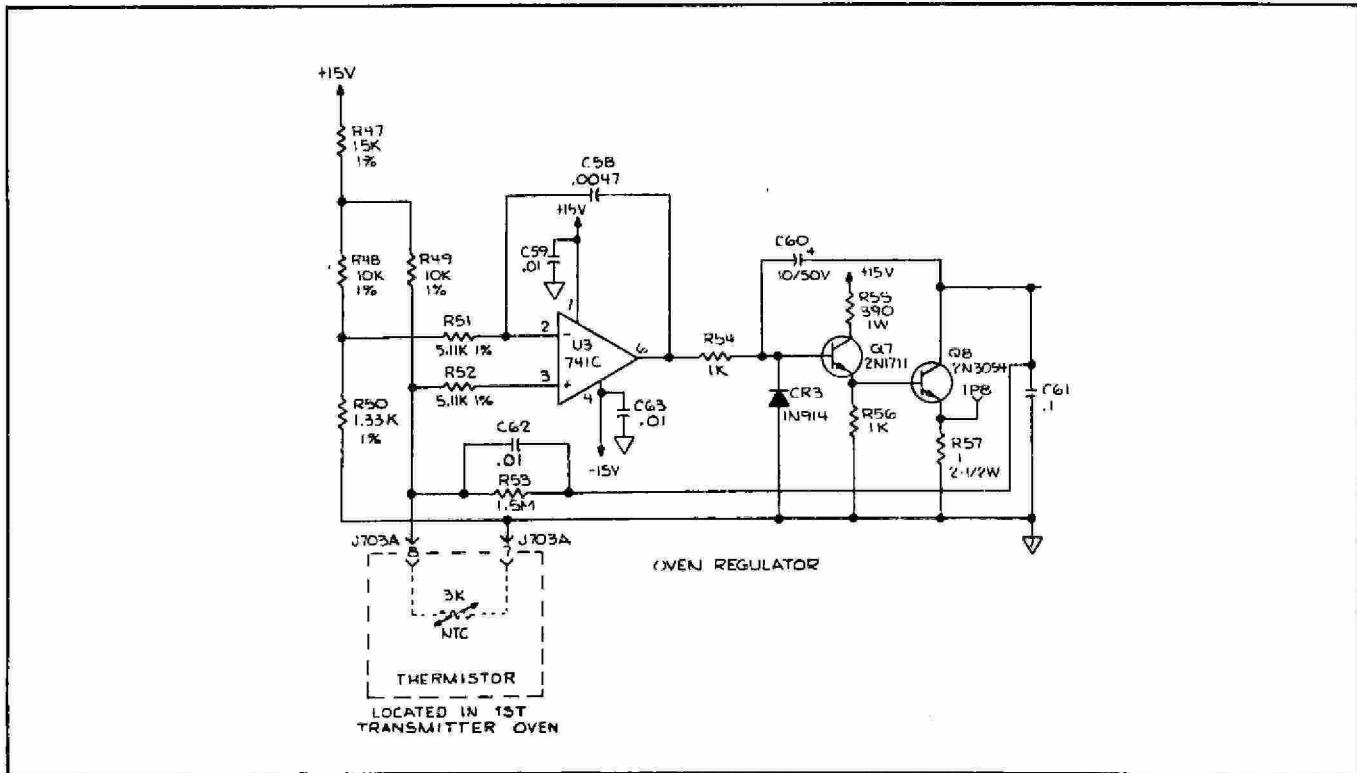


FIGURE 13-2. OVEN REGULATOR

The transmitter and receiver crystal oscillators are temperature stabilized by being placed in ovens with temperature regulation to about 0.1°C . The temperature controller electronics is physically on the Receiver PCB but the temperature sensor is located in the First Transmitter (particular transmitter in use) oven.

The negative temperature coefficient thermistor sensor connects to the Receiver through J703A pins 7 and 8 to a bridge circuit of R48, R50, R49, and the sensor resistance. Any imbalance in the bridge is amplified in U3 and applied to Q7. CR3 will prevent the base of Q7 from becoming excessively negative in the event of U3 failure. Q7 is a pass-gate driver which drives the pass-gate Q8. Current through Q8 flows through the heaters to +25 VDC. This circuit regulates within 0.1°C of the set point of $45^{\circ} \pm 3^{\circ}\text{C}$.

The regulator output current is first applied to the First Transmitter oven heater through J703A-9 and back to the Receiver oven through J703A-6. The Receiver oven is connected from pin 6 to pin 1 of J705. The current will then pass through the Second Transmitter oven heater or dummy load Q9 depending upon whether the Second Transmitter is installed in J703B.

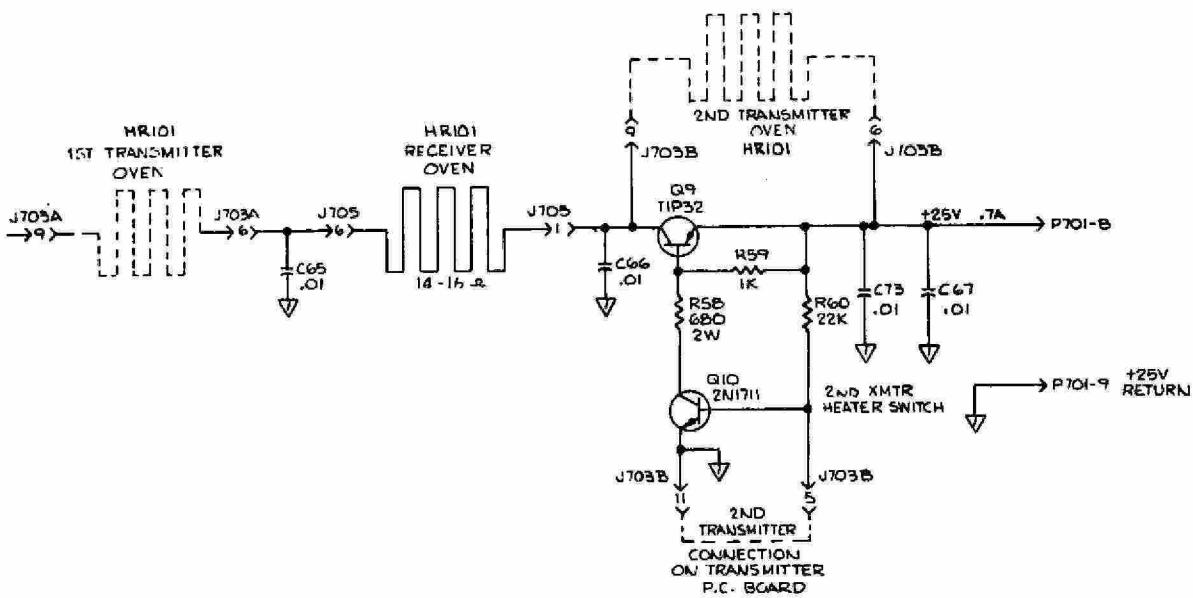


FIGURE 13-3. HEATER CIRCUITS

If the transmitter in J703B is in place, there is a jumper or short circuit across pins 1 and 5 of J703B. This cuts off Q10 (zero bias) which causes the base of Q9 to go to +25 volts (zero bias) cutting off Q9. The current then flows through the Second Transmitter oven heater keeping it warm and ready to use.

If the Second Transmitter is not installed, pins 11 to 5 of J703B are open. Q10 then turns on full (forward biased) dropping the voltage on the base of Q9 to about 16 volts which forward biases the stage so Q9 conducts. The current through Q9 is about the same as the current that previously went to the Second Transmitter oven heater.

+15 volts regulated is applied to a μ 723C integrated circuit voltage regulator U2. The circuit component selection in the regulator determines the value of the regulated voltage output. This is the oscillator Vcc for the First Transmitter crystal oscillator and the Receiver 10.670 MHz oscillator.

The 10.670 MHz oscillator depends on the value of crystal Y1 for its frequency and upon temperature regulation for its stability. The Vcc is the regulated +7.6 volts. The output is applied to an amplifier chain whose input is Q3.

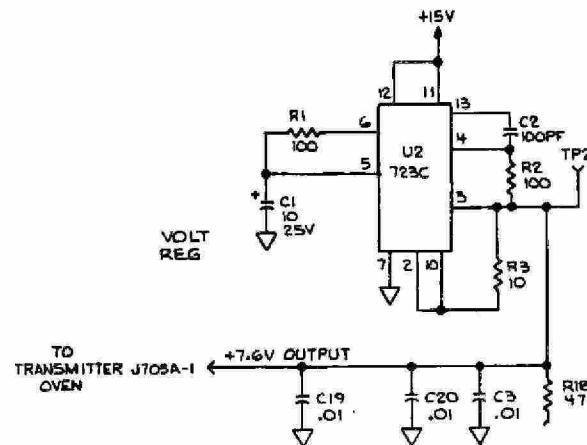


FIGURE 13-4. +7.6 VOLT REGULATOR

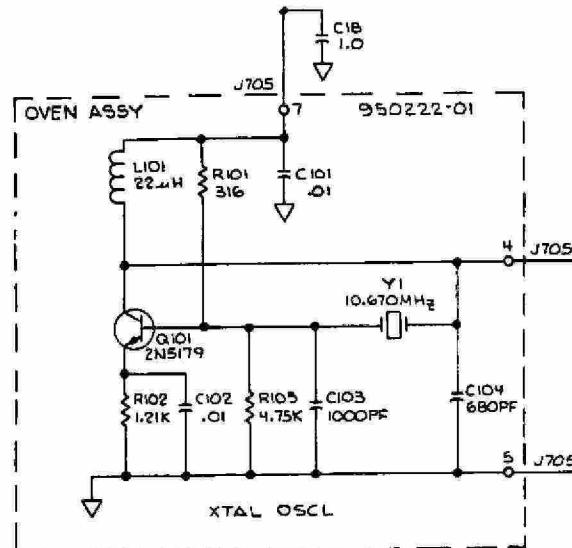


FIGURE 13-5. 10.670 MHz OSCILLATOR

The 10.670 MHz Oscillator signal is applied to emitter-follower Q3 which buffers the oscillator. R14 level set potentiometer is adjusted for 1.4 volts peak-to-peak from J703A-3 (E5) to ground. The wiper signal of R14 is applied to Low-Level output amplifier Q2 and to the High-Level input stage Q1.

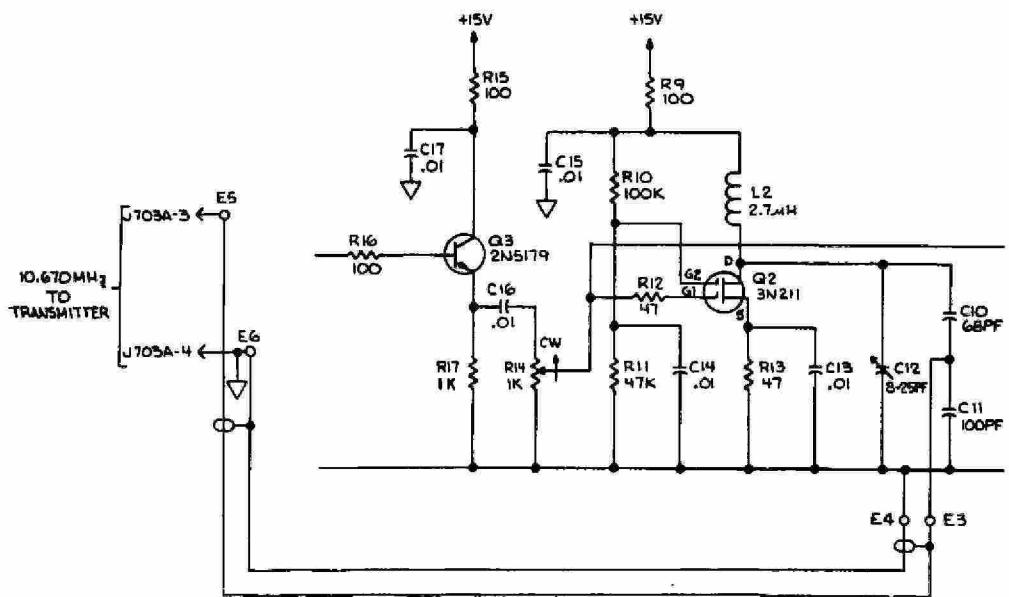


FIGURE 13-6. LOW LEVEL AMPLIFIER

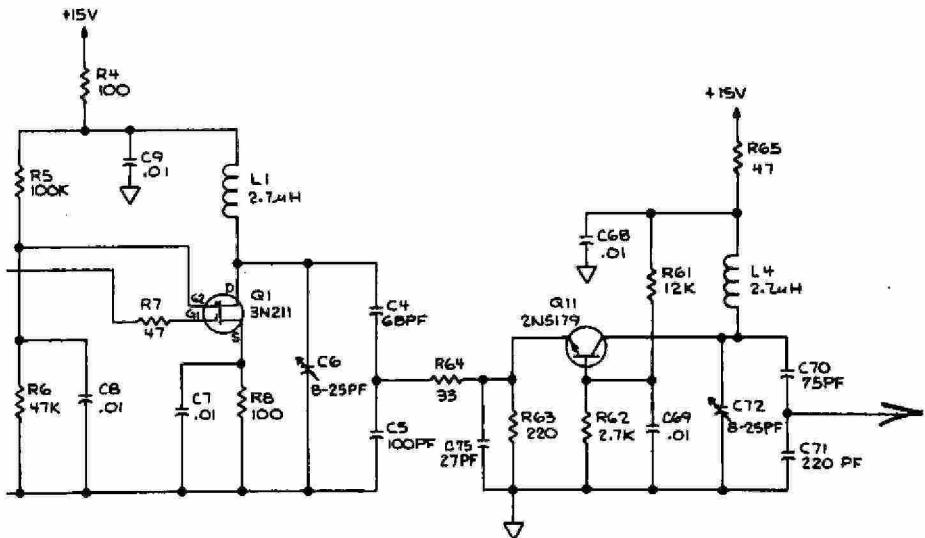


FIGURE 13-7. HIGH LEVEL AMPLIFIER

Q2 amplifies the Second Local Oscillator signal to 1.4 volts peak-to-peak and applies it to the First Transmitter through J703A-3. The gain of Q2 is fixed by the potential on gate 2 set by voltage divider R10 and R11. The output is maximized by adjusting C12.

The 10.670 MHz Second Local Oscillator signal as level set by R14 is applied to Q1 gate 1. Q1 amplifies the signal with a gain fixed by the potential on gate 2 determined by voltage divider R5 and R6. The signal is maximized by C6 and applied to grounded base output stage Q11. Q11 output is maximized by C72 and applied to the Receiver Second Mixer as reference.

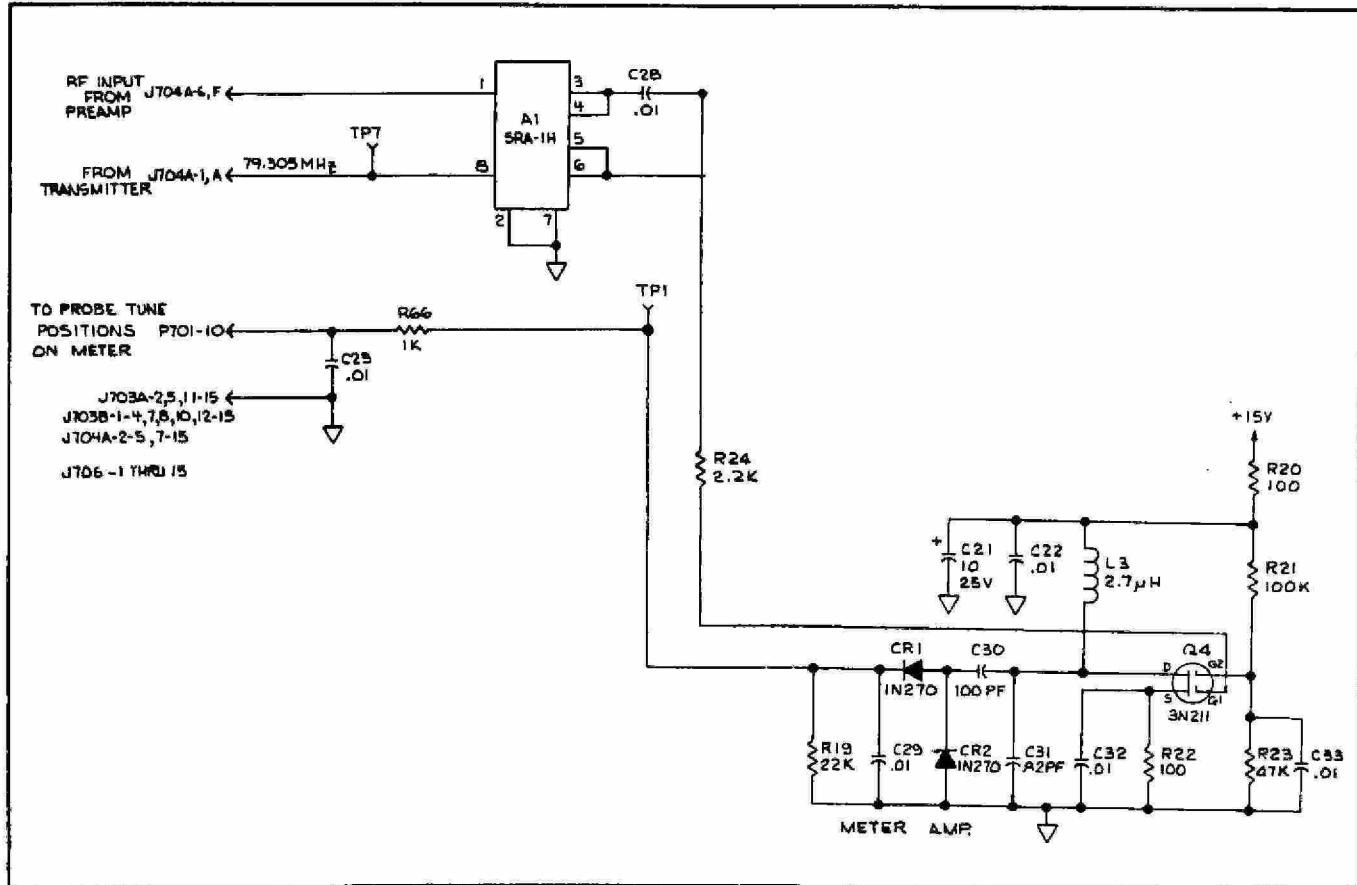


FIGURE 13-8. FIRST MIXER AND LEAKAGE CIRCUIT

The input from the RF Preamplifier contains the transmitted RF and the resonance signal. The First Local Oscillator input (79.305 MHz for proton) is applied to the Receiver First Mixer, A1. These two inputs to A1 produce the difference frequencies. The desired difference frequency is the 10.695 MHz resonance difference but the strongest signal is the 10.670 MHz difference between the Transmitter and the First Local Oscillator. This latter signal is the one read on the LEAKAGE meter.

The difference frequencies are applied to a FET amplifier Q4 where the signal is amplified. The gain of Q4 is governed by the potential on gate 2 with fixed voltage divider R21 and R23. The output of Q4 is detected by a positive detection circuit CR1 and CR2 with RC filtering. The DC output of this circuit is proportional to the signal from the First Mixer and is an indication of the tuning of the front end of the spectrometer.

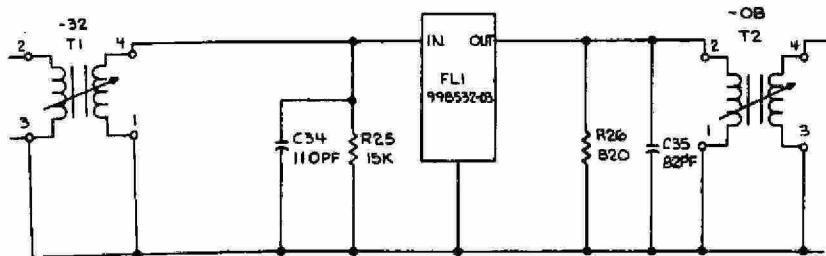


FIGURE 13-9. TUNED CRYSTAL FILTER

T1 is tuned to the desired difference frequency of 10.695 MHz. The crystal filter is tuned to 10.7 MHz \pm 15 KHz. The desired resonance sideband of 10.695 MHz is within this bandpass but all other sidebands are outside the range of the bandpass filter. The filtered output of FL1 is applied to tuned circuit T2, the input to the first IF amplifier.

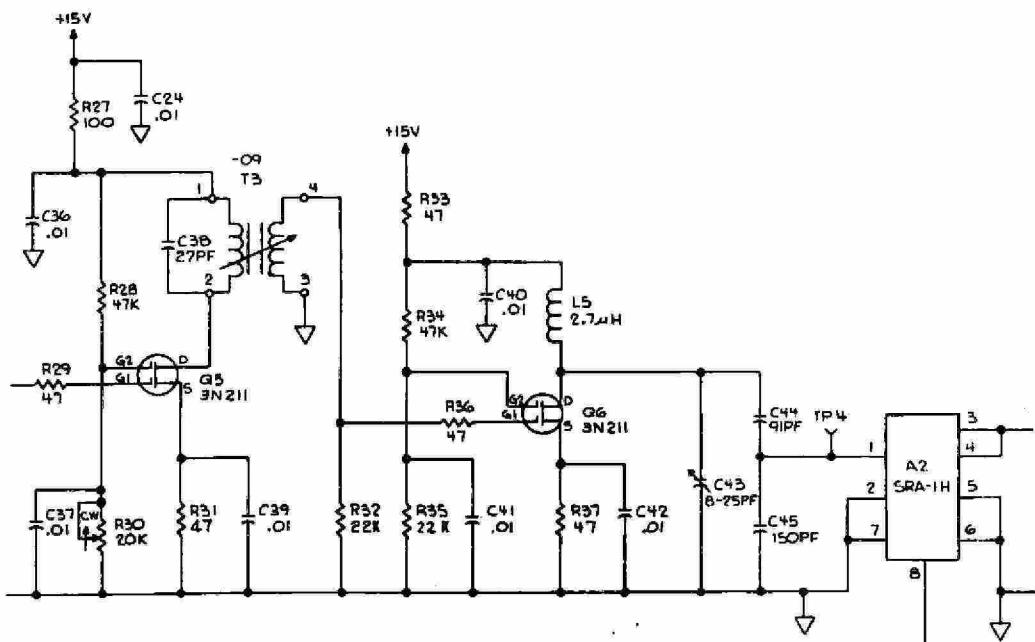


FIGURE 13-10. IF AND SECOND MIXER

The output of T2 is applied to IF Amplifier Q5 with IF gain controlled by R30. The output of Q5 is coupled across IF transformer T3 to the second IF Q6 where it is further amplified before being applied to the second mixer, A2. Also applied to A2 is the 10.670 MHz Second Local Oscillator signal. The difference frequency of 25 KHz is applied to the differential output amplifier.

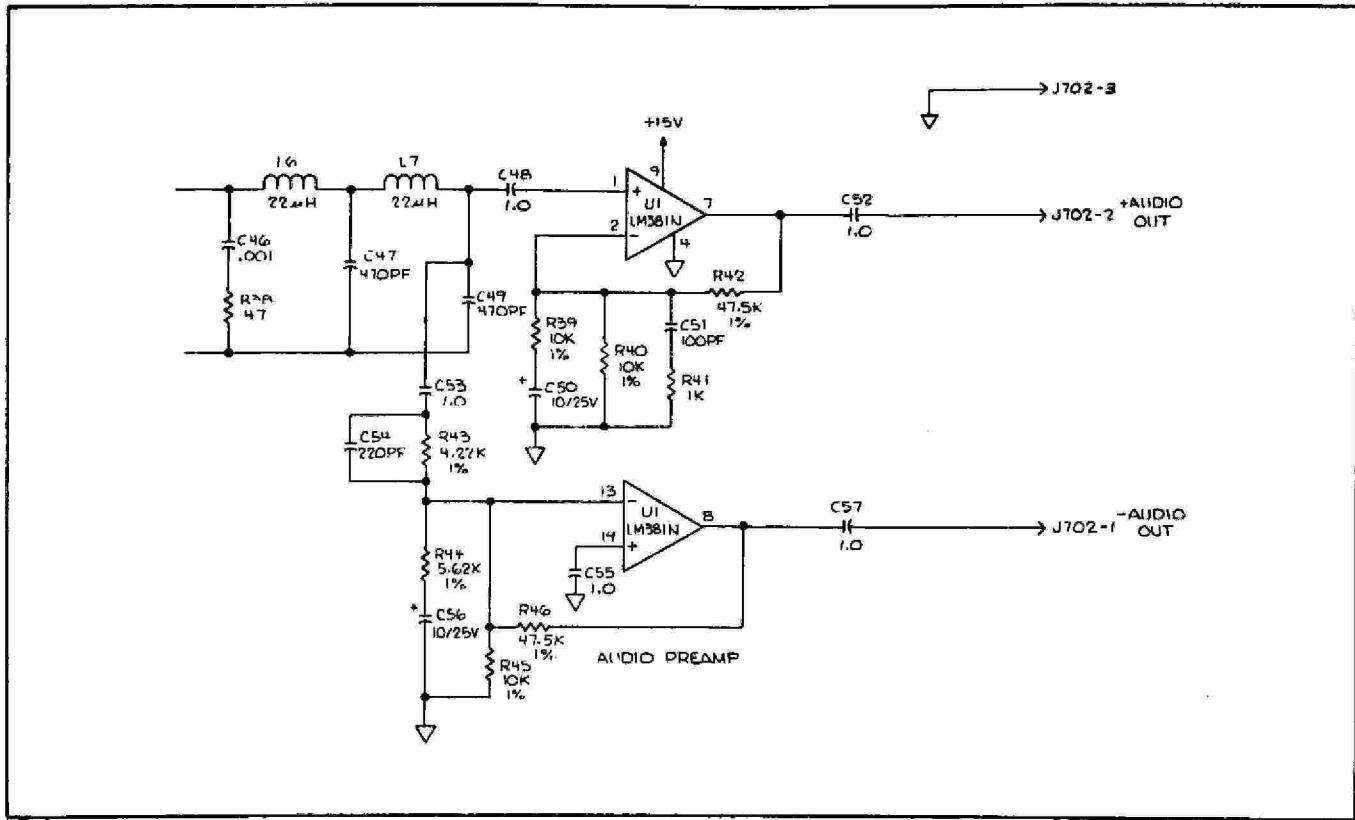


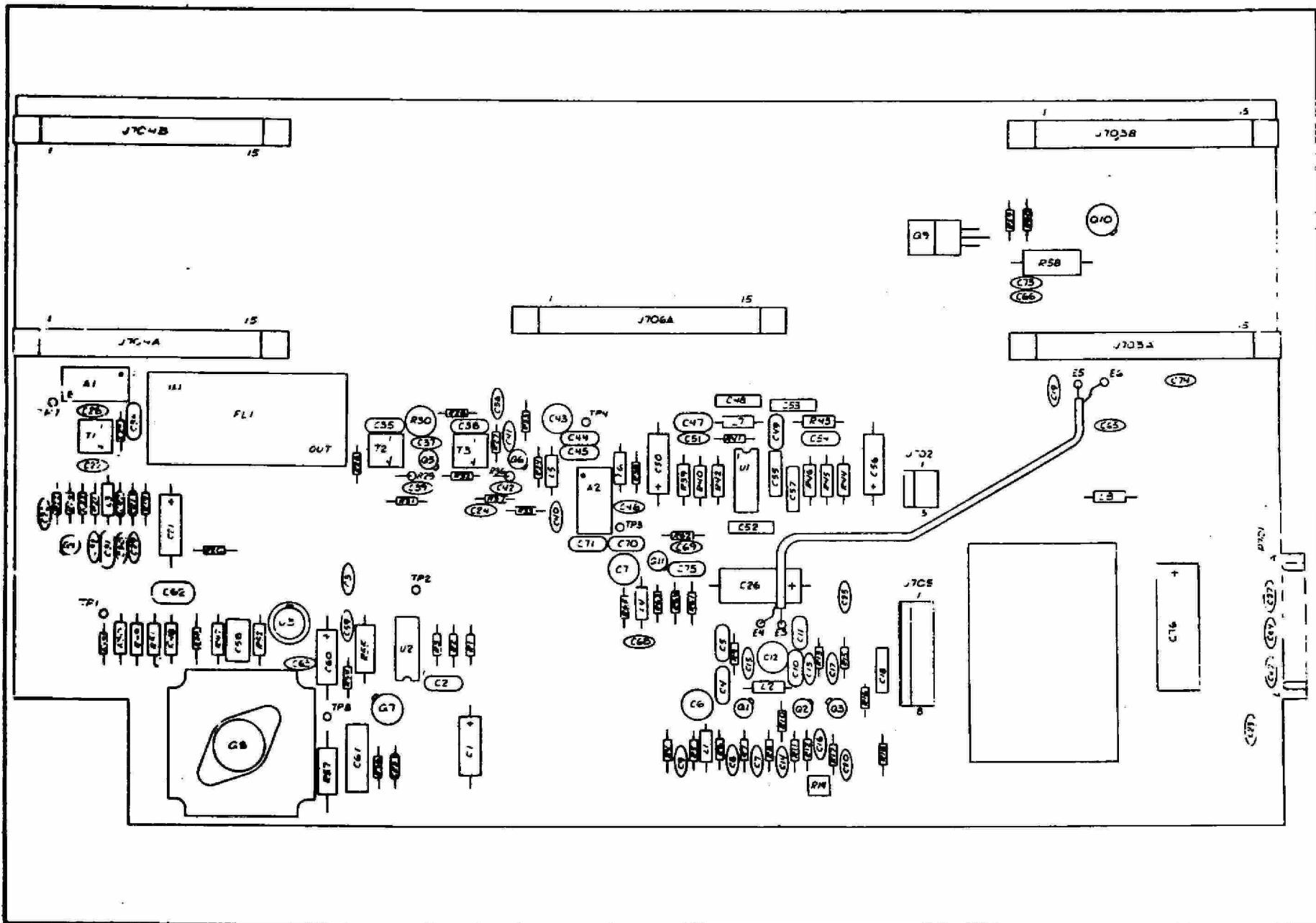
FIGURE 13-11. AUDIO OUTPUT

The output of the second mixer is applied to two operational amplifiers U1A and U1B. The signal to U1A is applied to the non-inverting input and to the inverting input of U1B. The outputs are complementary and applied to the Observe Channel Card.

13.3 TESTS AND ADJUSTMENTS

1. Measure the voltage from Voltage Regulator U2 at TP2. It should be 6.8 to 7.5 volts.
2. Measure the temperature of the inner oven. This temperature should be 43°C to 47°C.
3. Monitor J703A-3 with an oscilloscope and frequency counter.
 - a. The frequency should be 10.670 MHz.
 - b. Adjust C12 for maximum amplitude.
 - c. Set level to 1.4 volts peak-to-peak with R14.
4. Observe TP3 with an oscilloscope.

FIGURE 13-12. COMPONENT LAYOUT



- a. Peak the output with C6.
 - b. Peak the output with C72.
 - c. This output should be 2.5 to 3.5 volts peak-to-peak.
- 5. Monitor TP7 with an oscilloscope and frequency counter.
 - a. The amplitude should be 3.5 to 4.5 volts peak-to-peak.
 - b. The frequency should be
 - 1) 79.305 MHz for proton
 - 2) 73.985 MHz for fluorine.
- 6. Monitor J704A-6,F with an oscilloscope and frequency counter.
 - a. The amplitude of the signal measured will be that of the Transmitter signal — the NMR signal will be too weak to be measured.
 - b. The frequency will be:
 - 1) 89.975 MHz for proton
 - 2) 84.655 MHz for fluorine.
- 7. A sweep frequency generator is required to tune the IF strip.
 - a. Disconnect the input at J704A-6,F.
 - b. Insert the 90 MHz swept signal from the signal generator at J704A-6,F.
 - c. Connect an oscilloscope to J702 pin 2 and synchronize the display with the swept generator.
 - d. Adjust R30 for maximum output.
 - e. Adjust the following for maximum output with flat bandpass. The ± 3 dB points should be $10.7 \text{ MHz} \pm 0.015 \text{ MHz}$. T1, T2, T3, and C43.

f. Increase output signal until slipping is apparent at about 10 volts peak-to-peak.

g. Reduce sweep generator to 3 millivolts peak-to-peak.

h. Measure overall gain of the receiver:

$$\text{Gain} = 20 \log \frac{\text{midband signal (rms)}}{1 \text{ mV (rms)}}$$

= 55 dB minimum

= 562 voltage gain minimum.

i. Remove the swept generator and replace J704A-6,F.

8. Receiver Gain Adjustment

a. Insert the 2.55 Hz Water Sample in the probe and find the resonance signal in the Observe Channel.

b. Monitor the output at J702-2 of the receiver.

c. Sweep the magnet through resonance using the recorder and observe the oscilloscope.

d. Turn OBSERVE RF POWER to maximum.

e. Adjust R30 (receiver gain in IF strip) just below the point where a distorted or clipped pattern is seen on the oscilloscope as the magnet is swept through resonance.

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EM-390 TRAINING NOTES

SECTION 14.0
OBSERVE CHANNEL

14.1 FUNCTION

The Observe Channel receives the "audio" from the receiver, amplifies it, and applies it to the selected functions for LOCK, DC AMPLIFICATION, ACCESSORIES, INTEGRATION, or AMPLITUDE SET.

The switching for the various modes of operation is front panel controlled and is shown as each function is discussed.

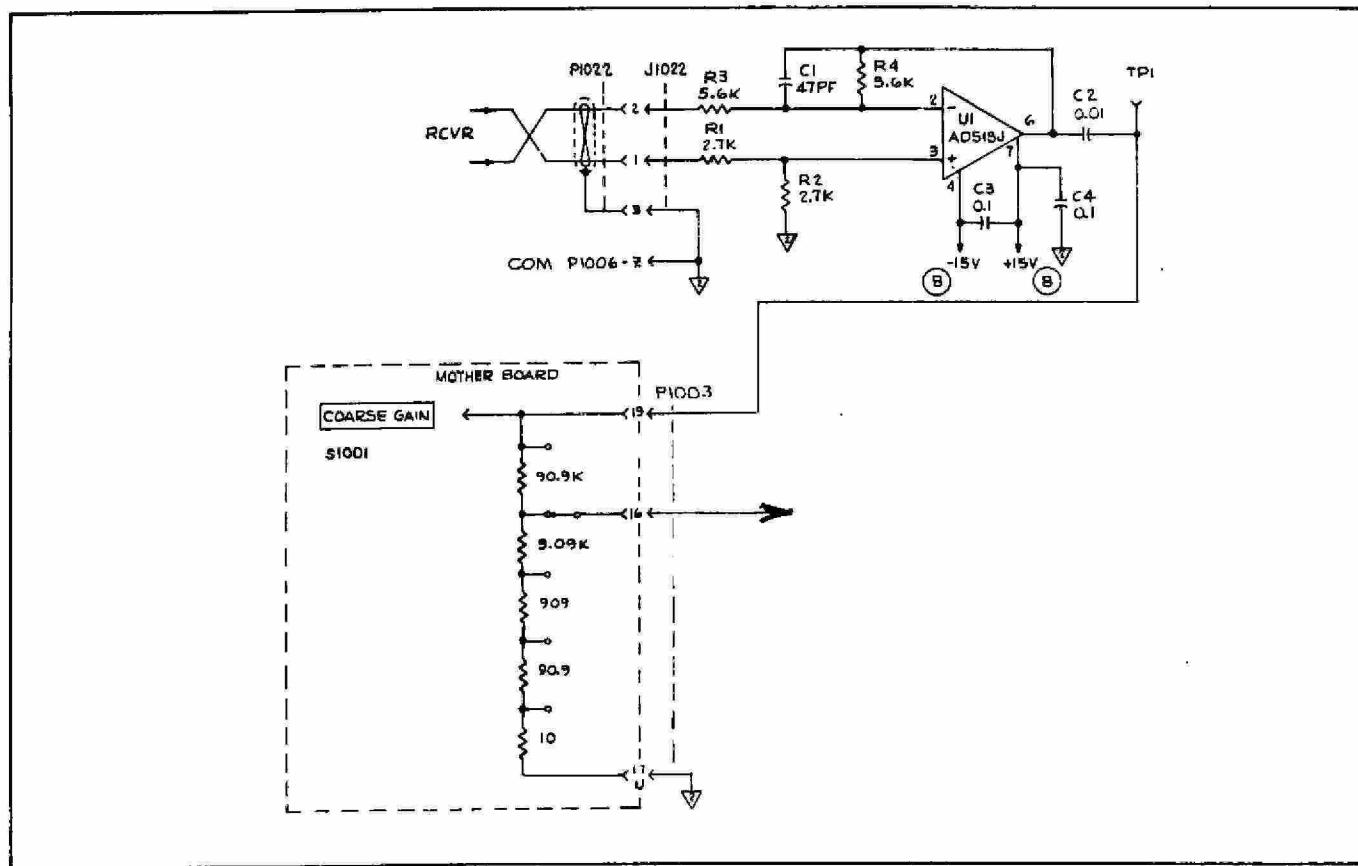


FIGURE 14-1. INPUT CIRCUITS

14.2 THEORY OF OPERATION

The 25 KHz Observe demodulated signals and the 20 to 30 KHz Lock demodulated signals are applied from the Receiver through J1022 to differential amplifier U1. The signals are in differential form (complementary output of the Receiver) and the single-ended output of U1 is applied to the step attenuator COARSE GAIN on the front panel. The output to the COARSE GAIN is also applied to the Lock Channel and is not attenuated by the divider. The attenuated signal is applied back to the Observe Channel.

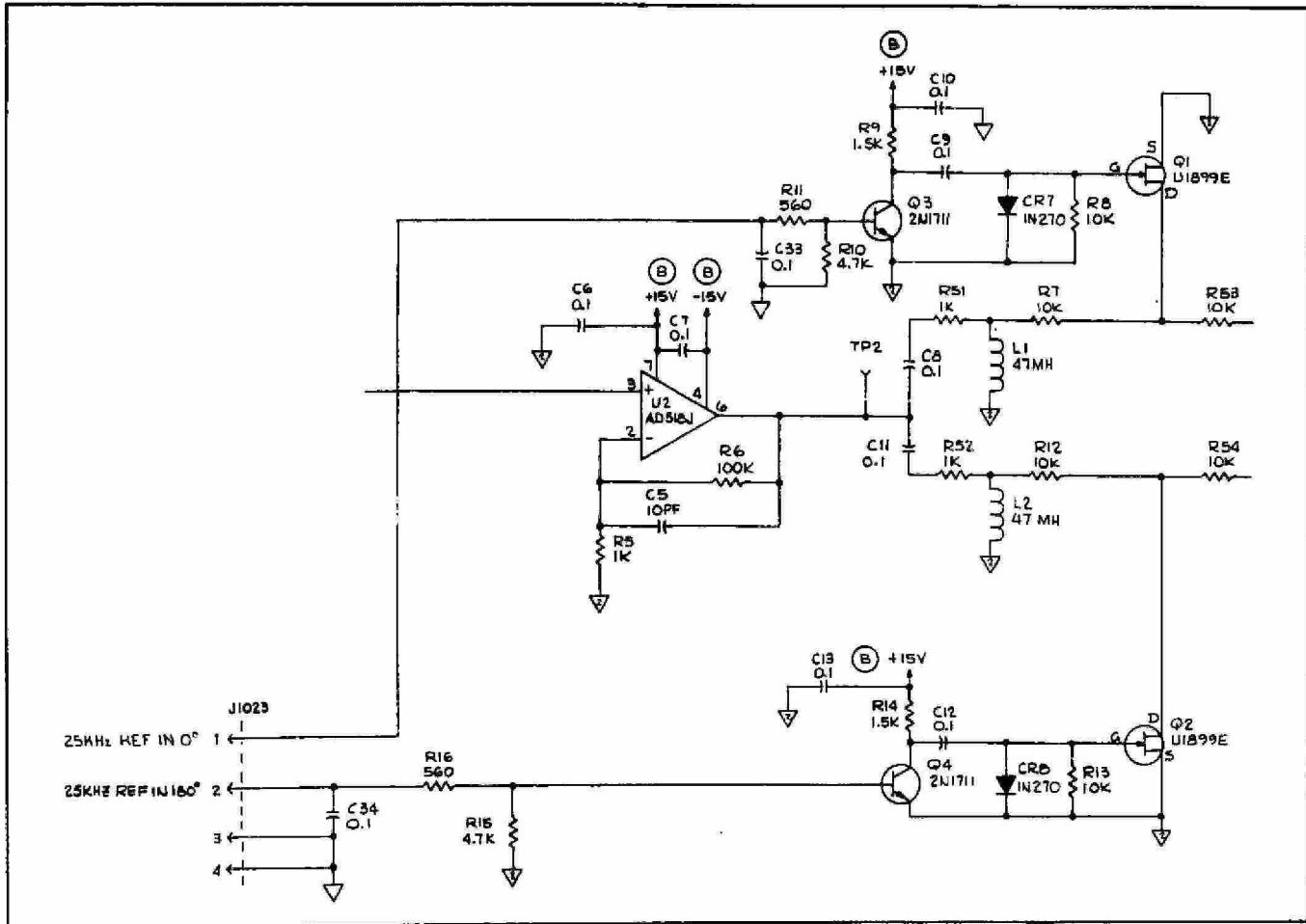


FIGURE 14-2. PHASE DETECTION

The attenuated signal from the COARSE GAIN control contains both 20 KHz to 30 KHz Lock data and the 25 KHz Observe data. The circuit of Figure 14-2 will phase detect the 25 KHz Observe data and all other inputs will be discarded. U2 amplifies the total input signal and applies it to the drains of FETs Q1 and Q2, each a half-wave phase detector operating in the absorption mode. The front panel OBSERVE PHASE control is rotated to set the reference phase to the proper point for purely absorption phase detection.

Recall that the reference phase inputs at J1023 from the Field Modulator are complementary square-waves from the Q and Q-bar outputs of a multivibrator. The square-waves are balanced in that they have 20 microseconds at +4 volts and 20 microseconds at 0 volts in each period. One phase of the input is applied to squaring amplifier Q3 which produces a 0 to 15 volt signal in its collector. This is applied to a clamp circuit consisting of C9, CR7, and R8 which clamps the positive peaks at +0.6 volt and sends the rest of the waveform negative. The +0.6 volt turns Q1 on full and the -14 volts turns Q1 off completely. During the time Q1 is on, ground is felt on the drain. Where Q1 is cut off, the half-cycle of information from U2 is allowed to pass. The LRC filter network then charges to the average value of the half-cycle and applies this signal to the output as a DC level to the inverting input of differential amplifier U3. The other phase of the reference input is applied to squaring amplifier Q4 which produces a 0 to 15 volt square-wave in its collector. This is applied to a clamp circuit consisting of C12, CR8, and R13 which clamps the positive excursion at +0.6 volt and sends the rest of the waveform negative. The +0.6 volt turns Q2 on full and the -14 volts turns Q2 off completely. During the time Q2 is on, ground is felt on the drain. When Q2 is off, the half-cycle of signal from U2 is allowed to pass. This is the alternate half-cycle of Q1's operation. The LRC filter network then charges to the average value of the half-cycle and applies this signal to the output of a DC level to the non-inverting input of differential amplifier U3.

In summary, for an input cycle of the 25 KHz, the 0° to 180° portion of the input sine-wave from U2 is passed and a DC level proportional to signal amplitude results and is amplified and inverted in U3. The 180° to 360° portion of the input sine-wave from U2 is passed and a DC level proportional to signal amplitude results which is amplified and not inverted in U3. In the output of U3 then the effect is of an amplified signal from a full-wave phase detector.

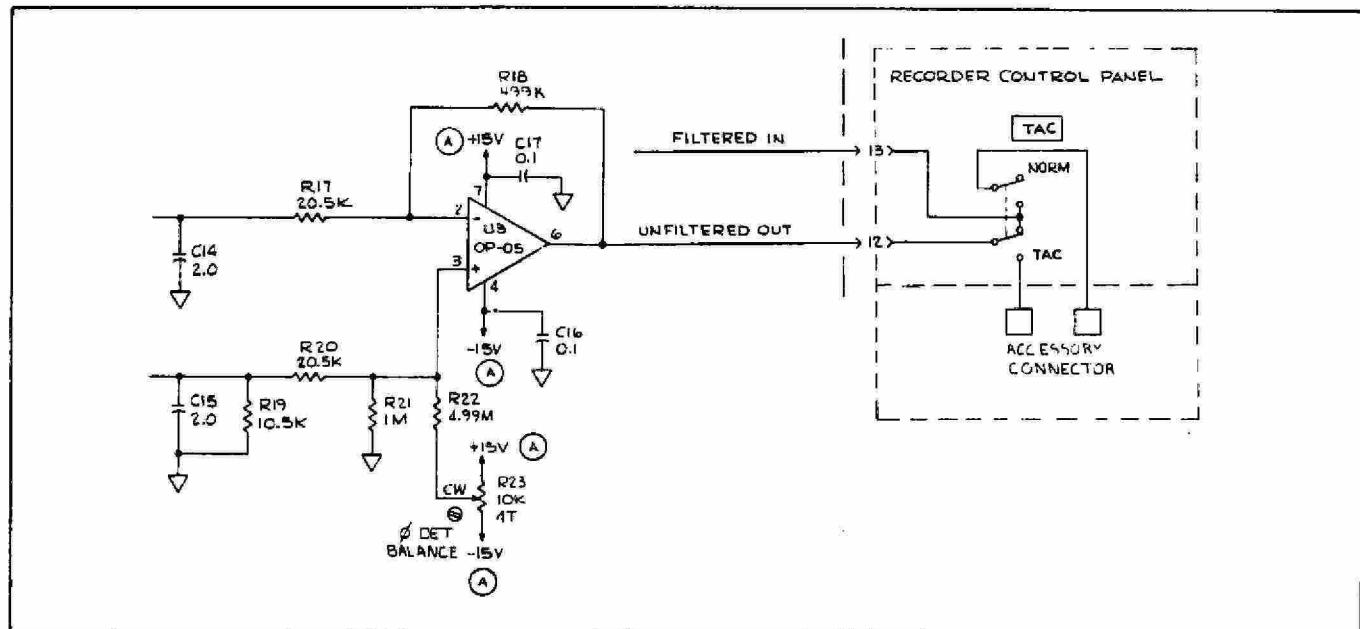


FIGURE 14-3. SIGNAL CONTROL

The half-wave phase detected signal from Q1 is applied to the inverting input of U3. The alternate half-wave phase detected signal from Q2 is applied to U3 non-inverting input. The DC level of the output is set by R23 for 0 volts out with both inputs zero. The combined output is applied through the TAC switch (also OSCILLOSCOPE switch) back to the card at pin 13 in NORMAL operation. In TAC or OSCILLOSCOPE modes the signal is also applied to the external time averaging computer or oscilloscope. The signal at pin 12, unfiltered output, is applied to the integrator circuits at pin 9 of the card in INTEGRATE mode.

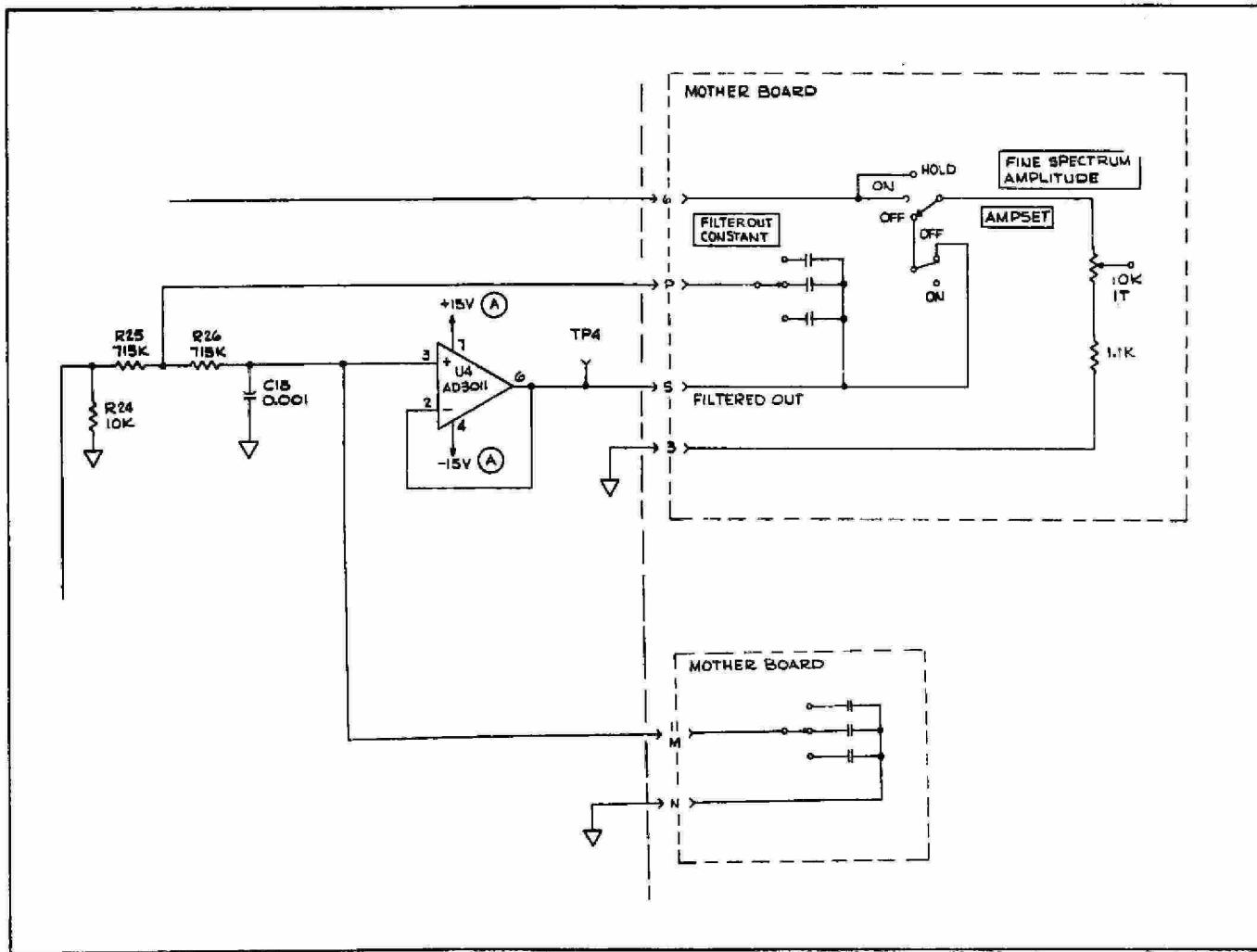


FIGURE 14-4. DC AMPLIFIER AND FILTER

The unfiltered phase detected signal is applied to U4 in the NORMAL mode. A seven position filter switch with capacity to ground supplies parallel filters to the input. An OPEN position allows the DC amplification without filtering. Across U4 in the feedback loop (series filtering) there are seven filter sizes available plus the OPEN position. The DC output is applied through the AMP SET and INTEGRATE/HOLD switches to the FINE SPECTRUM AMPLITUDE control which sets the level of the signal to the recorder.

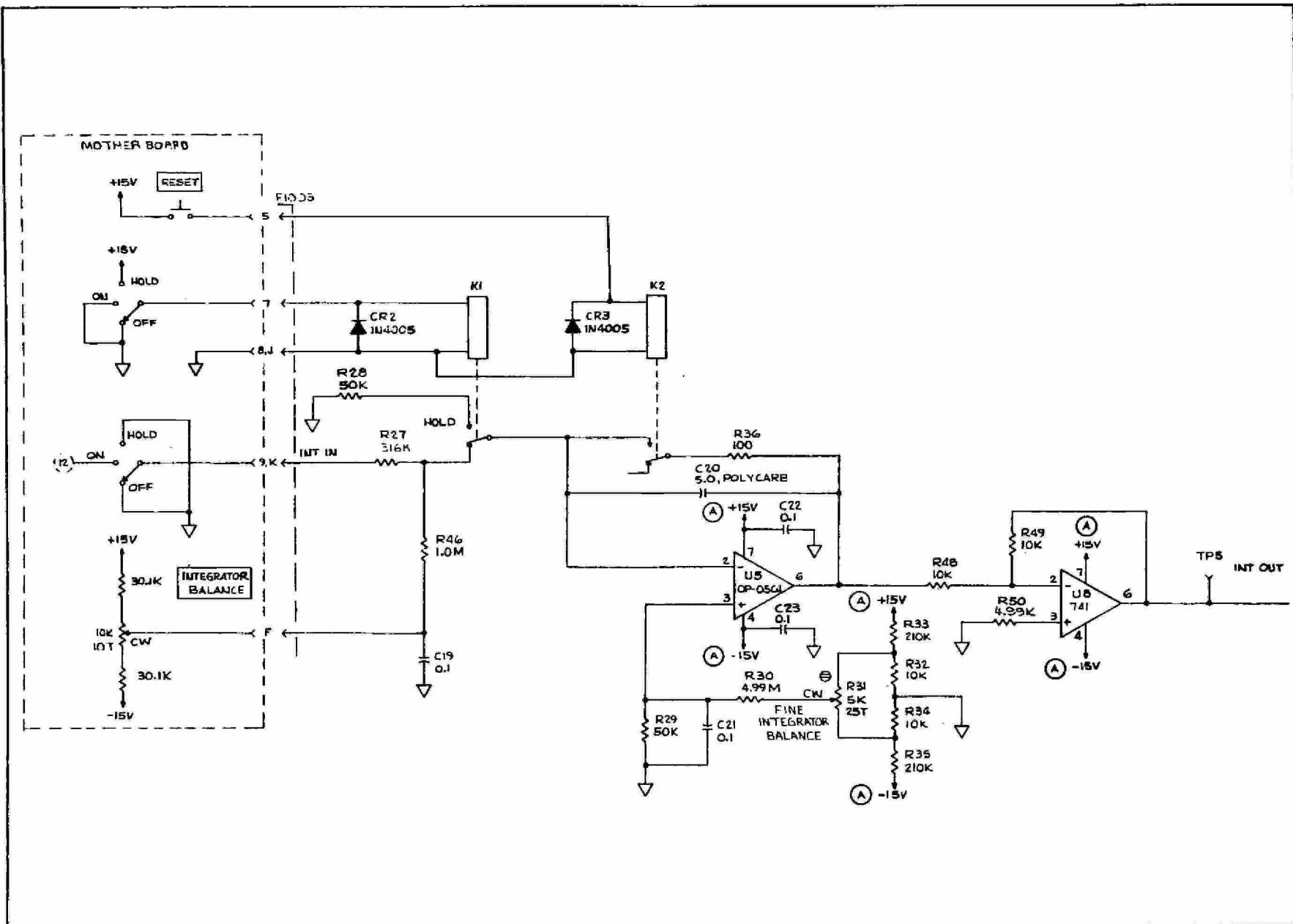


FIGURE 14-5. INTEGRATOR

The unfiltered signal from U3 is present on the INTEGRATE/HOLD switch from pin 12 of the card. In the INTEGRATE position, this signal is applied to the HOLD relay through pins 9 and K of P1005. The DC level is variable with the INTEGRATOR BALANCE control for proper integration. When HOLD is selected, relay K1 is energized and the incoming signal is removed from the integrator. The output level will remain constant for several seconds and then decay very, very slowly.

U5 is the analog integrator stage with fine balance set by R31. The integrating capacitor C20 may be reset at any time by energizing K2 by depressing the RESET button.

The integral is amplified and inverted by U8 and applied to the FINE SPECTRUM AMPLITUDE control for display on the recorder.

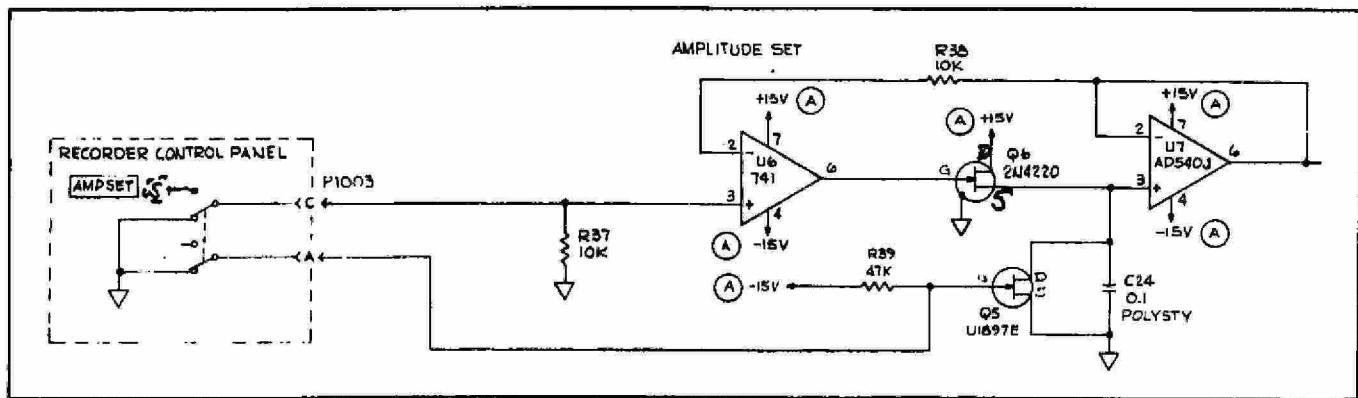


FIGURE 14-6. AMPLITUDE SET

When AMP SET is selected, the output of the FINE SPECTRUM AMPLITUDE control is applied P1003 pin C to U6 non-inverting input. At the same time ground is removed from P1003 pin A and FET Q5 turns off. This places C24 integrating capacitor into the circuit. The filtered input signal is then integrated to the highest peak in the spectrum.

The integrator consists of two operational amplifiers isolated by a FET source follower. Initially there is zero bias on the FET and the signal in is passed to charge the capacitor C24. After the peak has been passed, C24 retains its charge and Q6 is then biased off until a higher peak is encountered. If a higher peak is encountered as the spectrum is swept, C24 will charge to the level of this higher peak.

When NORMAL operation is again selected, ground is applied to Q5 turning it on and discharging C24 rapidly.

14.3 TESTS AND ADJUSTMENTS

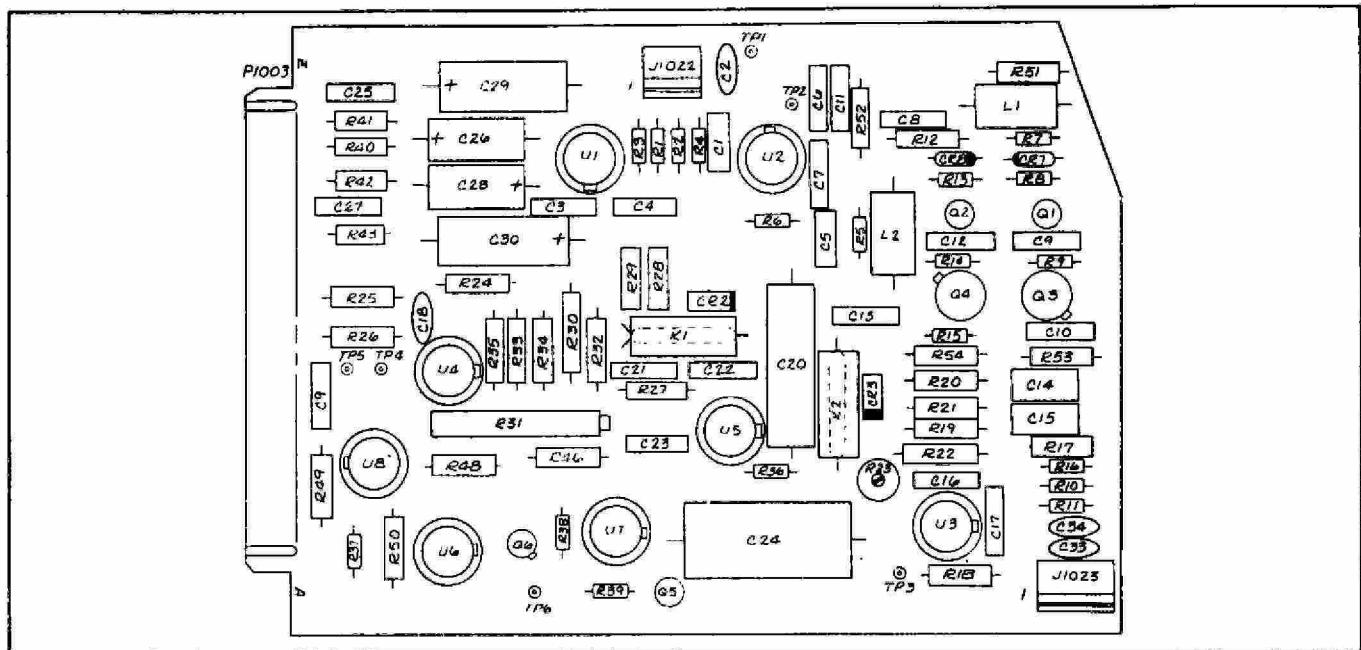


FIGURE 14-7. PART LAYOUT

1. The voltage gain from pins 1 and 2 of J1022 to TP1 for push pull inputs is 2 ± 0.3 .

Saturation (clipping) occurs at 22 volts peak-to-peak on the input. This level will produce 18 volts peak-to-peak at a frequency of 25 KHz.

2. The voltage gain from pin 16 of P1003 to TP2 is 100 ± 15 . Gain is measured at 0.01 volts peak-to-peak input and 1 volt peak-to-peak output at 25 KHz.

Saturation (clipping) occurs at e_{out} of 19 volts peak-to-peak with 0.19 volts peak-to-peak input at 25 KHz.

3. For 10^{-2} volts peak-to-peak (.01) input at pin 16 of P1003, the phase detector sensitivity at TP3 = 0.33 volt/degree $\pm 20\%$ for angles of 20° or less.

Phase detector reference levels at the card input are TTL logic levels.

Typical switching levels at the gates of Q1 and Q2 are 0 to -12 volts square wave.

4. The basic gain of the filtered operational amplifier U4 with no filter capacitors connected is unity. This measurement is made with 10 volts peak-to-peak at TP3.

U4 saturates and clipping starts at 25 volts peak-to-peak typically.

5. The AMPLITUDE SET circuit will hold ± 10 VDC output for 60 seconds with less than 1 percent change not including initial offset.

The initial offset is typically ± 0.3 VDC.

6. With the integrator input pins 9,K of P1003 grounded, drift can be adjusted to less than 2 millivolts in 5 minutes by the setting of R31 drift control.

An integrated voltage of 10 volts output should hold to less than 100 millivolts variation in 5 minutes.

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SECTION 15.0
LOCK CHANNEL

15.1 FUNCTION

The Lock Channel circuit board receives an "audio" signal (20 KHz to 30 KHz) from a buffer amplifier on the Observe Channel card and amplifies it by 40 dB (X100). The amplified audio signal is fed into two phase detectors in parallel, one with 0° phase and the other with 90° phase reference signals.

The signal detected with 90° phase reference (called the ABSORPTION MODE) is applied to the Meter Select and Driver circuits after 20 dB (X10) amplification. This signal is also used as the AUTOSHIM circuit input.

The circuit detected with the 0° phase reference (called the DISPERSION MODE) is applied to an integrator U2. The integrated output is the Field Lock Error Signal and is the major function of the Lock Channel Card.

A Meter Driver operational amplifier and dual slope detector applies a switch selected signal to the front panel meter.

15.2 THEORY OF OPERATION

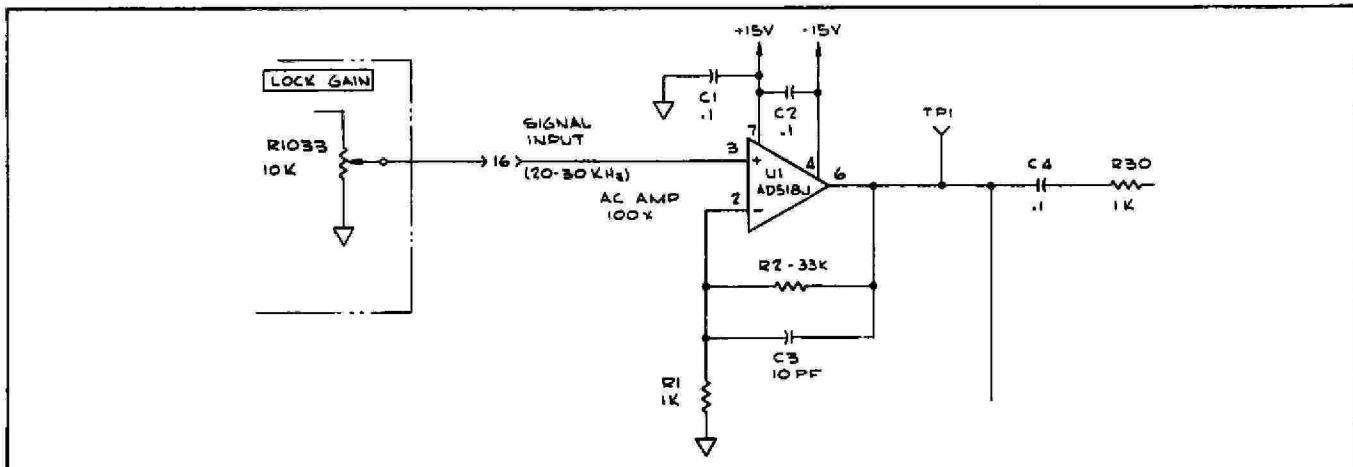


FIGURE 15-1. INPUT CIRCUITS

The input from the Observe Channel card is made first to the LOCK GAIN control on the front panel. From there it is applied to U1 non-inverting input to be amplified and applied to two phase detector circuits.

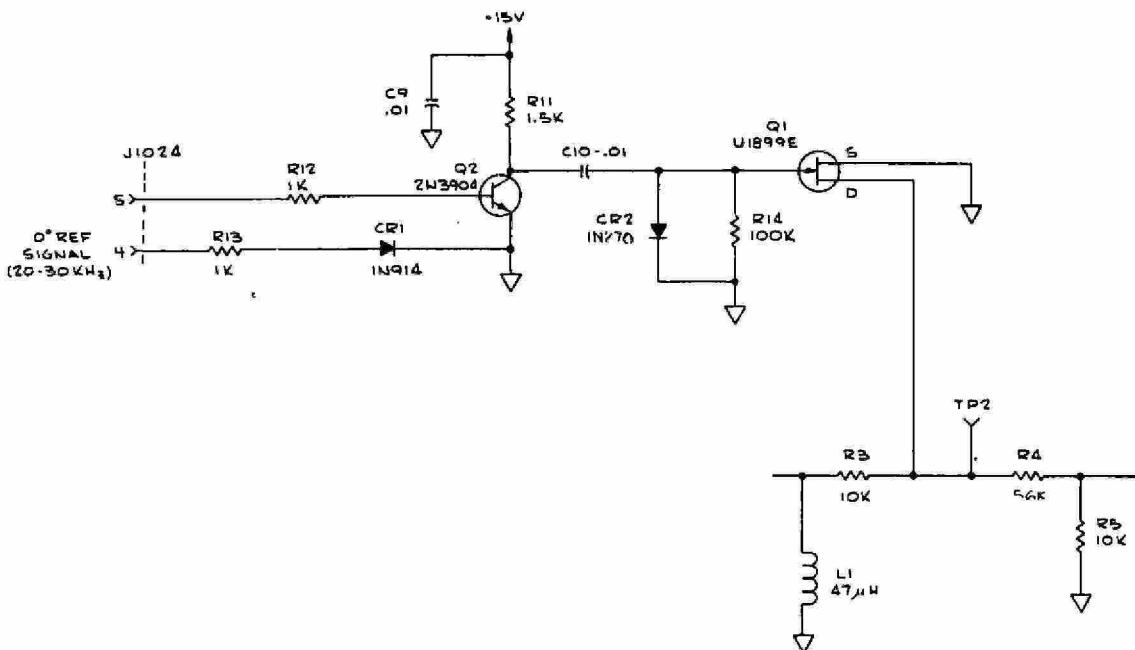


FIGURE 15-2. DISPERSION MODE PHASE DETECTOR

The 0° Lock Reference Phase input signal from the Field Modulator is of 90° (or 270°) relation with the signal from U1. The signal from U1 is applied to the drain of Q1.

The input TTL Logic 4 volt square wave applied at pin 5 of J1024 is amplified in squaring amplifier Q2 to a 0 to +15 volt squarewave. This waveform is clamped by C10, CR2, and R14 to 0.6 volt positive excursion to about -14 volts on the negative excursion. This turns FET Q1 on and off at the rate of the incoming signal.

When the phase relation of the reference and the signal from U1 are exactly 90° separated, the output of the phase detector is zero. This can be seen by assuming the signal leads the reference by 90° or the signal is at the 90° point (maximum positive) when the reference is at the 0° negative to positive transition. During the time the reference is positive, the output of the FET Q1 is zero or ground. When the reference passes 180° (signal is at 270° or maximum negative) the FET cuts off and the output of the signal is made and filtered. The DC average of the signal excursion from maximum negative to maximum positive is zero! The output of the phase detector is then zero for each half-cycle of the inputs. If the phase relation of the two signals vary only slightly, there will be a voltage produced in the filtered output during the half-cycle that Q1 is cut off. This output will be of such a polarity that when amplified, inverted, and applied to the Field Controller corrections will be made in the Field Sweep coils to bring the phase back to 90° correspondence.

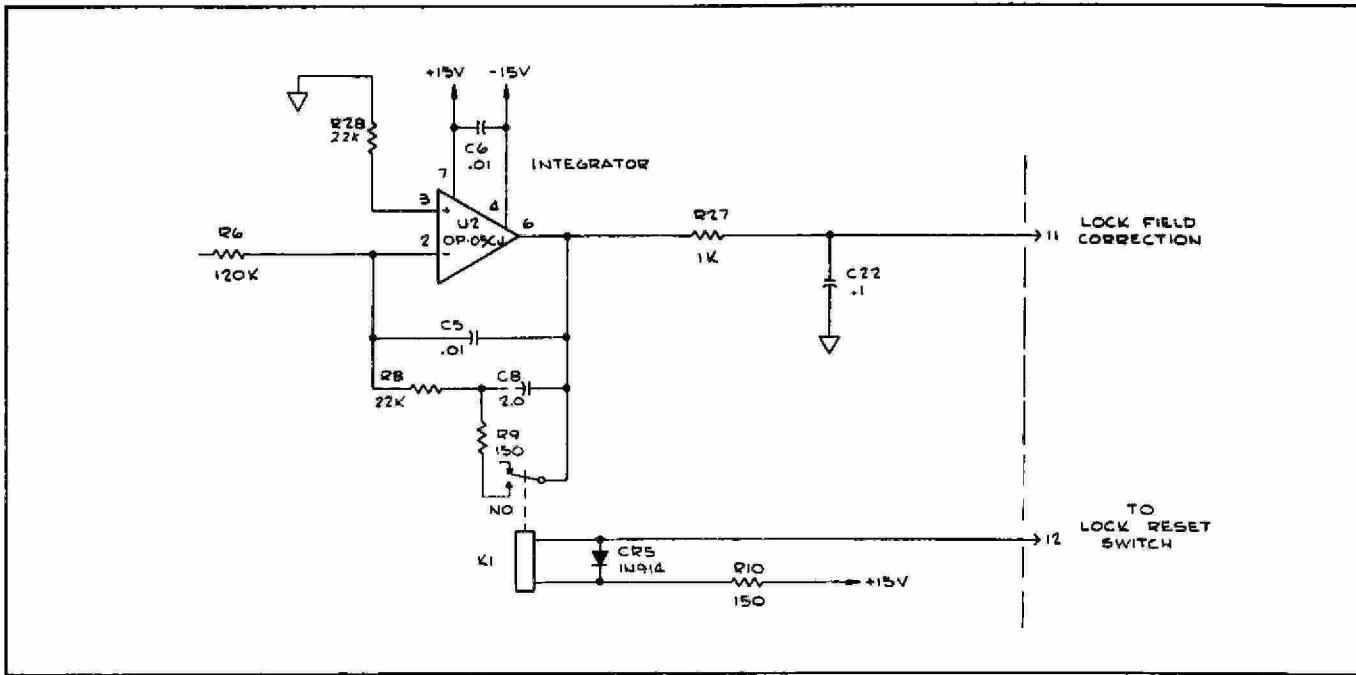


FIGURE 15-3. LOCK INTEGRATOR

The half-wave phase detected signal is applied to the inverting input of integrator U2. The output of U2 is made to the Field Control PCB for error correction in the lock. The integrator is reset by ground being applied to pin 12 when the LOCK MODE switch is placed in STANDBY. This energizes K1 allowing the integrating capacitor C8 to discharge through 150 ohms.

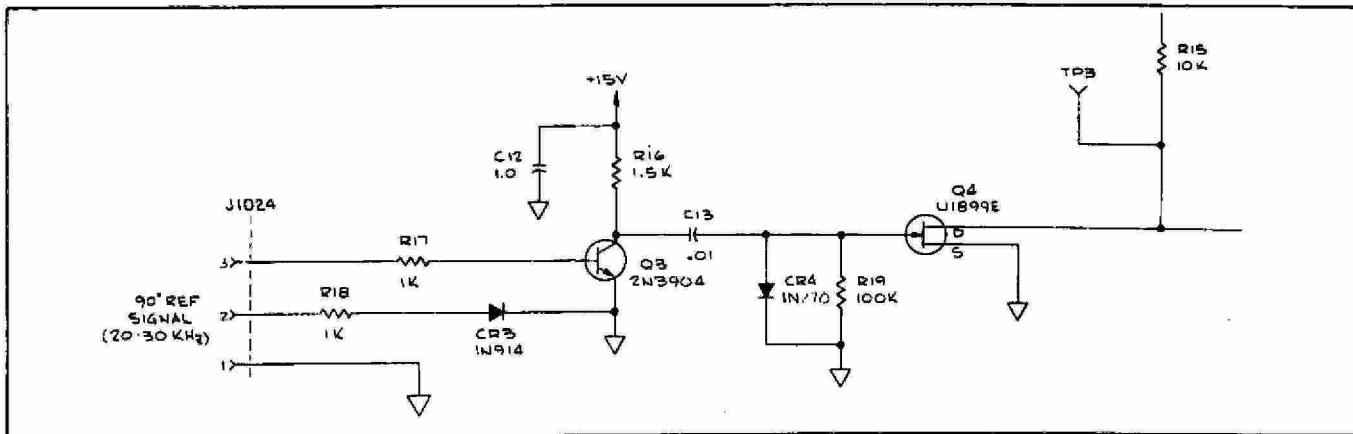


FIGURE 15-4. ABSORPTION MODE PHASE DETECTOR

The 90° Lock Reference Phase input signal at pin J1024-3 from the Field Modulator is of 0° (or 180°) relation with the signal from U1. The signal from U1 is applied to the drain of Q4.

The input TTL Logic 4 volt square-wave applied at J1024-3 is amplified in squaring amplifier Q3 to a 0 to +15 volt square-wave on the collector. This waveform is clamped by C13, CR4, and R19 to 0.6 volt positive excursion to about -14 volts on the negative excursion. This turns FET Q4 on and off at the rate of the incoming signal.

When the phase relation of the reference and the signal from U1 are exactly 0° (or 180°) separated, the output of the phase detector is maximum and is proportional to the signal amplitude from U1. This can be seen by assuming the signal and the reference are exactly in phase. The signal from U1 at zero degrees may be assumed to be at the low to high transition point (0) and rises to a maximum positive at 90° , etc. The FET Q4 turns on then during the positive portion (0 to 180°) of the input signal and 0 volts (ground) is output. During the portion 180° to 360° , the signal is negative and Q4 is cut off allowing the negative voltage into the output. The amplitude of the output depends then on the signal amplitude and the phase relationships of the two signals.

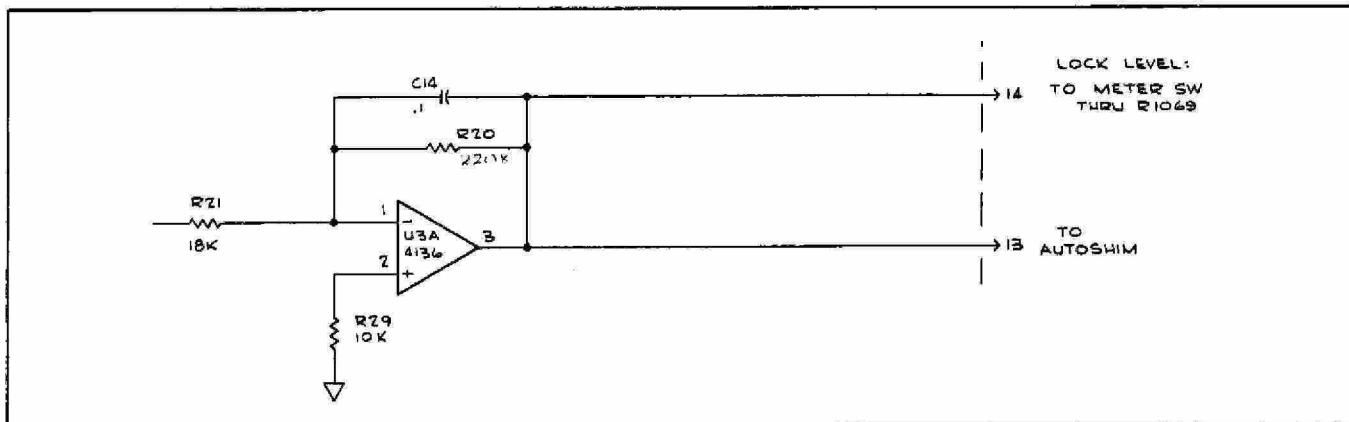


FIGURE 15-5. METER/AUTOSHIM OUTPUT

The half-wave phase detected signal is applied to the inverting input of DC amplifier U3A. This amplifier then supplies the DC level from the phase detector to the AUTOSHIM and the LOCK LEVEL position of the METER CIRCUIT.

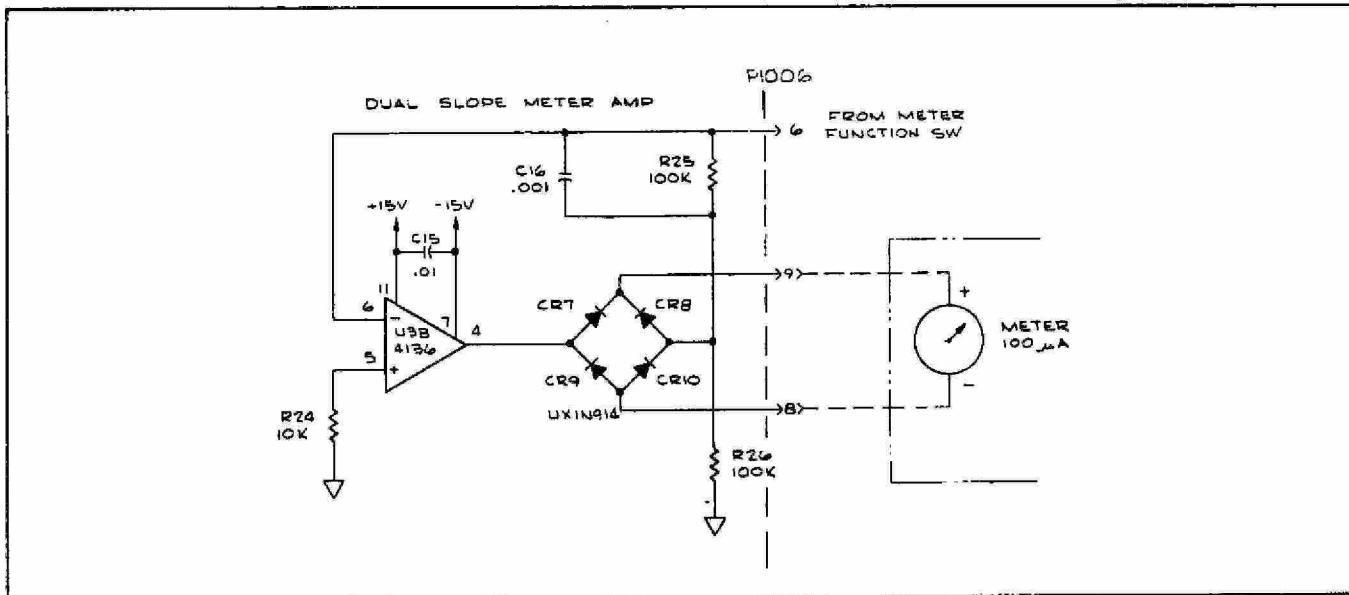


FIGURE 15-6. METER DRIVER/SLOPE DETECTOR

The various functions monitored by the METER switch are applied to inverting amplifier U3B which is applied to a bridge rectifier consisting of CR7, CR8, CR9, and CR10. Regardless of the polarity of the input, the output at pin 9 is always positive and the output at pin 8 is negative. This circuit then takes the absolute value of the input for meter display.

15.3 TESTS AND ADJUSTMENTS

1. Typical values of the input at pin 16 is 0.1 volts peak-to-peak when the system is locked.

Monitor the signal at TP1 with about 0.1 volt on the input. The gain of U1 will be greater than 50.

Saturation will occur with more than 0.47 volts peak-to-peak on the input and the signal at TP1 will be clipped.

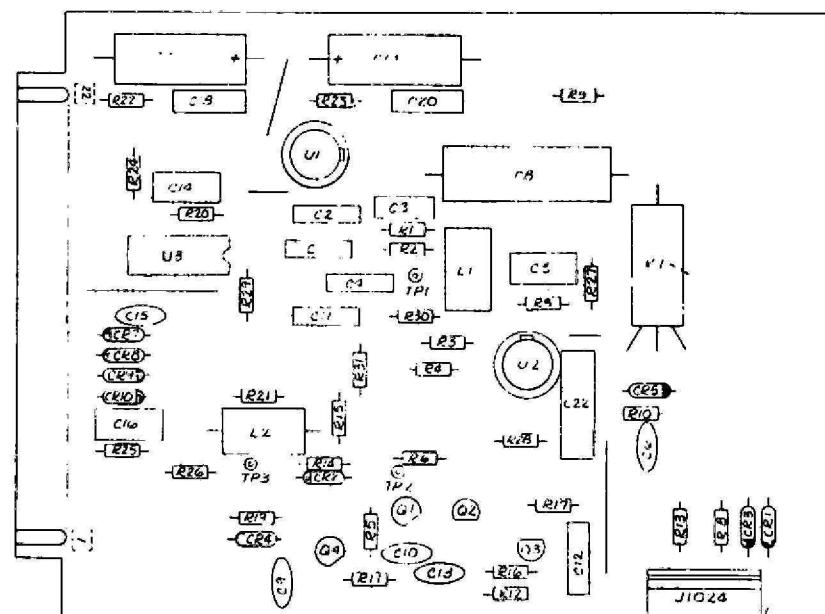


FIGURE 15-7. PART LOCATION