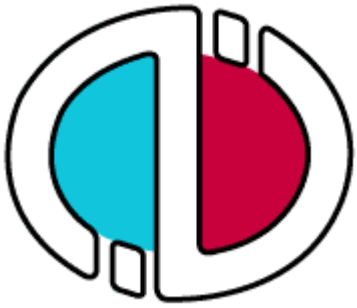

ANADOLU UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EEM 334 – Digital Systems II

LAB 3 – COMBINATIONAL CIRCUIT DESIGN

1. PURPOSE

In this lab, you will learn how to design a combinational circuit with different concurrent signal assignment techniques.

Inputs				Outputs		
A	**B**	**C**	**D**	**X**	**Y**	**Z**
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	1	0
0	1	1	0	0	0	0
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	0	1	1	0	1	0
1	1	0	0	1	0	1
1	1	0	1	1	0	0
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Figure 1: Truth Table of the design

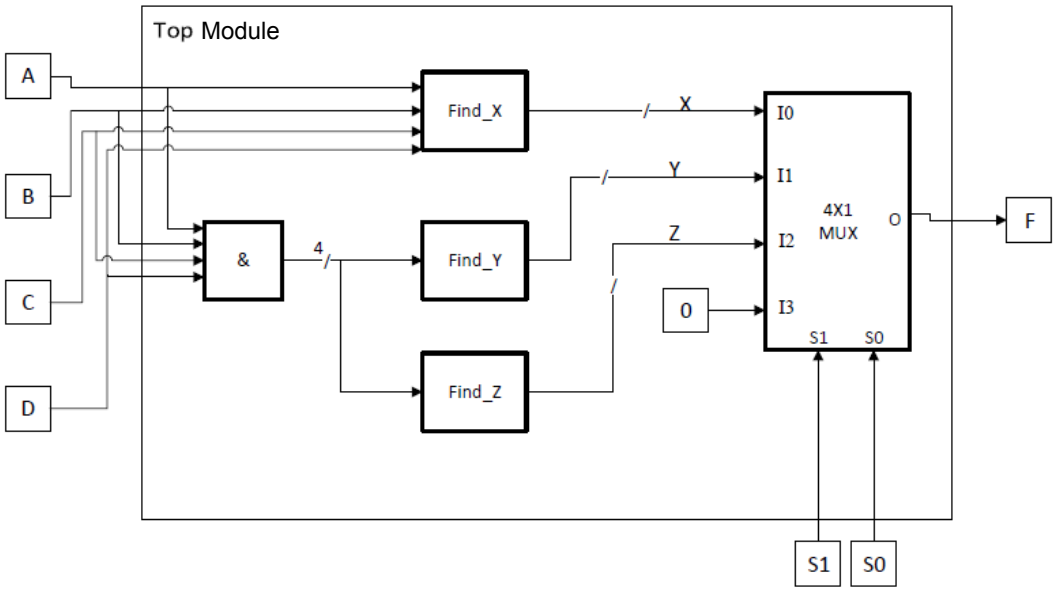

Figure 2: Top Module

2. BACKGROUND

In this lab, you will use the following signal assignment techniques;

1. Concurrent signal assignment:
   Example: A <= B and C;
2. Conditional concurrent signal assignment:
   Example : A <= B when B>2 else
   C when B=2 else
   0;
3. Selected concurrent signal assignment:
   Example : with B select
   A<= C when “00”
   D when “01”
   E when others;

3. PROCEDURE

In this lab, you will design four modules. Each module must provide following properties:

1. Find_X.vhd:
   - It has four inputs and each of them is 1-bit.
   - It has 1 output for X and it is also 1-bit.
   - Firstly, you must find a simplified Boolean expression for output X according to the truth table given in Figure 1 (Hint: Use the Karnough map)
   - Then, define X by using the concurrent signal assignment technique (<=).
2. Find_Y.vhd
   - It has 4-bit wide one input and 1 bit output (Y).
   - You must use the conditional concurrent signal assignment (when-else) to obtain Y.
3. Find_Z.vhd
   - It has 4-bit wide one input and 1 bit output (Z).
   - You must use the selected concurrent signal assignment (with-select-when) to obtain Z.
4. Top.vhd
   - In this module, you will implement the diagram given in Figure 2.
   - A, B, C, D, S0 and S1 are 1-bit inputs.
   - F is 1-bit output.
   - You must concatenate A, B, C and D inputs to obtain input signal of Find_Y and Find_Z modules. (A is the most significant bit.)
   - Find_X, Find_Y and Find_Z modules are the components of Top module. The outputs of these modules (X, Y and Z) will be connected to inputs of 4x1 multiplexer.
   - The final output (F) is the output of the multiplexer. It will be selected by S1 and S0.

Steps:

1. Implement Find_X, Find_Y and Find_Z modules as specified above.
2. Write a test bench and test these modules, individually.
3. Implement Top module and test it.
4. Show your simulation result to the lab assistant.
5. Create a UCF file. Connect A, B, C, D, S1 and S0 to switches and F to one of LEDs.
6. Load the design to FPGA.
7. Verify results and show them to the lab assistant.
8. Wait for your task.