ESKİŞEHİR TECHNİCAL UNIVERSİTY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EEM 334 – Digital Systems II

LAB 9 – FSMD CIRCUITS

ITERATIVE DIVIDER

1. PURPOSE

In this lab, you will design and implement an iterative divider as an FSMD circuit. The circuit will perform the integer division based on the long division method as shown in Figure 1.

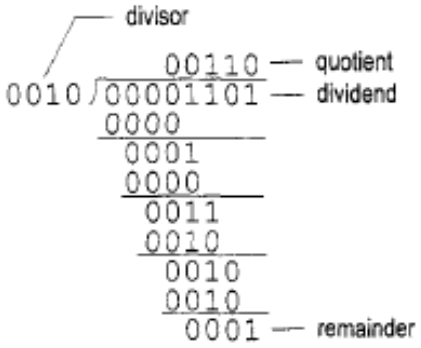

Figure 1: Long division of two 4-bit unsigned integers

The steps of the division can be summarized as follows:

1. Double the dividend width by appending 0's in front and align the divisor to the leftmost bit of the extended dividend.
2. If the corresponding dividend bits are greater than or equal to the divisor, subtract the divisor from the dividend bits and make the corresponding quotient bit 1. Otherwise, keep the original dividend bits and make the quotient bit 0.
3. Append one additional dividend bit to the previous result and shift the divisor to the right one position.
4. Repeat steps ***2*** and 3 until all dividend bits are used.

The data path and ASMD chart of the circuit that you will design are given in Figure 2 and Figure 3, respectively.

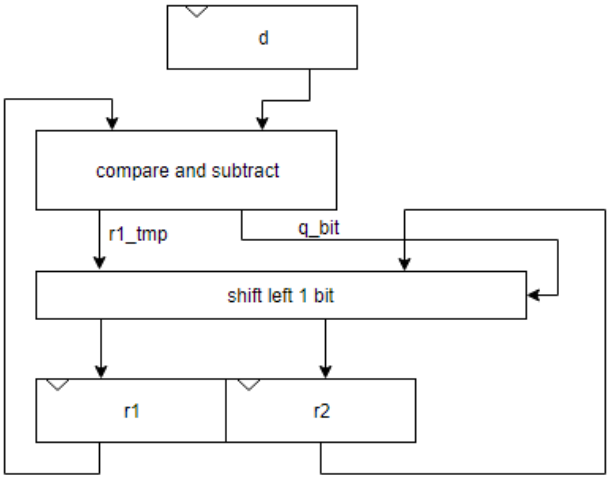

Figure 2: Data path of iterative divider

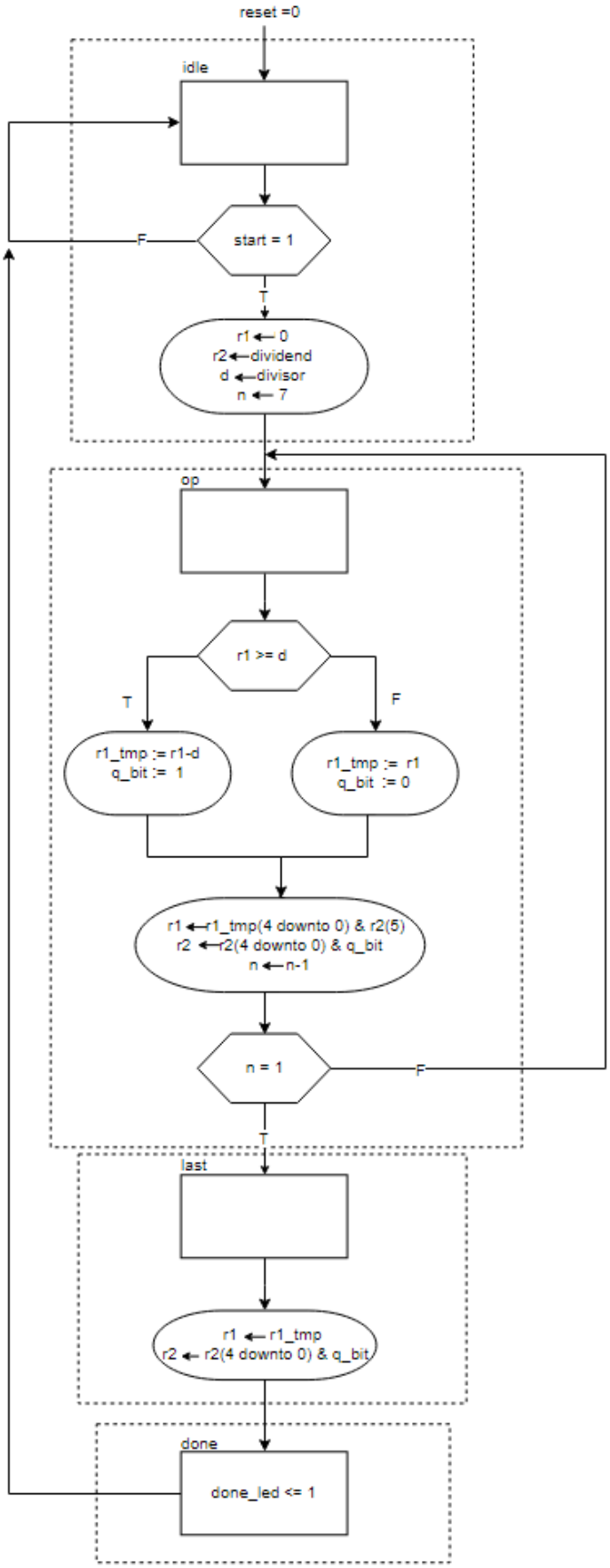

Figure 3: ASMD chart

2. BACKGROUND

An FSMD (finite state machine with data path) is combination of an FSM and a data path. So, an FSMD consists of a data path and a control path. FSM part of circuit is known as control path and data path is composed of data path registers, functional units, and related routing circuits.

The FSMD is used to implement digital systems described by the register transfer (RT) methodology. A control path specifies when and which RT operations should be performed. A data path performs RT operations.

3. PROCEDURE

You will design an iterative divider circuit according to the following specifications:

- Your circuit will divide 6 bit unsigned number to 4 bit unsigned number.
  (Numbers are unsigned not signals).
- A dividend and a divisor will be set by user in testbench.
- The operation will be started by setting a start signal.
- Set a ready signal as output for indicating that the result is valid.
- An asynchronous reset will put your circuit into a reset state, and clear all registers and outputs.

Steps:

1. Design your FSMD.
2. Create top module
3. Code your FSMD, make necessary connections between components and ports
4. Create a simulation to verify the functionality of the design.
5. Verify your results and show them to your assistant.
6. Wait for a new task.