Costa Rica Institute Of Technology

Electronics Engineering Department

Intel, Costa Rica

HANDS-ON WORKSHOP ON ELECTRONIC PACKAGING (EP) AND ELECTRICAL INTEGRITY (EI)

Design Proposal

Characterization of High-Speed Channels using the USB 3.0 Standard

Lectures:

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TEC intel

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Introduction and Motivation

Since 1996, the USB (Universal Serial Bus) was developed and introduced as a new way or method of establishing communication between a computer and peripheral devices, replacing at that time low-speed protocols that used serial and parallel ports [1].

Currently, the USB communication protocol has become common peripherals in mobile devices, tablets, video game consoles, among others, however due to the growing demand in the industry and massive data transfer, the USB standard has evolved in terms of transfer speed in addition to its mechanical connector scheme. Figure 1 shows the evolution of the USB standard, and Figure 2 shows the estimation of an eye diagram for USB 3.0 [2-3].

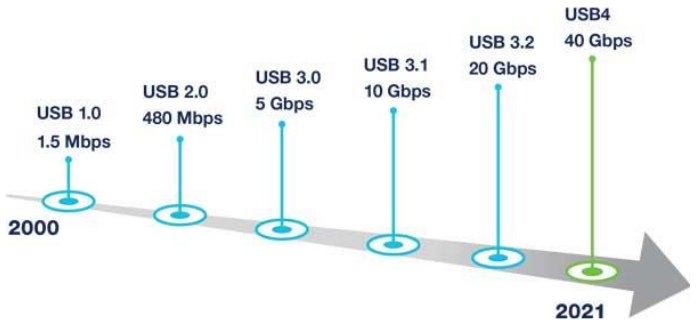


Figure 1 USB Technology Evolution, taken from [1]

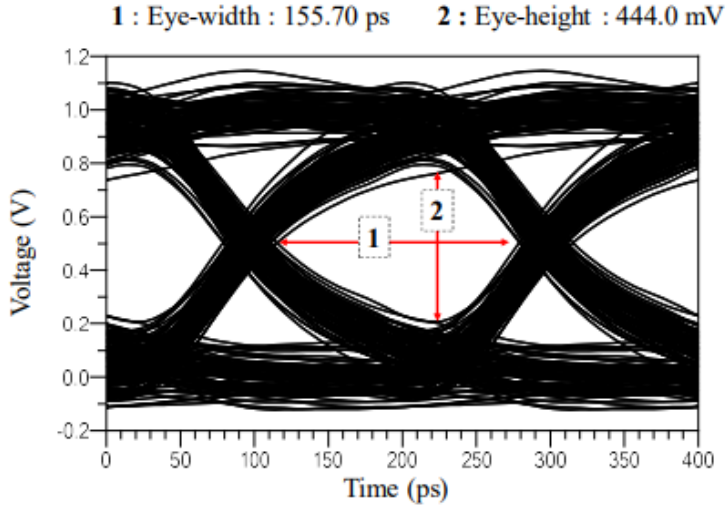


Figure 2 Eye Diagram estimation for USB 3.0, taken from [3]

Administrative Matters

Before starting, it is necessary to follow the following administrative guidelines:

Team Formation

The groups will be formed by **five members** and cannot be modified throughout the execution of the design challenge.

Mentor Assistance

All working groups will have access to mentoring support from TEC or INTEL. One mentor will be assigned per work team, where the date and time of consultation will be defined by each mentor.

Plagiarism

Any evidence of plagiarism will be thoroughly investigated. If corroborated, the team will not be allowed to continue.

Description

This design challenge proposes the integration of a measurement system for the characterization of high-speed channels based on the USB 3.0 standard, by means of a multi-layer system using PCB technologies.

During the execution of the challenge, each team must use engineering design methodologies, electrical integrity, and electronic packaging knowledge, which allows to generate documentation synthesizing the design process, integration and validation of the system using high frequency instrumentation such as a Vector Network Analyzer (VNA).

At the end of the design challenge, each member will have knowledge about the process and design of a laminated PCB system which allows to generate an access system for the characterization of high-speed channels in the USB 3.0 standard and checking by means of high frequency measurement systems the electrical integrity of the channel by means of basic knowledge of signal and power integrity (SPI).

Design Challenge

This design challenge will allow the integration of an access system to perform high-speed channel characterization using the USB 3.0 standard. Figure 3 shows a high-level block for the development of the access system.

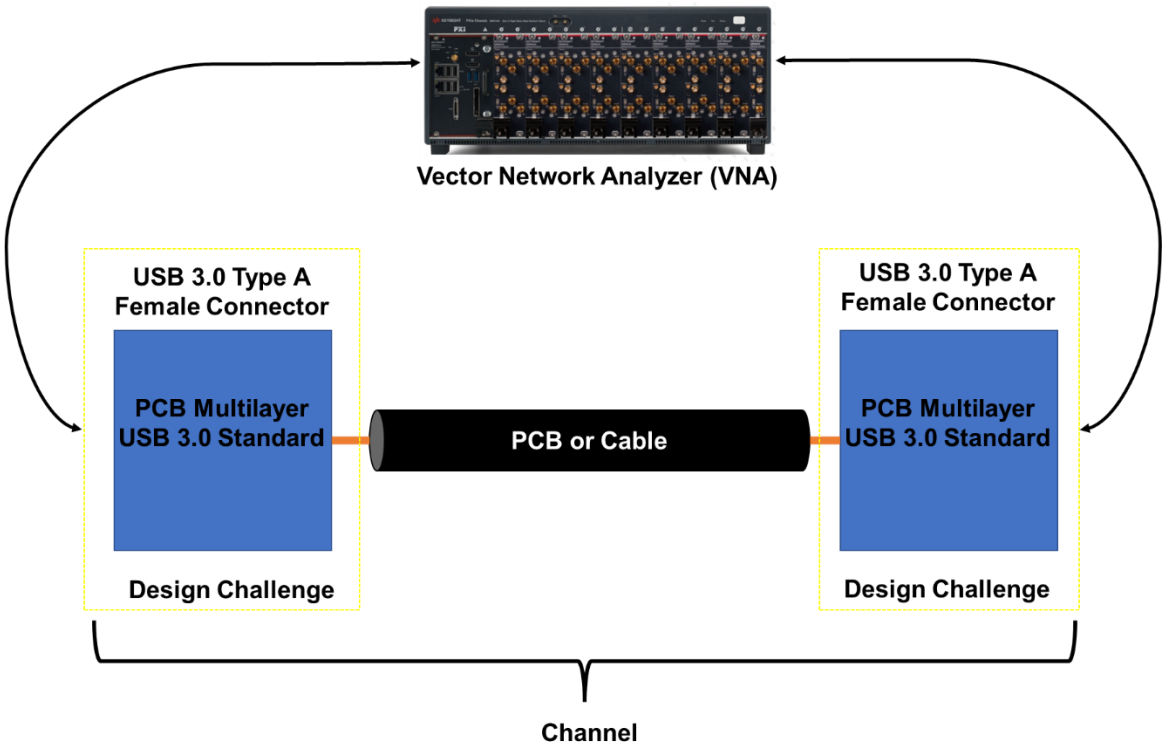


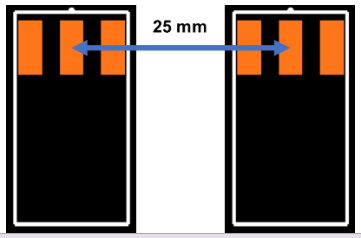
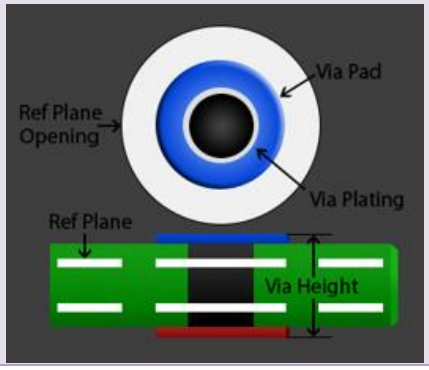
Figure 3 Proposed high-level diagram for the characterization of a channel using USB 3.0 standard

Requirements and Constraints

For the integration of the access system, the following requirements and restrictions should be used. Table 1 shows the requirements and restrictions of the access system for high-speed channel characterization using the USB 3.0 standard.

Table 1 Requirements and Constraints for high-speed channel characterization access system using USB 3.0 standard

Requirements	Constraints
The access system shall be integrated on a PCB using the USB 3.0 standard.	It shall use USB standard revision 3.0 in Super Speed (SS) mode and AC Coupling Capacitors are not necessary in this approach. Check following links (see link1, link2).

The PCB shall be a 4-layer stack-up using an FR-4 substrate.	The substrate shall be the one used by PCBWAY (see here). For this purpose, we will work with a thickness of 1.6 mm and cooper to 1 oz.
The access system shall have USB 3.0 type A connectors.	The USB connectors shall be Female and through-hole type. (see link1)
The access system shall have radio frequency connectors for connection to a vector network analyzer (VNA) PXIe Vector Network Analyzer Keysight Model M980xA Series.	The RF connectors shall operate for a bandwidth up to 15 GHz and the position of the connectors shall be edge mount soldered to the PCB with female connection method. (see here). RF connectors shall have a minimum of 25 mm spacing between active pads. 
For interconnection of layers, through-hole type via should be used.	The vias shall be dimensioned: • Via Hole Diameter 15 mils • Internal Pad Diameter 30 mils • Reference Plane Opening Diameter 54 mils • Via Height 63 mils • Via Plating Thickness 1 mils • Impedance = 50 Ω. • Tented Vias. 
The PCBs forming the access system shall have an area of 4000 $\boldsymbol{mm^2}$	PCBs shall be rectangular shape with dimensions: • 50 mm (width) • 80 mm (length).

PCB shall have silkscreen	The silkscreen shall contain the following: • Name of the group members (bottom layer preferred). • Details of pins and components

Analysis Questions

The following questions should be answered in relation to the design and discussed in the written report.

1. The spacing between the two signals of a differential pair impacts the differential characteristic impedance?
2. As long as the traces of a differential pair are matched in length, the total length has no impact on signal quality?
3. The traces of a differential pair must be perfectly matched in length?
4. High-speed differential pairs should be routed over a solid ground plane when possible?
5. What may be affected if SMA connectors with through-hole mounting are used instead of edge-mount?
6. What happens if bends smaller than 135° are used on high-speed signal within the PCB?

Deliverables and Grading

Grading

This section explains the requirements, deliverables, and grading. Please read and make sure to organize the execution of the design challenge and deliverables throughout the work time and not just before the deadline.

The grading of this design challenge will be based on:

- Design Methodology.
- System Integration through PCBs Technologies.
- System Validation with RF Equipment.
- Performance Analysis.
- Written Executive Report (IEEE Transactions Template here, written in English and maximum 5 pages).

The grading will be based on 0 to 100%, and table 2 details the percentage items for each item.

Table 2 Design challenge evaluation criteria

Item	Description	Percentage
Design Methodology	Requirements and design constraints analysis Solution conceptualization Design methodology conformation	20%
System Integration through PCBs Technologies	Correct creation of component libraries Compliance with design rules for the USB 3.0 standard Appropriate signal routing Area specifications compliance	50%
System Validation with RF Equipment	Appropriate equipment calibration S-parameters Extraction from VNA	5%
Performance Analysis	S-Differential Parameters Analysis	20%
Written Executive Report	This report should contain: • Abstract • Introduction • Design Methodology • Validation • Conclusion • Recommendations • References	5%
Total*		100%

***Two best groups will be given a prize**

Deliverables Submissions

To submit your deliverables you have to:

- Compress your deliverable folder in **ZIP** format. Not other format due to the TEC email account will be move to SPAM.

References

[1] G. C. Technology, USB - History & Timeline. [Online]. Available: https://bit.ly/3G3V9JE. [Accessed: 07-Nov-2022].

[2] “USB: Tektronix,” USB | Tektronix. [Online]. Available: https://www.tek.com/en/solutions/application/high-speed-serial-communications/usb. [Accessed: 07-Nov-2022].

[3] D. Lho, J. Park, H. Park, H. Kang, S. Park and J. Kim, "Eye-Width and Eye-Height Estimation Method Based on Artificial Neural Network (ANN) for USB 3.0," 2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2018, pp. 209-211, doi: 10.1109/EPEPS.2018.8534277.