Design Assignment 4: Pulse Width Modulation

EE460-Digital Design II

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Introduction

The aim of this lab assignment is to design an pulse wave modulated signals at a certain duty cycle. However, the pulse width modulation (PWM) is a technique to provide a logic 1 (on) and logic 0 (off) for a controlled period. As, in Figure 1 the PWM of 50% , 75%, and 25% duty cycle is displayed. Throughout this lab report the top design will be step by step implemented and the test bench simulation will be presented.

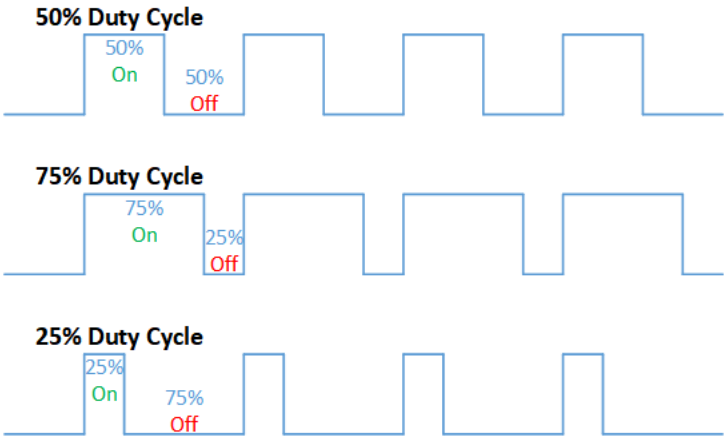

Figure 1- PWM signals with different duty cycles

Top Level Design

To choose the hardware components of this design first the Top module I/O signals was set, and the top design was split in to control unit and data path, as shown in Figure 2.

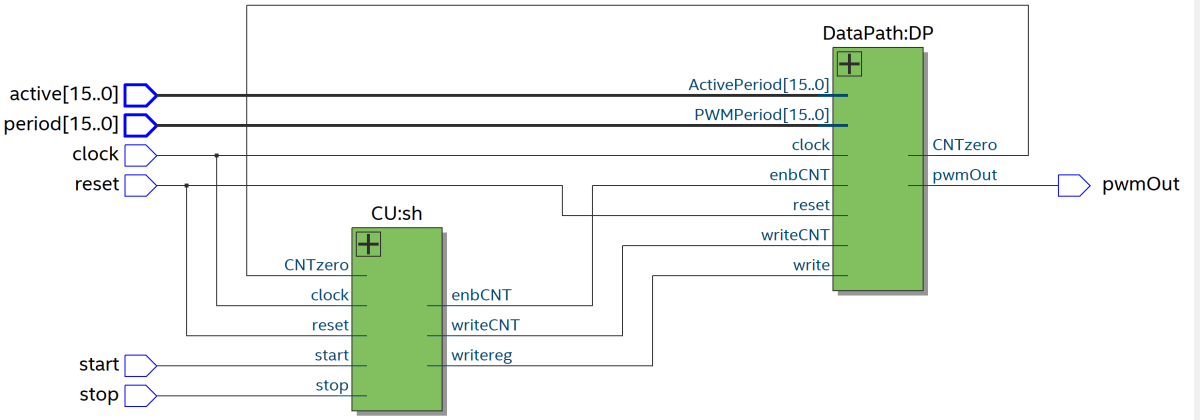

Figure 2- PWM Top Design

Input Data Path:

16-bit - active, and period

1-bit- reset, clock, enbCNT, writeCNT, write

Input Control Unit:

1-bit- reset, clock, start, stop

Output Data Path:

1-bit- CNTzero, pwmOut

Output Control Unit:

1-bit- enbCNT, writeCNT, write

Operation: count down 16 bits, equal to zero, less than

Two variables were set a register that will be used to hold its value and allow the process to be synchronized with the clock and each one of them was declared with its initial value. Moving to the input and output both were declared as registers to save their values.

Datapath

The Datapath consists of the 2 registers, count down counter of 16 bit, comparators (equal to 0, less than), all connected to generate the output signals PWMd which is the PWM period, PWMsig which is the active period shown in Figure3.

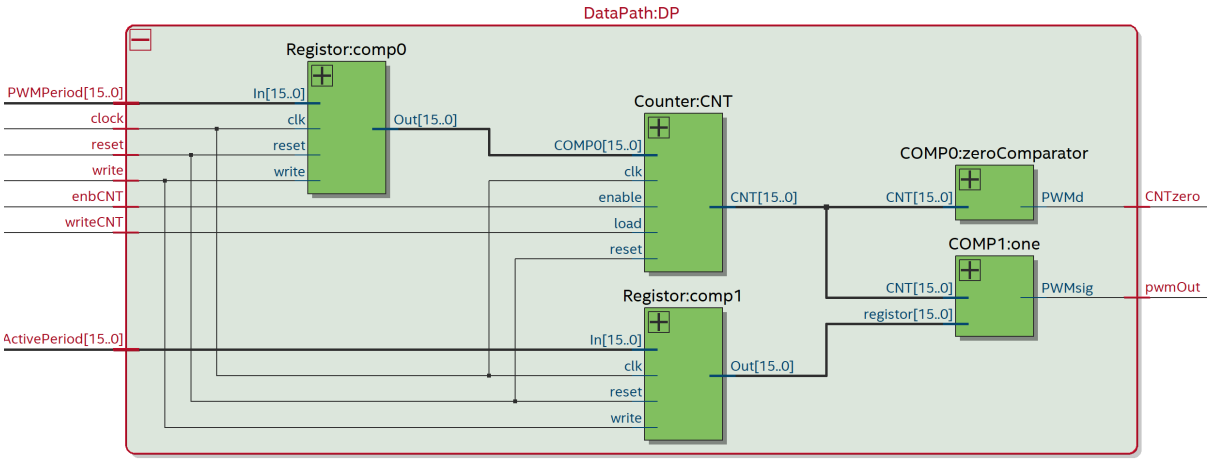

Figure 3- Datapath Design

The PWM module implements a 16-bit down-counter CNT, with two compare registers, COMP0 and COMP1. The value of COMP0 acts as the top value of the timer; COMP0 is loaded into CNT on timer underflow (when CNT == 0). The PWM output is set idle on CNT underflow and active on compare match with COMP1. COMP0 determines the PWM period, and COMP1 determines the active period. For that, first COMP0 value is sent to the CNT counter and the value generated from the CNT is compared by the value of COMP1 is less than an PWMsig flag is raised and if CNT value equals to 0 the PWMd will be equal to 1.

Control unit

The control unit is designed to take the input go, done and accordingly sends the control signals to the Datapath.

The CNTzero is a state signal sent from the data path to the control unit upon this signal and the state value the register write and the counter write and the counter load signals are being generated.

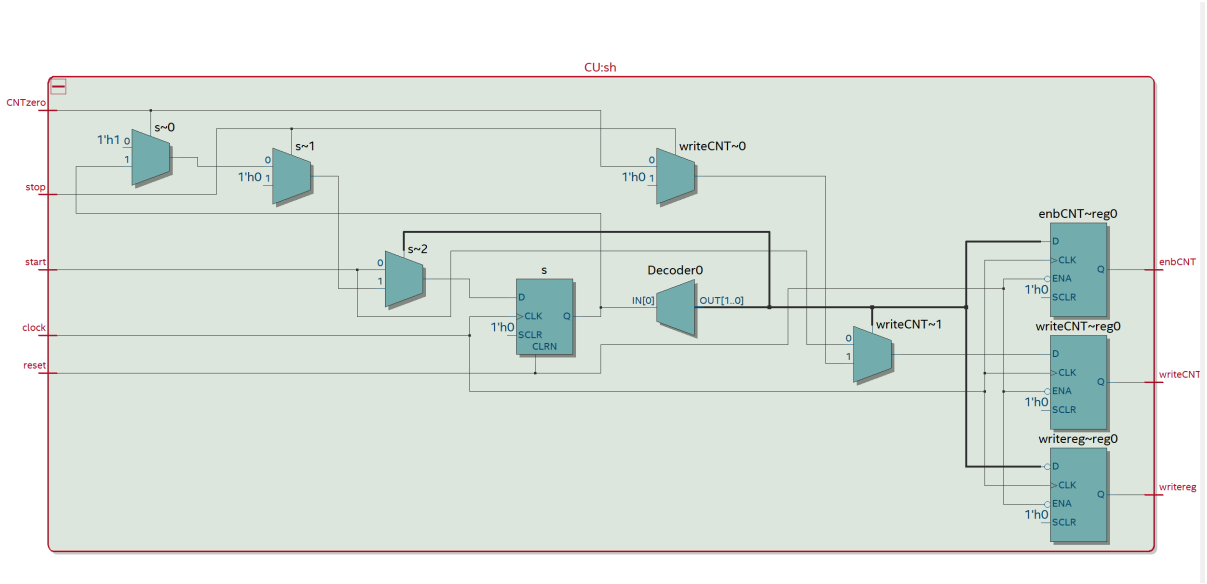

Figure 4- Control Unit Design

Table 1- The Control Signal Logic of The Control Unit

Reset==1	Reset=0	S0	S1
State =0	writeReg =0	writeReg =1	writeCNT=1
	writeCNT=0	Start =1 →s1 writeCNT=1	Stop =1 -> s0
	enbCNT=0	Stratr =0 → s0	CNTzer0 writeCNT=1
			Else stay in s1

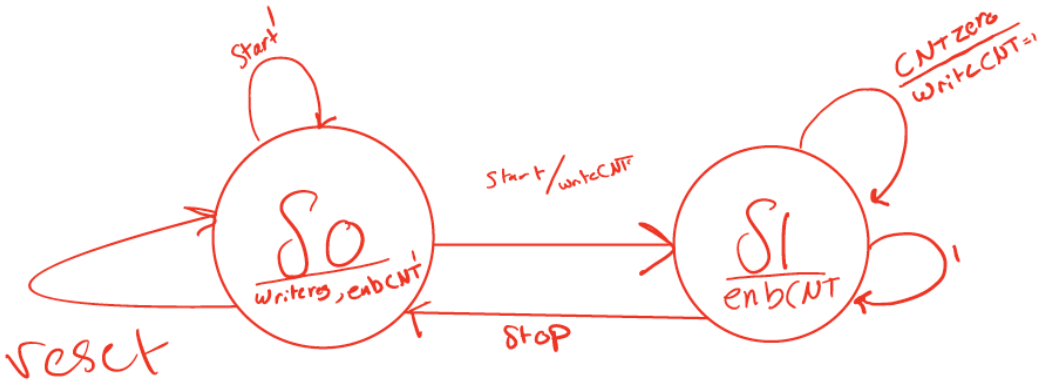

Figure 5- FSM Chart Diagram

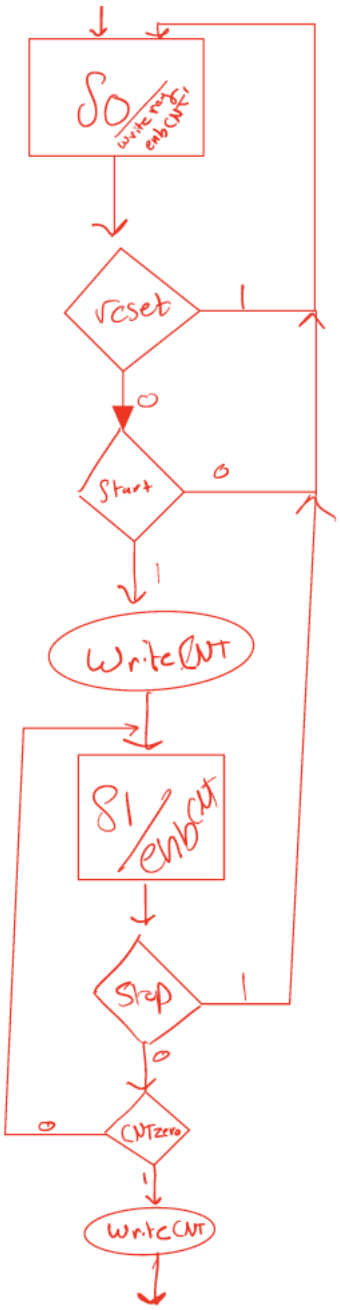

Figure 6- Control signal SM Diagram

Simulation and Timing Diagram

In the test code two situations were tested first when the period is 20 and the active period was 10 which generated an 50% duty cycle waveform, the second situation is when the period was 20 and the active period was 15 which resulted in 75% duty cycle waveform as shown in Figure 7.

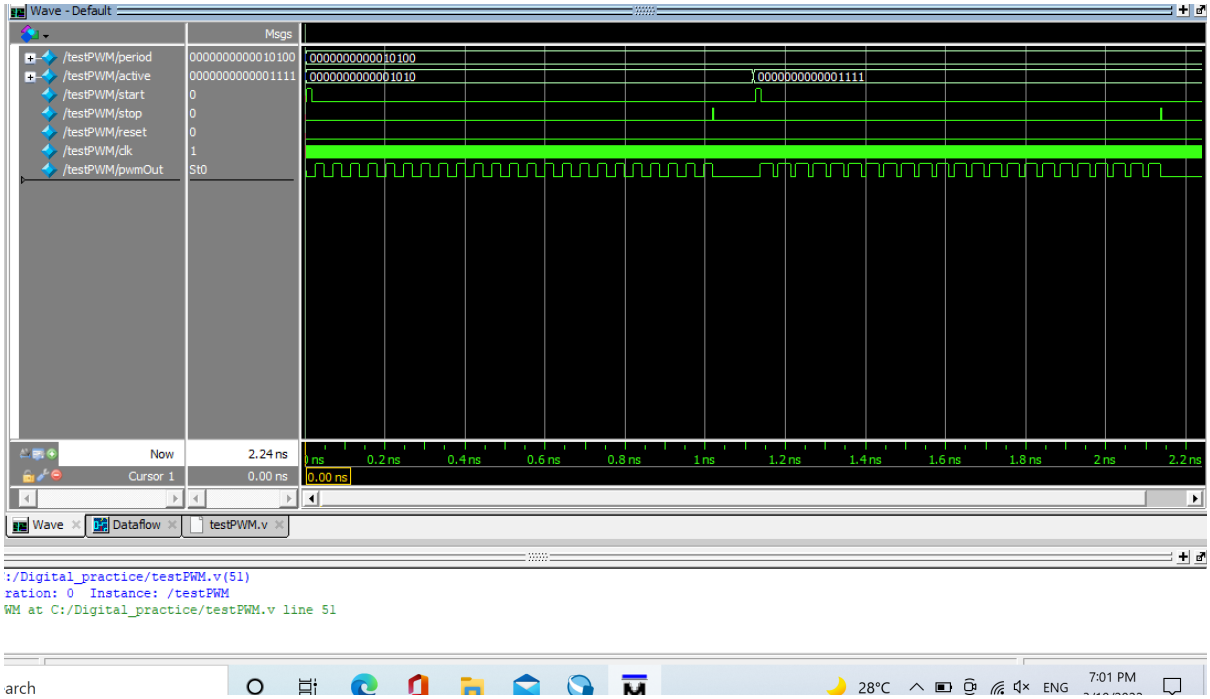

Figure 7- Test Bench Simulation