

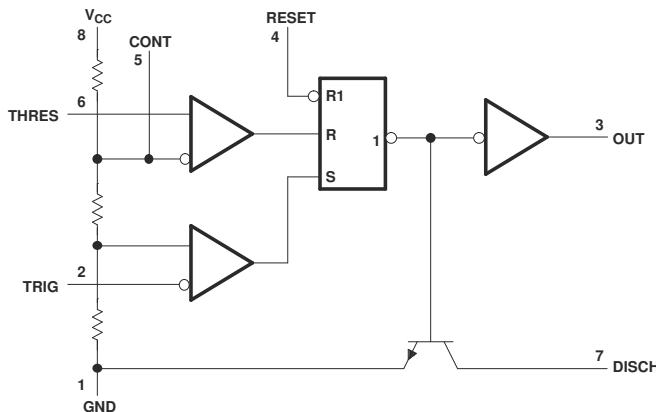
xx555 Precision Timers

1 Features

- Timing from microseconds to hours
- Astable or monostable operation
- Adjustable duty cycle
- TTL-compatible output can sink or source up to 200mA
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Pulse-shaping circuits
- Missing-pulse detectors
- Pulse-width modulators
- Pulse-position modulators
- Sequential timers
- Pulse generators
- Frequency dividers
- Industrial controls



Simplified Schematic

3 Description

The Nx555 and Sx555 devices are precision timing circuits capable of producing accurate time delays or oscillation. In time-delay or monostable operating modes, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle are controlled independently with two external resistors and a single external capacitor.

Each timer has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage pin (CONT). When the trigger input (TRIG) is less than the trigger level, the flip-flop is set and the output goes high. If TRIG is greater than the trigger level and the threshold input (THRES) is greater than the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) overrides all other inputs and is used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge pin (DISCH) and the ground pin (GND). Tie all unused inputs to an appropriate logic level to prevent false triggering.

The output circuit is capable of sinking or sourcing current up to 200mA. Operation is specified for supplies of 5V to 15V. With a 5V supply, output levels are compatible with TTL inputs.

Device Information

| PART NUMBER | OPERATING TEMPERATURE | PACKAGE ⁽¹⁾ |
|-------------|---|------------------------|
| NA555 | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ | D (SOIC, 8) |
| | | P (PDIP, 8) |
| NE555 | $T_A = 0^\circ\text{C}$ to 70°C | D (SOIC, 8) |
| | | P (PDIP, 8) |
| | | PS (SO, 8) |
| | | PW (TSSOP, 8) |
| SA555 | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | D (SOIC, 8) |
| | | P (PDIP, 8) |
| SE555 | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | D (SOIC, 8) |
| | | FK (LCCC, 20) |
| | | JG (CDIP, 8) |
| | | P (PDIP, 8) |

(1) For more information, see [Section 10](#).



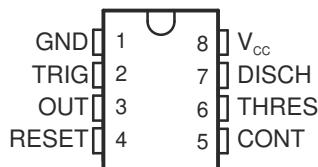
An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

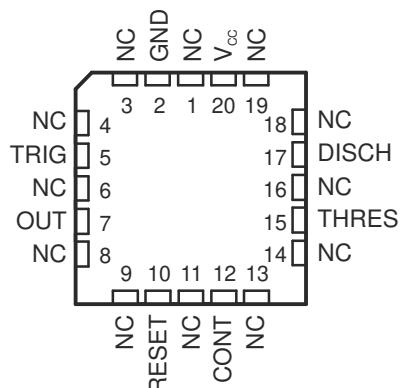
| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 6.3 Feature Description..... | 11 |
| 2 Applications | 1 | 6.4 Device Functional Modes..... | 13 |
| 3 Description | 1 | 7 Applications and Implementation | 14 |
| 4 Pin Configuration and Functions | 3 | 7.1 Application Information..... | 14 |
| 5 Specifications | 4 | 7.2 Typical Applications..... | 14 |
| 5.1 Absolute Maximum Ratings..... | 4 | 7.3 Power Supply Recommendations..... | 18 |
| 5.2 ESD Ratings..... | 4 | 8 Device and Documentation Support | 19 |
| 5.3 Recommended Operating Conditions..... | 4 | 8.1 Receiving Notification of Documentation Updates.... | 19 |
| 5.4 Thermal Information..... | 5 | 8.2 Support Resources..... | 19 |
| 5.5 Electrical Characteristics..... | 5 | 8.3 Trademarks..... | 19 |
| 5.6 Switching Characteristics..... | 7 | 8.4 Electrostatic Discharge Caution..... | 19 |
| 5.7 Typical Characteristics..... | 8 | 8.5 Glossary..... | 19 |
| 6 Detailed Description | 10 | 9 Revision History | 19 |
| 6.1 Overview..... | 10 | 10 Mechanical, Packaging, and Orderable Information | 20 |
| 6.2 Functional Block Diagram..... | 10 | | |

4 Pin Configuration and Functions

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)



SE555...FK PACKAGE
(TOP VIEW)



NC – No internal connection

Table 4-1. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|-----------------|--|--|--------------|---|
| | NO. | NAME | | |
| | D (SOIC), P (PDIP), PS (SO), PW (TSSOP), JG (CDIP) | FK (LCCC) | | |
| CONT | 5 | 12 | Input/output | Controls comparator thresholds, Outputs $2/3 \times VCC$, allows bypass capacitor connection |
| DISCH | 7 | 17 | Output | Open collector output to discharge timing capacitor |
| GND | 1 | 2 | — | Ground |
| NC | — | 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19 | — | No internal connection |
| OUT | 3 | 7 | Output | High current timer output signal |
| RESET | 4 | 10 | Input | Active low reset input forces output and discharge low. |
| THRES | 6 | 15 | Input | End of timing input. THRES > CONT sets output low and discharge low |
| TRIG | 2 | 5 | Input | Start of timing input. TRIG < $\frac{1}{2}$ CONT sets output high and discharge open |
| V _{cc} | 8 | 20 | — | Input supply voltage, 4.5V to 16V. SE555 maximum is 18V. |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|--|--------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage ⁽²⁾ | | | 18 | V |
| V _I | Input voltage | CONT, RESET, THRES, TRIG | | V _{CC} | V |
| I _O | Output current | | | ±225 | mA |
| T _J | Operating virtual junction temperature | | | 150 | °C |
| | Case temperature for 60 seconds | FK package | | 260 | °C |
| | Lead temperature 1.6mm (1/16 inch) from case | JG package, 60 seconds | | 300 | °C |
| T _{stg} | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values are with respect to GND.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|---------------------|-----|------|------|
| V _{CC} | Supply voltage | NA555, NE555, SA555 | 4.5 | 16 | V |
| | | SE555 | 4.5 | 18 | |
| I _O | Output current | | | ±200 | mA |
| T _A | Operating free-air temperature | NA555 | -40 | 105 | °C |
| | | NE555 | 0 | 70 | |
| | | SA555 | -40 | 85 | |
| | | SE555 | -55 | 125 | |

5.4 Thermal Information

| THERMAL METRIC⁽¹⁾ | | NA556, NE556, SA555, SE555 | SE555 | | NA555, NE555 | NE555 | | UNIT |
|-------------------------------------|--|---|----------------------|----------------------|-------------------------|--------------------|-----------------------|-------------|
| | | D (SOIC) | FK (LCCC) | JG (CDIP) | P (PDIP) | PS (SO) | PW (TSSOP) | |
| | | 8 PINS | 20 PINS | 8 PINS | 8 PINS | 8 PINS | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 125.4 | 92.2 | 125.0 | 98.5 | 124.5 | 164.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 64.9 | 67.6 | 73.3 | 77.8 | 61.2 | 70.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 73.2 | 66.7 | 114.9 | 61.0 | 79.3 | 104.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 14.3 | 61.6 | 44.4 | 43.9 | 16.5 | 8.2 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 72.1 | 66.5 | 106.6 | 60.3 | 77.8 | 103.1 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | 14.2 | 29.3 | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

at V_{CC} = 5V to 15V and T_A = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------|---|---------------------|------|------|------|------|
| THRES voltage level | V _{CC} = 15V | NA555, NE555, SA555 | 8.8 | 10 | 11.2 | V |
| | | SE555 | 9.4 | 10 | 10.6 | |
| | V _{CC} = 5V | NA555, NE555, SA555 | 2.4 | 3.3 | 4.2 | |
| | | SE555 | 2.7 | 3.3 | 4 | |
| THRES current ⁽¹⁾ | | | | 30 | 250 | nA |
| TRIG voltage level | V _{CC} = 15V | NA555, NE555, SA555 | 4.5 | 5 | 5.6 | V |
| | | SE555 | 4.8 | 5 | 5.2 | |
| | V _{CC} = 15V, T _A = -55°C to +125°C | SE555 | 3 | | 6 | |
| | | NA555, NE555, SA555 | 1.1 | 1.67 | 2.2 | |
| TRIG current | V _{CC} = 5V | SE555 | 1.45 | 1.67 | 1.9 | V |
| | | SE555 | | | 1.9 | |
| | V _{CC} = 5V, T _A = -55°C to +125°C | NA555, NE555, SA555 | 0.5 | 2 | μA | |
| | | SE555 | | 0.5 | 0.9 | |
| RESET voltage level | | | 0.3 | 0.7 | 1 | V |
| | T _A = -55°C to +125°C | SE555 | | | 1.1 | |
| RESET current | RESET at V _{CC} | | 0.1 | 0.4 | | mA |
| | RESET at 0V | NA555, NE555, SA555 | -0.4 | -1.5 | | |
| | | SE555 | -0.4 | -1 | | |
| DISCH switch off-state current | | | 20 | 100 | nA | |
| DISCH switch on-state voltage | V _{CC} = 5V, I _O = 8mA | NA555, NE555, SA555 | 0.15 | 0.4 | V | |
| CONT voltage (open circuit) | V _{CC} = 15V | NA555, NE555, SA555 | 9 | 10 | 11 | V |
| | | SE555 | 9.6 | 10 | 10.4 | |
| | V _{CC} = 15V, T _A = -55°C to +125°C | SE555 | 9.6 | | 10.4 | |
| | | NA555, NE555, SA555 | 2.6 | 3.3 | 4 | |
| | V _{CC} = 5V | SE555 | 2.9 | 3.3 | 3.8 | |
| | V _{CC} = 5V, T _A = -55°C to +125°C | SE555 | 2.9 | | 3.8 | |

5.5 Electrical Characteristics (continued)

at $V_{CC} = 5V$ to $15V$ and $T_A = 25^\circ C$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--|---------------------|-------|------|------|
| Low-level output voltage | $V_{CC} = 15V, I_{OL} = 10mA$ | NA555, NE555, SA555 | 0.1 | 0.25 | V |
| | SE555 | 0.1 | 0.15 | | |
| | $V_{CC} = 15V, I_{OL} = 10mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | | 0.2 | |
| | $V_{CC} = 15V, I_{OL} = 50mA$ | NA555, NE555, SA555 | 0.4 | 0.75 | |
| | SE555 | 0.4 | 0.5 | | |
| | $V_{CC} = 15V, I_{OL} = 50mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | | 1 | |
| | $V_{CC} = 15V, I_{OL} = 100mA$ | NA555, NE555, SA555 | 2 | 2.5 | |
| | SE555 | 2 | 2.2 | | |
| | $V_{CC} = 15V, I_{OL} = 100mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | | 2.7 | |
| | $V_{CC} = 15V, I_{OL} = 200mA$ | | 2.5 | | |
| | $V_{CC} = 5V, I_{OL} = 3.5mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | | 0.35 | |
| | $V_{CC} = 5V, I_{OL} = 5mA$ | NA555, NE555, SA555 | 0.1 | 0.35 | |
| | SE555 | 0.1 | 0.2 | | |
| | $V_{CC} = 5V, I_{OL} = 5mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | | 0.8 | |
| | $V_{CC} = 5V, I_{OL} = 8mA$ | NA555, NE555, SA555 | 0.15 | 0.4 | |
| | SE555 | 0.15 | 0.25 | | |
| High-level output voltage | $V_{CC} = 15V, I_{OH} = -100mA$ | NA555, NE555, SA555 | 12.75 | 13.3 | V |
| | SE555 | 13 | 13.3 | | |
| | $V_{CC} = 15V, I_{OH} = -100mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | 12 | | |
| | $V_{CC} = 15V, I_{OH} = -200mA$ | | 12.5 | | |
| | $V_{CC} = 5V, I_{OH} = -100mA$ | NA555, NE555, SA555 | 2.75 | 3.3 | |
| | SE555 | 3 | 3.3 | | |
| | $V_{CC} = 5V, I_{OH} = -100mA, T_A = -55^\circ C$ to $+125^\circ C$ | SE555 | 2 | | |
| Supply current | Output low, no load, $V_{CC} = 15V$ | NA555, NE555, SA555 | 10 | 15 | mA |
| | SE555 | 10 | 12 | | |
| | Output low, no load, $V_{CC} = 5V$ | NA555, NE555, SA555 | 3 | 6 | |
| | SE555 | 3 | 5 | | |
| | Output high, no load, $V_{CC} = 15V$ | NA555, NE555, SA555 | 9 | 13 | |
| | SE555 | 9 | 10 | | |
| | Output high, no load, $V_{CC} = 5V$ | NA555, NE555, SA555 | 2 | 5 | |
| | SE555 | 2 | 4 | | |

- (1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of [Figure 6-5](#). For example, when $V_{CC} = 5V$, the maximum value is $R = R_A + R_B \cong 3.4M\Omega$, and for $V_{CC} = 15V$, the maximum value is $R_A + R_B \cong 10M\Omega$.

5.6 Switching Characteristics

V_{CC} = 5V to 15V and T_A = 25°C (unless otherwise noted); characteristic values are specified by design, characterization, or both, and are not production tested

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|---|--|---------------------|------|-----|--------|
| Temperature coefficient of timing interval | Each timer, monostable ⁽²⁾ , T_A = MIN to MAX | NA555, NE555, SA555 | 50 | | ppm/°C |
| | | SE555 | 30 | 100 | |
| | Each timer, astable ⁽³⁾ , T_A = MIN to MAX | NA555, NE555, SA555 | 150 | | |
| | | SE555 | 90 | | |
| Supply-voltage sensitivity of timing interval | Each timer, monostable ⁽²⁾ | NA555, NE555, SA555 | 0.1 | 0.5 | %/V |
| | | SE555 | 0.05 | 0.2 | |
| | Each timer, astable ⁽³⁾ | NA555, NE555, SA555 | 0.3 | | |
| | | SE555 | 0.15 | | |
| t_r | Output-pulse rise time C_L = 15pF, T_A = 25°C, 20% to 80% | NA555, NE555, SA555 | 100 | 300 | ns |
| | | SE555 | 100 | 200 | |
| t_f | Output-pulse fall time C_L = 15pF, T_A = 25°C, 80% to 20% | NA555, NE555, SA555 | 100 | 300 | ns |
| | | SE555 | 100 | 200 | |

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Recommended Operating Conditions*.

(2) Values specified are for a device in a monostable circuit similar to [Figure 6-2](#), with the following component values: R_A = 2kΩ to 100kΩ, C = 0.1μF.

(3) Values specified are for a device in an astable circuit similar to [Figure 6-5](#), with the following component values: R_A = 1kΩ to 100kΩ, C = 0.1μF.

5.7 Typical Characteristics

data for temperatures less than -40°C and greater than 105°C are applicable for SE555 circuits only

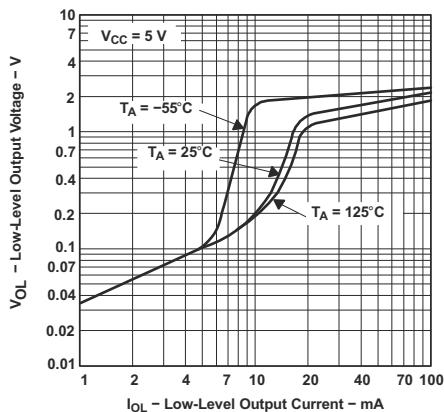


Figure 5-1. Low-Level Output Voltage vs Low-Level Output Current

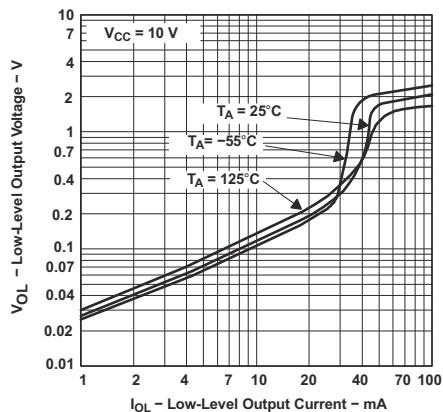


Figure 5-2. Low-Level Output Voltage vs Low-Level Output Current

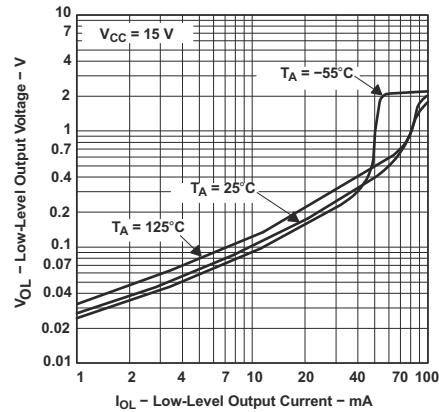


Figure 5-3. Low-Level Output Voltage vs Low-Level Output Current

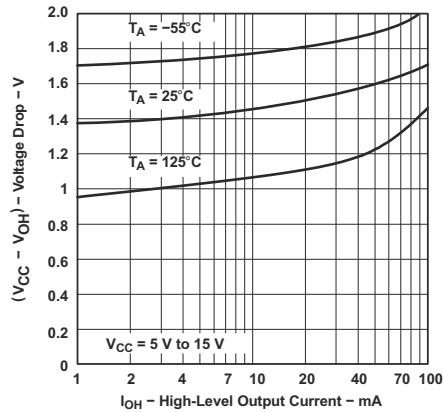


Figure 5-4. Drop Between Supply Voltage and Output vs High-Level Output Current

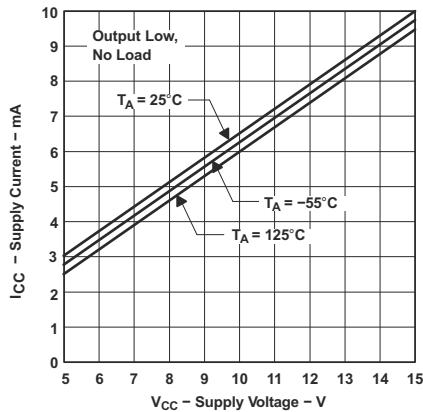


Figure 5-5. Supply Current vs Supply Voltage

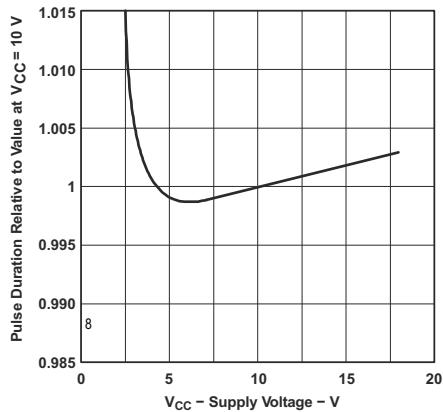
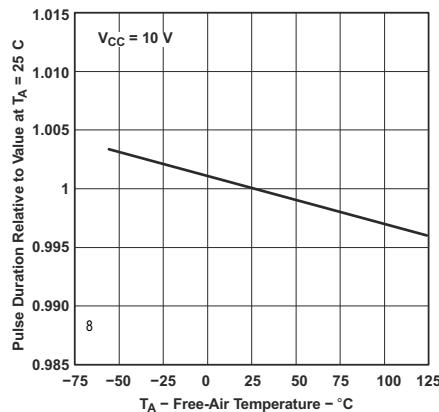


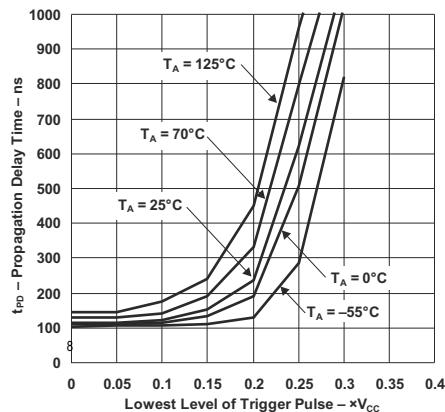
Figure 5-6. Normalized Output Pulse Duration (Monostable Operation) vs Supply Voltage

5.7 Typical Characteristics (continued)

data for temperatures less than -40°C and greater than 105°C are applicable for SE555 circuits only



**Figure 5-7. Normalized Output Pulse Duration
(Monostable Operation)
vs
Free-Air Temperature**

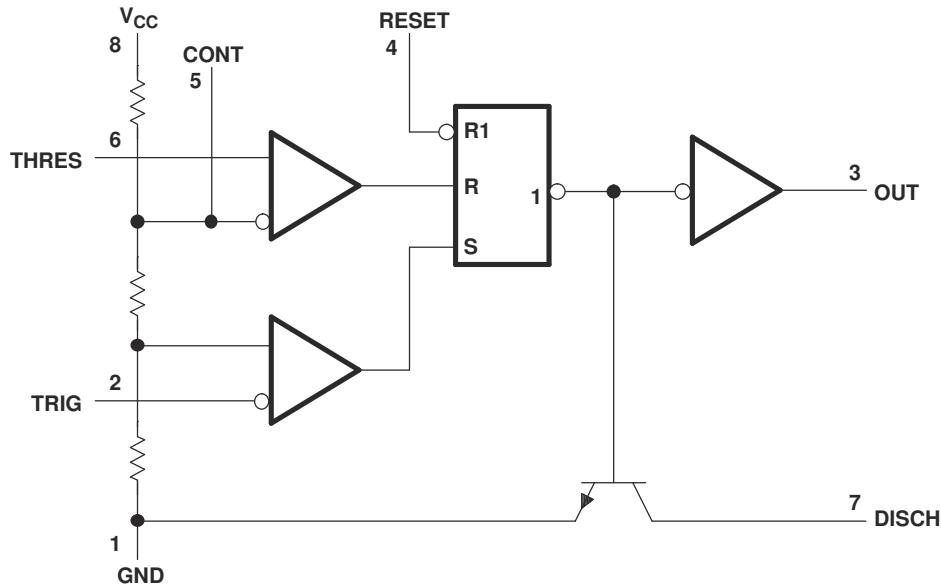


**Figure 5-8. Propagation Delay Time
vs
Lowest Voltage Level of Trigger Pulse**

6 Detailed Description

6.1 Overview

The Nx555 or Sx555 is a precision timing device for general-purpose timing applications from 10 μ s to hours or from < 1mHz to 100kHz. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor. Maximum output sink and discharge sink current are greater for higher V_{CC} and less for lower V_{CC}.

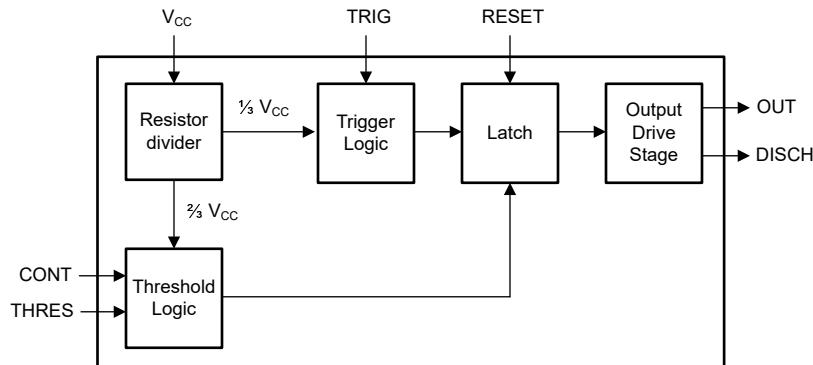


Note: Pin numbers shown are for the D, JG, P, PS, and PW packages.

Note: RESET can override TRIG, which can override THRES.

Figure 6-1. Simplified Schematic

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, Figure 6-2 shows how to connect any of these timers. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop (\bar{Q} goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop (\bar{Q} goes high), drives the output low, and discharges C through Q1.

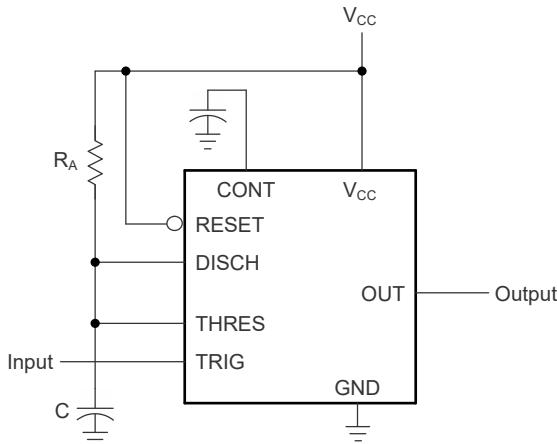


Figure 6-2. Circuit for Monostable Operation

Monostable operation is initiated when the TRIG voltage is less than the trigger threshold. After being initiated, the sequence ends only if TRIG is high for at least $10\mu s$ before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as $10\mu s$, which limits the minimum monostable pulse width to $10\mu s$. As a result of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1 \times R_A C$. Figure 6-4 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, as long as the supply voltage is constant during the time interval.

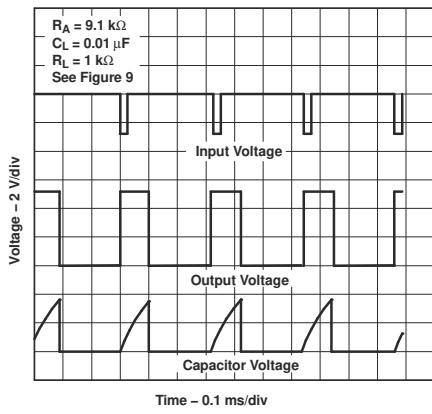


Figure 6-3. Typical Monostable Waveforms

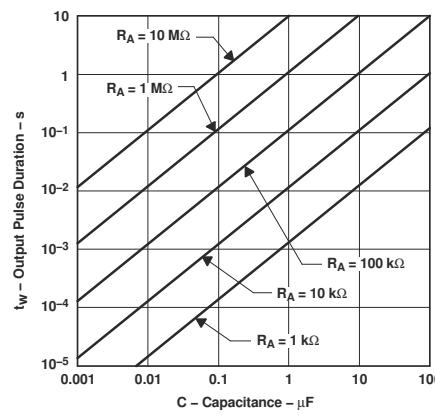
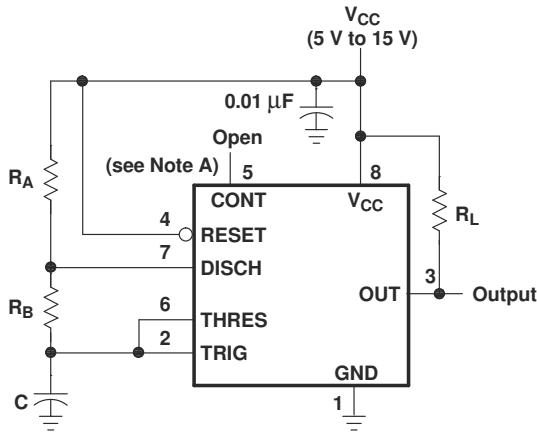


Figure 6-4. Output Pulse Duration vs Capacitance

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low for as long as the reset pulse is low. To prevent false triggering, when RESET is not used, connect RESET to V_{CC} .

6.3.2 Astable Operation

Figure 6-5 shows that adding a second resistor, R_B , to the circuit of Figure 6-2 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. Capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 6-5. Circuit for Astable Operation

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage. To reduce distortion, use at maximum frequency of 100kHz or below. If higher-frequency operation is required, consider using the [TLC555 LinCMOS™ Timer](#) instead.

Figure 6-6 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L are calculated as follows:

$$t_H \approx 0.693 \times (R_A + R_B) \times C \quad (1)$$

$$t_L \approx 0.693 \times R_B \times C \quad (2)$$

Other useful relationships for period, frequency, and driver-referred and waveform-referred duty cycle are calculated as follows:

$$T = t_H + t_L \approx 0.693 \times (R_A + 2R_B) \times C \quad (3)$$

$$f = \frac{1}{T} \approx \frac{1.44}{(R_A + 2R_B) \times C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{T} \approx \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{T} \approx 1 - \frac{R_B}{R_A + 2R_B} = \frac{R_A + R_B}{R_A + 2R_B} \quad (6)$$

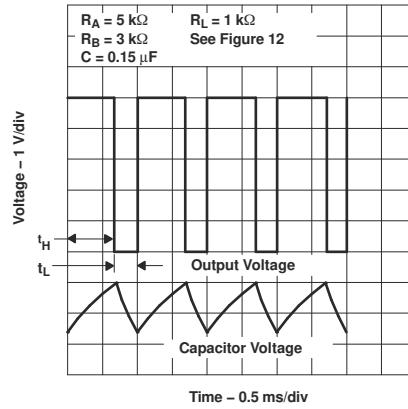


Figure 6-6. Typical Astable Waveforms

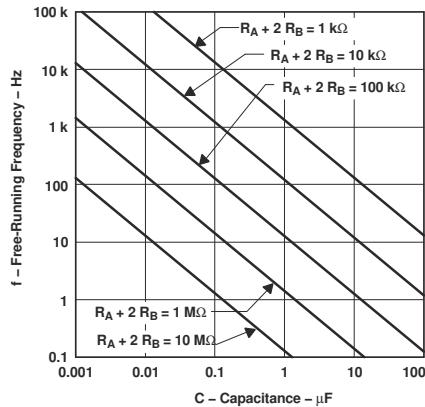


Figure 6-7. Free-Running Frequency

6.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of [Figure 6-2](#) can be made to operate as a frequency divider. [Figure 6-8](#) shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

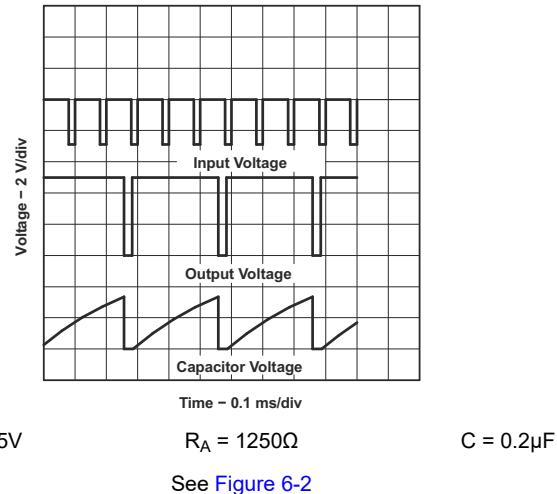


Figure 6-8. Divide-by-Three Circuit Waveforms

6.4 Device Functional Modes

[Table 6-1](#) shows the device truth table. For a valid reset voltage condition, use an external pullup resistor to V_{CC} (if using the RESET functionality), or short the RESET pin directly to V_{CC} (if the RESET functionality is not used).

Table 6-1. Function Table

| RESET VOLTAGE ⁽¹⁾ | TRIGGER VOLTAGE ⁽¹⁾ | THRESHOLD VOLTAGE ⁽¹⁾ | OUTPUT | DISCHARGE SWITCH |
|------------------------------|--------------------------------|----------------------------------|--------|---------------------------|
| LOW | Irrelevant | Irrelevant | Low | On |
| > MAX | < 1/3 × V_{CC} | Irrelevant ⁽²⁾ | High | Off |
| > MAX | > 1/3 × V_{CC} | > 2/3 × V_{CC} | Low | On |
| > MAX | > 1/3 × V_{CC} | < 2/3 × V_{CC} | | As previously established |

(1) Voltage levels shown are nominal.

(2) CONT pin open or 2/3 × V_{CC} .

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

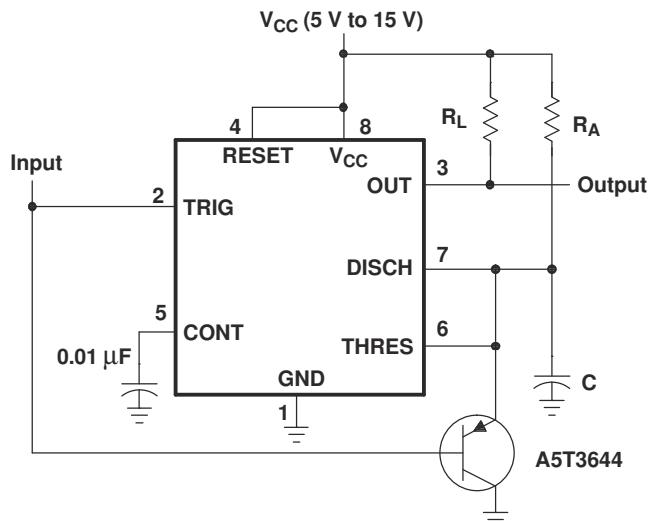
7.1 Application Information

The Nx555 and Sx555 precision timers use resistor and capacitor charging delay to provide a programmable time delay or operating frequency. This section presents a simplified discussion of the design process.

7.2 Typical Applications

7.2.1 Missing-Pulse Detector

The circuit shown in [Figure 7-1](#) can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in [Figure 7-2](#).



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 7-1. Circuit for Missing-Pulse Detector

7.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. Input stuck low cannot be detected because the timing capacitor (C) remains discharged.

7.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C > [\text{maximum normal input high time}]$. R_L improves V_{OH}, but is not required for TTL compatibility.

7.2.1.3 Application Curve

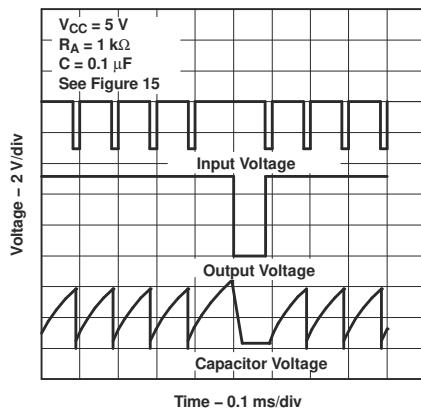
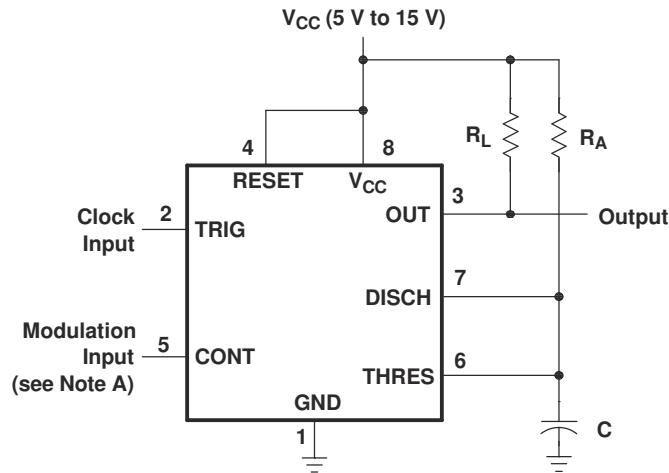


Figure 7-2. Completed Timing Waveforms for Missing-Pulse Detector

7.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 7-3 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 7-4 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape can be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 7-3. Circuit for Pulse-Width Modulation

7.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than $1/3 \times V_{CC}$. Modulation input can vary from ground to V_{CC} . The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC-based with an negative exponential curve.

7.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH} , but is not required for TTL compatibility.

7.2.2.3 Application Curve

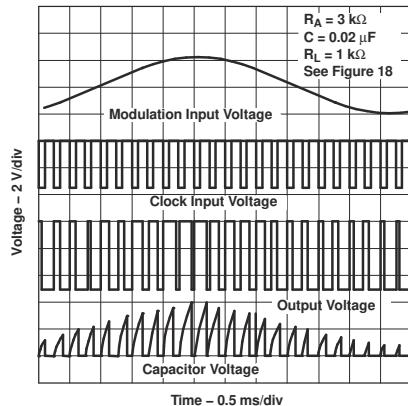
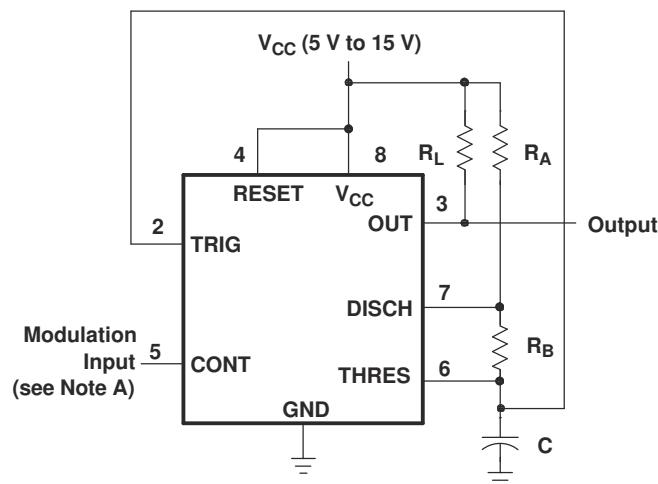


Figure 7-4. Pulse-Width-Modulation Waveforms

7.2.3 Pulse-Position Modulation

As shown in Figure 7-5, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 7-6 shows a triangular-wave modulation signal for such a circuit; however, any wave shape can be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 7-5. Circuit for Pulse-Position Modulation

7.2.3.1 Design Requirements

Both dc- and ac-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage.

7.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle are determined using the formulas in [Section 6.3.2](#). R_L improves V_{OH} , but R_L is not required for TTL compatibility.

7.2.3.3 Application Curve

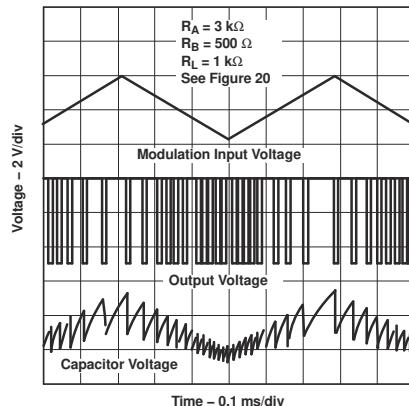
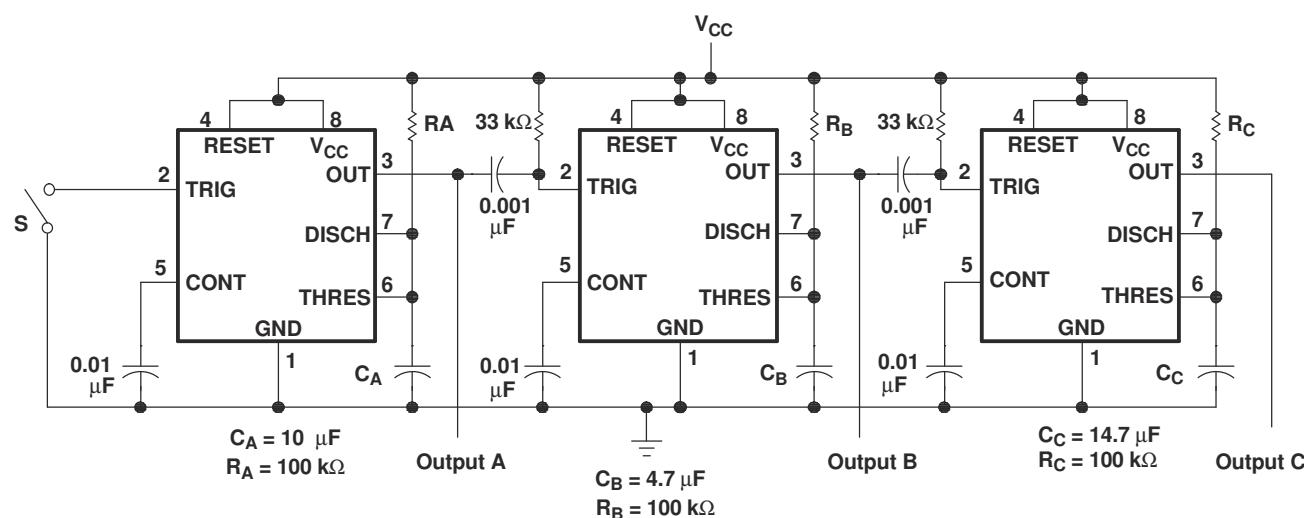


Figure 7-6. Pulse-Position-Modulation Waveforms

7.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. [Figure 7-7](#) shows a sequencer circuit with possible applications in many systems, and [Figure 7-8](#) shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: S closes momentarily at t = 0.

Figure 7-7. Sequential Timer Circuit

7.2.4.1 Design Requirements

The sequential timer application chains together multiple mono-stable timers. The joining components are the 33kΩ resistors and 0.001μF capacitors. The output high to low edge passes a 10μs start pulse to the next monostable.

7.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula. $t_w = 1.1 \times R \times C$.

7.2.4.3 Application Curve

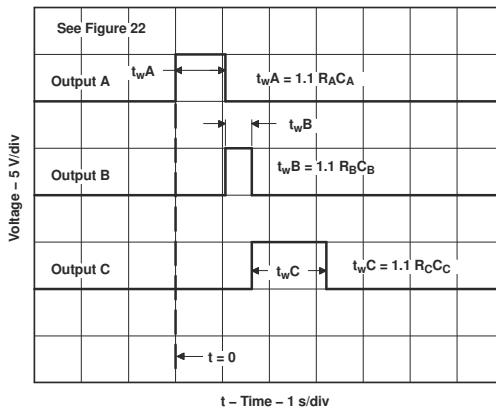


Figure 7-8. Sequential Timer Waveforms

7.3 Power Supply Recommendations

The Nx555 and Sx555 precision timers are designed to operate from an input voltage supply range between 4.5V and 16V (18V for SE555). A bypass capacitor is highly recommended from V_{CC} to the ground pin; a ceramic 0.1 μ F capacitor is sufficient.

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision I (September 2014) to Revision J (February 2025) | Page |
|---|------|
| • Updated list of end equipment in <i>Applications</i> | 1 |
| • Updated <i>Device Information</i> table..... | 1 |
| • Deleted package thermal impedance specifications from <i>Absolute Maximum Ratings</i> and added <i>Thermal Information</i> table with updated per-package thermal specifications..... | 4 |
| • Deleted <i>Handling Ratings</i> and moved storage temperature specification to <i>Absolute Maximum Ratings</i> | 4 |
| • Added <i>ESD Ratings</i> table..... | 4 |
| • Deleted redundant input voltage specification in <i>Recommended Operating Conditions</i> | 4 |
| • Changed <i>Operating Characteristics</i> title to <i>Switching Characteristics</i> , and clarified that values are specified by design or characterization and are not production tested..... | 7 |
| • Deleted initial error of timing interval specification in <i>Switching Characteristics</i> and clarified that output rise and fall times are 20% to 80% and 80% to 20%, respectively..... | 7 |
| • Changed functional block diagram to simplified schematic and moved to Overview..... | 10 |
| • Updated <i>Functional Block Diagram</i> | 10 |
| • Added CONT pin table note to Table 6-1, <i>Function Table</i> | 13 |

| Changes from Revision H (June 2010) to Revision I (September 2014) | Page |
|--|------|
| • Updated document to new TI enhanced data sheet format..... | 1 |
| • Deleted <i>Ordering Information</i> table..... | 1 |
| • Added Military Disclaimer to <i>Features</i> | 1 |
| • Added <i>Applications</i> | 1 |

| | |
|---|----|
| • Added <i>Device Information</i> table..... | 1 |
| • Added DISCH switch on-state voltage parameter..... | 5 |
| • Added Mechanical, Packaging, and Orderable Information section..... | 20 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-side navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| JM38510/10901BPA | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /10901BPA |
| JM38510/10901BPA.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /10901BPA |
| NA555D | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -40 to 105 | NA555 |
| NA555DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA555 |
| NA555DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA555 |
| NA555P | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU SN | N/A for Pkg Type | -40 to 105 | NA555P |
| NA555P.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 105 | NA555P |
| NA555PE4 | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 105 | NA555P |
| NA555PE4.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 105 | NA555P |
| NE555D | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | NE555 |
| NE555DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | 0 to 70 | NE555 |
| NE555DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 |
| NE555DR1G4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 |
| NE555DR1G4.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 |
| NE555DRG4 | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | 0 to 70 | NE555 |
| NE555P | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU SN | N/A for Pkg Type | 0 to 70 | NE555P |
| NE555P.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | NE555P |
| NE555PE4 | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | NE555P |
| NE555PE4.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | NE555P |
| NE555PS | Active | Production | SO (PS) 8 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | N555 |
| NE555PS.A | Active | Production | SO (PS) 8 | 80 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 |
| NE555PSR | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 |
| NE555PSR.A | Active | Production | SO (PS) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 |
| NE555PW | Obsolete | Production | TSSOP (PW) 8 | - | - | Call TI | Call TI | 0 to 70 | N555 |
| NE555PWR | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 |
| NE555PWR.A | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 |
| SA555D | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -40 to 85 | SA555 |
| SA555DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | SA555 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SA555DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 |
| SA555DRG4 | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -40 to 85 | SA555 |
| SA555P | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SA555P |
| SA555P.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SA555P |
| SE555D | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -55 to 125 | SE555 |
| SE555DG4 | Obsolete | Production | SOIC (D) 8 | - | - | Call TI | Call TI | -55 to 125 | SE555 |
| SE555DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 |
| SE555DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 |
| SE555DRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 |
| SE555DRG4.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 |
| SE555FKB | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE555FKB |
| SE555FKB.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE555FKB |
| SE555JG | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE555JG |
| SE555JG.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE555JG |
| SE555JGB | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE555JGB |
| SE555JGB.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE555JGB |
| SE555P | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | SE555P |
| SE555P.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | SE555P |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

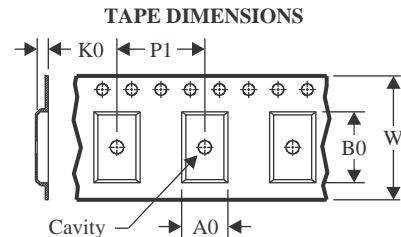
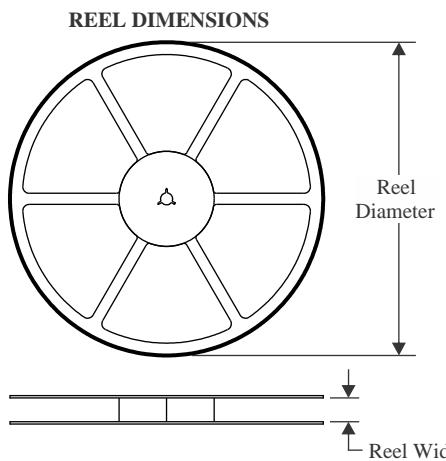
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SE555, SE555M :

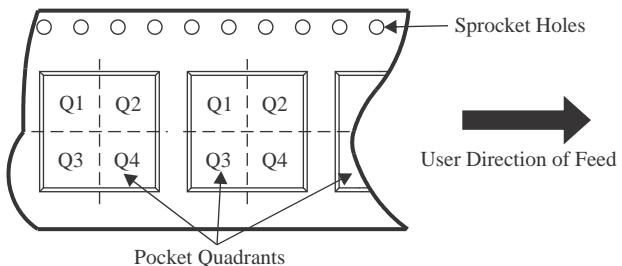
- Catalog : [SE555](#)
- Military : [SE555M](#)
- Space : [SE555-SP](#), [SE555-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

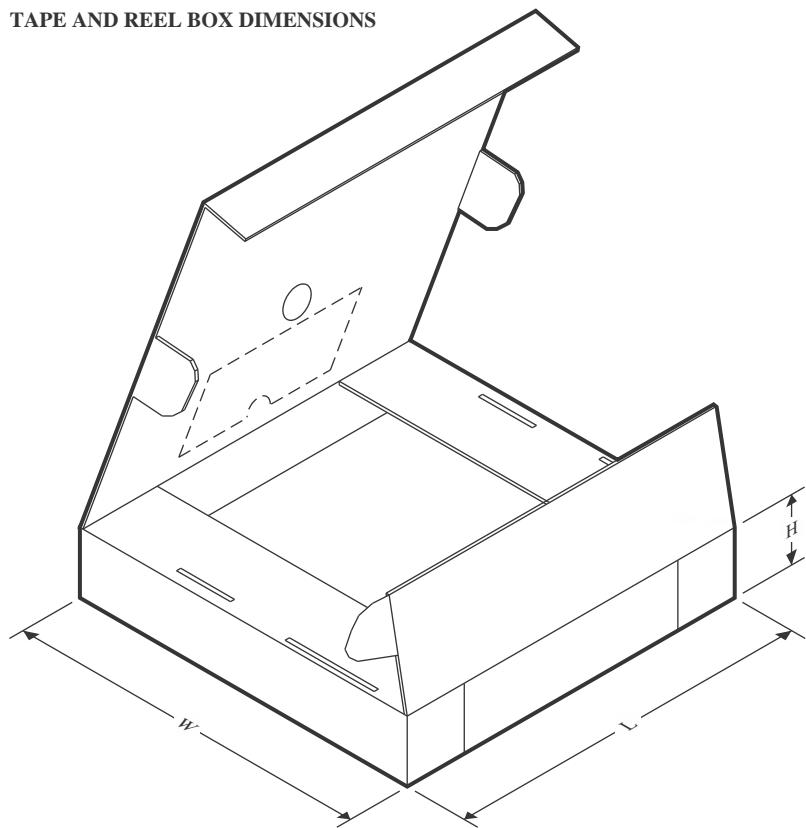
TAPE AND REEL INFORMATION

| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

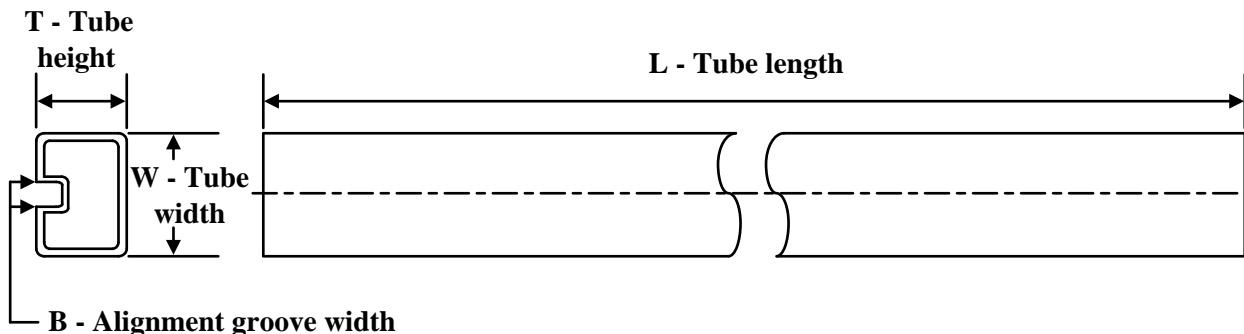
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| NA555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555DR1G4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555PSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| NE555PWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SA555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SE555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SE555DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| NA555DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| NE555DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| NE555DR1G4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| NE555PSR | SO | PS | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| NE555PWR | TSSOP | PW | 8 | 2000 | 353.0 | 353.0 | 32.0 |
| SA555DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SE555DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| SE555DRG4 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μ m) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| NA555P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NA555P | P | PDIP | 8 | 50 | 506.1 | 9 | 600 | 5.4 |
| NA555P.A | P | PDIP | 8 | 50 | 506.1 | 9 | 600 | 5.4 |
| NA555P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NA555PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NA555PE4.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NE555P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NE555P | P | PDIP | 8 | 50 | 506.1 | 9 | 600 | 5.4 |
| NE555P.A | P | PDIP | 8 | 50 | 506.1 | 9 | 600 | 5.4 |
| NE555P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NE555PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NE555PE4.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| NE555PS | PS | SOP | 8 | 80 | 530 | 10.5 | 4000 | 4.1 |
| NE555PS.A | PS | SOP | 8 | 80 | 530 | 10.5 | 4000 | 4.1 |
| SA555P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SA555P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SE555FKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SE555FKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SE555P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SE555P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

GENERIC PACKAGE VIEW

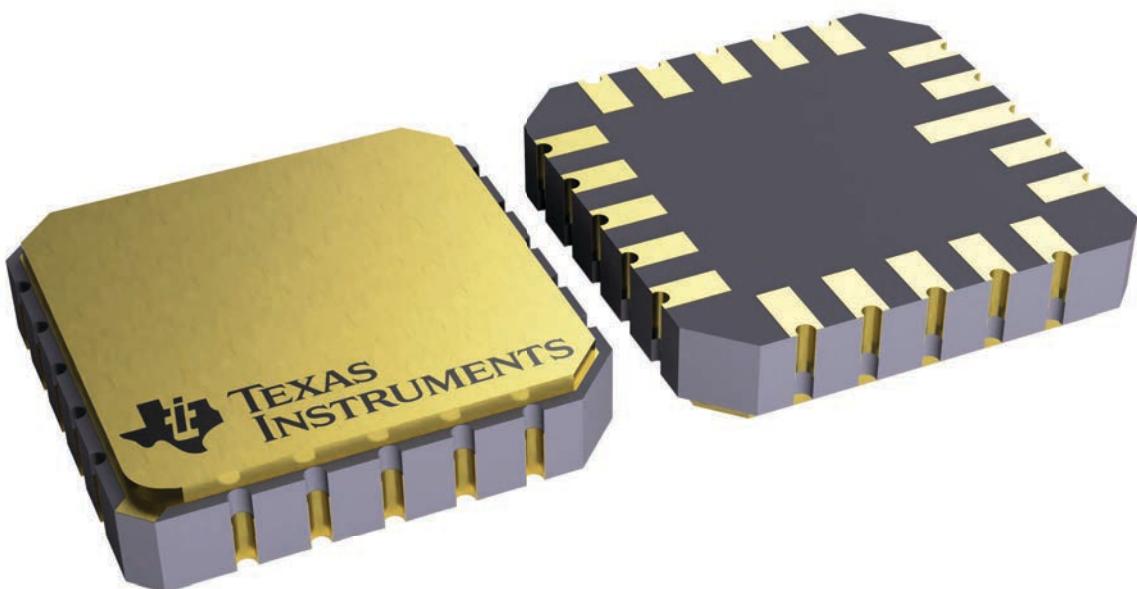
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

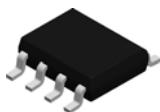
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

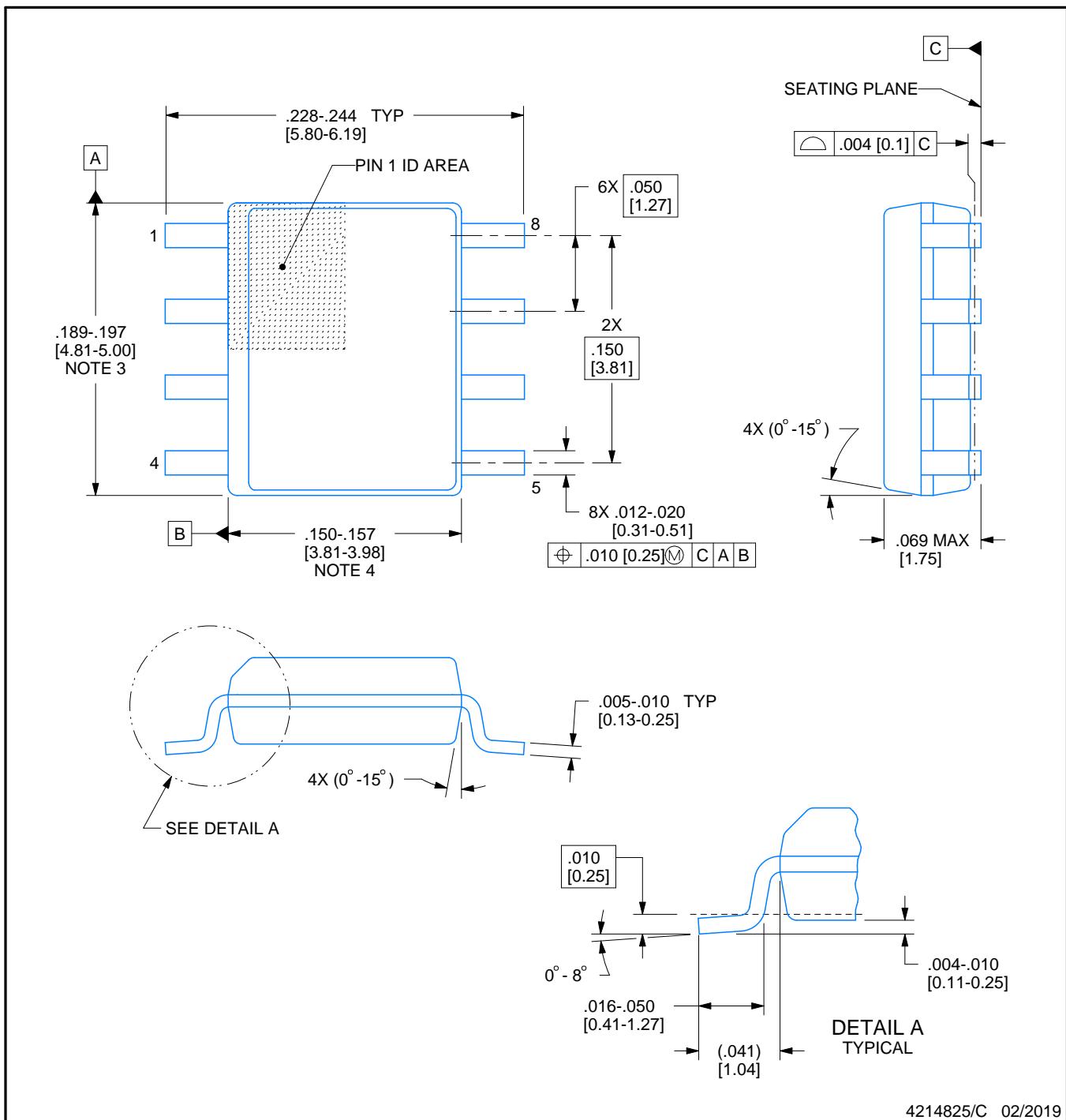
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

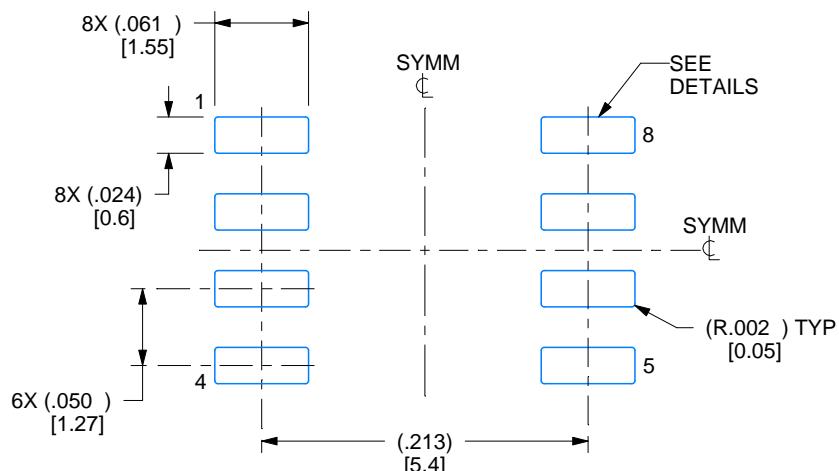
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

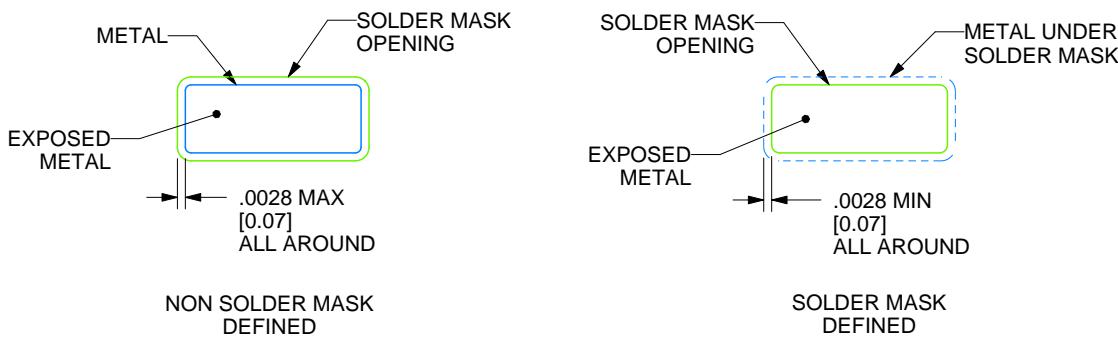
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

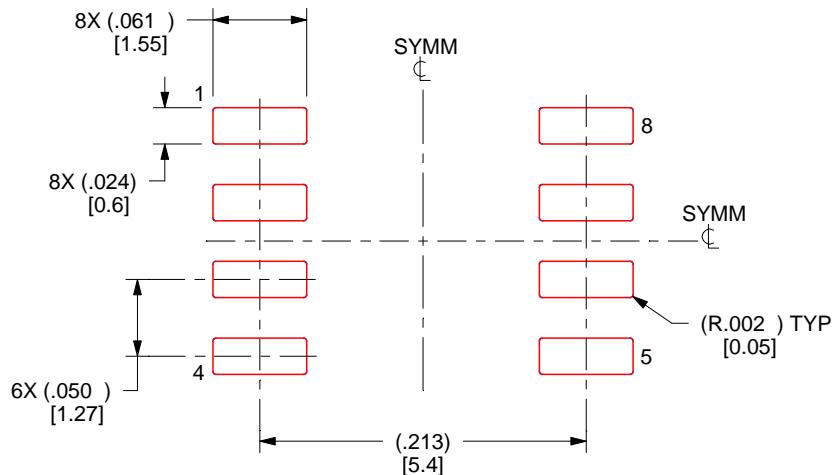
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

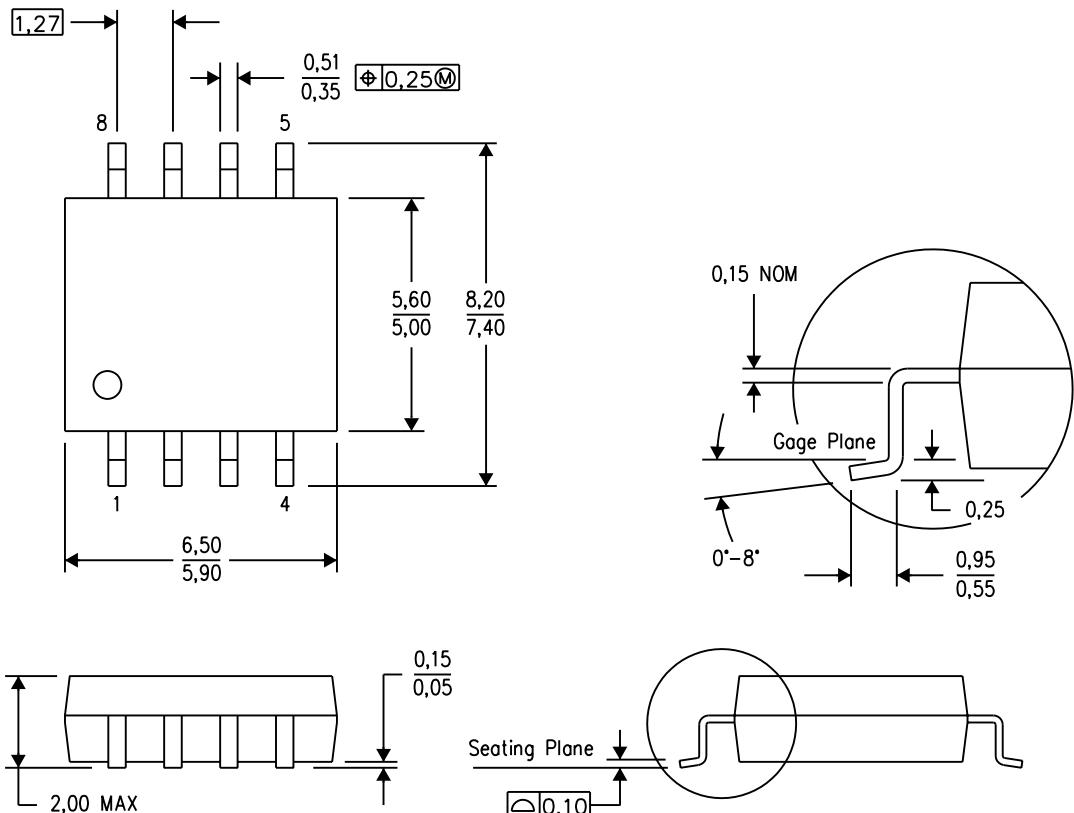
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

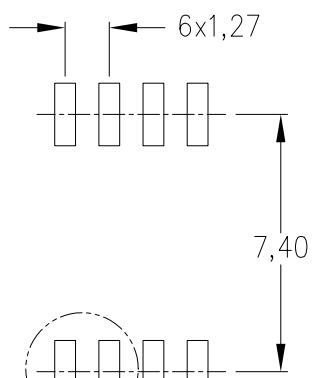
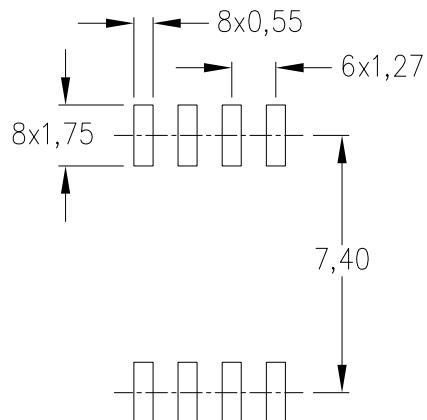
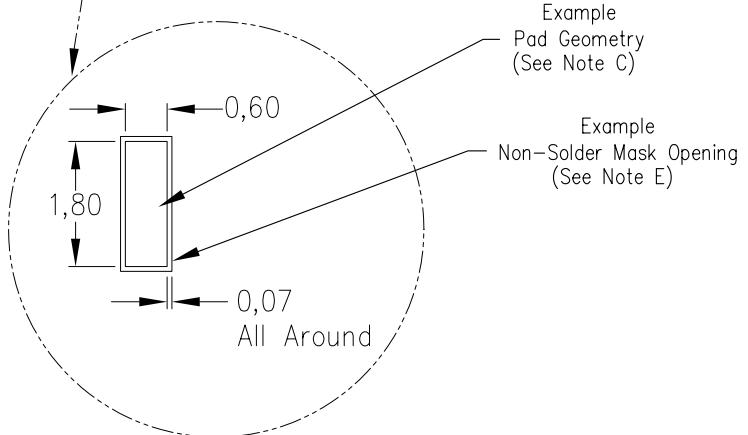


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Non-Solder Mask Opening
(See Note E)

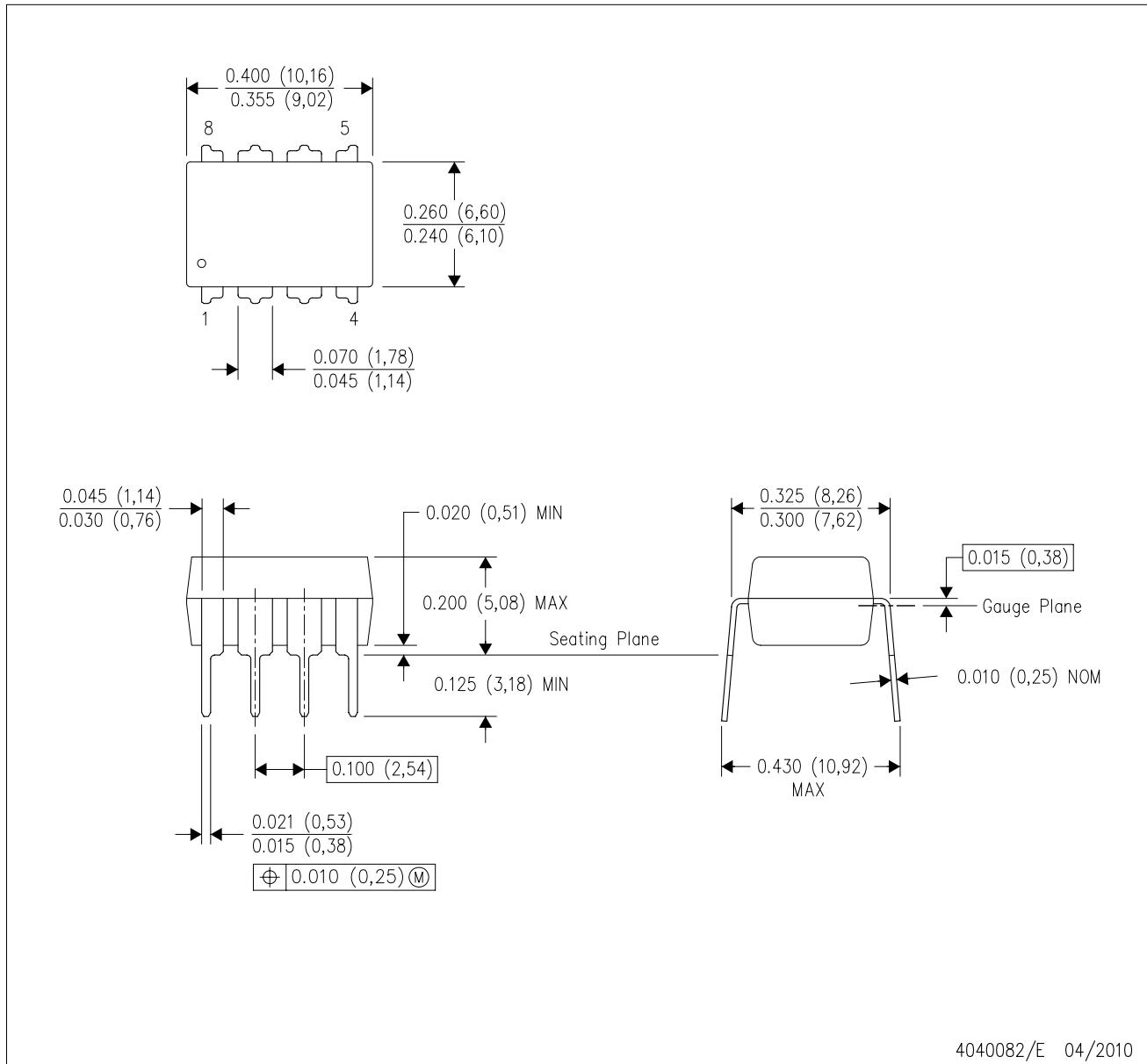
4212188/A 09/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

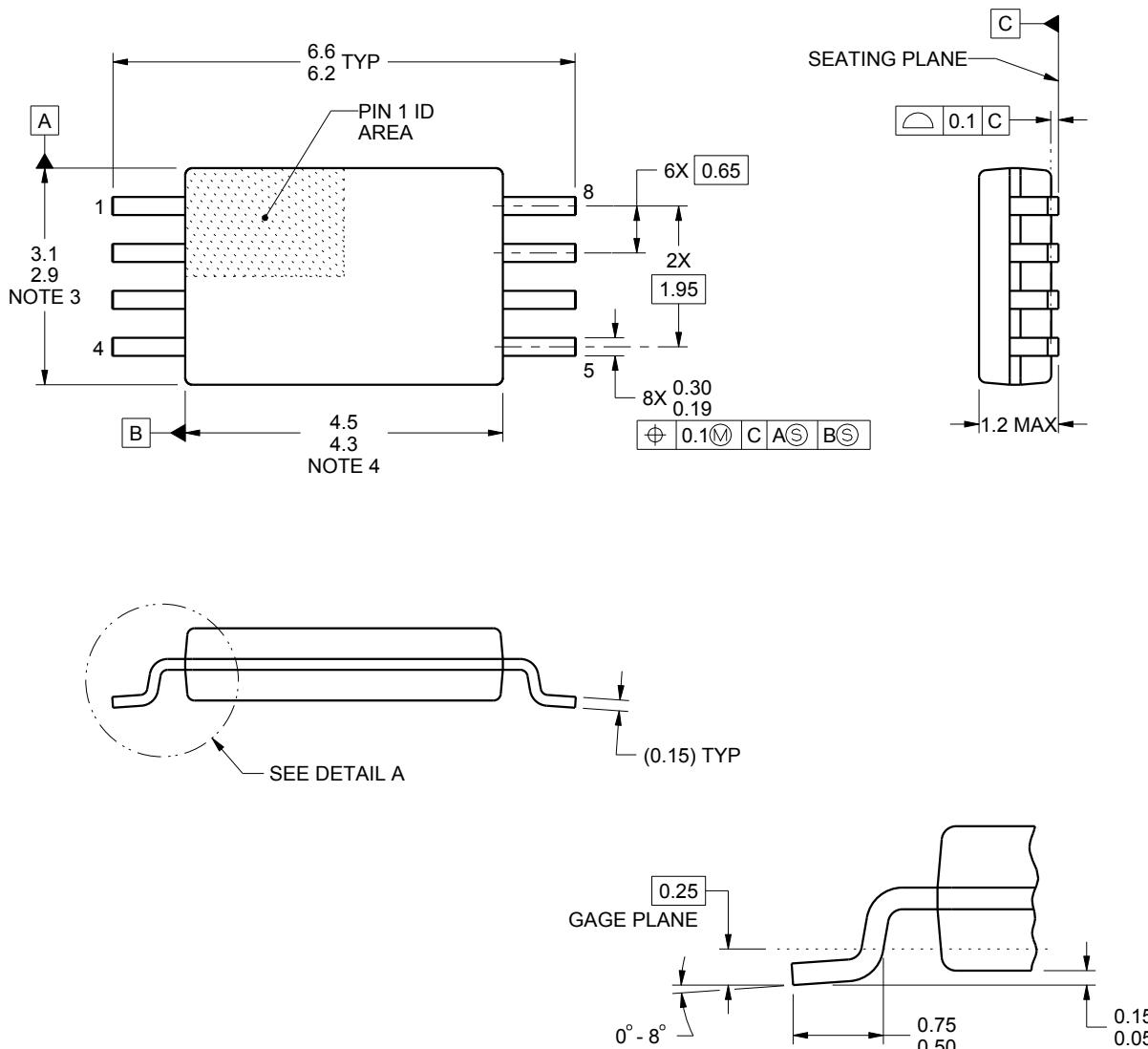
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



DETAIL A TYPICAL

NOTES:

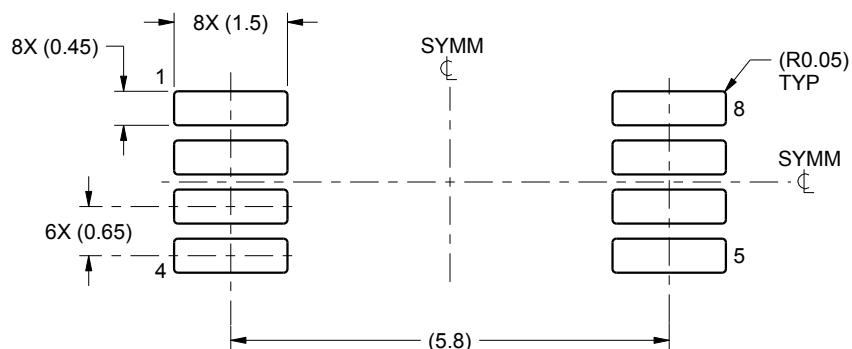
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
 5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

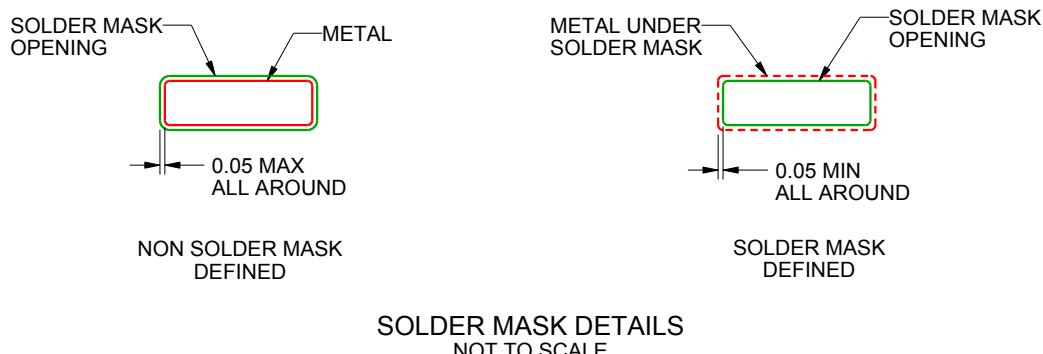
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

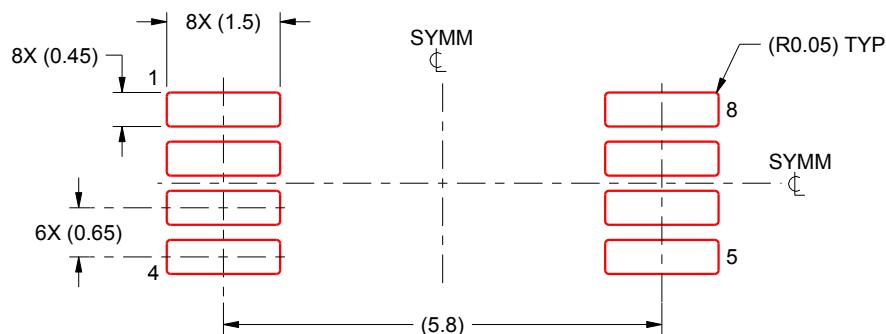
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

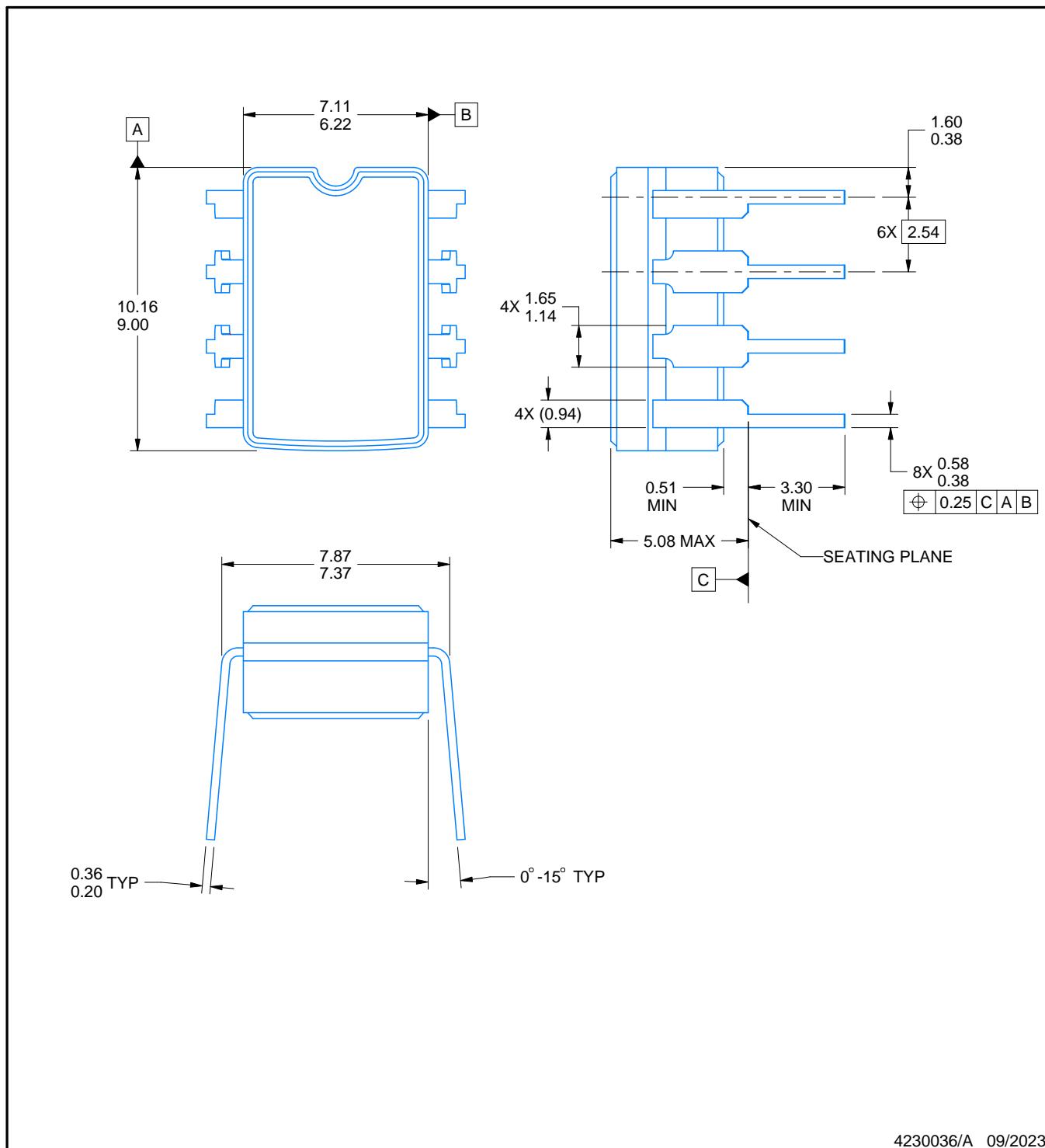
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

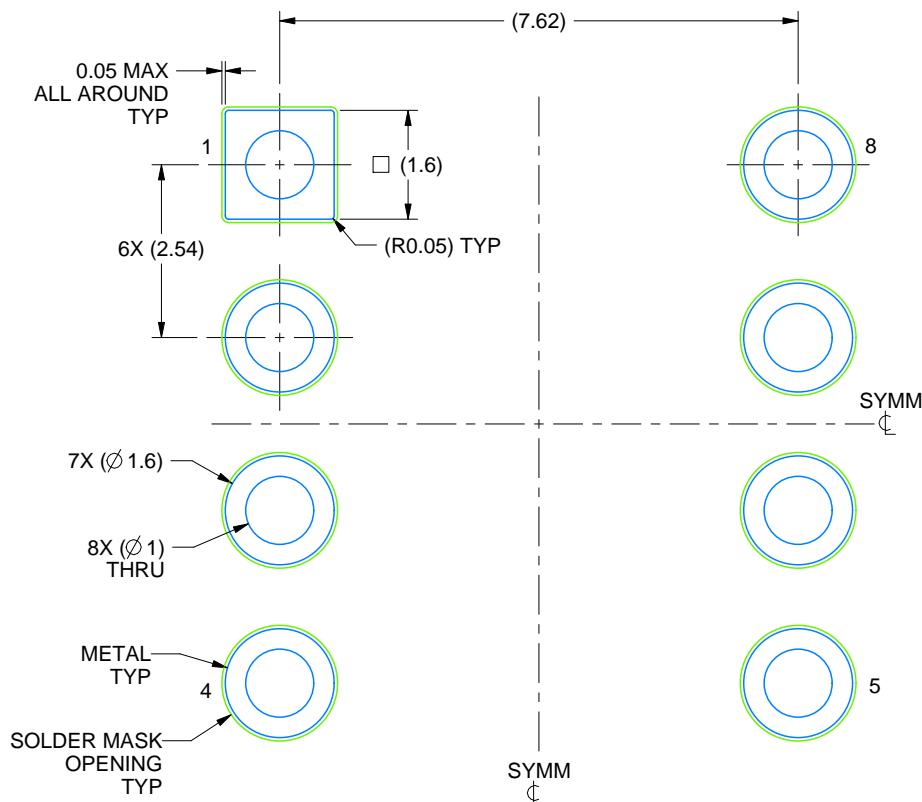
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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