Bridging HW and SW verification with VUnit co-simulation

Unai Martinez-Corral

About me

- Digital Electronics Design Group (GDED) at the University of the Basque Country (UPV/EHU) [unai.martinezcorral@ehu.eus]
- Antmicro [umartinezcorral@antmicro.com]
- GitHub: GHDL, VUnit, HDL, VHDL, EDA², F4PGA… [@umarcor]
- GitLab: IEEE-P1076 [@umarcor]

VHDL

Verification and Hardware Description Language

Computer language

Software and/or hardware

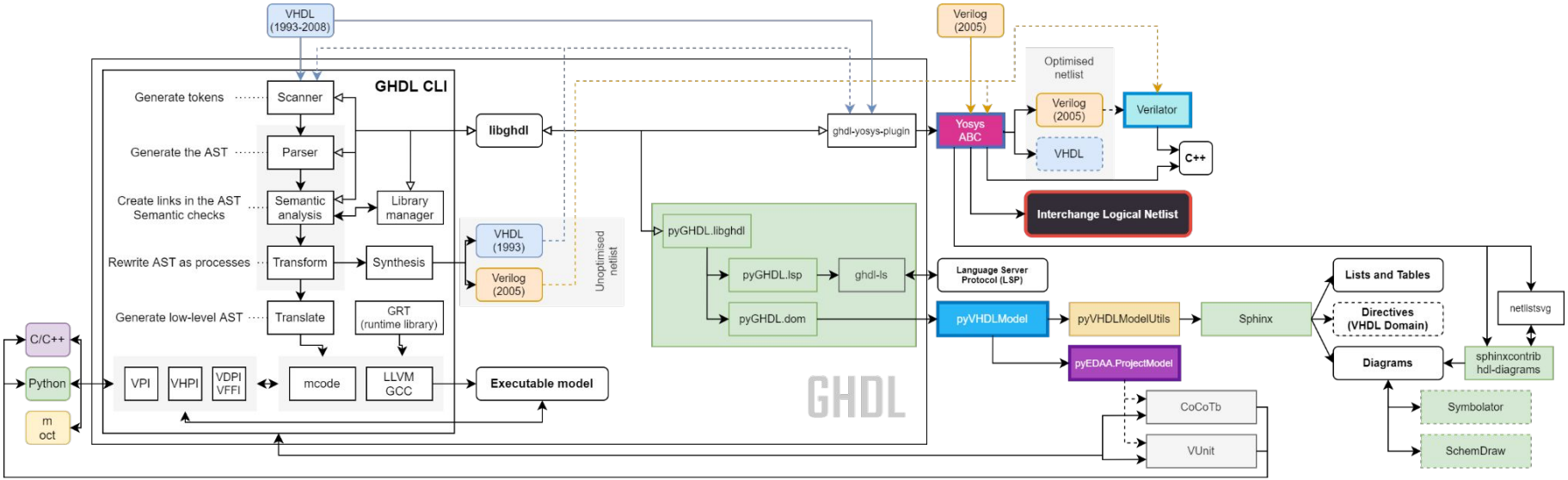
HDL co-simulation

- Indirect co-simulation:
  - Verilog Procedural Interface (**VPI**), also known as Program Language Interface (**PLI**) 2.0.
  - VHDL Procedural Interface (**VHPI**).

- Direct co-simulation:
  - Specific implementations of (a draft of) **VHPIDIRECT**, such as Foreign Language Interface (**FLI**) or Xilinx Simulation Interface (**XSI**).
  - Direct Programming Interface (**DPI**).

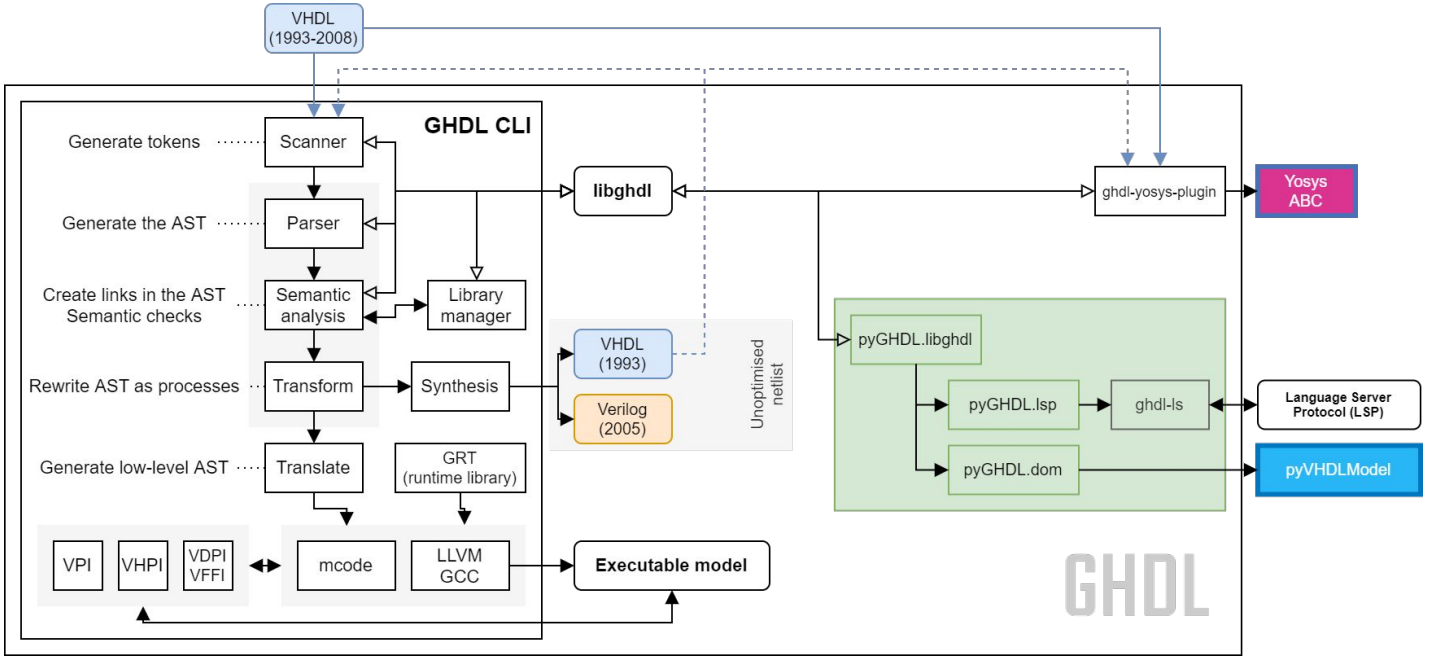
- Generation of C/C++ models/sources through a transpiler.
  - Verilated models.
  - CXXRTL (Yosys).
  - “Mixed-language” simulation.

GHDL: a VHDL toolkit



umarcor.github.io/SIEAV/VHDL.html

GHDL: compiling and executing VHDL

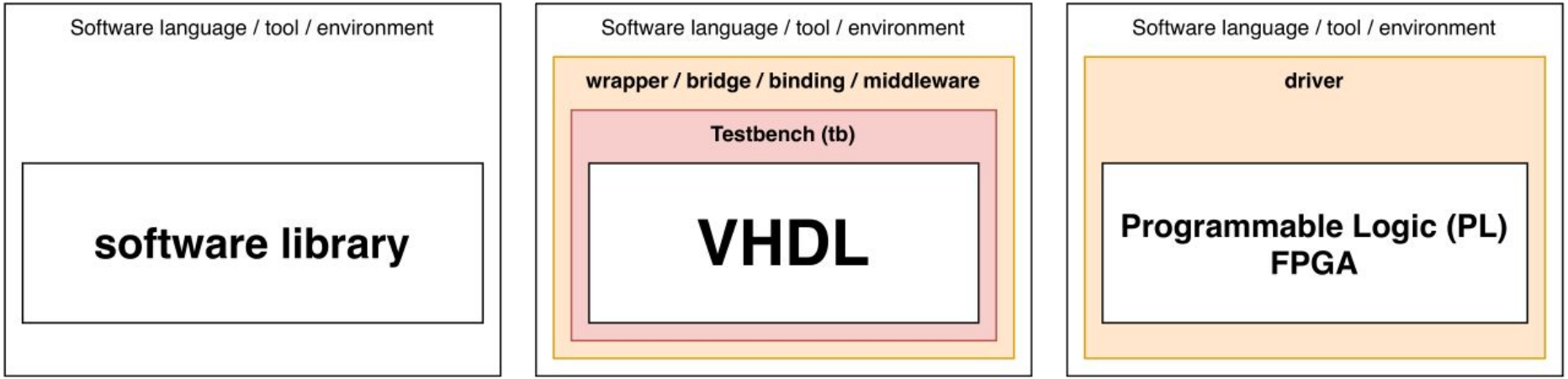


ghdl.github.io/ghdl/internals/index.html

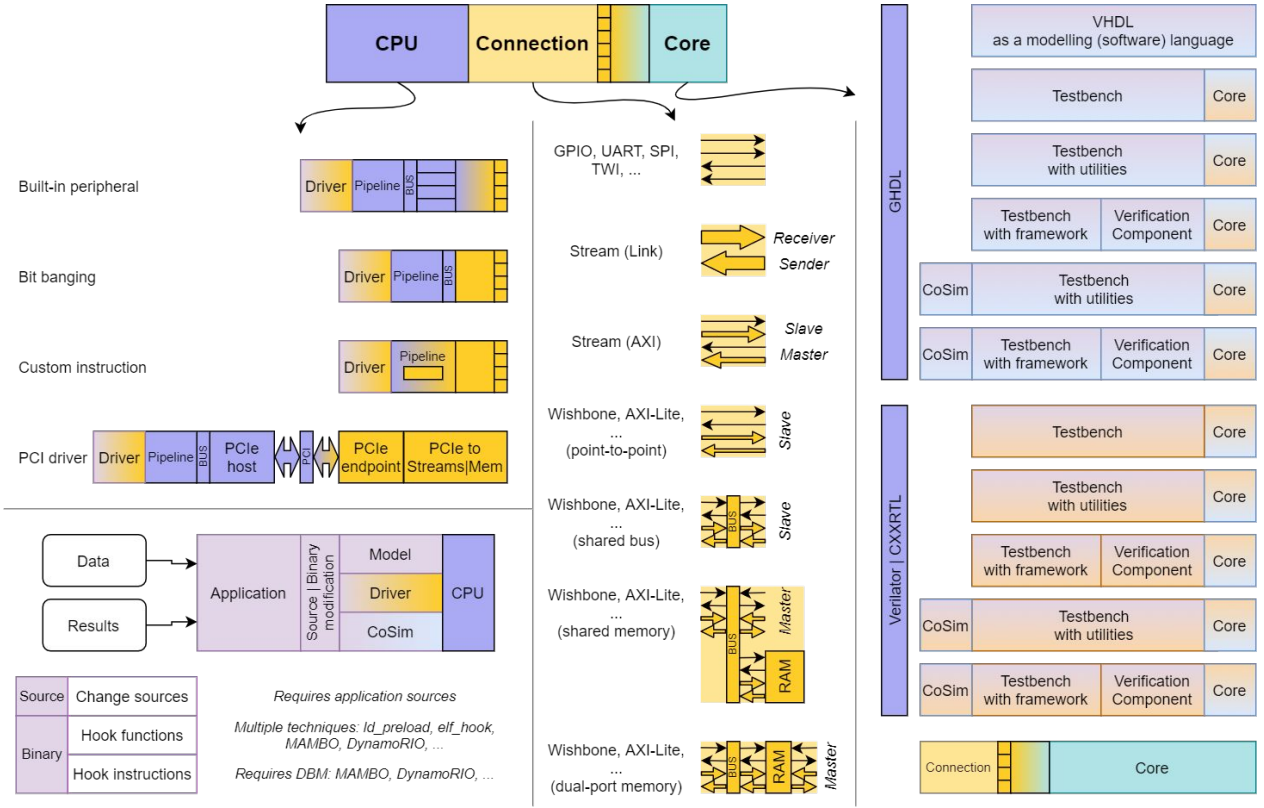
GHDL co-simulation [ghdl.github.io/ghdl-cosim]

- VHPIDIRECT
  - Have the signature of a VHDL subprogram match a foreign language.
  - Where and when to execute foreign functions is defined in VHDL.
  - With LLVM or GCC backends, foreign code can be provided as C/Ada sources, or called through a shared library.
- VPI
  - Use a C API to register callback functions.
  - Where and when to execute the callbacks is defined in the foreign language.
  - Foreign code is compiled into a shared library.
- ghdl_main
  - Wrap the whole simulation by calling GHDL as a function.
- Execution is always managed by GHDL.

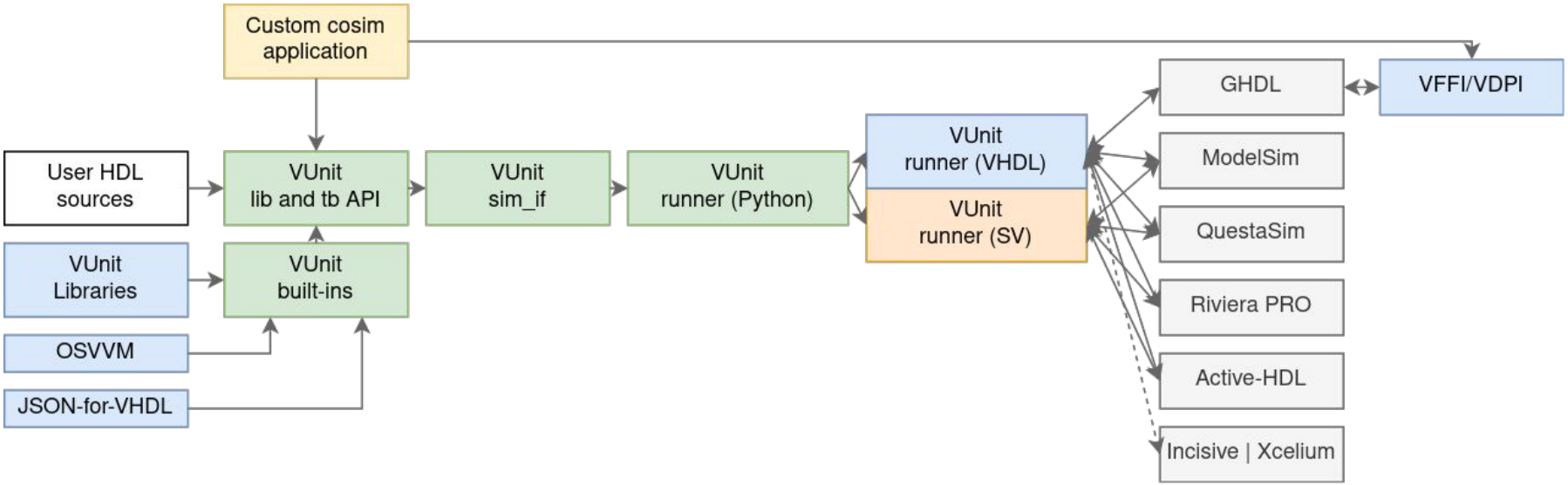
Functional verification of an HDL design



Digital twins

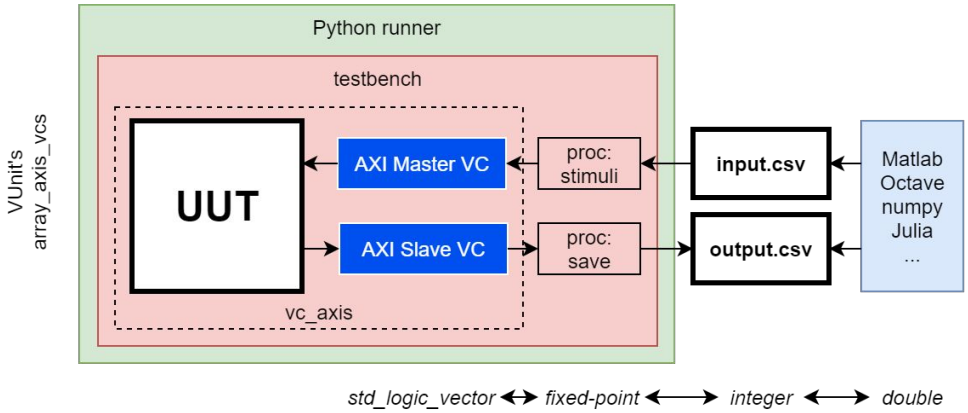


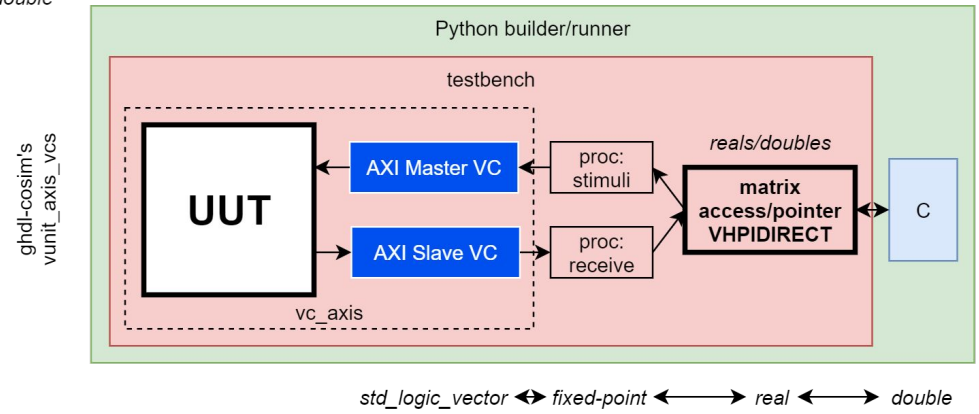
VUnit: an open source unit testing framework for HDLs



vunit.github.io/about.html

Array and AXI4 Stream Verification Components





ghdl.github.io/ghdl-cosim/vhpidirect/examples/arrays.html#array-and-axi4-stream-verification-components

ghdl/ghdl-cosim: vhpidirect/arrays/matrices/vunit_axis_vcs/run.py

```
from pathlib import Path
from vunit import VUnit

VU = VUnit.from_argv(vhdl_standard="2008")
VU.add_verification_components()

ROOT = Path(__file__).resolve().parent

VU.add_library("lib").add_source_files([ROOT.parent / "pkg.vhd", ROOT / "src" / "*.vhd", ROOT / "*.vhd"])

VU.set_compile_option("ghdl.flags", ["-frelaxed"])
VU.set_sim_option("ghdl.elab_flags", ["-frelaxed", "-Wl," + str(ROOT.parent / "main.c")])

VU.main()
```

Building the HDL design/simulation as shared lib

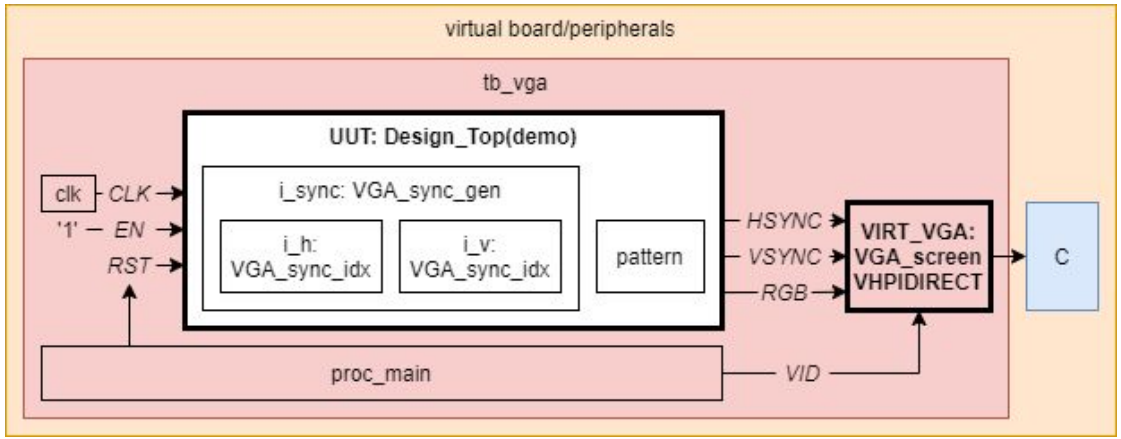
```
vu.set_sim_option('ghdl.elab_flags', [
      '-shared',
      '-Wl,-fPIC',
      '-Wl,' + str(ROOT.parent.parent.parent / 'quickstart' / 'wrapping' / 'exitcb' /
'caux.c')
])

vu.set_sim_option("ghdl.elab_e", True)
vu._args.elaborate = True
```

ghdl/ghdl-cosim: vhpidirect/shared/py/vunit/run.py
ghdl/ghdl-cosim: vhpidirect/shared/py/vunit/cosim.py

VGA (RGB image buffer)¶

ghdl.github.io/ghdl-cosim/vhpidirect/examples/arrays.html#vga-rgb-image-buffer

github.com/dbhi/vboard: vga

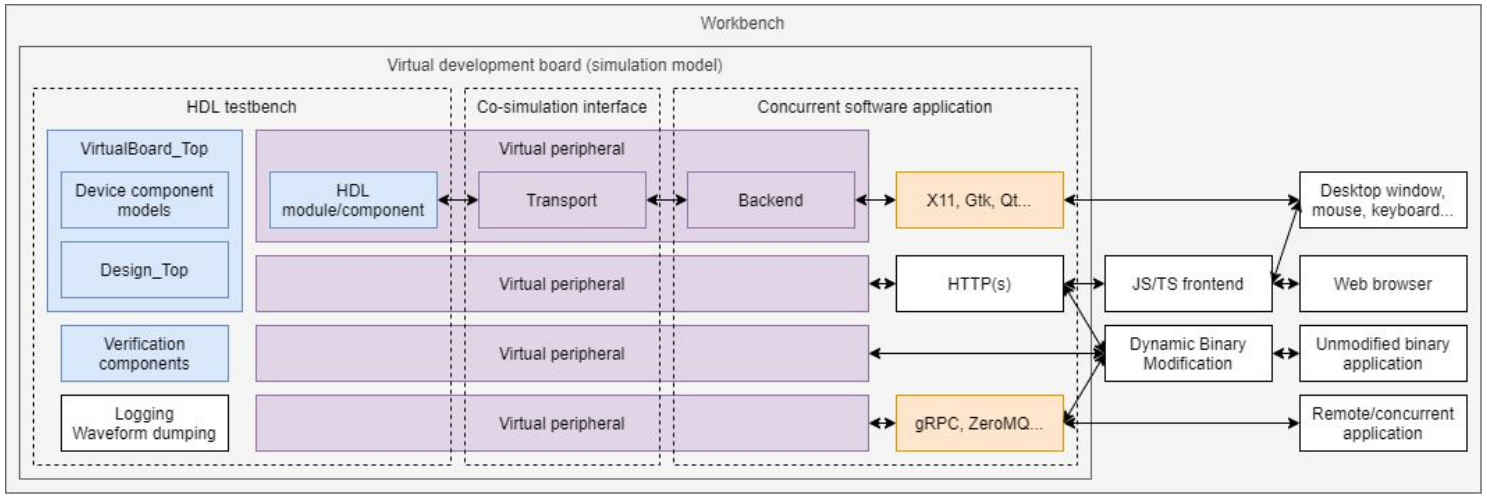


matplotlib

```
def plotxy(x, y, l):
        print("plotxy", x, y, l)

        xx = np.ctypeslib.as_array((ctypes.c_int * l).from_address(ctypes.addressof(x.contents)))
        yy = np.ctypeslib.as_array((ctypes.c_int * l).from_address(ctypes.addressof(y.contents)))

        plt.title("ghdl-cosim Python callback example")
        plt.xlabel("x axis caption")
        plt.ylabel("y axis caption")
        plt.plot(xx,yy)
```

ghdl/ghdl-cosim: vhpidirect/shared/pycb/run.py

Virtual development board



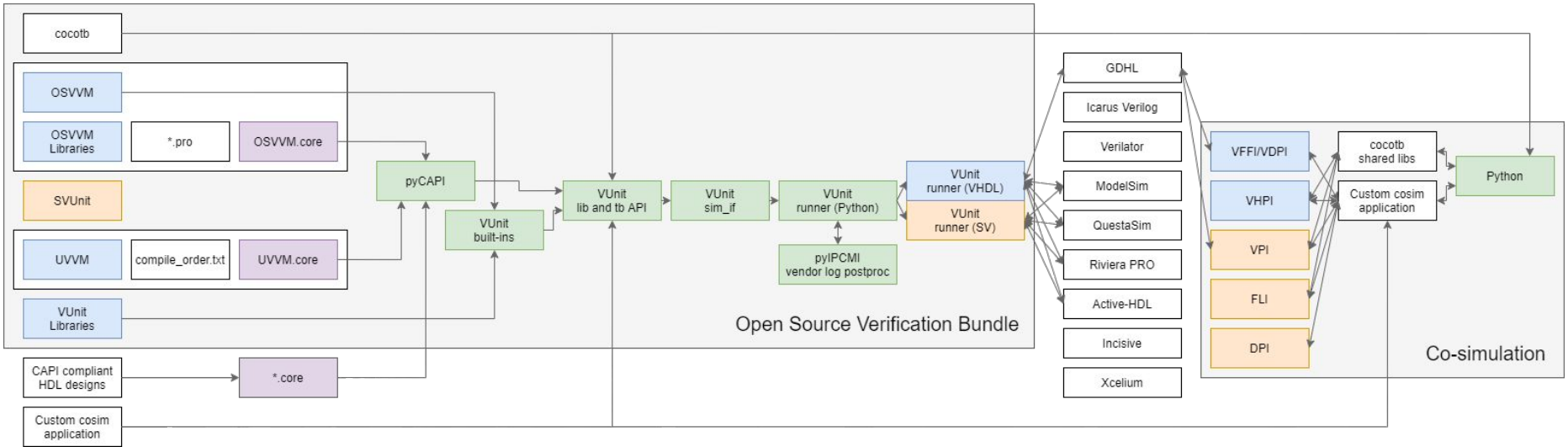
github.com/dbhi/vboard

- Virtual Nexys-4 like board [https://gitlab.ensta-bretagne.fr/bollenth/ghdl-vpi-virtual-board]
- An Interactive VHDL Testbench Using GHDL, Python, and Cocotb [https://blog.chuckstechtalk.com/software/2021/12/27/interactive-vhdl-testbench.html]
- Visualization of hyperspectral/multispectral image processing cores [https://github.com/VUnit/vunit/pull/568]

Open Source Verification Bundle

umarcor.github.io/osvb

Open Source
Verification Bundle



Additional content

github.com/umarcor/sieav

- umarcor.github.io/SIEAV/
- github.com/umarcor/SIEAV/releases/tag/tip

Additional content

- Xyce
- DBHI
- Renode
- vunit/cosim
- vunit/vunit_action